ISSN: 1863-5598

ZKZ 64717
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# Bodo´s Power Systems®

Electronics in Motion and Conversion

May 2012


*Fast Recovery Diodes for demanding IGCT Applications*

**PCIM**

# Bodo´s Power Systems®

## Hot Show Event

*Stop at the Podium at its Best*

**Wednesday, May 9th**
**Booth 12 / 670**
**12:20 - 13:20**

***"Efficient DC/DC Conversion"***

**Bodo Arlt, Editor Bodo’s Power Systems**


Bodo´s Power Systems®

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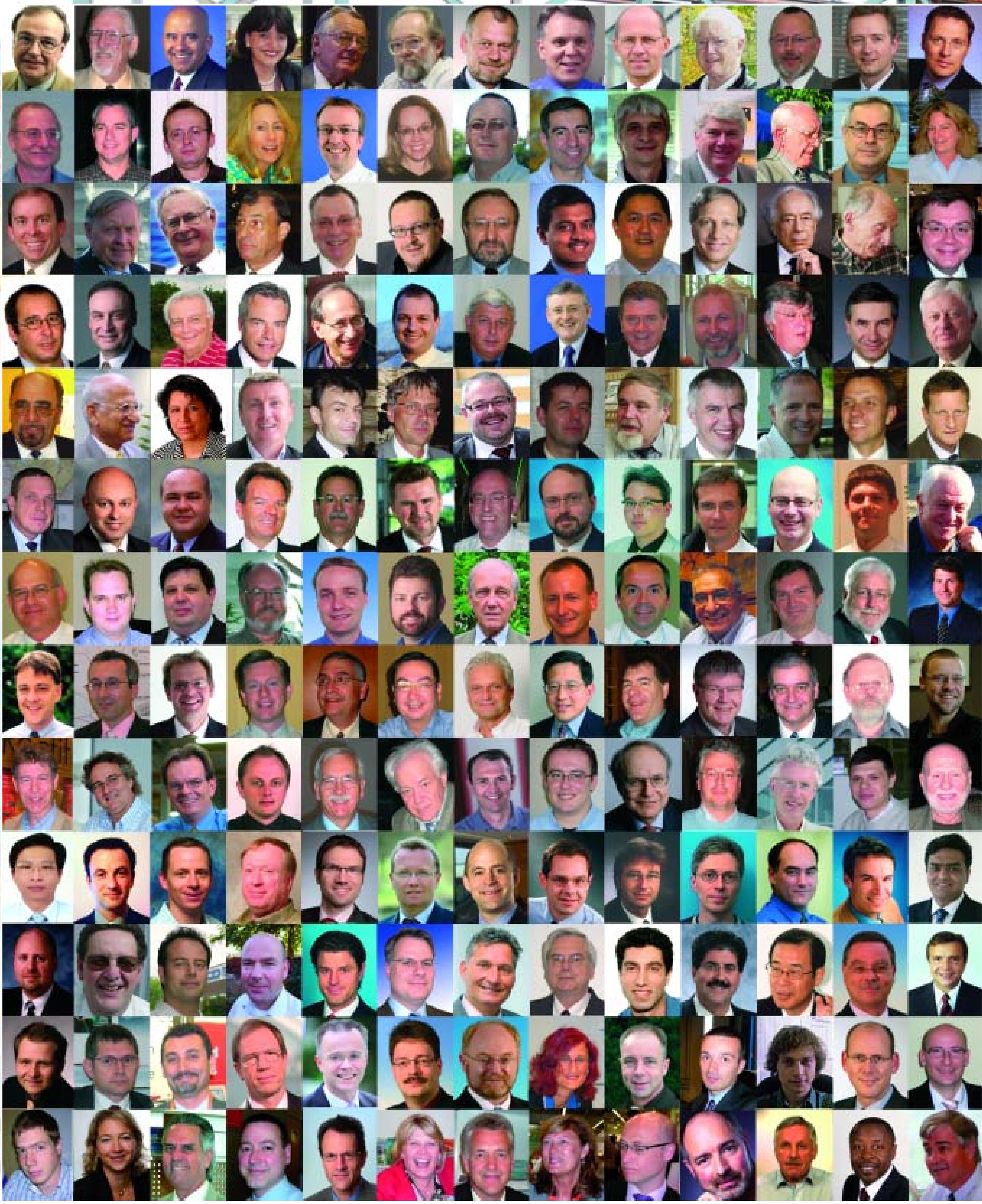
# The Gallery



Applications

# Expansion of Munich Technology Development Centre

FAIRCHILD SEMICONDUCTOR®
The Right Technology for Your Success™

The extended focus comprises

- Device and process simulation
- High Power Package development
- Technologists and Application experts for SuperJunction and Wide Bandgap Materials
- Automotive High Voltage Technical Marketing

The newly formed R&D centre, located in Munich, provides opportunities to new members to closely work with existing global Fairchild Technologists in US, Sweden and Korea, as well as to work in partnerships with Research institutes and hand selected partnership programs with competitors.

## Packaging Development Engineer

*Job description:*
You will be responsible to investigate new materials for the power semiconductor packaging, develop new packaging technologies and processes. You will define the design of new power semiconductor packages based on requirements from different applications in terms of functionality, quality and costs. Moreover you will support the assembly lines in the assessment and introduction of new assembly processes and equipment.

*Job requirement:*
We are looking for highly innovative and self-motivated individuals with a Master or PhD degree in Microsystems Technology, Material Science or Physics. At least 4 years experiences in the design of power semiconductor packages are desired. Mechanical and thermal simulation skills, experience with 3D mechanical CAD experience is of advantage.

## HV Technical Product Marketing Manager

*Job description:*
Work with automotive OEM's and suppliers to understand EV/HEV projects, requirements, and timing. Develop Fairchild product roadmaps for HV IGBT's, MOSFET's, Rectifiers, and Gate Drivers aligned with business strategy and opportunities and interface with Technology Development to coordinate technology roadmaps. Develop business cases for product developments and champion through the process. Launch new products, manage roll out and promotions to achieve objectives. Interface with automotive sales, providing product technical training and support.

*Job requirement:*
We are looking for innovative and self-motivated individuals, Master degree in Electrical Engineering, Physics or similar is a must, business background and Automotive experience is an advantage. At least 3 years of professional experience required.

## Device Simulation/Technology Experts

*Job description:*
Development and architectural innovation for Fairchild´s next generation High Voltage power devices including IGBT, SuperJunction FETs, SiC and GaN devices. You will be closely collaborating with teams in Sweden, US and Korea for process and package development.

*Job requirement:*
We are looking for highly innovative and self-motivated individuals, Master or PhD degree in Electrical engineering, Physics or similar. At least 3 years of professional experience required.

## Application and Marketing Manager, Silicon Carbide Technology

*Job description:*
You will be adding value to the systems of our customers, and at the same time realize and enabling the true value of Fairchild´s SiC components. You are a strong driver and will develop yourself towards a leading role and towards truly technology based business and market development.
Your knowledge of manifold approaches on power stage design impacts the rest of the system, e.g. cooling, control and filtering will enable novel power conversion designs to make use of the superior performances of our silicon carbide components.

*Job requirement:*
We are looking for highly innovative and self-motivated individuals with Master or PhD degree in Electrical engineering, Physics or similar. You have collected a solid background as power electronics designer in the power conversion industry and a deep understanding of power devices and converter systems.
At least 5 years of professional experience required. The location of this role could be either Kista/Sweden or Munich/Germany.

PCIM **Booth 11-320**

## We offer:

Start-up spirit in highly inspirational and expanding team in Munich; space for fundamental and scientific research; very competitive, performance oriented compensation schemes; high strategic impact and visibility within a global company.

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Free Subscription to qualified readers

Bodo´s Power Systems
is available for the following
subscription charges:
Annual charge (12 issues) is 150 €
world wide
Single issue is 18 €
subscription@bodospower.com

circulation ASC audit since 09/2008 print run 20 000

Printing by:
Central-Druck Trost GmbH & Co
Heusenstamm, Germany




## Events

**PCIM Europe,**
Nuremberg Germany, May 8th-10th
www.mesago.de/de/PCIM

**SMT Hybrid,**
Nuremberg Germany, May 8th-10th
www.mesago.de/de/SMT/home.htm

**Simulation in Automotive Lightweight,**
May 9th-10th www.vdi.de/simulationlightweight

**Sensor + Test,** Nuremberg Germany,
May 22nd-24th www.sensorfairs.de

**IMEC Technology Forums,**
Brussels, Belgium, May 22nd www.imec.be

**SiC work shop,**
Kista Sweden, May 27th-28th
www.b2match.com/isicpeaw2012/

**Technology in Electromobility,**
June 4th-5th www.vdi-wissensforum.de

**ISPSD 2012,** Bruges Belgium,
June 3rd-7th www.ispsd2012.com/

**Intersolar,** Munich Germany,
June 11th-15th www.intersolar.de/

**PCIM ASIA,** Shanghai China,
June 19th-21st www.pcimasia.com/

**CWIEME,** Berlin Germany, June 26th-28th
www.coilwindingexpo.com/

# One Hundred and Four Pages – a Big Edition!

This record breaking number results from the strong support of my contributors, from all areas of power, from around the globe. The theme throughout this issue is quality and reliability in IGBT Modules. It begins with cleaning the substrates for assembly, as described by Zestron – no matter how you mount the die you need a homogeneous contact. Die attach solutions come from materials manufacturers like Indium and Heraeus, while Thermacore explains how to optimize heat extraction. The article from Dr. Poech demonstrates how double-sided cooling improves system reliability. Overall this means no voids and a constant thickness for contacts. Sonoscan shows inspection solutions to insure proper solder thickness and void free die mounts.

Prof. Wolfgang reports from the recent Conference on Integrated Power Electronic Systems (CIPS) that the focus is on reliability. Traction applications need locomotives that work for decades. Offshore wind power requires very high levels of reliability, as windmills are typically out of easy reach for service or maintenance. The same applies to solar panels and inverters mounted on rooftops. These power systems all require a higher level of quality than consumer electronic products. If your TV or stereo fails, you can easily replace it with a new one.

The PCIM Europe in Nuremberg, together with SMT Hybrid Packaging, will highlight the synergy between power components, module manufacturing, and applications. May 8th, 9th and 10th will be busy days. Tutorials start even earlier, on the 6th.

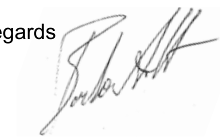
The Podium Discussion I lead will take place at the Forum in Hall 12, Booth 670, on Wednesday the 9th from 12:20 to 13:20. This year’s panel topic is “Efficient DC/DC Conversion.” Experts from the semiconductor industry will present a comprehensive message and then engage with the audience for questions and discussion.

Communication is the only way to progress. We delivered twelve issues last year and will continue this year each month, on time, every time. So far this year we have published 360 pages which result into 64 articles, and as a media partner, Bodo’s Power Systems is internationally positioned. Do not miss our Chinese version: www.bodospowerchina.com .

**My Green Power Tip for May:**
While attending the PEMD conference in Bristol, I saw police there using horses to control traffic and walking around the town on foot. This is a great green approach.

**See you in Nuremberg**

Best regards



## Power Integrations Agrees to Acquire CT-Concept Technologie AG

Power Integrations announced that it has signed an agreement to acquire privately held CT-Concept Technologie AG (known as CONCEPT) for approximately 105 million Swiss francs in cash, or about US$115 million, net of cash assumed.
Founded in 1986 and based in Biel, Switzerland, CONCEPT is a developer of highly integrated, energy-efficient drivers for high-voltage IGBT modules. The company's products are used in a range of high-voltage power-conversion applications including industrial motor drives, renewable energy generation, electric trains and trams, high-voltage DC transmission, electric cars and medical equipment. CONCEPT employs approximately 65 people and holds 14 patents with additional patents pending.
Balu Balakrishnan, president and CEO of Power Integrations, commented: "Our strategic focus is to offer the most innovative high-voltage power-conversion products across an ever-wider range of power levels and applications. CONCEPT fits perfectly within this strategy. Their innovative products bring integration, reliability and energy efficiency to very high-power applications — the same attributes we bring to lower-power applications.

*Balu Balakrishnan(l) and Wolfgang Ademmer (r)*

"CONCEPT's addressable market, already approaching $500 million, continues to expand with the growth in renewable energy, electric vehicles and high-efficiency industrial motors, and the efficacy of these clean technologies depends on cost-effective, efficient, reliable power electronics like CONCEPT's market-leading IGBT drivers. These dynamics make CONCEPT an extremely attractive business and an exciting addition to our company."
CONCEPT's management team and employees will remain at the company's Biel headquarters, which will become Power Integrations' center of excellence for high-voltage driver design. Wolfgang Ademmer will continue as president of CONCEPT and will also become a vice president of Power Integrations, reporting directly to Mr. Balakrishnan.
Mr. Ademmer commented: "We are very pleased to become part of Power Integrations, a company that shares our singular focus on delivering the most innovative power-conversion products for our respective end markets. Power Integrations' scale and vast customer base will help us accelerate the adoption of our products around the world. As part of Power Integrations, we can strengthen our unique position in the value chain providing innovative driver technology compatible with all major IGBT module manufacturers."

**PCIM Booth 12-102**

**www.igbt-driver.com**

## New IC Design Center in Tucson, Arizona

Cirrus Logic Inc. is expanding its operations in Tucson, Arizona USA, with the opening of a new 25,000 square foot IC Design Center on the city's northwest side. The Apex Precision Power™ technology business unit is based in Tucson and has more than 100 employees. Cirrus Logic has outgrown its existing office and lab space due to continued growth in IC product design activities. Design and manufacturing for Cirrus Logic's APEX hybrid products will continue at the company's original 50,000 square foot facility.
Cirrus Logic's IC design center will be the majority tenant inside a 3-year old office building located at 8950 North Oracle Road in the Tucson suburb of Oro Valley. A 35-member power analog IC design team, comprised of design engineers, product test engineers and layout engineers, will move into the leased office space just a short 10 minute drive from the manufacturing facility. A total of 8,900 square feet of lab will be built out on the building's first floor, which is shared with two other tenants. All 18,000 square feet of the building's top floor will be occupied by Cirrus Logic engineering staff in a collection of 33 works stations and 28 formal offices. The floor plan also includes four conference rooms, a dining and recreation area and two outside patios so staff can enjoy the scenic mountain views.
The most anticipated aspect of this move is the opportunity to build custom lab space to support the IC team whose design work targets audio and motor control markets. Work is underway now to create areas for infrared camera/thermal imaging product testing, temperature testing and a certified sound room. The latter boasts a sound drop of 45db across the complete sound spectrum to achieve normal conversation levels outside the lab.

**www.cirrus.com**

## High Power Cable Assemblies and Connectors for Power

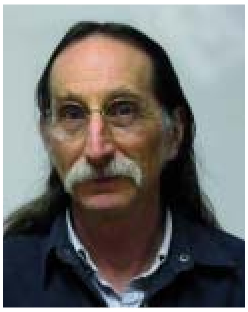
Richardson RFPD, Inc. announced it has completed a global distribution agreement with TRU Corporation, a leader in the design, development and manufacture of custom, high performance RF/microwave interconnect solutions. TRU's sophisticated, durable High Power cable assemblies provide power handling capabilities up to 6 times better than traditional RF assemblies. Their custom cable assembly capabilities provide expertise in power handling techniques, and are utilized to build a wide range of assemblies, sometimes over 100 feet. TRU's range of cables and connectors for High Power functions creates an opportunity to provide unique assemblies for niche applications.
In addition to their distinctive High Power cable assembly capabilities, TRU also offers a wide range of standard and unique RF connectors. Their EIA and MEIA line of connectors are specifically produced for High Power applications. These products provide Richardson RFPD with a complete power connector offering for their renewable energy, power conversion and interconnect customers.
Richardson RFPD's worldwide field sales engineering teams are now assisting design engineers in integrating TRU connectors and cable assemblies into High Power designs. For technical information or to explore TRU products online, please visit the TRU storefront on the Richardson RFPD website.

**PCIM Booth 12-235**

**www.trucorporation.com**

**www.richardsonrfpd.com**

# Patent Office Approves 6th CogniPower Patent



CogniPower announced the approval of the sixth patent in its growing portfolio of tools for more agile and efficient switched mode power conversion.Patent Application #12358465, "Apparatus and Method for Recycling the Energy from Load Capacitance" will issue as Patent Number 8134347. It describes a new way to conserve electrical energy.
According to Founder, Tom Lawson, "The patent covers a basic principle of recovering electric energy when switching a device off. Power need not always flow from source to destination. When a device is shut off, the energy stored in filter and load capacitance in the device normally bleeds off unproductively and is lost. This patent shows a way to draw that energy back, so that it is available for future use."
Often, equipment is left always ON, though it is actually used only a small percentage of the time. With this new technology, circuitry can be turned OFF when not in use, even when the OFF period is short. Prime applications include non-volatile memory and other computer I/O circuitry.
As the geometry of newer computing chips continues to shrink, the percentage of power lost to leakage increases. Energy saving strategies like slowing or stopping a computer's clock are no longer enough. It is better to reduce or remove the power supply voltage, but only if the stored energy can be recovered. The mechanisms for accomplishing energy recovery are patented here, with support from other enabling CogniPower patents.
Energy recovery is one of many techniques that become practical given the agility and flexibility of CogniPower switched mode power control technology.

**www.cognipower.com**

## Russian Semiconductor Industry Envisions 65nm Technology and Beyond

Heinz Kundert, president, SEMI Europe visited Russia after the Presidential elections on March 4th, he is now more optimistic about better investment conditions for semiconductor and related technologies in the years to come. Based on interactions with representatives of the government, industry, science and investment funds, he believes that the industry as a whole can expect more funding. Furthermore, Russians accession to the WTO will reduce import taxes close to zero by the end of 2012. There is also a noticeable sense of urgency about removing trade barriers and other time-consuming bureaucracy, especially for high-tech products.
Sitronics (Mikron) and Angstrem remain flagship companies in the Russian semiconductor industry. Both companies will further invest into "More than Moore" applications. Mikron has just opened a new fab with 200mm and 90nm nodes; it has also announced plans to build a new fab for 300mm and 65nm. The odds for the new fab are good; however, the outcome will depend on government funding. Angstrem will finally complete the Angstrem-T project that has been pushed out for some time. It seems that financing is secured. They expect first devices coming out of the new line by 2014.
Crocus Nano Electronics (CNE), a joint-venture between Santa Clara-based Crocus Inc. and the Russian national investment fund Rusnano, burst onto the scene with investment of around US$ 300 million. Their plan is to enter the MRAM market with 90nm, 65nm and finally even 45nm node size. CNE will address key markets such as storage, mobile communications, networking and cloud computing.
Skolkovo, the so-called"Russian Silicon Valley" seems to be shaping up. According the Skolkovo IT cluster representatives, there are already 170 applications of start-up companies who announced interest in doing research in the Skolkovo Science Park and 40 of them have already received grant approval. Eligible companies will move into the Skolkovo Science City as of 2013. Investments are mainly done for research equipment and activities.
SEMICON Russia will be held from May 14-16 in Moscow (www.semiconrussia.org).
SEMI strongly supports the industry development in Russia. SEMI is involved in industry advocacy and public policy, working with high-ranking government officials. The annual SEMICON Russia exhibition and technical conferences support the industry.

**www.semi.org/europe**

**www.pvgroup.org**

# Technology Distributor Launches e-Newsletter

Richardson RFPD, Inc., an Arrow Electronics Company, announces it is now accepting subscription requests for its quarterly e-newsletter highlighting the latest new products from the leading suppliers of RF, Wireless and Energy technologies.
Electronic design engineers and buyers looking for product details and purchase information on recently released components and solutions will find easy, one-click access to specifications for featured products, as well as links to supplier storefronts, technical articles, design tools, recent news, and upcoming events.
The New Products E-Newsletter is part of a best-in-class New Product Introduction (NPI) program, designed to provide Richardson RFPD's supplier partners with maximum exposure to design engineers developing the next generation of products for applications in aerospace and defense, broadcast transmission, machine-to-machine (M2M), renewable energy, and wireless infrastructure markets.
To subscribe to the Richardson RFPD New Product News E-Newsletter, visit

**PCIM Booth 12-235**

**www.richardsonrfpd.com/subscribe**



# SEMICON West 2012

SEMICON West 2012 connects contemporary and advanced innovations from the world's leading technology companies with the engineers, designers, scientists, and key decision-makers needing answers and solutions that improve performance and productivity and help move products to market. Learn about the latest developments in semiconductor manufacturing and explore new opportunities in emerging and adjacent markets such as LEDs, MEMS, and solar/PV. Choose from more than 50 hours of technical and business sessions and events, including FREE technical presentations at the TechXPOT stages, and visit the more than 400 exhibiting companies. Be there, Moscone Center, San Francisco, CA, July 10-12, 2012.

**www.semiconwest.org/?=bpn**

# "SKillbox" with 16 Components Designed to Help Students

Semikron has put together a SKillbox to show students the different packaging technologies used in power electronic systems. The first 23 boxes were handed over today during a visit of Bavarian university professors at Semikron.

The Semikron Skillbox is a collection of 16 power electronic components such as dismantable assemblies and cross-sectional components, designed especially for use in power electronic classes. The SKillbox was designed as an important visual aid for explaining the main packaging concepts used in power electronic systems," explains Dr. Uwe Scheuermann, who is responsible for component reliability at Semikron, is one of the key project managers in the Skillbox project, and contract lecturer in the area of electronic packaging at the University of Erlangen. The box also comes with information on module specifications and application areas and includes, for example, the pressure-contact module SKiiP3, which is used in wind turbines and elevators, as well as driver module SKYPER 32 Pro, which is used to drive IGBT modules. Also in the box are, for example, bipolar pressure-contact modules, disc-type components and the spring-contact module MiniSKiiP for solder-free PCB mounting.

*First 23 Skillboxes handed over during Bavarian professors' visit to SEMIKRON*

"We are involved in numerous research projects with universities and colleges," explained Dr. Thomas Stockmeier, Chief Technology Officer at Semikron during a visit by university professors which was organised by the European Center for Power Electronics and the Bavarian Power Electronics Cluster. "Our close cooperation with universities and colleges delivers important impetus in the area of research and development, and draws new talent to us at the same time. Active participation in eminent networks such as ECPE, the Bavarian Power Electronics Cluster and Energieregion Nürnberg is important added value for Semikron."

**PCIM Booth 12-415**

**www.semikron.com**

# Need High Power Inverter Design Support?

## Components > Designs > Assemblies

From active and passive component selection to development of complete assemblies, Richardson RFPD can help find the best solution for every high power (>10 kW) inverter design.

**Specializing in:**

- Global engineering and technical support for high power design projects
- Design and assembly of power semiconductor assemblies, power passive assemblies and inverter subsystems

**Component design-in from industry-leading suppliers:**

CDE Cornell Dubilier – Capacitor Solutions for Power Electronics
CONCEPT – Intelligent Power Electronics
KEMET – The Capacitance Company – Charged®
Kendeil
Maxwell Technologies
Microsemi – Power Products Group
Mitsubishi Electric
Ohmite
Priatherm
Recom
Tamura
Vincotech

Reduce development cost and time-to-market. Put Richardson RFPD's 30 years of high power assembly and design expertise to work for you.


pcim Booth 12-235

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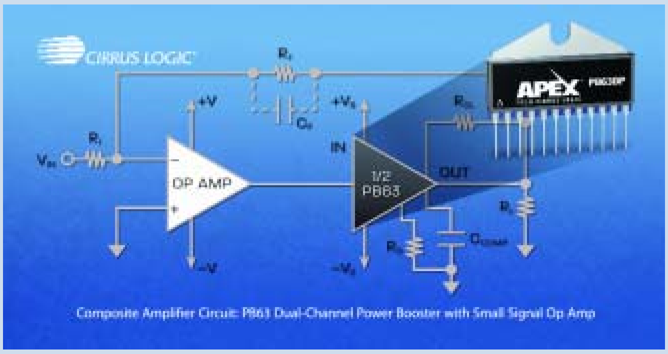
# Dual Power Booster Triples Speed Performance for Semiconductor and Flat-Panel Display Test Equipment

Cirrus Logic Inc. is expanding its popular and versatile Apex Precision Power® booster product family with a new dual-channel booster amplifier, the PB63. With a 1,000 V/µs slew rate and 1 MHz of power bandwidth, the PB63 accelerates power booster performance 300 percent compared to the company's previous industry benchmark power booster products. By pairing the economical "double booster" PB63 with one or two low-cost op amps, semiconductor and flat-panel test equipment manufacturers can now realize a combination of improved test equipment efficiency and productivity – in a more cost-optimized solution compared to traditional high-voltage amplifiers.


The PB63 features voltage operation of ±20 V to ±75 V and continuous output current drive capability of up to 2 A and is designed to provide both voltage and current gain when paired with a small signal, general purpose operational amplifier. This approach allows the user to optimize the accuracy, off set, input noise and settling time of the composite circuit.

"Through the PB63 booster amplifier, Cirrus Logic delivers the high-voltage performance our customers require, along with a significant speed boost, without having to turn to more expensive amplifier products to get the job done," said Greg Brennan, vice president and general manager, Cirrus Logic's Apex Precision Power® business unit. "Being able to pair the PB63 with an op amp of their choosing enables a flexible, cost-effective approach that allows OEMs to tailor performance for their applications."

The dual-channel amplifier design of the PB63 provides added value for high density board designs, such as pattern generators in flat panel display inspection systems, deflection circuitry in semiconductor inspection systems, scientific scanning electron microscopes, piezoelectric drivers in printer heads for industrial ink jet printers, and programmable power supplies in semiconductor automated test equipment.




Composite Amplifier Circuit: PB63 Dual-Channel Power Booster with Small Signal Op Amp

**Evaluation Kits, Pricing and Availability**

The PB63 is packaged in a 12-pin PowerSIP that affords additional savings on valuable board space, with a footprint that measures less than 1.5 square inches. It is available in sample quantities for evaluation and prototyping, as well as volume production and is priced at $128.94 USD in 1,000 quantities. The EK47 evaluation kit is available and includes a demo board and all associated hardware. Complete product information is online at www.cirrus.com. For technical support, contact Apex Precision Power product support at 800-546-2739, or apex.support@cirrus.com.

Cirrus Logic develops high-precision, analog and mixed-signal integrated circuits for a broad range of innovative customers. Building on its diverse analog and signal-processing patent portfolio, Cirrus Logic delivers highly optimized products for a variety of audio and energy-related applications. The company operates from headquarters in Austin, Texas, with offices in Tucson, Ariz., Europe, Japan and Asia. More information about Cirrus Logic is available at:

**www.cirrus.com**

Cirrus Logic, Cirrus, Apex Precision Power and APEX, are trademarks of Cirrus Logic Inc. All other product names noted herein may be trademarks of their respective holders.

# Compact 600V ICs for Energy Efficient Inverterized Motor Drive Applications

International Rectifier has introduced the IRS2334SPbF and IRS2334MPbF three-phase 600V ICs for inverterized motor drives used in energy efficient appliance and industrial applications.

The IRS2334SPbF is offered in an SOIC20WB package while the IRS2334MPbF is available in a QFN5X5 package featuring a footprint of just 25mm2 and designed with the appropriate creepage and clearance requirements to enable rugged and reliable designs at voltages up to 600V.


Inverterized motor drives offer efficiency greater than 80 percent compared to standard on/off drives that deliver less than 50 percent efficiency. The IRS2334SPbF and IRS2334MPbF offer a compact solution and simpler implementation that enable designers of applications such as power tools, refrigerator compressors and electrically controlled fans to utilize energy efficient inverters with the smallest form factor.

The IRS2334x family provides comprehensive protection including proprietary negative voltage spike (Vs) immunity for safe operation under extreme switching conditions and short circuit events. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channel can be used to drive N-channel power MOSFET or IGBTs in the high-side configuration.

The new ICs utilize IR's advanced high-voltage IC (HVIC) process which incorporates next-generation high-voltage level-shifting and termination technology to deliver superior electrical over-stress protection and higher field reliability. The IRS2334x feature under-voltage lock-out protection, integrated deadtime protection and shoot-through protection. Other features of the new devices include advanced input filter, lower di/dt gate driver for better noise immunity, output in phase with inputs and 3.3V input logic compatibility.

Production quantities are available immediately. The devices are RoHS compliant and datasheets are available on the International Rectifier Web site at www.irf.com.

Device Specifications:

| Part Number | Package | $V_{OFFSET}$ (V) | $I_{O+}$ / $I_{O-}$ (Typical) | $T_{ON}$ / $T_{OFF}$ (Typical) |
|---|---|---|---|---|
| IRS2334SPbF | SOIC20WB | 600 | 200mA / 350mA | 530ns |
| IRS2334MPbF | QFN5X5- 28L | 600 | 200mA / 350mA | 530ns |

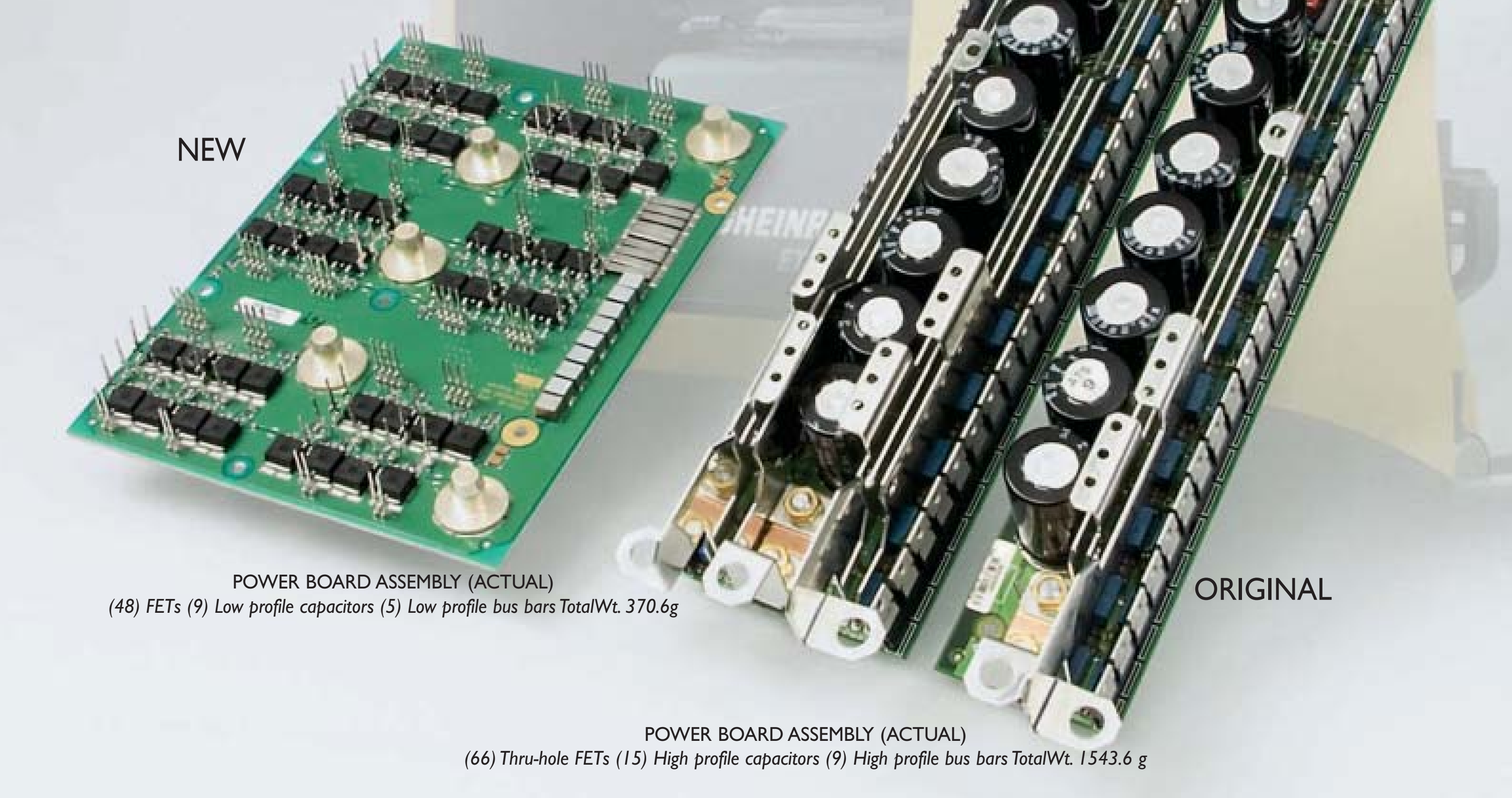
Production quantities are available immediately. The devices are RoHS compliant and datasheets are available on the International Rectifier Web site at www.irf.com.

International Rectifier is a world leader in power management technology. IR's analog- and mixed-signal ICs, advanced circuit devices, integrated power systems, and components enable high-performance computing and reduce energy waste from motors, the world's single largest consumer of electricity. Leading manufacturers of computers, energy-efficient appliances, lighting, automobiles, satellites, aircraft, and defense systems rely on IR's power-management benchmarks to power their next generation products.

**www.irf.com**

**Visit us at PCIM Europe, 8th – 10th May 2012, Hall 11, 111**

# Bergquist Thermal Clad Turns Big Power Modules Into Small Powerhouses.




POWER BOARD ASSEMBLY (ACTUAL)
*(48) FETs (9) Low profile capacitors (5) Low profile bus bars Total Wt. 370.6g*

POWER BOARD ASSEMBLY (ACTUAL)
*(66) Thru-hole FETs (15) High profile capacitors (9) High profile bus bars Total Wt. 1543.6 g*

## With Thermal Clad® Jungheinrich Forklift Converted All The Power Into Half The Space.

### Bergquist Thermal Solutions let you increase power capacity without adding size.

Jungheinrich, a leading European forklift manufacturer, needed to reduce their motor control size and cost while maintaining power output levels. Thermal Clad insulated metal substrates (IMS®) allowed their engineers to replace high profile thru-hole FETs, capacitors, and bus bars with fewer low profile, surface mount components.

This sleek new design reduced package size by over 50%, all without sacrificing a single watt of power. Thermal Clad's unique dielectric coating dissipates heat more efficiently than FR-4 or other PCBs – ideal for high watt-density applications such as motor control.

*"We needed to reduce our processing cost, it was too labor intensive. With Thermal Clad we were able to automate, dissipate the heat better, and reduce our size by at least 50%."*
*Stephan Taube*
*Electronic Development Engineer of Jungheinrich Forklifts*

### Automated assembly lowers manufacturing costs.

Cooling with Thermal Clad IMS eliminates the need for heat sinks, clips, fans and other discrete components that increase package size and require costly manual assembly. Now, using surface mount technology, Jungheinrich was able to automate much of the assembly process thus reducing cycle times and long-term manufacturing costs.

### Get your FREE Sample.

To qualify for a FREE Thermal Clad Select Sample, please visit our web site or call today.

FREE Select Sample.

Call **+31 (0) 35 5380684** or visit **www.bergquistcompany.com**

Booth 12-632

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**Thermal Materials • Thermal Substrates • Fans and Blowers**

# Power Electronics Engineers – a Rare Breed

*By Alfred Hesener, Senior Director Applications & Marketing, Fairchild Semiconductor*

In many economies throughout the centuries, only materials and energy were considered resources, but not IP or human resources. That is changing now, as all industries, and in particular electronics and semiconductor companies, are forced to reduce their usage of materials and energy, but at the same time technology is becoming more and more complex. This shift in priority and value of resources is however not in line with what is happening on the job market for engineers right now.

In a media-hungry, "digital" world, power electronics as a profession doesn't have a very exciting reputation, although the same factor that is driving many companies and economies to change, namely, energy cost, is at the center of very visible activity that is influenced by power electronics, like renewable energy, electro-mobility, power distribution, energy consumption of appliances, solid state lighting, and others. So where does that disconnect come from?

It seems at first glance that in power electronics most of the important discoveries have already happened. Topologies don't change much, power switch performance is approaching a "glass ceiling", and increasingly complex control ICs take care of all the functions so engineering intelligence is no longer required. But is that really the case?

In fact, power electronics as an engineering discipline has never been as exciting as it is right now. We are right on the edge of many important developments: New power switch technologies, like SiC or GaN, are coming to market, there is a huge demand for new power electronics subsystems in many, many applications, and people are starting to understand that engineers can do better things than nuclear power plants or bridges, things that actually contribute to improving both the quality of our lives as well as the environment.

Considering all this, it is understandable that good power electronics engineers are difficult to find. This also makes the recent decision of the German government to reduce the funding for PV systems even more difficult to understand. What used to be a innovative, industry-leading sector "Made in Germany" is now, only a few years after its boom, facing very difficult times. And the reason that was given was the cost for the electricity consumer – not considering all the hidden cost that has to go into treating nuclear waste, as the current difficulties of the German government handling the nuclear storage facility in Asse (Niedersachsen, Germany) amply demonstrate.

With the disconnect between strong demand in many applications, and little supply of good engineers, our hopes must rest on the Universities. But few good power electronics students are making it through, it seems that the perception of the population also has a lot of impact on what is happening there. As a result, the little talent that exists converges in a few companies, that in turn become market leaders, and the large number of small and medium size enterprises that is the backbone of industrial innovation in Germany and other industrialized countries, is starting to suffer.

It is important that we take care of our engineers. In the past, the work conditions of engineers were not the best – offices were not attractive, equipment was not good, training and career development were difficult topics to address. In the 90'ies, when I started, there were plenty of engineers, and they had to develop and deliver results. They still have to do that now, but our understanding of a motivating work environment, proper work-life balance, and achieving premium results and innovation has progressed significantly. After all, it is these results and innovations that are the source of competitiveness of the industrialized countries like Germany.

At Fairchild, we aim to provide exactly that. A motivating work environment must comprehend a workplace that considers all important factors for our engineers. We design our office spaces, like in our new TDC (Technology Development Center), to be motivating and uplifting. All the human factors must be considered, from ergonomics to a healthy choice of lunch. Equally important is the availability of leading-edge equipment, so that new ideas can be tested and verified quickly and easily. Combined with a good team spirit and information exchange, this attracts the more experienced engineers, allowing to address what hat may be the most important factor nowadays, the know-how. Experts communicating with each other will not only find good solutions faster, it is also a much more motivating environment for them. Personal development and career progression for engineers must include technical skills to a large extent – it is the value they are carrying around with them, that nobody can take away. It is therefore not surprising that at Fairchild a large variety of technical trainings and information exchange possibilities is available, from informal "lab rounds" to a large library of training modules. Even beyond is the possibility to participate in trainings as a trainer, like in Fairchild's Power Seminar series, sharing what our experts know as well as improving one's own understanding.

We have come a long way since the old days, but the decision to work in this exciting field must happen in your own mind.

**PCIM Booth 11-320**

**www.fairchildsemi.com**

# CIPS 2012 – Reliability is Improving by Orders of Magnitude

## *235 engineers and scientists attended the conference.*

*Attendees came from 17 countries in Asia, America and Europe. CIPS 2012 stands for the 7th International Conference on Integrated Power Electronics Systems. The conference is organized by ETG, the Power Engineering Society within VDE and co-organized by ECPE, the European Center for Power Electronics. IEEE PELS and ZVEI are technical co-sponsors.*

*By Prof. Eckhard Wolfgang, ECPE*

The program for this year's conference included 14 conference sessions with the presentation of 77 technical papers: Three Keynote papers, 9 Invited papers, and 65 regular papers. 25 of the regular papers were presented in the dialogue/ poster session. It is worth to mention that 22 of the papers are coming from industry, 19 from a joint cooperation between industry and academia, and 36 from academia alone.

The main focus of the contributions was on system integration, packaging, high power modules, wide band gap components, magnetic components and EMI, and systems and components reliability.

The conference was opened by a keynote paper on "Extreme Efficiency Power Electronics" presented by Prof. Johann Kolar/ ETH Zurich. His studies are based on a generalized description of degrees of freedom and selected measures for efficiency improvement of power electronics converters. The analysis starts with loss calculations and measurements of all components of the converter. Always a compromise has to be made between efficiency and power density. A control strategy is outlined which ensures maximum efficiency for partial loads. The efficiency of telecom rectifier modules e.g., has been improved from 92% in 1995 to 97% in 2012. Likewise for photovoltaic converters an increase from 93 to 99% has been achieved for Si power semiconductors.

Three sessions dealt with reliability, although it was an issue of many other presentations as well. Prof. Patrick McCluskey/ CALCE University of Maryland, USA, gave an overview in his keynote speech on "Reliability of Power Electronics Under Thermal Loading". He discussed the dominant failure mechanisms in components, including the power module, capacitors and boards. Specific focus was placed on the power module interconnects including wirebonds, planar interconnect, die attach and substrates, and the reliability concerns associated with increased power levels, increased power density, and higher junction temperatures. Ways of improving packaging design were presented.

Nine invited speakers presented overviews on topics like:

"Advanced Cooling for Power Electronics": Dr. Sukhvinder Kang/ Aavid, USA, described an improved heat sink with staggered fins which means an increased fin density along the air flow direction. This results in an uniform baseplate temperature of the IGBT module. Regarding liquid cooling helicoidal flow paths were introduced which create a strong secondary flow with high velocity to achieve a high heat transfer coefficient at the flow channel wall and parallel flow paths to reduce liquid velocities and the corresponding pressure gradient.

"Analysis of Innovative Packaging Technologies and Trends for Power Modules": - A. Avron/ Yole Development, France

"Electromagnetic Modeling of EMI Input Filters": Dr. Ivana Kovacevic/ ETH Zurich, Gecko Research GmbH, Switzerland, discussed an efficient design method for EMI filters and power converter systems regarding both electrical functionality and EMC design constraints using GECKO EMC for simulations.

"Combined Reliability Testing: An Approach to Assure Reliability under Complex Loading Conditions": Dr. Olaf Wittler / Fraunhofer IZM, Berlin investigated combinations of thermal cycling and vibration as well as moisture and vibration.

Integrated Power Electronics has to include passive components as well, and therefore the development of magnetic components and integrated filtering was treated in two sessions. New ways to integrate such components even monolithically using appropriate add – on – technologies will become important for advanced integrated power electronics.

Important results concerning the integration of magnetics in the low power regions were treated in the invited paper "Integrated, High Frequency DC-DC Converter Technologies Leading to Monolithic Power Conversion": Dr. Ashraf Lofti, Enpirion Inc. USA,Q. Li, Prof. Fred Lee/ Virginia Tech, USA

"Integrated High Power Modules": Prof. Mark Johnson/ University of Nottingham, UK. Constraints and possibilities for higher level integrations from several aspects were treated comprehensively.

"SiC and GaN Devices – Competition or Coexistence?": Prof. Nando Kaminski/ University of Bremen, Dr. Oliver Hilt/ FHB Berlin. It was the aim of the authors to find fields of possible applications for both groups of devices. Currently, it seems that GaN-transistors are ideal for high frequency integrated circuits up to 1000 V (maybe 2000 V) and maximum a few 10 A current while SiC devices are rather suited for discrete devices or modules with breakdown


All the power you need...
...for highest reliability applications

voltages abov 1000 V and basically no limit in current. Only Schottky-diodes are in direct competition and it looks like an either-or situation determined by the GaN material quality and cost. The packaging, however, is more and more the limiting factor for wide-bandgap devices and modules with respect to switching speed and high temperature operation.

„Planar Interconnect Technology for Power Module System Integration": Prof. Norbert Seliger/ HS Rosenheim, Karl Weidner/ Siemens Corporate Technology, Munich. For the first time SiPLIT® – the Siemens Planar Interconnect Technology was presented in a conference. This package features thick Cu interconnects on a high reliable insulating film for power semiconductor chip top contacts. Due to the conductor structure and contact technology, on-resistance and stray inductances are very low compared to state-of-the art wire bonds. In addition large area contacting improves the power cycling capability and surge current robustness significantly. SiPLIT® provides excellent possibilities for system integration, like double side cooling, integration of passives and sensors, etc.

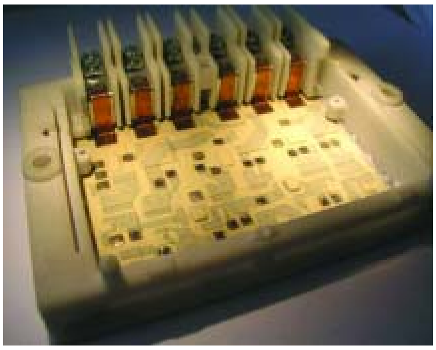

*Figure 1: Highly integrated prototype inverter module containing input rectifier, output inverter, current sensors and decoupling capacitors applying the Siemens planar interconnect technology SiPLIT®.*

"Reliability of Planar SKIN Interconnect Technology": Dr. Uwe Scheuermann / Semikron, Nuremberg, presented reliability data of the planar SKiN technology. This technology is based on three silver sintered layers: power chip attach on top side to a flexible circuit board, power chip attach to the DBC substrate, and DBC substrate to the heatsink. This solderless power module has the benefit of a very low thermal resistance. The active power cycling results are very impressing: For a temperature swing $\Delta$ Tj = 70 K (Tjmin = 80°C; Tjmax = 150°C), three million cycles can be achieved. The corresponding failure mode is a fracture in the Ag sintering layer between the chip topside contact and the flexible circuit board. In summary the improvement of power cycle lifetime in comparison to classical base plate modules applying a 70K temperature swing is 190 times for the SKiN technology.

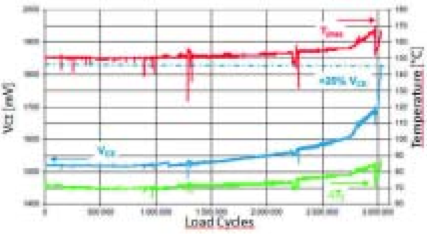


*Figure 2: Active power cycling result of a Semikron SKiN device for $\Delta$Tj = 70K. This is an impressive example for improvements by two orders of magnitude obtained from several new technlogies ( silver sintering in case of Semikron ).*

Nine regular contributions discussed silver sintering from different points of view: Dr. Karsten Guth et al/ Infineon Technologies, Warstein, compared two emerging technologies for the chip-to-substrate interconnect, namely diffusion soldering and silver sintering. Power cycling testing was chosen to give an application relevant assessment of the reliability performance. Compared with today's power cycling limit for Tj, max of 150°C, a 30 – 60 fold increase of power cycling reliability was found for both new technologies. The failure happened, however, not in the wire bonds but in the substrate material used.

Mrs. Silke Kraft et al./ Fraunhofer IISB, Erlangen, compared silver sintering DBC (copper metallization on ceramics) and DBA (aluminum metallization on ceramics). The setup with DBC showed a 17, the one with DBA a 2.7 times higher statistical lifetime than the soldered and wire bonded reference. Mrs.Kraft was elected as one of the two winners of the ECPE Young Engineers Award. The other winner is Gernot J Riedel/ ABB Corporate Research, Switzerland for his presentation on "Reliability of Large Area Solder Joints within IGBT Modules: Numerical Modeling and Experimental Results.

Further contributions came from: University and INSA Lyon; Virginia Tech and NBE Technologies; Oak Ridge National Laboratory; Osaka University; Heraeus; Danfoss Silicon Power; Safran Group and University of Bordeaux and Lyon. This represents just a part of worldwide activities in this field. Major goals are reduction of the mechanical force and easier manufacturability.

The conference was closed by a keynote on "SiC Device and Power Module Technologies for Environmentally Friendly Vehicles" which was presented by Dr. Kimimori Hamada/ Toyota Motor Corporation, Japan. He pointed out advantages by using SiC modules due to their higher operation temperature of SiC of 250°C in comparison to 150°C for Si modules. Cooling can be done at higher coolant temperatures with higher cooling power. He explained the necessity for new materials which can withstand higher temperatures as well as higher temperature swings. Toyota is focusing on SiC MOS switches, but several improvements have to be made, like reducing crystalline defects, achieving high electron mobility, and ensuring high reliability of the gate oxide layer. In addition issues for power modules include the development of high-temperature die attaches, plastic sealing, and a high-temperature primer which has to secure the required reliability by adhering the device, lead frame, and plastic.

In summary the CIPS 2012 has sharpened the focus towards system integration by new concepts for packaging and joining. Results of reliability investigations show potentials for increasing the lifetime by factors of 60 to 190. Such improvements will for sure change technologies for future power electronics systems very much, because the benefits are beside reliability electrical, mechanical and thermal too.

The organization committee decided to continue the CIPS in 2014 in March at Nuremberg.

*Figure 3: CIPS 2012*
*General Chair Prof. Leo Lorenz (center), Technical Chairs Prof. Dieter Silber (left) and Prof. Eckhard Wolfgang*

The peer reviewed papers are available in printed form (ETG-Fachbericht 133; VDE Verlag GmbH, Berlin – Offenbach; ISBN 978-3-8007-3414-6), on a CD-ROM and will be ready for downloading from the VDE Verlag digital library as well as from the IEEE digital data base Xplore in April.

**PCIM Booth 12-470**

**www.ecpe.org**

# Electronics Industry Digest

*By Aubrey Dunford, Europartners*

**GENERAL**

In 2011 worldwide TV shipments fell for the first time since 2004, slipping 0.3 percent to 247.7 M units, so NPD DisplaySearch. LCD TV shipments increased by 7 percent to just over 205 M units in 2011—a substantial slowdown from the double digit growth in previous years.

**SEMICONDUCTORS**

Worldwide semiconductor revenue is projected to total $ 316 billion in 2012, a 4 percent increase from 2011, so Gartner. The semiconductor industry is poised for a rebound starting in the second quarter of 2012, because the inventory correction is expected to conclude this quarter, foundry utilization rates are bottoming, and the economic outlook is stabilizing.

Europe's semiconductor industry continues to rank as the No. 1 industrial sector for R&D investment intensity, so the ESIA. This is the conclusion of the European Commission 2011 European Union Industrial R&D Investment Scoreboard, which annually calculates and ranks R&D intensity (investments over net sales) of 1400 listed companies worldwide. With a ratio of 14.8 percent of annual R&D expenditure over annual sales, the semiconductor sector's R&D intensity leads other sectors such as biotechnology or software as a High R&D intensity sector, with semiconductor R&D investments reaching € 3.4 billion in 2010 amongst the surveyed companies.

The emerging market for Gallium Nitride (GaN) power semiconductors is forecast to grow from almost zero in 2011 to over $ 1 billion in 2021, so IMS Research. One of the key reasons for the promising outlook for GaN power devices is because GaN is a wide bandgap material which offers similar performance benefits to Silicon Carbide (SiC) but has greater cost reduction potential.

Semtech, a supplier of analog and mixed-signal semiconductors, has acquired Cycleo for $ 5 M in cash. The stockholders will be able to earn up to an additional $ 16 M in cash based on the achievement of revenue and operating profit goals over the next four years. Headquartered in Grenoble, France, Cycleo develops IP for wireless long-range semiconductor products used in smart metering and other industrial and consumer markets.

Worldwide sales of semiconductor manufacturing equipment totaled $ 43.53 billion in 2011, representing a year-over-year increase of 9 percent, so SEMI. North America surpassed Taiwan as the region with the highest amount of spending with $ 9.26 billion in equipment sales. The Korea market claimed the second place for the second year in a row with $ 8.66 billion in sales; Taiwan fell to the third position with a regional decrease of 24 percent.

European sales of semiconductor manufacturing equipment totaled $ 4.22 billion in 2011, representing a year-over-year increase of 80 percent. The worldwide wafer processing equipment market segment increased 15 percent, the assembly and packaging segment decreased 14 percent, and total test equipment sales decreased 9 percent. Semiconductor fab equipment spending is expected to remain level in 2012, so SEMI. Eight companies, including Samsung and Intel, will keep their fab equipment spending level above $ 2 billion in 2012.

The Top 15 semiconductor equipment suppliers grew 13 percent in 2011, so VLSI Research. The lithography equipment suppliers, ASML and Nikon, grew 27 percent combined, more than twice the industry growth rate and ASML became the largest equipment supplier, in front of Applied Materials. Japanese equipment suppliers also recorded higher than average growth rates. Advantest led growth of the Japanese suppliers by recording 28 percent sales increase in 2011. Verigy acquisition contributed to Advantest's performance. Equipment spending was driven by aggressive capacity expansion in the foundry and logic sectors, the result of increasing demand for mobile devices.

Graphensic is a new company in Sweden that is a spin-off from Linköping University. The company aims to produce single layer graphene on hexagonal silicon carbide for the electronic equipment market. Graphene is the Nobel prize material which has created an astonishing range of new possible applications originating from its versatile properties. Among applications of epitaxial graphene on silicon carbide are next generation electronics, allowing faster technology changes in development of new devices for energy and environmental systems.

**OTHER COMPONENTS**

Heliatek has inaugurated the company's first production facility for the manufacture of flexible organic solar panels in Dresden. Based on organic semiconductor materials, these flexible solar panels offer greater freedom of use than conventional photovoltaic products. The company has invested € 14 M in the construction of this first production line and has created over 75 new jobs in recent years. While other organic manufacturers rely on printing processes, Heliatek is the only company in the world that specializes in solar panel manufacture using vacuum deposition of small molecules (oligomers) on flexible film. The advantages lie in better process control, higher efficiency, and longer life span.

This is the comprehensive power related extract from the « Electronics Industry Digest », the successor of The Lennox Report. For a full subscription of the report contact:

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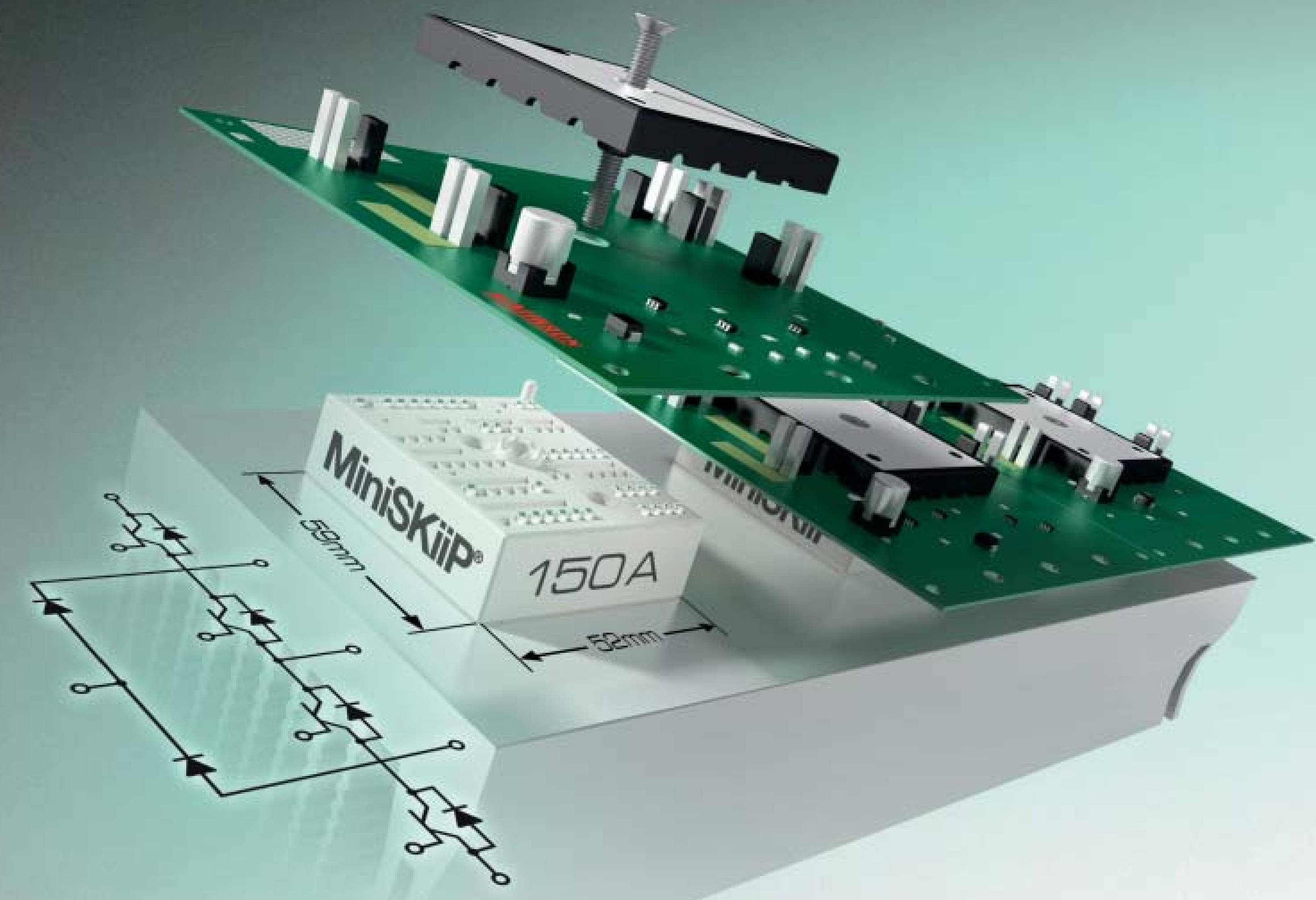
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# Maximum Power Point Tracking Comes to Servers and Routers

*By Linnea Brush, Senior Research Analyst, Darnell*

Maximum Power Point Tracking (MPPT) has become standard in photovoltaic (PV) inverters, and it could now revolutionize distributed power systems for servers and network equipment, such as routers. MPPT achieves levels of efficiency and cost-effectiveness in PV systems that are now available to distributed power systems – but it needs digital power management to do it. The result is a new approach to power architecures in electronic equipment that has been dubbed the "Maximum Power Point Tracking (MPPT) Power Architecture."

Taking digital control to its furthest point yet, the MPPT Power Architecture includes voltage adjustments at the point-of-load in an "open architecture" system. It is not a new idea, since some system makers are already implementing it in electronic equipment, and there are proprietary digital technologies available. As a result, it has established a foothold that is expected to expand the market for new digital converter designs.

The MPPT Power Architecture is akin to the concept behind maximum power point tracking used in PV systems. In PV, the change in current-voltage properties as the module heats up or receives more light can be an important source of efficiency losses in solar arrays. If the inverter that generates grid-compatible electricity is not tuned to the output voltage and current conditions, it will waste more of the electricity than it should. MPPT addresses this problem.

A similar problem exists in distributed power architectures, where system designers are having an increasingly difficult time developing power subsystems that can supply all of their system's power needs, due to the widely varied and changing power requirements of today's complex logic devices. The inflexibility of fixed-voltage power subsystems, contrasted with the need to adjust and tweak power supply voltages during and after development, translates into increased design risk.

With the MPPT Power Architecture, not only is adjustment taking place at the bus converter level, it is also taking place at the POL level. Each POL can be adjusted independently, and the bus converter is also adjusted to meet the needs of each individual POL as they are adjusted. This is not a trivial function, and it requires precise control at each power load, from the isolated converter level down to the point of load.

Basically, the MPPT Power Architecture allows the tracking of load impedances of the POLs, not just optimization of the bus voltage. Such tracking makes "MPPT-on-the-board" suited for applications such as server and network equipment powering – but this will require new converter designs, most likely incorporating some form of digital control. Some companies have already started making such products.

One such example is from Exar Corp., who developed what they call a "field-programmable power subsystem," or FPPS™. This approach is similar to how MPPT searches for the optimum combination of voltage and current to properly supply the loads. In this way, the power subsystem actively interacts with the main system in real time, permitting real-time reconfiguration based on rapidly fluctuating line and load requirements.

The value of digital power has always been the functions it can provide, but that functionality has become more defined and focused. Applications have already been identified that favor digital control, and products have been developed that meet those requirements or offer certain features that are critical to updated system designs. These are the so-called "legacy" applications for digital power management and control. They are large markets that will keep the traditional distributed power architectures in use for many years, with many of them incorporating digital control at some level. The new power architectures, by contrast, incorporate digital power right from the beginning, and that makes them different from the legacy architectures.

Based on these trends, Darnell Group has identified the current "best" markets for digital power. Some have emerged from the slow-but-inevitable march toward a "Smart Grid"; others come from standards and the demand for increased energy efficiency. For example, microinverter technology was pioneered by Enphase Energy Inc., and in recent years a number of microinverter start-ups have emerged, some with novel approaches to incorporating the technology, including digital control.

Microinverters convert the DC electricity generated by photovoltaic (PV) modules to AC at each individual module. Most PV inverters perform another function, which is to pull the optimum combination of current and voltage from the modules in a PV system in order to maximize output by watt. The current and voltage produced by PV modules, and thus the point that delivers the optimal combination of the two, changes over time. MPPT tracks that point and has become standard for inverters.

SPARQ Systems uses advanced digital control techniques to eliminate unreliable hardware and produce "more efficient, compact and lightweight microinverters." Higher quality power is generated by SPARQ microinverters over all solar irradiation levels due to a patented digital control technology that produces extremely low total harmonic distortion (THD) in the output current, even at very low illumination levels.

With increasing demand for Solar PV battery-based systems, the need for battery charging equipment is also growing. Power-One's (formerly National's) SolarMagic™ ICs for charge controller solutions enable maximum power transfer between solar panels (sources) and various loads while charging the battery at the optimum rate in mismatch conditions. The MPPT digital controller and full bridge driver ICs are designed to control high-efficient dc-dc converters commonly found in off-grid charge controller applications such as solar, automotive, marine, and street lighting applications.

Digital power management is also part of many energy management solutions, since "intelligent" data communication is an essential feature of these systems. Data acquisition and power measurement accuracy is challenging for both data centers and utilities, but the requirements differ for each industry.

Dynamic power measurement and control is needed in "critical" or complex systems that monitor utility meters, for example. If recorded data from a large spectrum and range of distances are needed, and if the data need to be tracked accurately and precisely, the more likely


an energy management system will incorporate digital power management.

Energy efficiency at full load has always been critical for power supply systems, and the focus is now shifting to efficiency over the entire load range. To meet ac line-emission harmonic standards, manufacturers add power factor correction (PFC) techniques to the switch-mode circuitry. This can increase cost and lower efficiency, however, so digital active power factor correction is often used. Traditionally, PFC has been implemented with a standard analog controller that worked on average current-mode control. Digital enables the use of two or more multi-phased or interleaved boost converters to achieve PFC.

These are just the latest trends in digital power management's long evolution. Darnell is updating its “Digital Power Electronics” forecasts report, and will include a detailed analysis of these opportunities. In addition, Darnell's Power Forum (DPF '12) will be featuring papers that identify the new markets for digital power management and control, including the implications for evolving power architectures. DPF '12, being held in San Jose on September 19-21, will address the latest advancements in digital power technologies and how companies can meet original equipment manufacturer needs at all levels.

Darnell's Power Forum

http://dpf.darnell.com/index.php

# Fast Recovery Diodes for Demanding IGCT Applications

## *Safe and smooth operation at harsh conditions*

*Fast recovery diodes, though an integral part of inverter design, have seldom received the same attention as the switching elements like IGBTs or IGCTs. As a result, Clamp, Neutral-Point Clamping and Free-Wheeling Diodes often have limited the optimal equipment design. Recognizing this, ABB has developed a new range of fast diodes offering enhanced Safe Operating Areas (SOA) and controlled (soft) recovery at very high di/dt and dv/dt levels.*

*By Jan Vobecky, Björn Backlund and Thomas Setz ABB Switzerland Ltd, Semiconductors and Jaroslav Homola and Ladislav Radvan ABB s.r.o. Czech Republic, Semiconductors.*

**Introduction**

The recent performance increases of the IGCT, achieved with the introduction of the HPT-IGCT [1], can be fully utilized in the inverter design only if the accompanying fast recovery diodes (FRDs) can match the IGCT performance. Pure SOA and di/dt increases are to no avail, if other diode parameters are deteriorating in the process, making FRD design a very delicate task. The trick is to find the right balance between diode on-state (Vf) and switching losses (Erec), RB SOA, softness, surge current (IFSM), minimum and maximum junction temperature (Tj) and cosmic ray withstanding capability. Before going into detail how this balance has been accomplished in the new ABB FRDs, let's take look at some general considerations for an IGCT-Diode.

**Diode switching**

Figure 1 shows the turn-on and turn-off of an IGCT diode on a freewheeling position (DUT). The forward current, IF, is switched off with a certain diF/dt (determined by the driving voltage and the di/dt limiting inductance Li), and continues to flow in the reverse direction until the pn junction is able to block reverse voltage. At this time, the reverse recovery current has reached its peak value IRM. The subsequent decay of the current and rise in reverse voltage are mainly determined by the diode itself and the applied voltage as a function of time. The applied voltage shape depends on the circuit of the application.

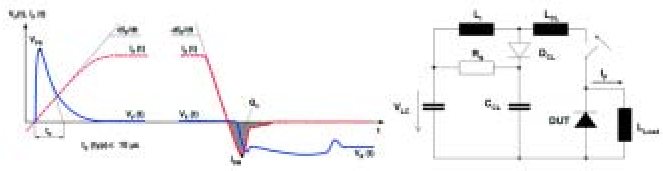

*Figure 1: Turn-on and turn-off of a freewheeling diode (left) in the circuit with the IGCT-switch (right)*

It is the goal of the diode design engineer to ensure that the tail current decays in a "soft" manner, meaning without ringing or overshoot provoking "snap", and that tail current and tail time are so short as to not contribute much to turn-off losses, despite reverse voltage being already high at this time. In addition long-term reliable operation must be assured under the application specific conditions of electro-thermal cycling and at the presence of cosmic rays.

**Diode overload conditions**

During a surge, the junction heats up to a temperature well above its rated maximum value. Therefore, the diode is no longer able to block rated voltage, so the rated surge current ($I_{FSM}$) values are valid only for $V_R$ = 0 V after the surge, i.e. without reapplied voltage. Although a single surge does not cause any irreversible damage to the silicon wafer, it should not be allowed to occur too frequently.

The shape of $I_{FSM}$ of applications depends on the protection concept and the electrical circuit and is therefore individual. The sinusoidal waveforms described in the datasheets typically don't appear in applications with fast switching diodes. $I_{FSM}$ is a standardized value that enables comparison of datasheets of different devices and even of different manufacturers. When $I_{FSM}$ is expected to be close to the diode capability, it is recommended to contact the diode manufacturer for assistance.

**Diode selection**

When selecting the diode, it must be kept in mind that one cannot "have it all". An improvement in one parameter often leads to a disadvantage in another parameter. When looking at the voltage rating and size we have to consider the following trade-offs:

**Voltage class**

Diodes with higher blocking voltage typically show:

- Higher forward recovery voltage VFR during turn-on
- Increased ruggedness while turning off at compared voltage
- Higher on-state and switching losses
- Much lower cosmic radiation FIT rate at compared voltage

**Diode-size**

Diodes with larger diameter show:

- Increased leakage current
- Lower forward recovery voltage VFR during turn-on
- Lower on-state losses

- Lower softness at reverse recovery
- Increased ruggedness (RBSOA)
- Increased reverse recovery losses Erec and charge Qrr
- Proportional to the silicon area higher cosmic radiation FIT rate at compared voltage
- Higher surge current
- Lower thermal impedance
- Higher clamping force. From a mechanical point of view, it is often preferable to clamp IGCT and its related diodes in one single clamp system.

**Achieving the aim**

*Figure 2 Fast recovery diodes with 63 mm (H-size) and 85 mm (L-size) pole pieces.*

High SOA IGCTs for state-of-the-art voltage source inverters have achieved the current handling capability over 5 kA at a 2.8 kV DC link voltage. Since they have the potential to operate above 125°C, the complementary free-wheeling and neutral point clamping diodes have to follow this trend, if placed into a common stack. This requires turn-off of higher currents at the same di/dt and DC link voltage, and at higher temperatures. The new diodes 5SDF 11H4505, 5SDF 20L4520 and 5SDF 28L4520 have been developed for this purpose (see Figure 2). While their maximal junction temperature is $T_{jmax}$ = 140°C, the difference between them is the location on the technology curve, with one optimized for low on-state losses (Low Vf) and two for low switching losses (Low $E_{rec}$) – see Figure 3. The latter is available in two package versions (H and L) with two different power handling capabilities. The clamping force of all three diodes is compatible with that of the IGCT (typically $F_n \approx$ 40 kN) to allow for the placement into a common stack.

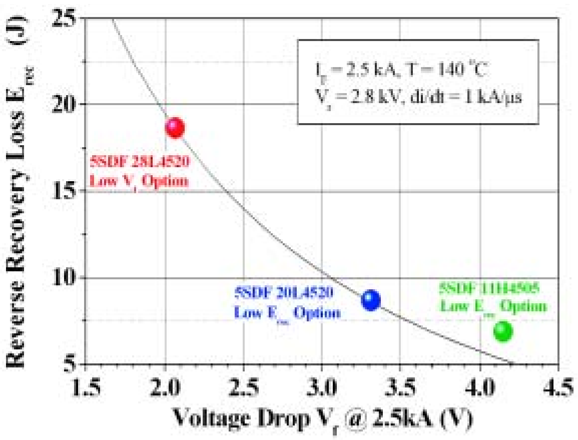


*Figure 3: Technology points $E_{rec}$ vs. $V_f$ of the new FRDs from ABB.*

One issue with increasing operation temperature is the increasing leakage current, which must be kept within the limits required for thermal stability with a safety margin typically up to ≈150°C. This is achieved by a good design of the anode doping profile well compatible with junction termination, which has to have a reliable surface passivation and sufficient cooling through a massive molybdenum disk directly bonded to the silicon wafer. The control of excess carrier lifetime via the radiation defects (irradiation), which is needed to reduce the reverse recovery losses Erec and achieve a high RBSOA, must be also well optimized not to increase the leakage current above a certain limit above which thermal runaway may occur.

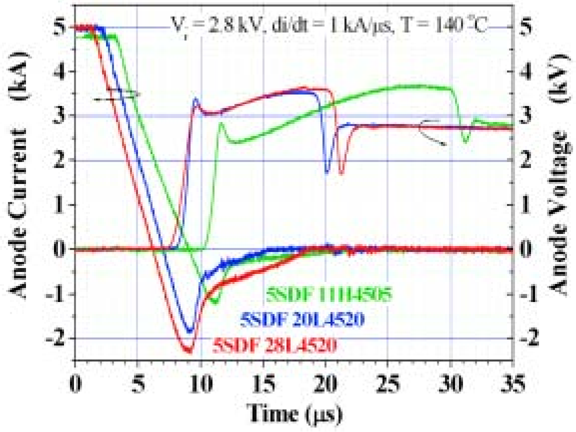


*Figure 4: Reverse recovery waveforms close to the SOA limit*

**Device performance**

The diode for the HPT-IGCT applications has to withstand current levels towards 5.5 kA with subsequent turn-off at a 2.8 kV DC link voltage with occasional excursions up to 3.2 kV. The diodes 5SDF 11H4505, 5SDF 20L4520 and 5SDF 28L4520 are therefore rated at 5.0 and 5.5 kA, respectively, up to $T_{jmax}$ = 140°C. The typical reverse recovery waveforms are shown in Figure 4.

At the same DC link voltage, the diode has to safely turn-off at current densities below 1 A/cm², where the voltage overshoot $V_{pkr}$ and oscillations usually take place. Figure 5 left illustrates this situation by showing the turn-off waveforms for the two forward currents If with and without the voltage overshoot caused by the snap-off of tail current. Figure 5 (right side) then summarizes the behavior of „Low $E_{rec}$“ diodes in the whole range of low currents and temperatures. Since the guarantee of cosmic ray withstanding capability of 100 FIT at 2.8 kV dictates the usage of the starting silicon specification with a relatively high resistivity, excessive demands are placed on the design for soft recovery.

To cope with this problem, the lifetime control and n-base thickness are carefully optimized at the same time. Figure 5 then confirms the fairly well known fact that under equivalent conditions, the diode with a smaller area operates at a higher current density (Hsize) and is therefore softer than the larger one (Lsize). It is also shown that towards zero current density, the voltage overshoots are below the diode breakdown voltage and the diodes are turning off without destruction in the whole temperature operation range.

Excellent diode softness is the prerequisite for the reliable operation of a clamping diode or a free-wheeling diode without a di/dt choke. In these cases, the stray inductances of around 300 nH allow for di/dt towards several kA/µs, only limited by the stray inductance and the speed of the turn-on switching device (see Figure 6 left). The higher the forward current prior to turn-off, the higher di/dt and overvoltage take place. As the diode is subjected to extreme dynamic avalanche effect with subsequent current filamentation, the turn-off ruggedness grows with increasing diode size thanks to a lower current density under equivalent conditions (see Figure 6 right). All the diodes compared in this figure have the same doping profiles and thicknesses and differ only in the size of the active area. Since the 5SDF 20L4520 and 5SDF 28L4520 have the area above 50 cm², they typically achieve the last pass turn-off current about 1.5 kA and 1.0 kA at 2.8 – 3.2 kV DC link voltage at 125°C and 140°C, respectively. The 5SDF 11H4505 with the active area above 36cm² typically achieves a last pass turn-off current above 1.4 kA at 2.8 kV DC link voltage and 140°C.

As the typical application circuits with IGCTs require the current handling capability of about 400 A in this regime, the new diodes provide a sufficient safety margin in the whole temperature range.

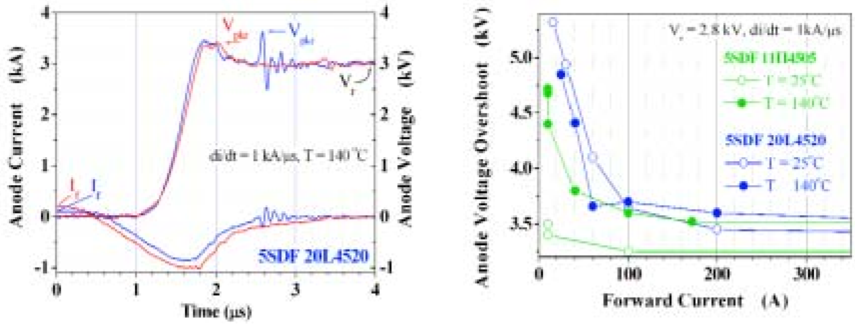


*Figure 5: Turn-off waveforms at low forward currents (left) and voltage overshoot $V_{pkr}$ vs. forward current $I_f$ of the „Low $E_{rec}$“ diodes (right).*

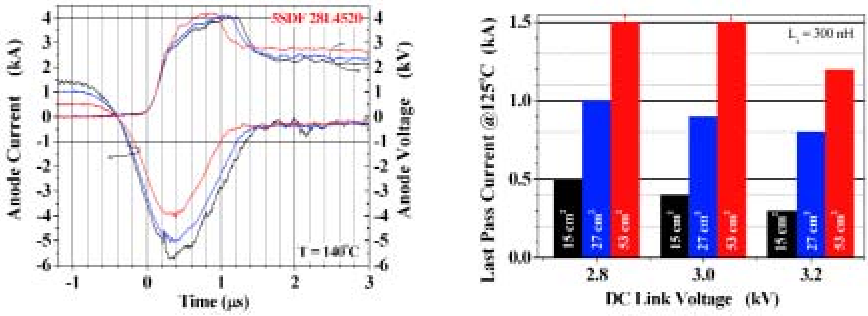


*Figure 6: Reverse recovery of L-size diode with di/dtmax up to 10 kA/ms at Vr = 3.2 kV (left) and average turn-off ruggedness vs. DC link voltage Vr with diode active area as a parameter (right).*

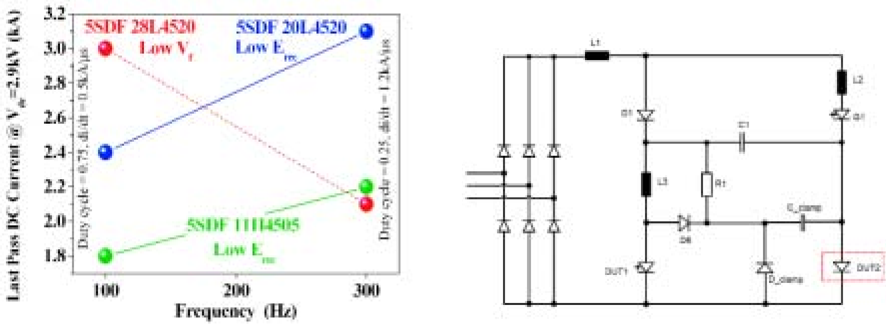


*Figure 7: Current handling capability of the diodes at Frequency testing (left) in a synthetic circuit (right)*

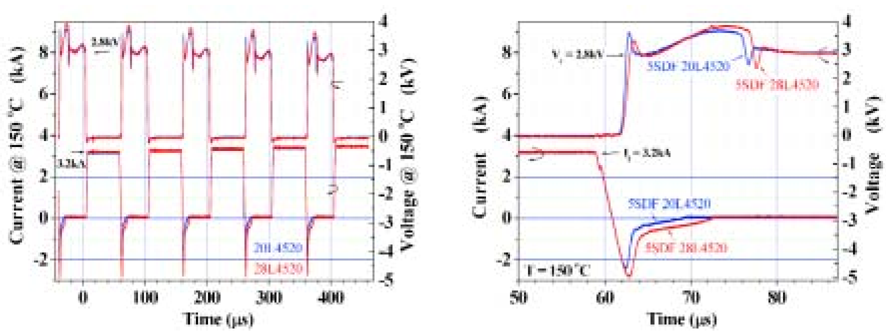


*Figure 8: Current and voltage waveforms of the diodes 5SDF 20L4520 and 5SDF 28L4520 during multipulse test (left) and a zoom into a single cycle (right).*

### Testing at application-like conditions

Diode parameters, characteristics and limits are measured during the qualification and are required for the datasheet. The datasheet is the basis for dimensioning of the application where it will be used. The final word on whether the diode can provide the expected performance or not can only be given when the device has been tested at real application conditions. To reduce this uncertainty, ABB additionally tests diodes at application-like conditions.

One important test is done in a synthetic circuit that has a large degree of freedom in setting parameters such as currents, voltages, frequencies, duty cycles, di/dt and the performance of the water cooling (case temperature) allowing the diodes to be tested at very harsh operation conditions. This circuit is schematically shown in Figure 7 right with highlighted diode under test as “DUT2”. The aim of the test is to stress the diodes under frequency operation conditions up to the thermal stability limit. ABB typically uses two working points during verification. One is with high on-state losses and low switching losses, which is typically at f = 100 Hz, duty cycle 0.75 and di/dt = 0.5 kA/µs. The other one is vice versa with high switching losses and low on-state losses at f = 300 Hz, duty cycle 0.25 and di/dt = 1.2 kA/µs. With these two conditions, we check the thermal stability performance of the diode under extreme operating conditions. The last pass DC currents in Figure 7 confirm that the new developed diodes cover the whole range of relevant magnitudes of power handling capability.

A second important test is the high frequency switching capability. Depending on the needs of the system control of the customer application, frequencies up to some kHz for a number of switching pulses are needed. To qualify this capability, ABB tests its diodes in a special burst switching circuit up to very harsh conditions. An example of 5-pulse switching of the diodes with f ≈ 10 kHz and di/dt ≈ 2 kA/µs at reverse recovery at a starting junction temperature of Tj = 150°C is seen in Figure 8 where the 5SDF 20L4520 and 5SDF 28L4520 show a good switching behavior at these harsh conditions.

Another example of very fast switching is the operation of 5SDF 20L4520 and 5SDF 28L4520 at the position of free-wheeling diode in the circuit with 4.5 kV IGBT. It has been proved that the diodes provide safe and very soft reverse recovery at the overload conditions in the circuits with IGBTs, namely at the DC link voltage of $V_r$ = 3.6 kV, stray inductance $L_\sigma$ = 200 nH and di/dt ≈ 3.6 kA/µs (T = 125°C). In summary, the application of the newly presented diodes can be extended to other applications beyond those with IGCTs, especially when a safe and smooth operation at harsh conditions is needed.

### Literature


[1] T. Wikström, T. Stiasny, M. Rahimo, D. Cottet, P. Streit, „The Corrugated P-Base IGCT – a New Benchmark for Large Area SOA Scaling“, Proc. ISPSD´07, Korea, pp. 29-32, 2007.


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# NEW ENHANCED AGILENT TECHNOLOGIES B1505A POWER DEVICE ANALYZER/CURVE TRACER.

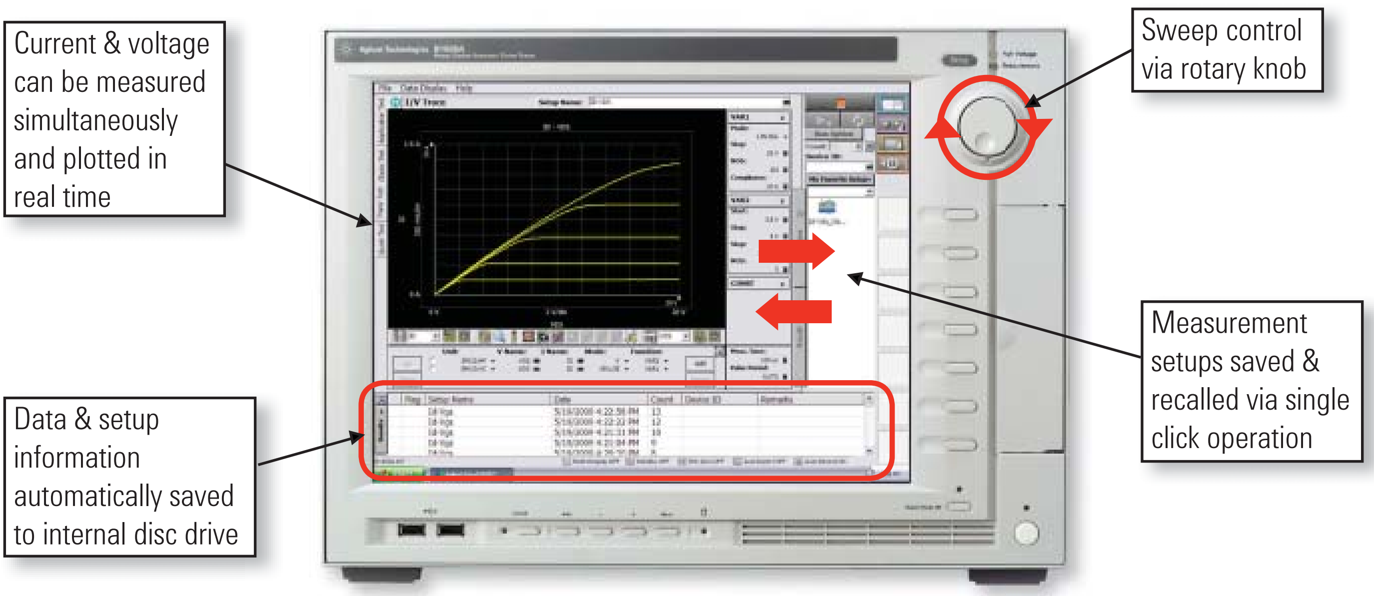
The B1505A is an integrated solution that provides researchers and device / process development engineers of power devices with high-voltage and high-current source and measurement capabilities. The fully integrated curve tracer mode makes it easy for users to take advantage of its PC-based EasyEXPERT software. The all in one analyzer / curve tracer unit is designed to characterise all current, emerging and evolving power devices from sub-pA to 1500A / 10kV with μΩ and 10μs pulse capability.

**Key Features of the Agilent B1505A Power Device Analyzer/ Curve Tracer**

- Device characterisation at up to 1500A and 10000V in a single instrument.
- μΩ evaluation of low on-resistance power devices at high current.
- Sub pico-amp leakage measurement capability at high voltage.
- 10μs current pulse width; the shortest current pulse width in the industry.
- Medium current measurement with high voltage bias, (e.g. 500mA at 1200V).
- Capacitance-Voltage (CV) measurement with up to 3000V DC bias.
- Quick device-check capability enabled by curve tracer mode.
- Easy operation and data management control with PC-based EasyEXPERT software.
- On-wafer testing and prober control.
- Standard device test fixture with interlocks for a safe measurement environment plus test fixture adapter to enable use of industry standard curve tracer fixtures.
- Upgradeable and scalable hardware architecture with ten module slots.

Power devices / power modules, including IGBT, Diode, power MOSFETs and power management ICs are a growing device category that requires both high-power and high-accuracy test capabilities. In order to meet emerging standards for improved energy efficiencies, power devices must function ever more efficiently even as they continue to become more complex, smaller and faster. New devices using wide band gap materials such as silicon carbide (SiC) or gallium nitride (GaN) have been widely developed in order to achieve higher efficiencies. To meet performance and safety requirements these developments require high-voltage on wafer measurement capabilities of greater than 3000V to reduce development and qualification times.

**New Enhanced Agilent Technologies B1505A Power Device Analyzer / Curve Tracer.** Meeting your Ultra High Current (**± 1500A**), Ultra High Voltage (**± 10000V**) and Swept CV (**±3000V bias**) Device Testing needs.




Booth 12-655

Agilent Technologies

# New Measurement Technologies for Static Characterisation of Power Devices from sub-pA to 1500A and 10kV

*Rapid advances in power device technology are rendering conventional measurement equipment a thing of a past. High current conduction tests of more than 1000A, sub pico ampere leakage current measurements and evaluation of breakdown voltages of up to 10kV become ever more important.*

*By Hisao Kakitani and Ryo Takeda, Agilent Technologies International, Japan Ltd.*

**Power device characterisation challenges**
New power device technology developments are significantly increasing junction current densities and breakdown voltages. Standard data sheet rated operating current for a super junction MOSFET or FET made from emerging materials such as SiC now easily exceed 100A, while the on resistance of low voltage devices is less than 1mΩ. The saturation voltage of an IGBT in the 1000A current rating class is less than 1V while the breakdown voltage continues to increase year upon year. Researchers around the world are now developing devices with up to 10kV breakdown voltage using new semiconductor materials. To ensure long term reliability, utilising these new components, it is critical to evaluate the devices at the extremes of their operating specification. Understanding temperature dependent device parameters is also critical in power device development. I-V characteristics are therefore measured over wide temperature ranges. Temperatures can range from less than -55C to more than 300C with leakage currents at low temperatures routinely less than 1pA. Curve tracers and other conventional measurement equipment are unable to measure such low leakage currents on new evolving devices and materials.

**Ultra High current evaluation challenges**
Conventional curve tracers are no longer suitable for modern high current device evaluation for the following reasons.

Modern devices have on-resistances less than 1mΩ which continues to decrease on an annual basis. Accurate measurement of this on-resistance requires a precision source that can apply constant current to the device plus an accurate voltmeter with full Kelvin connection capabilities. However, conventional curve tracers do not have this current source functionality and rely purely on voltage sourcing. This makes it difficult to accurately characterise the device.

Measuring devices at wafer level can drastically reduce characterisation turn-around-time, (TAT) due to the omission of the packaging process. However, the voltage drop on a curve tracer connection cable, at currents greater than a few 10's of amperes is significant. There is no easy way to eliminate this voltage drop from a wafer prober plus curve tracer set up so most people do not attempt it.

Additionally, lack of pulse width control coupled with lack of wafer monitoring capability causes significant device self heating problems when high current curve tracers are employed.

**Ultra High voltage evaluation challenges**
Breakdown voltage characteristics and sub-threshold leakage current measurements are useful parametric measurements in obtaining some basic physical insight into device behaviour. However, up until now, there has been no commercially available equipment. For example a conventional curve tracer is limited in leakage current resolution to a few µA. This is not sufficiently accurate to measure the true characteristics of a wide band gap GaN or Si device at low temperatures. Additionally, a conventional curve tracer does not provide sufficiently short pulses to avoid device self heating. At 3kV and above there is no commercially available standard measurement solution. Researchers have had to design and build their own test system using transformers and other power sources with their inherent safety and traceable measurement accuracy issues.

**High Voltage Medium Current evaluation challenges**
I-V characteristics near "safe operating area", (SOA) are important for high voltage MOS devices and IC's. When a high voltage is instantaneously applied to a device its impedance rapidly changes. I-V characterisation at high voltage is important from a reliability perspective. However, there is a lack of suitable measurement equipment that can provide sufficient voltage and current, with short enough pulses, to avoid device self heating effects. For example, traditional electrostatic discharge, (ESD) testing equipment has sufficient voltage but has no pulse or leakage measurement capability and lacks accuracy. This renders it unsuitable for device characterisation.

**Next Generation Testing Technology and Curve Tracer Architecture in B1505A**
Next generation testing technologies with curve tracer capabilities are necessary to solve today's power device development problems. The following paragraphs cover the technologies, architectures and capabilities that were developed as part of the Agilent Technologies B1505A Power Device Analyzer / Curve Tracer.

**Ultra High Current Test Technology**

Figure 1 below shows the basic circuit diagram of a next generation curve tracer with accurate high current measurement capabilities. It is critical to have not only voltage sweep capability but also current sweep capability on the collector supply. Using SMUs (Source Monitor Unit) for both gate step generator and drain voltage supply provides unprecedented accurate on-resistance measurement by utilising the SMUs in constant current source and voltage monitor mode. An essential by product of this

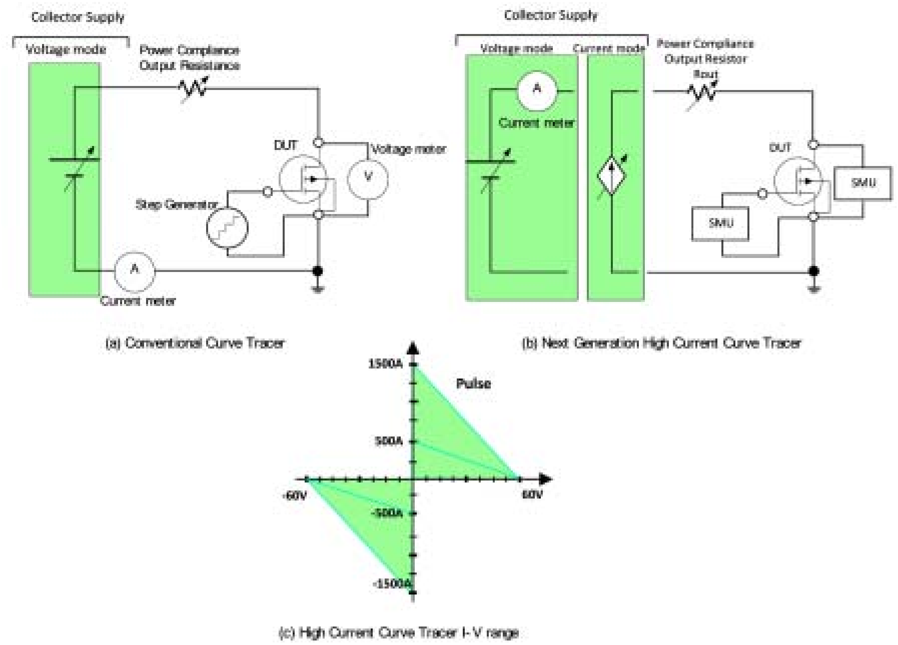



*Figure 1: Next Generation High Curve Tracer Basic Block Diagram*

approach is accurate leakage current measurement. An SMU has the capabilities of a current source, a voltage source, a current meter and a voltage meter all packaged in a single unit. Because the source and measurement circuitry is so intimately integrated it has significantly better measurement performance than would be possible by using various discrete independent instruments.

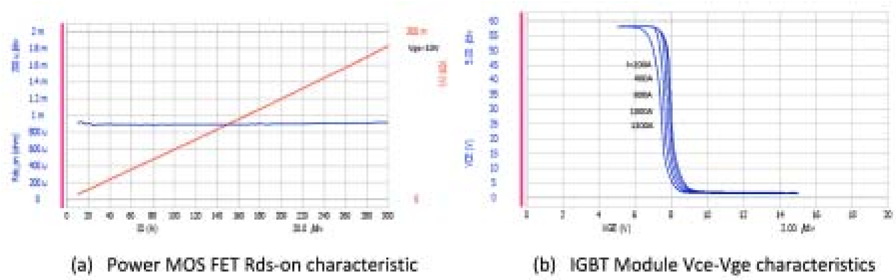



*Figure 2: Typical Static Characterisation by Current Source*

If a voltage is swept, on a conventional curve tracer, when measuring high current the actual device applied voltage is variable due to the low device impedance. This variable voltage is a result of dynamic device impedance, low residual resistance and both ohmic and non-ohmic contact resistances. However, an SMU in current source mode continuously monitors and adjusts the current by using an internal feedback circuit. This ensures constant current operation which allows fast measurement and characterisation of both Rds(on)-Id, (MOSFET) or Vce-Vge, (IGBT). Figure 2 below shows typical curves obtained using the B1505A SMU technology.

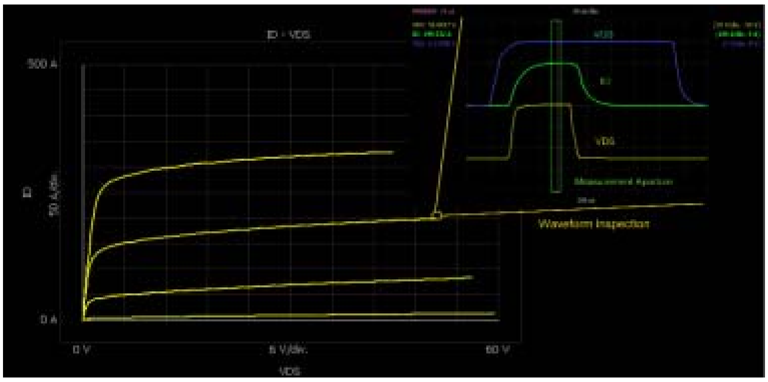



*Figure 3: LDMOS ID-VDS Characteristics and Oscilloscope View Function*

Pulse width control from 10µs to 1ms and waveform monitor capabilities, as implemented in B1505A, are additional important features of the next generation curve tracer. Measurements are optimized by checking both output settling and measurement timing with the Oscilloscope View (I/V) capability. This is shown in figure 3 below.

When carrying out temperature depend or on-wafer measurements extension cables are always necessary to connect the test equipment to a thermal chamber or prober. In these cases the drive voltage has to be high enough to overcome the IR voltage drop in the extension cable. The B1505A collector supply voltage is 60V which allows 400A current output at Vce = 5V. Residual resistance is 100mΩ as calculated in equation (1) below.

$$Ic = \frac{60V - Vce}{40mohm + R\_residual} \quad \text{---} \quad \text{equation (1)}$$

A low inductance, co-axial extension cable, was specifically developed for the B1505A in order to minimize current settling time. The time constant is defined as L/R where R is the compliance resistance and L is the cable inductance.

**Ultra High Voltage Test**

A 3kV high voltage SMU, (HVSMU) has been available on the B1505A since its introduction in June 2009. This innovative unit has pA level current measurement capability at 3 kV bias potential. It utilises a current meter on its high side which is made possible by careful attention to guarding and the use of special insulation materials. This architecture is not suitable for voltages beyond 3kV. To overcome this limitation Agilent Technologies developed a new 10kV architecture which utilises two wide dynamic range SMUs, one on the high side driving a high speed voltage amplifier and the other on the low side measuring current with pA resolution. This new architecture can output

10kV pulses with a period and pulse width of 100µs. Figure 4 below details this new high voltage measurement architecture.

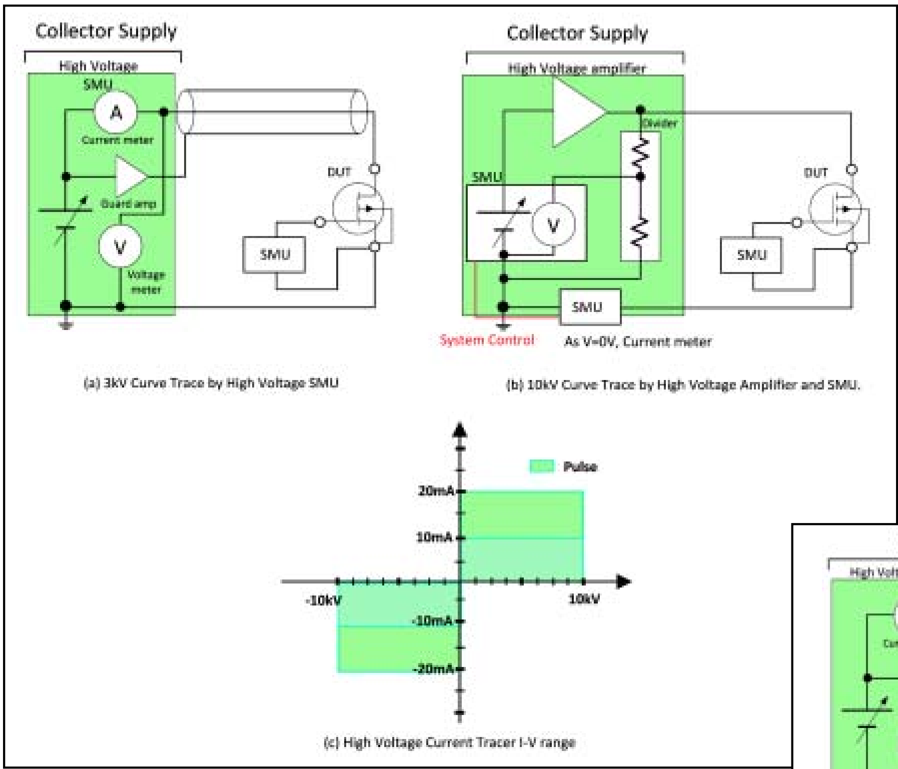
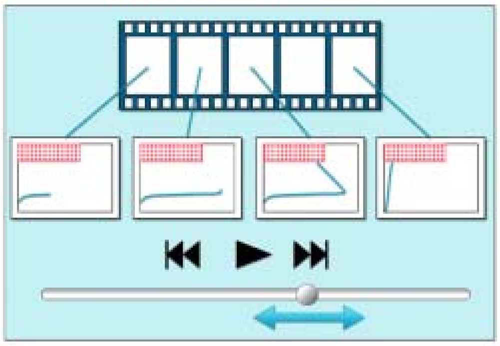
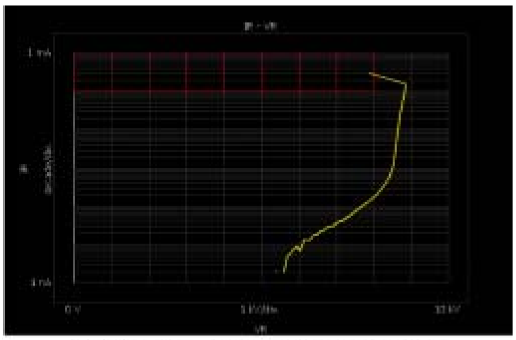



*Figure 4: Next Generation High Voltage Curve Tracer Basic Block Diagram*

Other important features during high voltage testing are device under test protection and curve trace record functions. It is particularly important to record the measurement curve even when the device is accidentally destroyed. The B1505A has had both “stop-light” and “auto record” functionality as standard since introduction. This is now extended to encompass the new ultra high voltage and ultra high current modules. Figure 5 below shows examples of this “auto record” and playback function.



(a) Auto Record function



(b) High voltage diode leakage & breakdown

*Figure 5: Feature of Auto Record Function*

**High Voltage Medium Current Test**

Pulsed medium current in hundreds of mA at high voltage can be generated using the architecture shown in figure 6(a) below. The architecture consists of a charged capacitor, fast semiconductor switch and SMU. Charge in the capacitor is applied to a device as a fast pulse by controlling the switch. This architecture is deployed in the B1505A and the pulse width can be continuously varied from 10µs to 1ms. Peak current can be limited using three different range resistors. Figure 6(b) below shows the I-V range available on the B1505A high voltage medium current test module. As an example 500mA measurement is possible at 1200V. The B1505A architecture allows the remote switching between 3kV SMU and pulse generation circuit. This enables the capability to measure pA level leakage current, breakdown voltage and high voltage medium current measurement all in a single automatic sequence without changing equipment or connections.

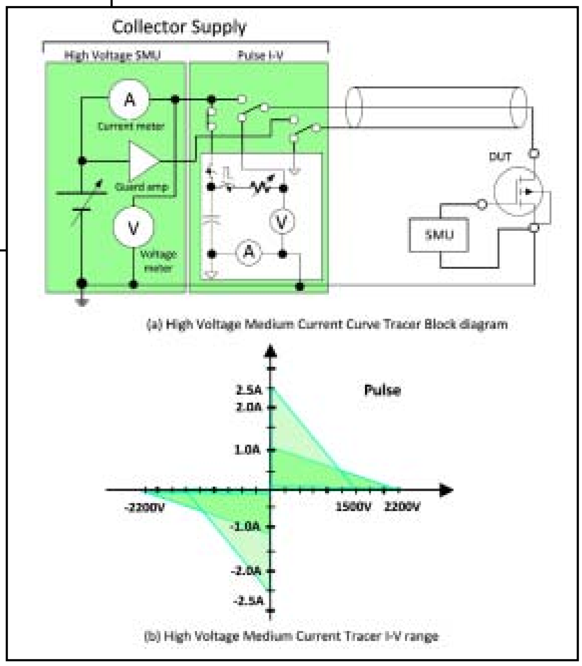



*Figure 6: High Voltage Medium Current Curve Tracer*

**Summary**

Today’s new power devices require new and innovative techniques for accurate test and characterisation. The Agilent Technologies B1505A meets all the requirements for high current, high voltage and medium current measurement at high voltage bias. With its next generation curve tracer architecture and sophisticated software environment it allows detailed device characterization, automated test and operator safety with its carefully considered safety interlocks. It comes with a wide variety of dedicated test accessories which coupled with its next generation architecture ensures unparalleled performance and ease of use in power device evaluation and characterisation.

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# EconoPACK™ 4

## The world standard for 3-level applications

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The EconoPACK™ 4 is an optimized module for 3-level applications like

- Uninterruptible Power Supply
- Solar Inverter
- High Speed Drives

where a robust design, high efficiency and less harmonics are needed.

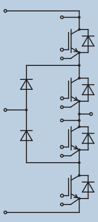
For these applications starting with 50 kW up to 125 kW, the EconoPACK™ 4 can be used to build up one phase. For higher power ratings modules can be switched in parallel.
All modules are equipped with the state-of-the-art IGBT4.
Further information are available on request.

The degree of efficiency for the two 3-level topologies, NPC1 and NPC2, has to be evaluated depending on the switching frequency.

- EconoPACK™ 4 NPC2 topology for low and medium switching frequencies (approx. $f_{sw}$< 12 kHz)
- EconoPACK™ 4 NPC1 topology for high switching frequencies (approx. $f_{sw}$≥12 kHz)

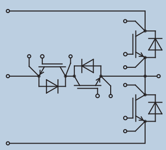
**NPC1 topology**

- 650V IGBT4
- Optimized for $f_{sw}$≥12 kHz
- Portfolio
  - F3L200R07PE4
  - F3L300R07PE4



**NPC2 topology**

- 650V/650V IGBT4
- 650V/1200V IGBT4
- Optimized for $f_{sw}$<12 kHz
- Portfolio
  - F3L400R07PE4_B26
  - F3L300R12PT4_B26
  - F3L400R12PT4_B26



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# The major difference between a conventional IGBT and RB-IGBT is the reverse blocking capability

*Power conversion efficiency and reduction of power loss is the main target of power electronics. The development of 3-Level power converters realized by neutral-point-clamped technology (NPC) was one big step in higher efficiency converters. The presented power module realizes an advanced NPC (A-NPC) topology to minimize power loss with Fuji's 6th generation IGBT and Fuji's unique reverse blocking IGBT (RB-IGBT) dies.*

*By Daniel Hofmann, Thomas Heinzel and Fred Eschrich, Fuji Electric Europe*

Due to increase in power consumption the power conversion efficiency and reduction of power losses in power conversion systems become more and more important. A multi-level topology is one of the most effective configurations in power conversion for DC-link power. A very common solution for improved efficiency regarding to multi-level power converters is the Neutral-Point-Clamped (NPC) 3-level power converter. A 3-level topology allows decreasing switching losses as well as a reduction in size of filter by enhanced spectral performance of output voltage and increase of switching frequency.

Fuji investigated another type of NPC 3-level power module named advanced NPC (A-NPC). This generation of power module utilizes a reverse blocking IGBT (RB-IGBT) for the clamping of output to the neutral point. Besides, the reduction of switching loss, a minimization of filters and low conduction loss could be achieved.

This article shows the basic function of the RB-IGBT chip and module as well as possible applications for Wind Power, Photovoltaic (PV) and Drives circuit.

**3-Level Topologies**

Fuji Electric's RB-IGBT is not the only way to create a 3-Level topology. There are several other topologies to realize a 3-Level configuration. Two well-known topologies which are called NPC1 and NPC2 reach comparable advantages like Fuji's 3-Level solution.

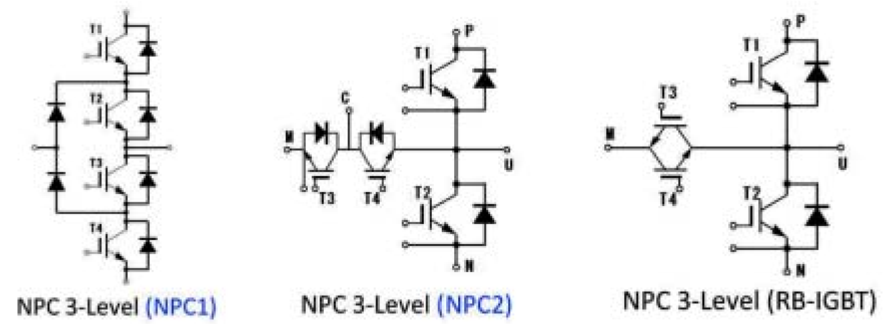


*Figure 1: Three widely used 3-Level topologies.*

**NPC1:**

The advantage of the topology is that the chips only have to block half of applied voltage by reason of two IGBT chips in series. Additionally the breakdown voltages Vces of all switches (T1 to T4) are only half of a 2-Level inverter which leads to less loss. The disadvantage of this topology is the usage of many switches and therefore many components. The on-state voltage Von increases as a result of all IGBTs in series. Every single IGBT on state loss contributes to the on-state loss and leads to higher loss than in a 2-Level inverter.

**NPC2:**

This topology has less components than NPC1 and looks quite similar to Fuji's A-NPC solution. Instead of RB-IGBT this topology uses two IGBT chips and two diodes. One IGBT is connected in series with a diode in blocking direction and connected antiparallel with the other IGBT and diode. The merit of this topology is the reduction of Von loss because of using only a single IGBT in series and hence less switches. Therefore one IGBT chips has to block the full voltage. Consequentially the chip needs to be higher rated and implies higher switching loss. T1 and T2 have the same breakdown voltage as the 2-Level half bridge without any advantage.

**A-NPC:**

The A-NPC solution by Fuji has the same advantages as NPC2 according to number of components and low Von loss due to single switches in series. The additional merit of this topology is even lower loss by reason of the usage of RB-IGBT. A single RB-IGBT can substitute an IGBT and diode in series which leads to a miniaturization and less loss. The disadvantage as seen in NPC2 is the needed full blocking voltage capability of main switches and the high breakdown voltage of T1, T2 as in 2-Level topologies.

Regarding to the device loss of the topologies in dependency of switching frequency it is quite obvious that up to 30 kHz the A-NPC has an advantage compared to all other NPC topologies (fig.2). Above 30 kHz the switching loss of A-NPC becomes higher than the NPC1 configuration.

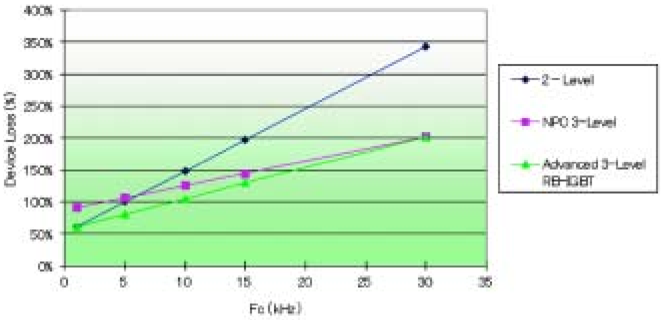


*Figure 2: Devices loss against switching frequency for 2-level, NPC 3-level and A-NPC configurations.*

**Example of a Fuji A-NPC module**

*Figure 3a: 3-Level module 4MBi300VG-120R-50 in M403 package.*

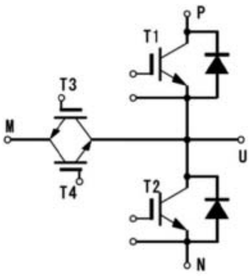


*Figure 3b: Equivalent circuit of A-NPC module with T1, T2 as main switches and T3, T4 as RB-IGBT switches.*

The 3-level module is a single-phase module in M403 package with footprint of 110mm x 80mm with optimized arrangement of the terminals for the construction of A-NPC power converters. According to figure 3 the external view and the circuit diagram of the module with main terminals U, N, M, and P on the top and auxiliary terminals arranged at the edge is shown. The equivalent circuit in figure 3a shows two main switches T1 and T2 made of V-Series IGBT chips (6th generation) by Fuji and the clamping switches T3 and T4 (RB-IGBT) which are connected in anti-parallel. Main switch IGBT's are rated with 1200V/300A for instance for the A-NPC module 4MBI300VG-120R-50. Due to only half DC-link voltage applied to clamping of output U to the neutral point M the needed RB-IGBT's capability is 600V/300A. The usage of RB-IGBT dies with its bi-directional switching capability is leading to an improvement of loss. Conventional IGBTs don't have enough reverse blocking capability and therefore a FWD in series connection is needed. Otherwise a leakage current flows along the surface of the IGBT die when a reverse voltage is applied between collector and emitter.

The major difference between a conventional IGBT and RB-IGBT is the reverse blocking capability of RB-IGBT. The IGBT structure which belongs to NPT technology was improved by adding a junction isolation region. As shown in figure 4 (b) the RB-IGBT structure has a junction isolation region which is missing in the conventional IGBT figure 4 (a). The dicing surface or also lateral face is generated during the chip manufacturing process. The chips are cut out from the wafer with crystal deformations and high–density crystal defects. At this lateral face a continuous generation of carriers from the crystal defects is transported by an electric field and lead to a large leakage current at negative voltage. Due to the applied reverse voltage from Emitter to Collector holes are generated. An additional hole will be created at the other edge of the cell between Collector and p+ area. According to the whole generation a current flows through the Base into the Emitter and a large leakage current occurs.

By applying a positive Gate-Emitter voltage this leakage current can be reduced as demonstrated in fig. 5. As long as Vge = + 15V is applied the RB-IGBT is in on-state and the generated flow of electron due to reverse voltage decreases. Only a small leakage current remains. The blocking voltage characteristic is shown in figure 5. The blue curve represents the RB-IGBT with shorted Gate-Emitter. The forward and reverse blocking capability is related to the 600V chip with same blocking voltage value. Cyan colored wave form shows an improvement and extended reverse blocking behavior of RB-IGBT when positive voltage of 15V is applied between Gate and Emitter. Furthermore a conventional NPT-IGBT also with Vge of +15V is indicated in red. The insufficient capability of reverse blocking is visible.

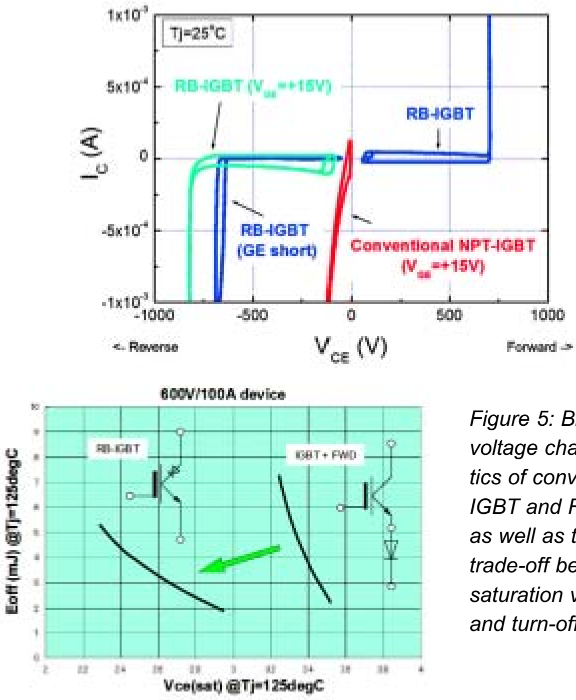


*Figure 5: Blocking voltage characteristics of conventional IGBT and RB-IGBT as well as the trade-off between saturation voltage and turn-off energy.*

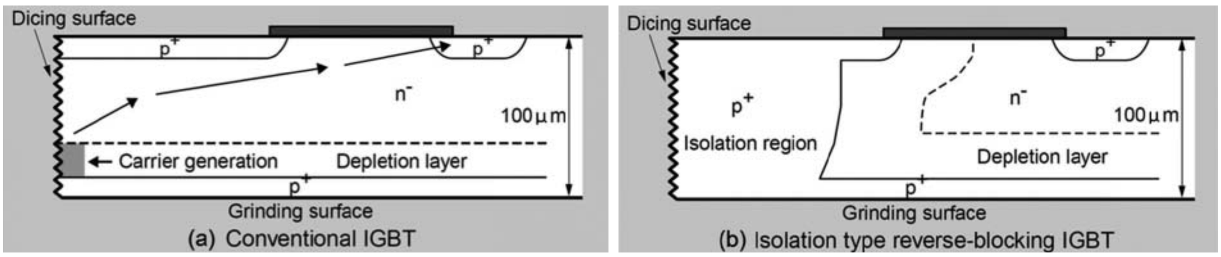


*Figure 4: Cross sectional view of conventional chip and RB-IGBT [1].*

Anyway, in spite of the strong distinctions both IGBT types have almost the same structure of active area. Therefore switching speed and trade-off curve of Von are similar. In case of applied reverse voltage after forward conduction the RB-IGBT operates like a conventional FWD and reverse recovery behavior resembles each other. Regarding to trade-off relationship between saturation voltage Vce(sat) and turn-off loss Eoff for RB-IGBT and normal IGBT with diode in series a clear benefit is obvious in figure 5 for a 600V and 100A device at 125°C. Turn-off characteristic for RB-IGBT is similar to IGBT with additional diode. However, RB-IGBT has much lower Vce(sat) compared to IGBT and diode as a result of no additional diode. This improvement contributes to a minimization of power loss by using a bi-directional switch.

The advantage of a 3-Level inverter topology is quite evident in the comparison of loss. The series connection of two IGBTs like in NPC1 leads to high switching loss. In case of NPC2 and A-NPC Von loss are smaller. Four switches with FWD is the cause of higher Von loss in NPC2. In contrast, A-NPC uses two IGBT and two RB-IGBT which leads to less Von loss. Remarkable is the efficiency of A-NPC with 97,73% and NPC2 with 97,59%. This improvement of 0,14% is significant due to the save of energy over time when an inverter operates several years.

**Operation modes of RB-IGBT module**

In total there are three different switching modes available for the 3-Level module.

Table 1 demonstrates an overview of operating switches in dependency of chosen switching mode. The on-state of a switch means always that a bias gate voltage level of +15V is applied. Contrary the off-state represents a reverse bias gate voltage level of -15V.

When a switch is declared in sw-state then the IGBT is connected to the drive circuit and gets an input gate signal.

| SW Mode | Load L | T1 | T2 | T3 | T4 |
|---|---|---|---|---|---|
| A | U – N | SW | OFF | OFF | OFF |
| | P – U | OFF | SW | OFF | OFF |
| B | P – U | OFF | OFF | SW | ON |
| | U – N | OFF | OFF | ON | SW |
| C | M – U | SW | OFF | OFF | ON |
| | M – U | OFF | SW | ON | OFF |

*SW: Connect to drive circuit and input gate signal*
*ON: Bias voltage of gate +15V*
*OFF: Bias voltage of gate -15V*
*$V_{cc2} = V_{cc1/2}$*
*Table 1: Switching mode A, B and C for RB-IGBT module*

**A-Mode:**

This mode describes the usage of the main switches T1 and T2 as a half-bridge. The load is clamped between U and N. Hence T2 is in OFF state and T1 switches. RB-IGBTs are not in use and OFF. For the opposite way round the load is connected between U and P.

**B-Mode:**

In mode B one of the RB-IGBTs is switching during the other is in on-state. Consider T3 switches then T4 is used as FWD. In order to keep the leakage current inside of T4 as low as possible T4 has to be in on-state. In the first case the load is clamped between P and U. T3 switches while T4 is in on-state and acts like a FWD.

**C-Mode:**

The C-Mode is used in the case that the load is clamped between M and U. Here T1 switches while T3 is OFF and T4 is ON which again means that T4 behaves like a diode. T2 is OFF in this switching mode due to clamping of load. In the inverse case T3 is ON while T4 is OFF and T2 is now switching. T1 is for the whole time period in off-state.

An idea of how to switch the IGBTs in a single-phase test setup is given by fig. 6. The load is clamped between U and N. T1 and T3 operate and the flowing current is marked in red.

T4 is in a steady on-state meanwhile T2 is in off-state for the whole time.

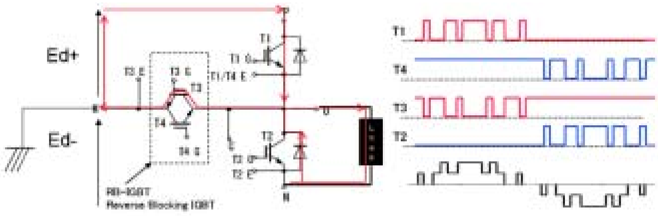


*Figure 6: Pulse wave form for the load clamped between U and N. Current flow is marked in red.*

The resulting output wave form of a 3-level configuration contains three levels of energy (0 energy, ½ energy, 1 = full energy) and the shape is more sinusoidal than a 2-Level topology.

**Switching Waveforms of RB-IGBT**

An experimental setup was created to record turn-off, turn-on, reverse recovery and short circuit behavior of the RB-IGBT.

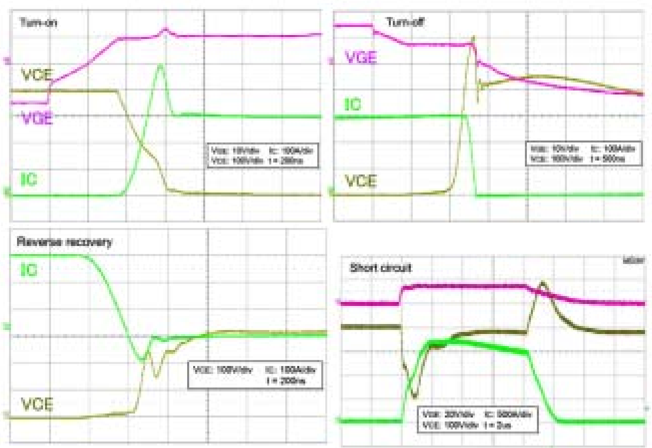


*Figure 7: Switching behavior of RB-IGBT (turn-on, turn-off, reverse recovery, short circuit).*

In case of turn-on, turn-off and reverse recovery the conditions have been used with

Tj = 25°C, Vcc = 400V, Vge = +/-15V, Rg = +8,2/-39Ω,
Snubber = 1,84uF, Ls = 34nH.

According to short circuit conditions the experimental setup used

Tj = 125°C, Vcc = 400V, Vge = +15/-0V, Rg = +8,2/-100Ω,
Snubber = 0,67uF.

Turn-on of RB-IGBT is faster than the turn-off if we take care of the time scale. The current peak due to diode is approximately 190A which is appropriate. The reverse recovery of RB-IGBTs are demonstrated in figure 7 where the main switch IGBT T1 with Rg,on of 10Ω is switching while T4 RB-IGBT is in on-state.

The short circuit behavior for RB-IGBTs is obvious in figure 7 as well. The short circuit capability of the RB-IGBT is 10µs. The gate resistances are determined at +8,2Ω and -100Ω hence it is clearly that RB-IGBT is able to withstand such a short circuit condition for 10µs.

The new technology by Fuji Electric is unique and very promising. Applications like photovoltaic inverters or UPS already use this

| Type Name | Main Switch | RB-IGBT |
|---|---|---|
| 4MBi400VG-060R-50 | 600V/400A | 600V/400A |
| 4MBi300VG-120R-50 | 1200V/300A | 600V/300A |
| 4MBi200VG-170R-50 | 1700V/200A | 1200V/200A |

*Table 2: Line-Up of 3-Level modules*

topology and emphasize the high efficiency of this configuration.

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[1] Fuji Electric Journal Vol. 75 No. 8, 2002

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# Advantages of Double-Sided Cooling Concepts for Power Semiconductors

*A parametric study of the influence of chip mounting details on the junction temperature*

*Enhanced cooling concepts allow higher output power. New joining technologies (e.g. Ag sintering) allow higher operating temperatures without strong restrictions in reliability. Coming closer to the edge of silicon device operating temperatures, the on-chip temperature distribution might affect performance and should be considered in addition to the average junction temperature dictated by thermal resistance.*

*By Max H. Poech, Fraunhofer Institute for Silicon Technology ISIT, Itzehoe, Germany*

**Introduction**

Conventional power semiconductors are joined on their entire back side by soldering or sintering to a DBC substrate (DBC = Direct Bonded Copper) in order to achieve good heat dissipation. The semiconductors top side is electrically contacted by means of wire bonds which do not provide a significant heat dissipation path.

A large area joint on the power semiconductors top side by soldering or sintering to a second DBC reduces the thermal resistance and increases the thermal mass adjacent to the chip. The latter is advantageous in case of pulse loads being significantly shorter than 1 s. Since the semiconductors top side cannot be contacted at the entire surface due to the gate contact and isolation requirements, cooling to both sides will usually not result in half of the thermal resistance. Instead, it is typically reduced by about one third, which is equal to an additional heat dissipation of about 50% via the top-side connection.

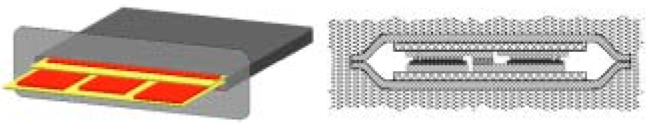

*Figure 1: Schematic view and cross sectional view of a double sided cooled, double DBC assembly ("slot module", FhG IISB), with semiconductor chips joined between the DBCs [1]*

The position of the semiconductors top side contact areas may have an unfavorable influence in particular on the temperature distribution on the chip. These effects are described with the following model calculations.

**Model calculations**

Utilizing an axisymmetric approximation, the model describes the DBC - Si-chip - DBC stack, with 0.3/0.38/0.3 mm Cu-$Al_2O_3$-Cu DBCs, 0.2 mm thick Si and Ag sinter joints (30 µm). This sort of model has successfully been used before [2] with the advantage of short calculation times suitable for parameter variations. The lateral dimensions represent 10x10 mm² Si, 15x15 mm² Cu (DBC top side) and 25x25 mm² DBC. Heat supply is performed by a constant power loss density in the upper 40 µm Si, the heat is removed to ambient temperature with a heat transfer coefficient of 5000 W m$^{-2}$ K$^{-1}$ acting at the DBC outer surface, which corresponds to a moderate water cooling. In figure 3 to 5, showing the temperature distribution within the stack, the temperature rise against ambient is shown. Mainly, the chip top contact area has been varied in size (percentage of chip area) and position.

**Results**

The results of the model calculations are presented in table 1 and figure 2.

| Model | $R_{TH}$ K/W | $\frac{T_{MAX}}{T_{MEAN}}$ | $\frac{T_{MIN}}{T_{MEAN}}$ | $\Delta T$ relative |
|---|---|---|---|---|
| 1. single sided cooling, bottom | 0.691 | 1.23 | 0.82 | 0.41 |
| 2. single sided cooling, bottom (4-times) | 0.349 | 1.32 | 0.73 | 0.59 |
| 3. single sided cooling, top, 22% centered | 4.77 | 1.73 | 0.22 | 1.51 |
| 4. both sides cooling, top, entire area | 0.341 | 1.24 | 0.81 | 0.43 |
| 5. both sides cooling, top, 19% centered | 0.408 | 1.07 | 0.90 | 0.17 |
| 6. both sides cooling, top, 22% centered | 0.401 | 1.06 | 0.93 | 0.13 |
| 7. both sides cooling, top, 25% centered | 0.393 | 1.07 | 0.93 | 0.14 |
| 8. both sides cooling, top, 42% centered | 0.365 | 1.15 | 0.92 | 0.23 |
| 9. both sides cooling, top, 46% connected, 22% centered not connected | 0.356 | 1.46 | 0.85 | 0.61 |

*Table 1: Results of the model calculation, thermal resistance $R_{TH}$, maximum and minimum chip temperature, each divided by the mean value by area of the chip temperature, as well as their difference.*

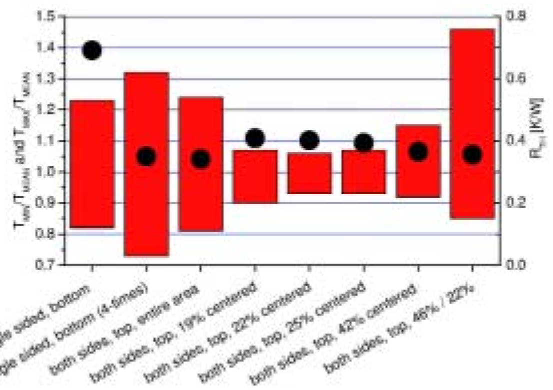


*Figure 2: Results of the model calculations, spread of relative chip temperatures (columns) and thermal resistance $R_{TH}$ (symbols)*

With good heat dissipation, there is always a temperature gradient from the chip center to the edge [3], due to lateral heat spreading in the substrate (Figure 3). Indeed, the better the cooling, the wider is the temperature distribution on the chip, valid for single and both-sided cooling (Table 1, Model 1, 2 and 4, Figure 2). The local junction temperature is known to affect reliability of conventional assemblies [4].

With the 4-fold heat transfer coefficient of 20000 W $m^{-2}$ $K^{-1}$ acting at the DBC bottom side, which implies significantly improved flow conditions achieved by a more sophisticated cooling structure, one can achieve a thermal resistance with single-sided cooling being equal to double-sided cooling, however bought with a much higher temperature spread on the chip (Table 1, Model 2). Thus, double-sided cooling appears to be efficient even with moderate effort in cooling channel design.

The non-relevant single-sided cooling via the partially joined top side (Table 1, Model 3) provides an unacceptable high thermal resistance together with an inadequate temperature spread (thus not included in Figure 2).

The results further show, that the layout of the chip top contact can be used to effectively reduce the width of the temperature distribution (Table 1, Model 5 to 8, Figure 4). Contacting the chip top side at an area less than 50% centrally favorably affects the width of the temperature distribution, with an optimum in terms of homogeneous chip temperatures at about 20 - 25% of the chip area at a slightly poorer thermal resistance.

If the chip center is left out in the chip top side contact (Table 1, Model 9, Figure 5), i.e. the top contact compares to a ring shaped area on the chip surface, then the temperature distribution is considerably wider. In fact, in case of a temperature rise of 150 K at 25°C cooler temperature, the mean junction temperature of 175°C will be encountered, but locally a semiconductor temperature of 244°C will be caused by the temperature distribution, which is assumed to be functionally critical for Si semiconductors.

**Discussion**

As has been shown, the chip top side contact shape can be used as an efficient design parameter to optimize thermal performance in double-sided cooled assemblies. Since the heat source in the semiconductor is generally assumed closer to the Si chip-top side, the assembly is not strictly symmetric, i.e. the single sided cooling is even slightly worse than twice the thermal resistance of the double-sided cooling assembly when assumed ideal (Table 1, Model 1 and 4).

The axisymmetric model overestimates the minimum chip temperatures, because the colder corners are not considered. Therefore, the width of the temperature distribution on the chip is larger, but uncritically extended to lower temperatures in reality. Experience has shown, that the assessment of the critical high temperatures in the chip centre is largely mapped correctly. Although the discretization in the model is relatively coarse, with the grid lines shown in the graphs of the temperature distributions, the strong influence of the varied parameters is clearly visible.

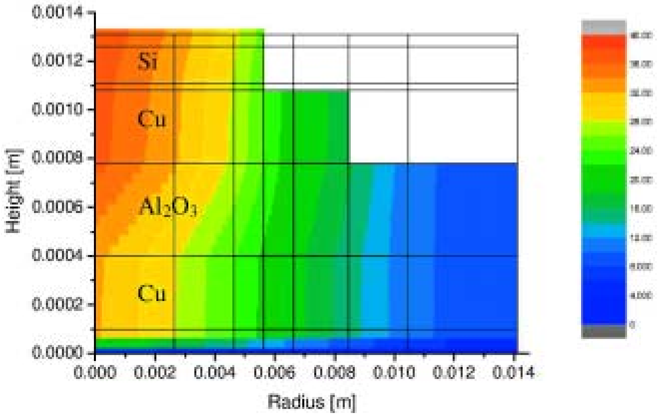


*Figure 3: Temperature distribution within a conventional assembly Si-chip on DBC, single sided cooling, bottom, $P_L$ = 45 W (left = axis of symmetry at chip centre; right = DBC edge)*

Today, it is not yet fully understood, how the width of the temperature distribution on the chip affects its electrical performance. In addition to this thermal aspect, the electrical conductivity of the metallization is relevant in terms of current distribution [4], which in particular may result in the case of over-current to a local increase of the power loss and, thus, can cause a semiconductor defect.

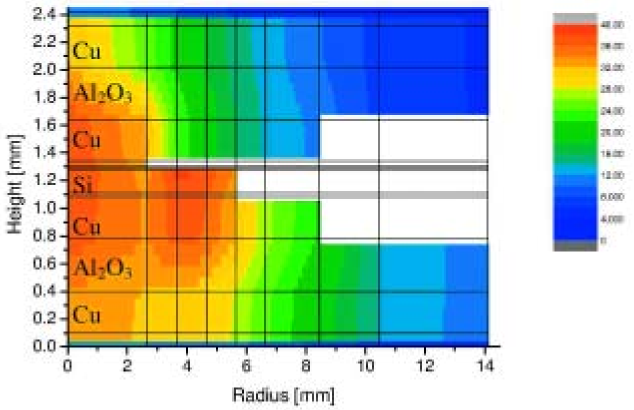


*Figure 4: Temperature distribution within a double-sided cooled stack assembly DBC-Si-DBC, Si top contacted centrally at 22% of chip area, $P_L$ = 90 W.*

In almost all cases calculated here, the maximum DBC temperature on the cooler side is actually higher than the average chip temperature, and in the other cases only slightly lower. Thus, making use of the possible junction temperature, the water cooling circuit will convert locally to an evaporation cooler, a fact being less critical with regard to thermal resistance, but with regard to a corrosive attack (cavitation) or to a formation of deposits from possible contamination in the cooling medium [2]. Boiling can be counteracted with an increased pressure in the cooling circuit (for water about 5 bar for 150°C, nearly 10 bar for 175°C), while the common ethylene glycol admixture increases the boiling point only a few degrees.

**Conclusion, Summary**

Of course, this parametric study is not intended to be exhaustive, but it already shows that top benefits can be achieved with double-sided cooling concepts, or significant disadvantages have to be taken into account, depending on the contact area on the chip top side.

With a centered top contact, a low thermal resistance combined with an almost homogeneous junction temperature can be achieved.

Prerequisite for a favorable assembly concept is, of course, that the semiconductor manufacturer provides the chip layout and the metallization in such a manner that the gate contact is placed in a corner, and that the surface can be joined in a suitably large, centrally placed window.

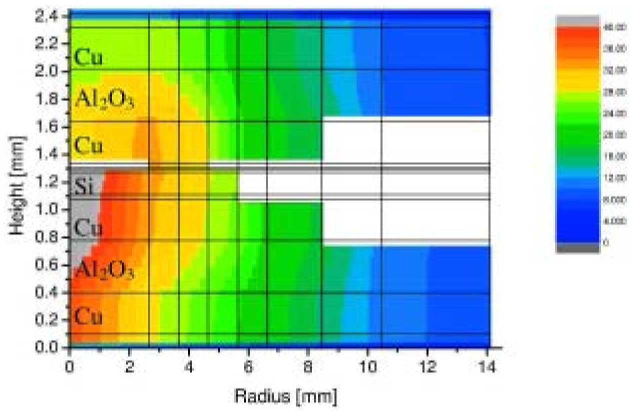


*Figure 5: Temperature distribution within a double-sided cooled stack assembly DBC-Si-DBC, Si top contacted ring shaped with 46% of chip area, 22% centrally are not connected, $P_L$ = 90 W.*

For direct water cooling acting on the DBC, evaporative cooling is expected at higher loads, which has to be considered and optimized in terms of coolant medium and flow conditions.

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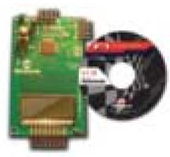

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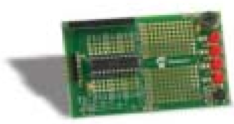

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# Vertically Integrated Inverter Topology

## *High efficiency and small form factor*

*Optimized inverter design requires looking beyond the component level to maximize Efficiency and minimize Size, Weight, Stray Inductance and Cost. Danfoss, SBE and Methode collaborated on an inverter concept that takes a system level approach*

*By Siegbert Haumann and Klaus Olesen, Danfoss Silicon Power GmbH; Michael Brubaker, SBE Inc.*

The first generation Toyota Prius was introduced in 1997 in Japan (2001 worldwide), making it the first mass-produced hybrid electric vehicle. In 2010 the cumulative worldwide sales reached 2 million units, now in its third generation. A variety of additional hybrid electric vehicles primarily out of Japan but recently also out of the US, the European Union and Korea made their market debut since. This activity has been spurred by the success and acceptance of the Prius and its family members.

J.D Power and Associates expects approx. 1.3 million electrified (EV and HEV) vehicles, a 7.6% market share, by 2017 in the US alone. 149 electrified vehicle models are expected to be available by then.

With the broad introduction of HEVs and EVs in basically every OEM's model line-up, e-traction and all associated technologies are now scrutinized to meet the pressure for lower cost, which is in part expressed in the requirement for higher power density and an increase in efficiency. Improvements in these areas are important to attract a broader customer base and to assure commercial viability for the OEMs.

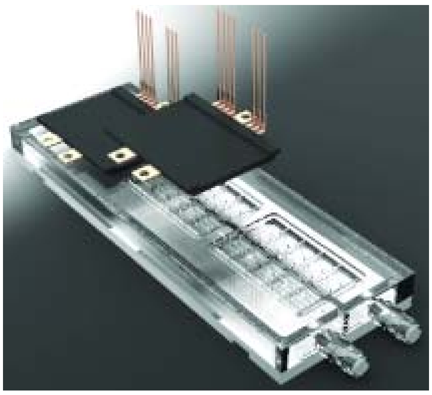

*Figure 1: Danfoss Mold-Module, direct liquid cooled with highly efficient double sided ShowerPower®-Turbulators.*

For this reason, the automotive market is expected to be a significant technology driver in inverter technology. Power Density, Efficiency and Cost will be demanded by power electronics and thermal engineers for the coming years to meet automotive needs.

At the same time traction inverters for commercial vehicles and inverters for renewable energy applications are also expected to see significant growth and strive for higher efficiency and lower cost. However, the volumes for these applications are typically only a fraction of the volumes seen in automotive. Therefore the companies developing inverters for these applications are often resource constraind and have to rely on their component suppliers to offer efficient solutions that meet their needs.

Where most component suppliers have a great understanding of their own products, most offer only catalogue designs to meet a variety of applications and leave the system design to their customers. This leaves many inverter designs far from being optimized.

Danfoss Silicon Power GmbH in Flensburg, Germany, SBE Inc. in Barre, Vermont, USA and Methode in Chicago, USA pooled their resources and knowledge and developed a design concept of a vertically integrated inverter that offers high power density and low cost. The concept focuses on the power electronics portion of the inverter only as many customers consider the driver circuit key to their own know how and a way to differentiate their design from the competition.

**The Design**

Integrated inverter topologies are essential for cost, weight, and space reductions to achieve mass adoption of electric vehicles. A return of investment of less than 2 years is needed for the majority of buyers to accept a premium price and choose an electrified vehicle over a conventional, combustion engine alternative. An integrated topology offers the best use of space combined with optimized performance. The vertically stacked inverter presented here utilizes a common, double-sided liquid cooler for the IGBT modules, DC link capacitor, and bus conductors. The design shows an inverter topology for approx. 80kW.

Film capacitors offer lower losses and higher operating temperatures than conventional electrolytic capacitors. The next generation SBE Power Ring Film Capacitor™ further enhances film capacitor performance using a unique annular form factor. The large ratio of diameter to height provides very low losses combined with excellent heat transfer,

*Figure 2: Danfoss Eplus power module on a ShowerPower® cooler.*

which translates into the highest possible ripple current per unit capacitance.  When combined with an optimized terminal arrangement, the annular film capacitor can offer an inductance value below 5 nH.

**Benefits of molded power modules for traction applications**
Traditional bondable frame based power modules, often equipped with metal-matrix-base plates, have for several years been used successfully for automotive traction applications. They show a good degree of thermal and mechanical robustness and can integrate a whole inverter power stage in one single package. The thermal mass of the base plate provides a good degree of thermal spreading which is especially appropriate in non-optimized thermal stacks.

The disadvantages of the bondable-frame module technology are becoming more and more clear for each new generation of HEV's: The technology road-maps for the automotive OEM's show that bondable frame-modules have reached their limits regarding cost, size and weight and the lack of scalability makes them harder and harder to fit into the scarce space available.
Transfer molded power modules offer a number of advantages over the frame based power modules which becomes especially clear in automotive applications.
Molded power modules are robust and thus extremely vibration resistant making them ideal for under-the-hood automotive applications; the mechanical robustness allows for a significant mechanical force to be applied to the modules when pressed into thermal interface material which ensures the thinnest thermal interface layer possible.
The power stage of the traction inverter can be broken down into single phases or even single functional switches allowing for a true scalable design approach.

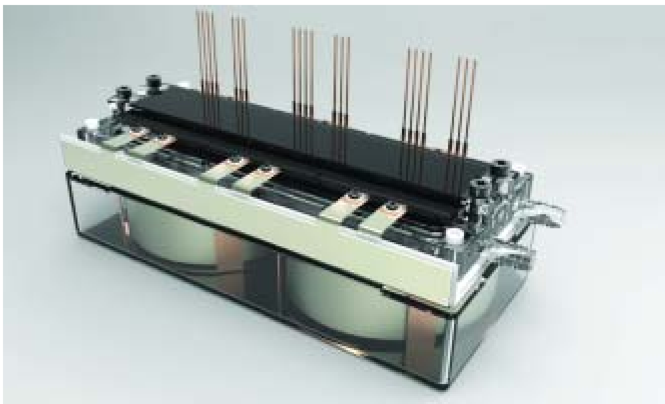

*Figure 3: SBE/Methode Film Capacitor bank with vertically integrated busbar structure*

Molded modules offer superior thermal cycle and lifetime capabilities and can accept higher working temperatures.
Cost is reduced significantly by converting to transfer molding technology. The module design is simplified, which allows for a reduction manufacturing steps involved compared to frame base modules. Assembly of the bondable frame onto a base plate (glue dispensing, frame assembly, adhesive curing), wire bonding to the bondable frame, sil-gel filling (and curing) and lid assembly (glue dispensing, lid assembly, adhesive curing) are all substituted by one single process namely the transfer molding process.

The key features of the ShowerPower® cooling principle are the highly efficient cooling performance,  the ability to cool flat surfaces homogenously even across large areas, and the scalability allowing for compact designs, in this case ensuring a uniform temperature distribution through the three power modules as well as the bus bar. Combining molded module technology with ShowerPower® offers the opportunity for very compact and easily scalable designs; it is even possible to do 3D assemblies and double-sided cooling solutions as seen in this inverter topology.
Double sided cooling is very important to manage the heat load provided by losses in the bus conductors and DC link capacitor.  For film capacitors, the bus losses are much higher than the capacitor losses, and care must be taken to avoid biasing the capacitor losses beyond the safe operating temperature.  The arrangement shown here limits the bus temperature rise and is also effectively pulling heat from the capacitor terminals.
The advantages of the annular form factor film capacitor cannot be fully utilized without a suitable bus structure.  The Methode laminated bus provides a minimized conductor spacing to present a very low inductance at the IGBT terminals.  With a suitable bus structure, total inductance values of less than 20 nH are possible, which is on the same order as the internal package inductance of the IGBT.

**Conclusion**
In Summary, the vertically integrated design topology as shown offers excellent power density and inverter efficiency. It shows that by taking a system level design approach and some level of customization, a cost competitive inverter topology that meets automotive reliability criteria is feasible.  Alternatively frame based, industrial power modules could be used for non-automotive applications posing less stringent shock and vibration requirements.

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# mAgic - Novel Sintering Materials for Die Attach on DCB

*The trend in power electronic towards a longer life time and increased power density create the need for new die attach material with entirely different properties. This article will compare alternative die attach technology to lead free solders.*

*By Thomas Krebs, Heraeus Materials Technology, Hanau*

**Soldered DCB Modules**

The usage of SnAg and SnAgCu solders for the die attach in DCB modules is well established in the industry. Knowledge for material and process, as well as the soldering equipment is available. On the other hand solders have some limitations: thermal fatigue leads to solder joint degradation, a maximum operation temperature of 125°C restricts the power density. Newer developments of lead free solder compositions like Innolot or the unique HT-Alloy of Heraeus allow an increase in operation temperature up to 150°C. These alloys demonstrated their improved durability under temperature cycling in benchmark tests using DCB substrates and can be used as drop-in solutions.

A common drawback of all solder pastes are the flux residues on the DCB after soldering and the flux condensates in the reflow oven. The cleaning of flux residues and condensates creates non-negligible cleaning costs and rework efforts.

**Alternative die attach solutions**

**Low Temperature Joining Technology**

To overcome the limits of solders in terms of life time and power density, the low temperature joining technology (LTJT) was developed [1].

In comparison to soldering the LTJT technology provides a significantly higher thermally and electrically conducting die attach joint. In combination with the high melting point of silver (961°C) and consequently a higher possible operation temperature, the LTJT technology makes it possible to have an increase of power density in the module design. Furthermore, since the operating temperature of the module is significantly lower than the melting temperature of silver, the die attach material will not show noticeable ageing.

The drawback of the LTJT technology is the relatively high process temperature of 280°C and the special high process pressure. Detailed process know-how and very high process accuracy are mandatory to avoid a damage of the semiconductor during processing.

**Nano Silver Material**

Nano Silver materials help to overcome some of the issues caused by LTJT. Typical process temperatures for nano silver paste are 200-250°C. The required process pressure varies from 1-5 MPa [2]. Similarly to LTJT, nano silver pastes result in pure silver interconnects. The high volume content of organics used in nano Ag pastes leads to long sintering profiles and limitation on bond line thickness. A processing of layers >20µm will create dry-out channels in the silver layer. Besides the improved compensation of thermo-mechanical stress a thicker bond line would equalize peaks of the DCB surface (Figure 1).

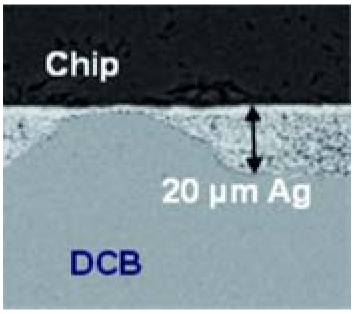


*Figure 1: Roughness DCB Substrate [3]*

Due to its particle size and biocide property of Ag, health and safety hazards are of concern for nano silver materials [4].

**Diffusion Bonding**

Another alternative to conventional soldering is diffusion bonding [5]. Intermetallic phases providing high melting points are created during processing. As an example in a SnCu-Cu-system $Cu_3Sn$ (melting point of 676°C) and $Cu_6Sn_5$ (melting point of 415°C) are formed. Thanks to its high melting point this intermetallic die attach layer will show a lower fatigue degradation compared to solder. The reliability of such a system is proven for operation temperatures of 170°C [5]. The homologue temperature of this system at 170°C is 65%, for conventional lead free solder it would already be 90%.

A proper processing of this material requires very thin solder layers (approx. 10µm) and process pressure (≤6MPa) [5].

**mAgic Sinter Materials**

Heraeus has developed a family of interconnect material based on micro scaled silver particles. Dedicated additives enable sintering at low temperatures and low process pressures. The Heraeus Microbond Ag Interconnect (mAgic) materials combine high performance with easy handling. The mAgic silver sinter materials are a product platform consisting of mAgic sinter pastes for medium to high power devices and mAgic sinter adhesives for low to medium power devices.

mAgic sinter pastes are mainly formulated with silver powder and solvents. Depending on the formulation and power electronics design they can be sintered with low pressure or no pressure. The resulting sintered joint consists of a porous structure of sintered silver particles without organic residues (Figure 2 left). The metallurgical-bonded connection ensures low electrical resistivity and high thermal conductivity, as well as high adhesion strength. The high melting point of silver (961°C) at an operation temperature of 170°C leads to a homologues temperature of 36%. The high melting temperature of silver will allow a further increase in operation temperature without the risk of joint degradation.

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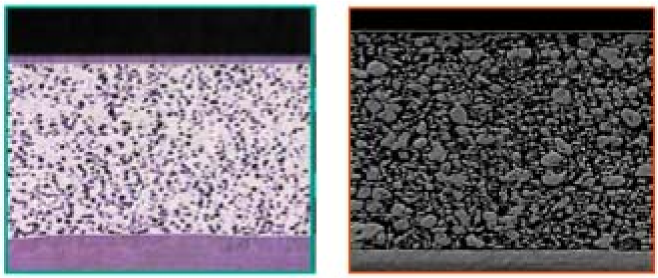
An Event organized by VDI Wissensforum www.vdi.de/charginginfrastructure mAgic sinter adhesives consist of micro scaled silver powder in a polymer matrix (Figure 2 right) and are processed in a curing step without pressure. The pores in the resulting joint are filled with cured resin. The sintered joints provide thermal and electrical conductivities comparable to solders (Figure 2). The thermal performance of packages using mAgic adhesive is equal to soldered devices (Figure 3). The resin matrix in the sintered joint results in a higher flexibility of the sinter adhesive material when compared to mAgic paste or solder. The temperature stability of the mAgic sinter adhesives is significantly higher compared to solders, allowing higher operation of the packages.



| Material property | SnAg 3.5 Solder | mAgic Paste | mAgic Adhesive |
|---|---|---|---|
| Process temperature [°C] | 230-260 | ≥ 220 | 180 - 200 |
| Electrical resistivity [mΩ-cm] | 0.01 - 0.03 | ≤ 0.01 | ≤ 0.05 |
| Thermal conductivity [W/m-K] | 20 - 50 | > 70 | > 30 |
| CTE [ppm/K] (below/above Tg) | 25 - 30 | ≤ 25 | 50 / 110 |
| E-Modulus @ 25°C [GPa] | ~ 30 | > 35 | 4.2 |
| Shear strength @ 25°C [N/mm²] | ~ 40 | 10 - 25 | ≥ 15 |
| Residue free | No | Yes | Yes |

*Figure 2: Cross section mAgic Paste (left) and Adhesive (right) and comparison of their properties in relation to solder*

**mAgic Sinter Adhesives**

mAgic adhesives provide several advantages compared to solder for the die attach on DCB. Solders are limited to operation temperatures of 125°C – 150°C. mAgic adhesives like the ASA859-Series can be used up to 200°C.

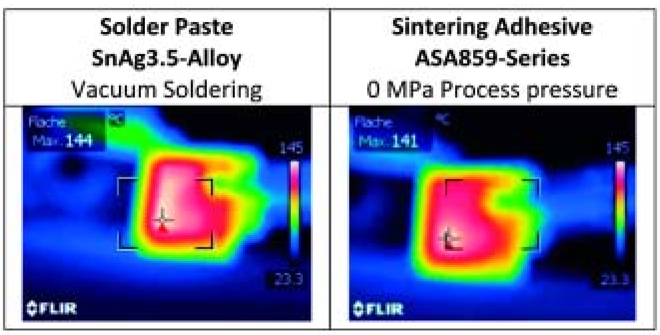



*Figure 3: Thermographical Measurement of Diode in 10A DC Operation Mode*

Based on the higher flexibility compared to solders mAgic adhesives are capable to absorb more thermo mechanical stress caused by the CTE mismatch of Die and substrate. This property leads to an improved stability of the performance compared to solder (Figure 4). This becomes more important for the large dies used in DCB modules.

Die attach with solder paste creates substantial direct and indirect process costs. Flux residues have to be cleaned after reflow to enable a reliable wire bonding process. The cleaning costs of DCB substrates are significant. Flux condensates make oven cleaning necessary and equipment downtime creates even more costs. Solder splattering during the vacuum reflow process requires 100% inspection of soldered modules. In case solder contaminates a wire bonding pad the part has to be reworked or scrapped. The inspection and the re-work of the modules are mainly done manually. mAgic adhesives are residue free materials. No substrate or equipment cleaning is required. No splatters occur during the curing of mAgic adhesives; making manual inspection and rework of the substrates obsolete. These properties will provide a cost advantage of mAgic adhesive compared to solder (Figure 5). mAgic adhesives should preferably be cured in a pre-heated batch oven. Temperature or pressure profiling is not required.

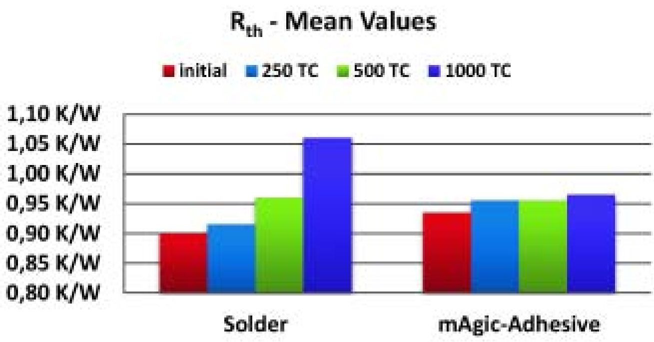



*Figure 4: $R_{th}$ measurements of DCB substrates in passive thermo-cycle test (-40/+150°C)*

For a reliable interconnect, mAgic adhesives require a NiAu or Ag interface on the die and substrate surface. Oxidation or transformation of the non-precious metal surfaces leads to an increase of the electrical resistance and a drop in the bond strength.

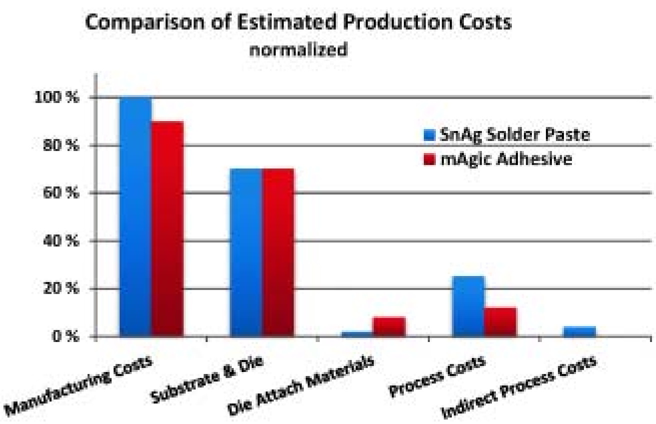



*Figure 5: Comparison of estimated Production Costs*

**mAgic Sinter Paste**

In the mAgic product family, mAgic sinter pastes have the highest thermal performance. This die attach layer provides the advantages of pure silver like high thermal, electrical conductivity and increased reliability. The melting temperature of the mAgic sinter paste layer is 961°C. To enable sintering an Ag or Au finish at the interconnect interfaces are required today. The materials are suitable for sintering in air.

The mAgic paste product group consists of several product formulations, which are tailored in performance and processing. Highest per-

formance in terms of thermal conductivity is provided by the Ag-sinter paste ASP016-series which requires a pressure assisted sintering process. The recommended process for the ASP016-series is displayed in Figure 6.

In order to simplify the sintering process for large dies further, the ASP131-series was developed. This material can be used in a no pressure sintering process (see Figure 7) for die sizes up to 100mm².

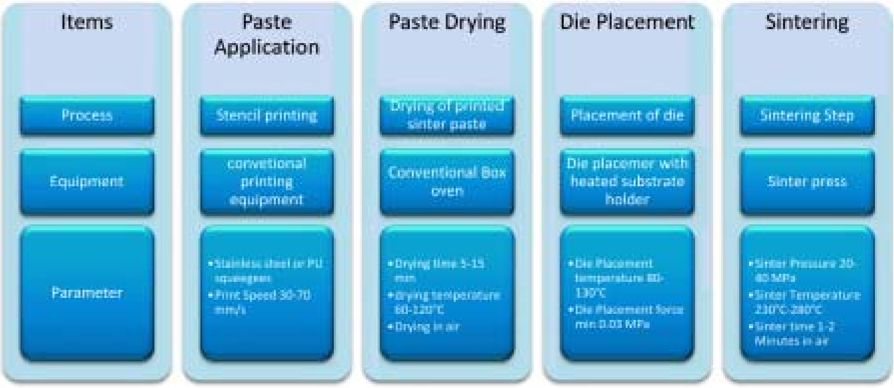



*Figure 6: Process flow for pressure-assisted sintering mAgic 016 Paste Series*

Depending on the process parameters this material shows a porosity of about 15% after sintering. The porosity of this material depends mainly on the sintering pressure applied during processing. The higher the pressure the lower the porosity of the die attach layer. Depending on the porosity adjusted in the sintering process the materials provide a thermal conductivity of ≥170W/m·K and an electrical resistivity ≤0.007mΩ·cm. Devices built with the ASP016-series demonstrated their durability by passing several hundred thousand power cycles.

The no pressure process results in die attach layer with a porosity of 30-40% after die attach. The higher porosity of the sintering layer compared to pressure assisted assemblies, affects the thermal conductivity of the interconnect layer. The thermal conductivity of such a layer will be in the range of 70 W/m·K.

Packages manufactured in a no pressure sintering process provide an improved thermal conductivity compared to vacuum soldered modules. Comparing the different sintering processes, modules sintered by the use of pressure provide a significant higher thermal capability compared to devices sintered without pressure (Figure 8). This is due to the denser structure of the attach layers created by a pressure assisted process.

No matter which process and performance of die attach layer is selected, all mAgic materials provide improved reliability and increased thermal performance in comparison to soldered die attach layers. And they will not leave flux residues or solder splatters after processing.

**Summary**

Beside an increased life time, higher power density and increased operation temperature, are the ongoing trends in power electronics. Due to its low operation temperature and fatigue, lead free solders do not provide the required performance.

Diffusion soldering is a valuable alternative of die attach technology. Due to its thermomechanical stability it makes it possible for devices to have a long life. Special die back side metallization and pressure assisted processes are required.

Compared to diffusion soldering, sintered layers provide a higher melting temperature and consequently a lower homologues temperature. Furthermore, they are compatible with standard silver Die backside metallization.

mAgic sintering materials provide tailored properties and can be used in various processes. mAgic adhesive is easy to handle and - compared to solder has improved reliability, higher operation temperatures and lower total costs. mAgic sintering paste allow highest operation temperatures and provide an increased thermal conductivity. In combination with its ductility it ensures a long life time for power electronic devices.

The performance of the Ag interconnect in combination with the wide process window and simplified handling, compared to LTJT or


*Figure 7: Example of Process flow for no pressure sintering process of mAgic 016 Paste Series with die sizes up to 100mm²*

To allow the usage of lower sintering pressure the ASP043-series was developed. This sinter paste can be processed according to the process given in Fig 6 and at a process pressure of 10 MPa and less. The thermal and electrical performances are similar to those of the ASP016-series. The lower process pressure will minimize potential damage of the devices caused by the process pressure. Additionally it will enable a sintering of larger areas using existing equipment simply by reducing the required pressure.

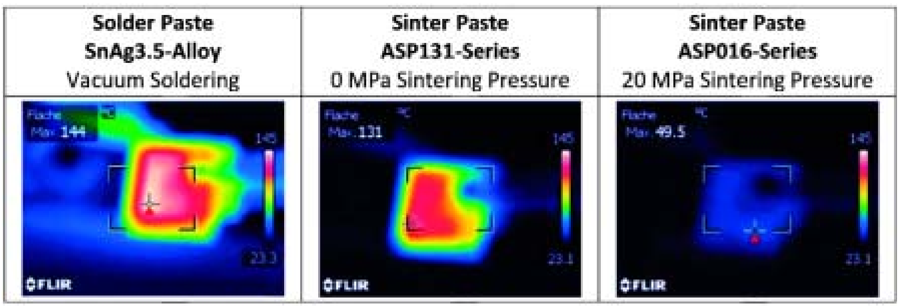



*Figure 8: Thermographic Measurements of soldered, pressure free sintered and pressure assisted sintered modules*

nano-Ag materials enables mAgic to give a high performance for die attach material in industrial use for next generations of power electronics.

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# Silicon Carbide MOSFETs Demonstrate Superior High Frequency Performance Under Hard Switched Conditions

## *Comparative performance of SiC 1200V MOSFETs vs. comparably-rated silicon MOSFETs and IGBTs at 30kHz and 100kHz+ using a SEPIC demonstration*

*Comparing the performance of 1200V silicon carbide (SiC) MOSFETs with 1200V silicon MOSFETs and IGBTs at high frequency is critical to establish the difference in device losses and power-handling capabilities between the technologies. Using a demonstration platform that can be set to emulate a given set of parameters (e.g., switch voltage, current, frequency and case temperature) that the devices will face at high power under hard-switched conditions, the difference in losses between the device technologies can be characterized by comparing DC input power.*

*By Bob Callanan (Applications Manager, SiC Power Devices) & Julius Rice (Applications Engineer), Cree, Inc.*

Because it is not practical to build separate platforms (retrofitted with SiC devices) for each potential application, (including grid connected solar inverters, power factor correction circuits, motor drives, interruptible power systems, etc.), it was necessary to design a demonstration platform to overcome this limitation. A transformerless DC-DC converter platform with a single ground-referenced switch affords the capability of recirculating the load current back to the input link, eliminating the inherent limitations of a transformer-based platform (prohibitively high losses through proximity and skin effects of the transformer windings at high frequencies).

The single-ended primary inductor converter (SEPIC) provides the ability to buck/boost without inverting the output voltage, thus making it an ideal platform to compare relative device performance between SiC MOSFETs and comparably-rated conventional silicon MOSFETs and IGBTs.

**Comparison of the devices under test**

The comparison included the best available examples of a 1200V silicon MOSFET (Microsemi APT28M120B2)[1], the highest current 1200V silicon MOSFET in a TO-247 package available (its maximum current rating at 100°C is similar to that of the SiC MOSFET); a 1200V silicon IGBT (Infineon IGW40N120H3)[2], a 1200V/40A trench and field-stop device with a forward voltage of 20A, closely matching the SiC MOSFET; and finally, the 1200V SiC MOSFET (Cree's CMF20120D)[3], which has the lowest gate charge with a gate voltage of 20V. All devices were housed in TO-247 plastic packages. (See Table 1 for comparative specifications.)

| Parameter | SiC MOSFET CMF20120D | Si IGBT IGW40N120H3 | Si MOSFET APT28M120B2 |
|---|---|---|---|
| Breakdown Voltage | 1.2kV | 1.2kV | 1.2kV |
| Max Current | 17A, $T_C$=100°C | 40A, $T_C$=100°C | 17A, $T_C$=100°C |
| Forward Voltage at 20A | 1.68V,$T_J$=25°C<br>1.98V,$T_J$=150°C | 1.70V,$T_J$=25°C<br>1.79V,$T_J$=150°C | 9.6V,$T_J$=25°C |
| Total Gate Charge | 91 nC, $V_{GS}$ = 20V | 185 nC, $V_{GC}$ = 15V | 300 nC, $V_{GS}$=10V |
| Total Gate Energy ($V_G$*$Q_G$) | 1.82 µJ | 2.78 µJ | 3 µJ |

*Table 1: Comparison devices specifications summary*

**SEPIC demonstrator design platform**

The SEPIC topology chosen for the demonstration platform is a simple design with a buck/boost characteristic, allowing the converter's output current to be re-circulated back to the input while the device under test (the switch) is operating at a duty cycle slightly higher than 50%. SEPIC converter topology is not widely used for high power operation (largely due to high switch stress); however, it is an ideal platform for this demonstration. In this converter, the voltage across the switch is twice the input voltage, and the current through the switch is twice the output current. Thus, the input DC supply has to provide just half of the desired switch voltage. Furthermore, because the switch is referenced to ground, precise measurements of voltage and current are greatly simplified.

As shown in Figure 1, the SEPIC platform schematic consists of a switch (the device under test, or DUT); a diode (D1); a blocking capacitor (C1); output capacitor (C2); and two inductors (L1 & L2). The output current is fed back into the input source ($V_{IN}$) as shown by the arrows. The controls consist of a simple peak current mode controller, which is fed from a current transformer to sample the drain of the device under test. Input for the current mode controller is supplied from an error amplifier used to regulate the (re-circulated) output current; which in turn is measured by a Hall-effect sensor. Diagnostics include a high frequency current-viewing resistor to observe the DUT current and a Kelvin-connected voltage probe to measure the DUT voltage. The gate driver is isolated to prevent a ground loop being formed around the current-viewing resistor.

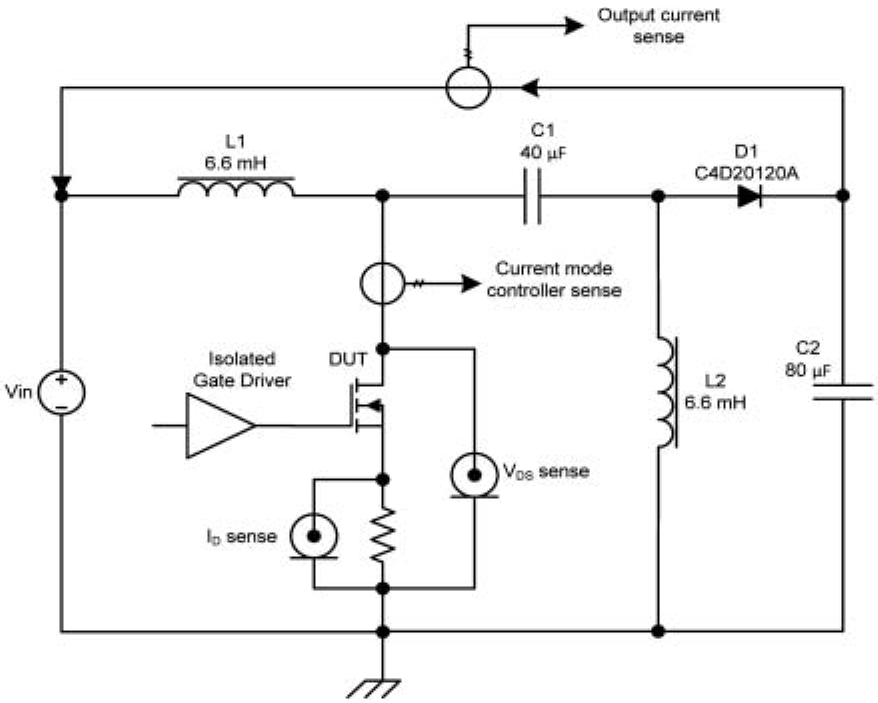


*Figure 1: SEPIC Converter Schematic*

**SEPIC Demonstration hardware**

The SEPIC hardware is shown in Figure 2. A lower rack assembly houses the high voltage and logic power supplies along with the SEPIC inductors. The remainder of the converter and control board are located above the rack assembly in an acrylic enclosure. A monitor displays voltage and current waveforms for the device under test, while four digital meters display input voltage, total system loss, delivered current and delivered power.

The SEPIC demonstration unit facilitates the ability to change out devices under test by mounting the switching devices on separate connectorized daughter-boards with heat sinks, and then connecting them to the main power board.

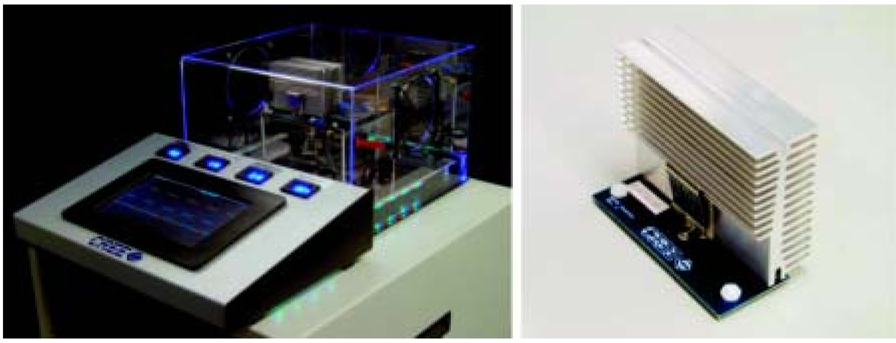

*Figure 2: SEPIC Demo and Daughter Card*

**Comparison results at 30kHz**

The first results from the SEPIC demonstrator plot the input power vs. the switch current for each of the switches under test. Since they are tested under identical conditions with identical circuits, the difference in input power between switches is a direct measurement of switching losses.

To simplify the comparative data, the input power vs. peak switch current for the CMF20120D SiC MOSFET was used as a baseline, and this data was subtracted from the input power vs. peak power

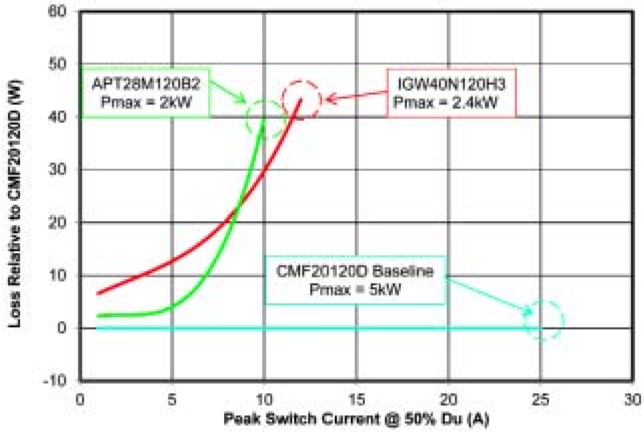


*Figure 3: Relative Switch Loss Comparison at 30kHz; $V_{DS}/V_{CE}$ = 800V*

switch current of the other devices. The result shows the increased switch losses of one device under test vs. another.

A plot of the system input power loss relative to the SiC MOSFET vs. peak switch current is presented in Figure 3. The input voltage to the SEPIC demonstrator was 400V, resulting in a switch voltage of 800V. The test was terminated when the thermal design limits were exceeded.

The silicon carbide MOSFET (CMF20120D) achieves the highest switch current (25A) with delivered power of 5kW. The silicon IGBT IGW40N120H3) reaches a maximum switch current of 12A, for delivered power of 2.4kW, with the device's higher switching losses being the limiting factor. The silicon MOSFET (APT28M120B3) reaches a maximum switch current of just 10A, or delivered power of 2kW; however, the device's higher conduction losses limit its efficiency and maximum current.

The test results also demonstrate the devices' efficiency instead of relative power loss. The switches under evaluation all have fairly low losses, while the inductors as part of the SEPIC demonstrator have significant (but predictable) $I^2R$ losses. Thus, while it is difficult to see performance differences between switches in a straight efficiency plot using the combined input and output power, this can be mitigated by subtracting inductor losses from the total system loss.

A plot of switch efficiency vs. peak switch current is show in Figure 4, which clearly shows the SiC MOSFET is the highest efficiency switch that can deliver 5kW of power. The silicon IGBT delivers less than half the power (2.4kW), and has efficiency approximately 1.2% lower than the SiC MOSFET. The silicon MOSFET, while its peak efficiency is only about 0.25% lower than the SiC device, delivers the least amount of power (2kW), and because of its high conduction losses, its efficiency drops rapidly as current is increased.

**Comparison results at 100kHz**

Testing at 100kHz compared only the SiC MOSFET and the silicon MOSFET, since the silicon IGBT switching losses were so high that hard-switched operation at this frequency was impractical.

Input power losses (system-wide) relative to the SiC MOSFET vs. peak switch current is presented in Figure 5. Once again, input voltage was 400V, resulting in a switch voltage of 800V, and the test was terminated when thermal design limits were exceeded. The results demonstrate that at the higher frequency, the SiC MOSFET achieved

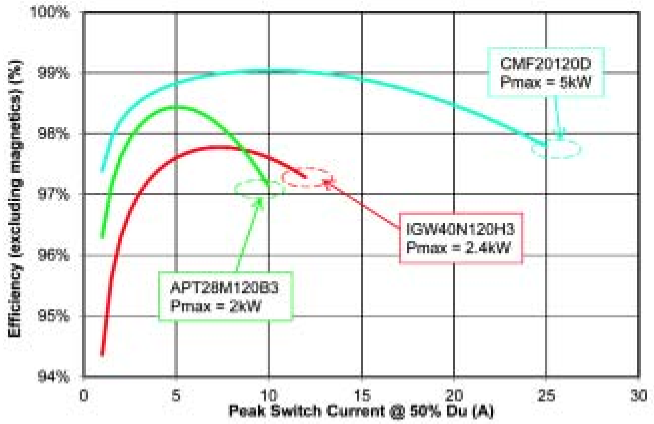


*Figure 4: Efficiency (excluding magnetics loss) Comparison at 30kHz; $V_{DS}/V_{CE}$ = 800V*

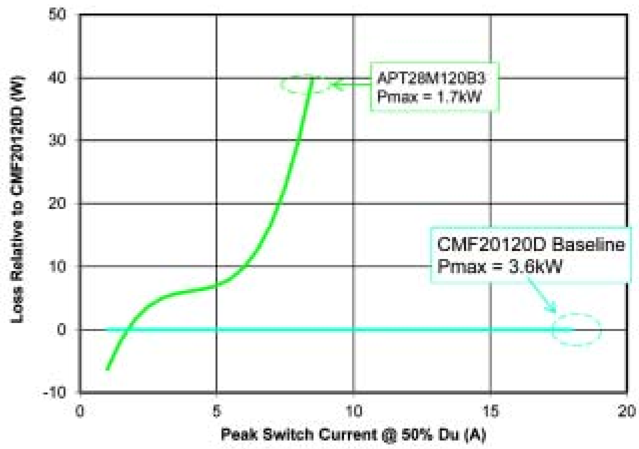


*Figure 5: Relative Switch Loss Comparison at 100kHz; $V_{DS}/V_{CE}$ = 800V*

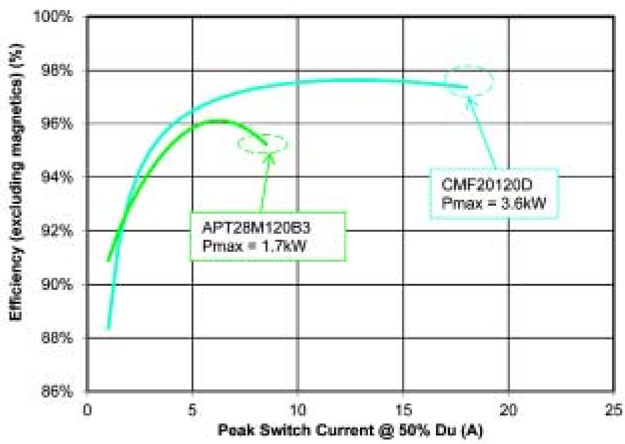


*Figure 6: Efficiency (excluding magnetics loss) Comparison at 100kHz; $V_{DS}/V_{CE}$ = 800V*

the highest switch current (17A) with delivered power of 3.6kW, while the silicon MOSFET reached a maximum switch current of only 8.5A with delivered power of just 1.7kW. It should be noted that below 1.5A, the silicon device exhibited lower losses than the SiC MOSFET (indicated by the negative relative loss in Figure 5), which is attributable to the silicon MOSFET's higher transconductance. However, the silicon device's higher on-resistance causes its conductance losses to increase dramatically as the current increases, thus causing higher power dissipation than the SiC device for the majority of the test currents.

The efficiency measured at 100kHz is shown in Figure 6. Once again, the magnetics losses have been subtracted to make it easier to compare switching device performance. The results demonstrate that the SiC MOSFET achieves the highest overall efficiency, with delivered power of 3.6kW at an 18A peak current. The silicon MOSFET reaches a maximum of only 8.5A with delivered power of 1.7kW, and it does not achieve higher overall efficiency than the SiC MOSFET (except when current is less than 2A).

**Conclusions**

Loss performance and power handling capability of Cree's silicon carbide 1200V MOSFET was compared with an Infineon 1200V silicon IGBT and a Microsemi 1200V silicon MOSFET, using a SEPIC converter demonstration platform at high power under hard-switched conditions to emulate actual power applications. Tests conducted at 30kHz and 100kHz with 800V across the switching devices demonstrate that the SiC MOSFET can process twice the current with approximately 40W lower loss than either of the silicon devices.

**References**

[1 ]http://www.microsemi.com/en/sites/default/files/datasheets/APT28M120B2_L_B.pdf
[2] http://www.infineon.com/dgdl/DS_IG40N120H3_1_1_final.pdf?folderId=db3a30431c69a49d011c6f86019b00a1&fileId=db3a304325305e6d0125921b9364704d
[3] Cree CMF20120D datasheet link: www.cree.com/products/pdf/CMF20120D.pdf

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# Cleaning of Power Module Substrates

## *Contaminants must be removed from the surfaces*

*For energy-efficiency reasons, modules produced today have ever increasing performance requirements with greater packaging density (for instance in automotive or industrial applications). Accordingly, even the slightest contaminants remaining on the surface impede the reliability required in these critical and highly sensitive applications.*

*By Thomas Kucharek, Team Leader, Application Technology ZESTRON Europe*

Cleaning modules for power electronics/IGBT modules is a must in a solder paste based process. Which requirements have to be met and which advantages can be realized by an optimized cleaning process?

In the power module manufacturing process, contaminants typically remain on the substrate and chip surfaces. To guarantee the highest process reliability, these contaminants must be removed from the surfaces through a cleaning process. Previously, flammable solvents were used in the cleaning process as no alternatives were available. Today however, cleaning with water-based media is the standard.

**The need for cleaning in power module production**

There are several process flows for power module production and thus different stations, where cleaning is usually required. The production process flow may differ due to the field of application, such as for automobile and industrial operation, as well as due to the design and functionality defined by the end customer.

Usually, the first production step is the die attach to the copper substrate by soldering, for example of IGBTs and diodes (Figure 1). Afterwards, production flows may vary. In any case, there are two points where cleaning is recommended. The first point would be after die attach by soldering to prepare the modules for wire bonding and the second would be after heat sink soldering before the modules are further processed, i.e. moulded, wire bonded and/or connected to frames.

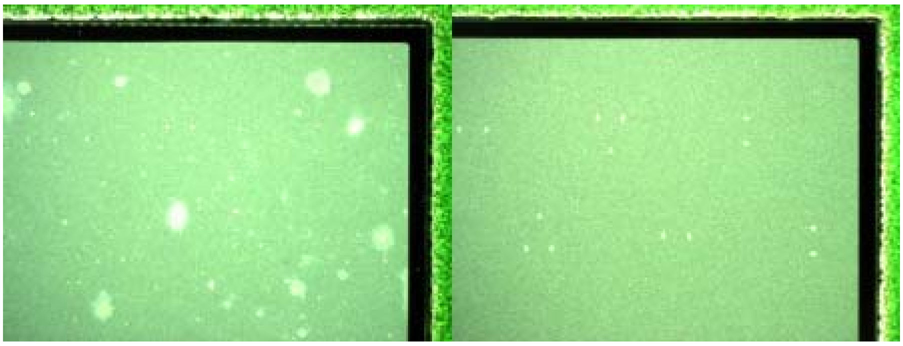

*Figure 2: Diode uncleaned (left) and cleaned (right)*

Irrespective from the process flow and final module structure, contaminants such as oxide films and flux spatter remain on the chip and substrate surface after soldering. These residues have a negative impact on subsequent processes such as wire bonding or moulding. Wire bond adhesion is often impaired when flux splatter remains on surfaces. Residues on the substrate and chip surfaces can impair achievable shear values for copper, diodes and IGBTs. Since these values are often used for the cleanliness qualification, it is necessary to completely remove all residues in a suitable cleaning process.

**Advantages of an optimized cleaning process**

While traditionally, solvents were used to clean power electronics, water-based cleaning processes became the standard over the past few years. Water-based cleaning agents specifically developed for power electronics provide excellent cleaning performance while ensuring material compatibility and long-term reliability of the modules at the same time. As a prime side-effect, they provide significant better VOC (Volatile Organic Compound) and health and safety data.

Production practice confirmed several advantages of optimized cleaning processes in the fields of wire bonding quality and reliability (shear tests and power cycling), moulding and material compatibility, which shall now be further described.

**Wire bonding quality – Shear tests**

There are two main issues which influence the quality of wire bonding. The first are flux residues on the substrate after soldering and especially flux spatter remaining on the chip surfaces (Figure 2). Bonding on uncleaned chips leads to insufficient quality and often results in either unnecessary high bonding power, leading to heel cracks or even chip defects, or lift offs due to poor wire connection.

Another quality feature for power modules are visually flawless and spot-free substrates and chip surfaces. However, the sol-

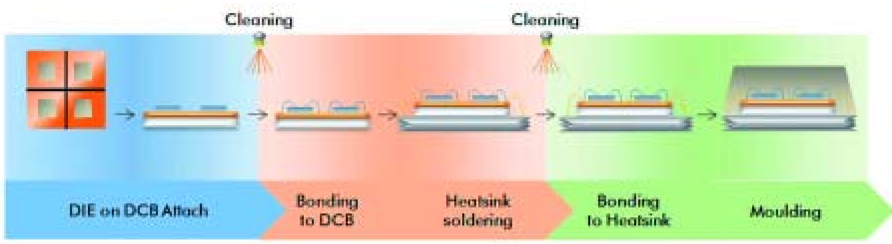


*Figure 1: Cleaning applications in power module production*

dering process or unsuitable cleaning agents, among other things, can lead to heavily oxidized parts. These oxide layers on the surface also lead to problems during bonding and can impair the production yield (Figure 3).

A suitable cleaning process must therefore achieve excellent cleaning performance to remove all flux residues from soldering and be able to activate oxidized surfaces. With a cleaning process specifically adjusted for power modules, the surfaces are optimally prepared for bonding. Production practice proved that water-based, pH-neutral and surfactant-free cleaning media can achieve this relative to formerly used solvents. They deliver good bond yields as well as visually flawless parts.

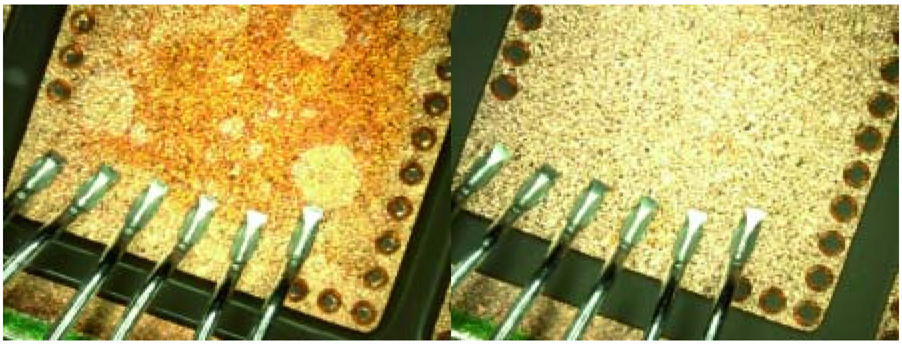

Figure 3: Bonds on oxide layer (left), bond on a copper substrate activated by cleaning (right)

The quality of the wire bonds is usually evaluated by shear testing. A stable process with high shear values is required for production yield. Modules failing to pass shear tests can have an immense effect on efficiency and costs, especially if the substrates are already soldered to the heat sink.

Zestron investigated the effect of cleaning on shear values in an internal study based on several customer projects. In a first step, results showed that an optimized cleaning process leads to a significant increase of shear values compared to uncleaned substrates (Figure 4). The second part of the study investigated different cleaning technologies (MPC and surfactants) regarding their ability to prepare the surfaces for the bonding process. Thereby, it was proved that water-based cleaning agents lead to higher shear values than conventional surfactants, as they do not leave any residues on the surfaces after rinsing.

Depending on the overall production process settings, even plasma treatment, which has been typically necessary, can be saved if a suitable water-based process is used. This in turn leads to significant cost reduction potential.

**Long-term reliability – Power cycling results**

The aim of cleaning is always to guarantee the modules' long-term reliability. The widely used method to qualify the long-term reliability or lifetime is powercycling. The modules are stressed based on specific life cycle models of their dedicated application with their lifetime being measured in cycles.

If the modules have not been sufficiently cleaned and contaminants still remain on the chip and substrate surfaces, they often fail to pass power cycling tests. The most common failures are bond lift-offs caused by poor bond connections due to residues. Once a bond connection fails, the stress on the others is raised, usually leading to an exponentially increasing number of bond failures finally resulting in the breakdown of the power module.

Cleaning the modules prior to bonding has a significant impact on the power cycling results. If the residues from soldering are removed completely in an optimized process and the bond quality is thereby improved, long-term reliability is increased showing in excellent power cycling results. In comparison, modules cleaned in a conventional process statistically show shorter life times.

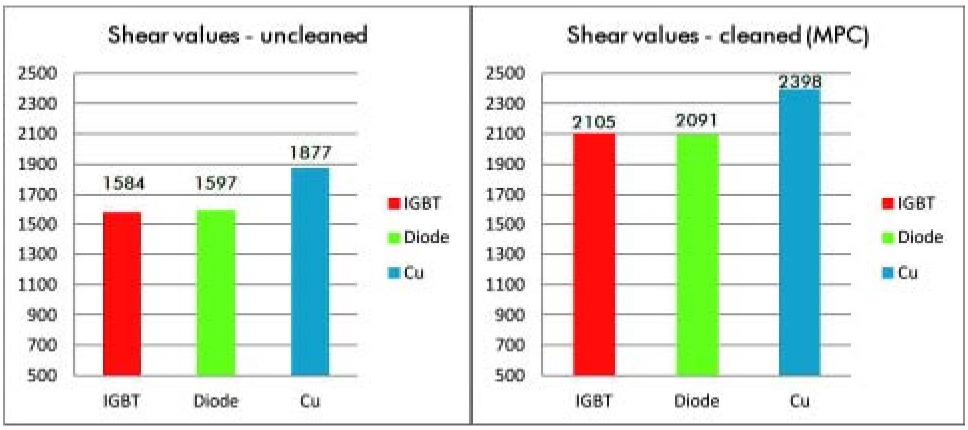


*Figure 4: Shear-value comparisons: uncleaned power module (left); modules cleaned before bonding (right)*

**Moulding adhesion**

The cleaning process also impacts the quality of the moulding. In many cases, there is a moulding applied to the bonded substrates to protect them from environmental influences. Contaminants play a decisive role with regards to moulding adhesion and thus also reliability. Flux residues on the substrate surface reduce the adhesion forces of the moulding, which in turn may lead to delamination. They may also lead to electrochemical migration beneath the moulding and thus to field failures. In the course of several cleaning projects it was proven that cleaning increases the adhesion forces while limiting delamination defects and thereby improves the moulding reliability.

**Material compatibility**

When looking for a cleaning process for power electronics, the cleaning performance is usually the main fact of interest with regards to bonding and production yield. However, another important aspect is often neglected in the first place: the compatibility of the cleaning process with the power modules' materials.

Cleaning agents for power modules must meet exceptional requirements in this area. Thus, the cleaning agent selection is critical to ensure it does not affect various chip passivations or the substrate surface. Unsuitable cleaning agents attack the passivations thus leading to the impairment of the chip function (Figure 4).

It is therefore recommended to test not only the cleaning performance but also to ensure the material compatibility of the cleaning agent before a process is implemented.

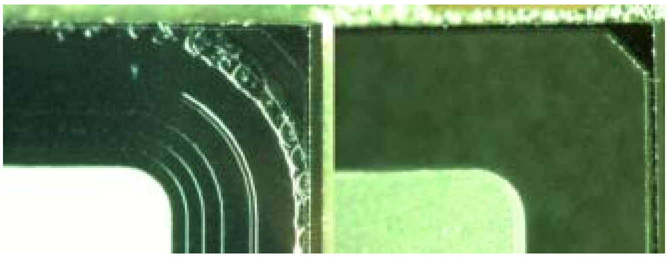

*Figure 5: glass passivation of a thyristor: attacked by an unsuitable cleaning agent (left) and optimally cleaned (right)*

**Summary**

Cleaning power modules before bonding is a must to ensure their long-term reliability. Adjusted processes with cleaning agents specifically developed for power modules ensure highest cleanliness levels and thus increase bond and mould quality. At the same time, they ensure compatibility with chip passivations and substrate materials.

Significantly improved results of the shear test and power cycling qualification finally lead to an increase in production yield. Zestron has already implemented several high volume processes in this area for automotive and industrial applications and is ready to support you with the selection or optimization of your power electronics cleaning application.

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# Acoustic Determination of IGBT Module Solder Thickness

## *A color map has the advantage that specific colors can be assigned to thickness ranges*

*Under ideal conditions, the solder pad immediately above the heat sink in an IGBT module will be free from any voids or disbonds, and will be of the same specified thickness over the whole area of the pad. Voids and disbonds in the solder reflect heat back toward the die, an undesirable situation in a module where the thermal budget has been carefully designed. Uneven thickness of the solder can also cause thermal problems.*

*By Tom Adams, Consultant, Sonoscan*

Sonoscan has recently developed and incorporated into its P300™ Acoustic Micro Imaging system a technique known as the Time Difference Mode that evaluates the thickness of the solder at each of the thousands or millions of x-y coordinates scanned by the moving transducer. During the same scan the transducer also performs normal reflection-mode acoustic imaging to find voids and other gap-type defects. Internal features such as voids are imaged in the same frame as the thickness data. The two simultaneous processes are described below.

**Imaging Voids and Other Internal Features**

As the transducer raster-scans the surface of the IGBT module's heat sink, it alternately pulses ultrasound into the module and receives the return echoes. It performs both functions thousands of times per second while scanning. Software records and measures echoes received and assigns a proportional color to each echo. The pixels from each coordinate make up the acoustic image of internal features.

Ultrasound pulsed into the module is reflected by material interfaces, but not by homogeneous materials. In a defect-free IGBT module there are several material interfaces at various depths. In addition, there may be defects such as voids that present their own additional interfaces. In order to avoid imaging too many interfaces at once, the return echo signals are generally selected by arrival time to image only a specific depth. The whole thickness of the solder layer, for example, can be imaged by selecting echoes whose arrival time indicates that they were reflected from a depth between the heat sink and the material on the other side of the solder layer. Technically, gates are set at the two desired depths, the heat sink to solder interface and, in the case of the IGBT module described here, the solder to copper interface. Only echoes whose arrival times indicate that they lie between these two gates are used to make the acoustic image. Echoes from other depths are ignored.

Figure 1 is the acoustic image, made by pulsing ultrasound through the heat sink, of three solder pads on a fairly large IGBT module. As described above, gates were set at the solder to heat sink and solder to copper interfaces in order to image the whole thickness of the solder.

The solder itself appears gray in Figure 1 largely because the gating includes the solder to copper interface which, like most interfaces between two bonded solid materials, appears gray because the echoes are of medium amplitude. The irregular white features in the solder are voids. They are white because the solder to air interface at the top of each void causes it to reflect nearly 100% of the ultrasound and thus produce the highest amplitude echo signals. To judge the impact of the voids on thermal dissipation, it is often desirable to measure the total area of the solder pad occupied by voids. In Figure 1, the areas of the three solder pads, left to right, are respectively 7.62%, 9.51% and 3.72% occupied by voids.

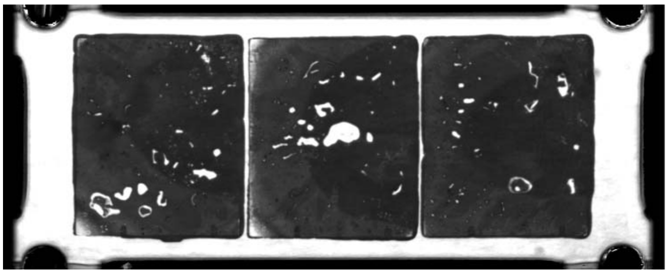

*Figure 1: In this acoustic image, white features are voids in the solder layer.*

**Evaluating Solder Thickness**

As the transducer scans the module, software looks for echoes from the two gates that have been set, one at the heat sink to solder interface, and one at the solder to copper interface. Between these two gates, software records medium-strength echoes from solid to solid interfaces (gray) and high-amplitude echoes from solid to air interfaces (white).

But it can also measure in nanoseconds the time that is required for ultrasound to travel between the two strong echoes, and thus evaluate the distance between the gates and their respective depths. The difference between these two depths is the thickness of the solder at any given x-y coordinate.

The two waveforms in Figure 2 display the amplitude of ultrasound reflected from each of the various internal interfaces. Made by pulsing ultrasound into a single x-y position and collecting return echoes from all depths, the waveform lets the operator position gates precisely. Between these two gates lies the solder layer.


*Figure 2: As solder becomes thinner, the peaks representing the heat sink (#1) and the copper (#2) grow closer together.*

The two waveforms in Figure 2 were obtained from two different locations on the middle solder pad shown in Figure 1. The waveform marked “Thick Solder” is from an area where the solder is quite thick, while “Thin Solder” is from an area where the solder is much thinner. In both images, #1 identifies the interface between the heatsink and the solder, while s#2 identifies the interface between the solder and the copper. The scale at top measures the time difference between the two echoes in nanoseconds. Where the solder is thin, markers #1 and #2 are much closer together. The waveform thus shows not only the amplitude of the echoes, but also - by the location of the peaks - the distance between the two interfaces, and thus the thickness of the solder. In regions where the solder is extremely thin or absent, the two echoes merge into a single echo. A color map can be used to assign colors to the various thicknesses.

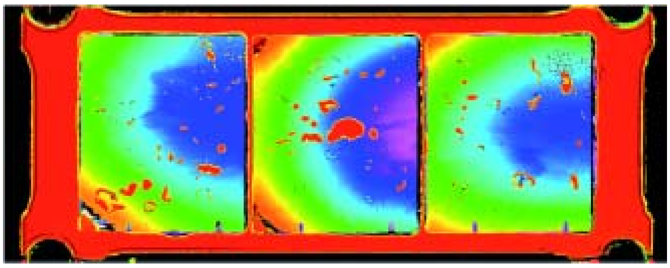

*Figure 3: Voids in the solder are red. A continuous-spectrum color map identifies solder thickness from thickest (dark blue) to thinnest (orange and red).*

Figure 3 shows the same portion of the IGBT module as Figure 1, but includes solder thickness data along with internal defects. The color map used here employs a continuous spectrum. Regions of solder having the greatest thickness are pink. This thickness is seen only in the second pad from the left. In the solder pads imaged here, the solder generally becomes thinner as you move to the left - dark

blue, light blue, green, and eventually red. Some of the upper left and lower left corners have small areas of red and black. In these regions, the distance between the two gates is very small.

Note that most of the voids are red, although some of the smaller voids appear other colors such as green. The voids that are red are close to the heat sink to solder interface, and there is very little solder above them. It is possible that these voids (air bubbles) migrated upward to the heat sink when the solder was fluid. Some smaller bubbles remained at lower depths.

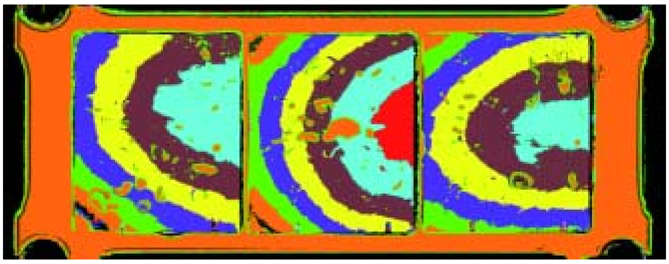

*Figure 4: Non-continuous color map makes it easier to identify accept and reject solder thicknesses.*

In Figure 4 a color map using arbitrary, non-continuous colors was applied. Each color represents a thickness range. For inspection of modules, such a color map has the advantage that specific colors can be assigned to thickness ranges that are within specifications and to those that are outside specifications. The usual practice is to assign perhaps 9 or 10 colors, of which about 3 are outside specifications. This arrangement makes the identification of a module as accept or reject very simple.

In Figure 4, each color represents a thickness range of about 45 microns. Since there are at maximum (in the center solder pad) a total of 8 colors, the greatest thickness of solder (red) is about 360 microns. Red areas might lie outside specifications, as would the black regions at the left corners of the two left solder pads. Black represents very little or no solder (i.e., a thickness from 0 to 45 microns), as seen in Figure 3. Orange represents a thickness from 45 to 90 microns. The voids nearest in depth to the heat sink also appear orange because, like the underlying bonded copper layer, they are very close to the heat sink.

The purpose of the Time Difference mode when applied to IGBT modules is to speed and simplify the inspection process. The thickness ranges are specified by the user of the system. If all colors displayed in the image match the colors in the color map that indicate acceptable solder thickness, the module is accepted.

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# Advances in ASICs for Open Loop Hall-Effect Based Current Transducers

## *The on-chip thermometer and digital to analogue converters generate analogue corrections*

*Optimisation of cost and reduction of size are driving the need to integrate the components in current transducers using Application Specific Integrated Circuits (ASICs). The target of cost optimisation means that standard commodity silicon processes with no special manufacturing steps must be used.*

*By David Jobling, ASIC Development Manager, LEM SA; Plan-les-Ouates, Geneva, Switzerland*

This leads to a paradox: How to use an ASIC made entirely of elements whose critical parameters vary by several hundred ppm °C to make measurements with a precision of 1 – 2% over all operating conditions? The target is made even more challenging when the need for a very fast response time is added. This article describes a new LEM ASIC which achieves this objective while at the same time adding extra functionality.

*Picture 1: LEM's HXS series: Open Loop Hall effect based current transducers using the previous LEM ASIC generation*

**Technology and quality evolution**

In many current measurement applications it is advantageous that the measuring circuits are isolated from the measured current, and in these cases the magnetic field due to the current can be concentrated at a sensor to which it is sensitive. In an ASIC a Hall cell may be used to transform the magnetic field into a voltage. A Hall cell, however, is not only a particularly unstable element, but additionally its properties are usually not guaranteed in an ASIC manufacturing process.

Current transducer architectures have been developed which are insensitive to the stability and linearity of the magnetic sensor, for example the closed loop architecture shown in Figure 1a. However, such an architecture is still sensitive to offsets in the sensor, and in any case the ultimate goal for cost and reliability is to develop an open loop transducer containing no electrical components except the ASIC – see Figure 1b - while having the performance of a closed loop architecture.

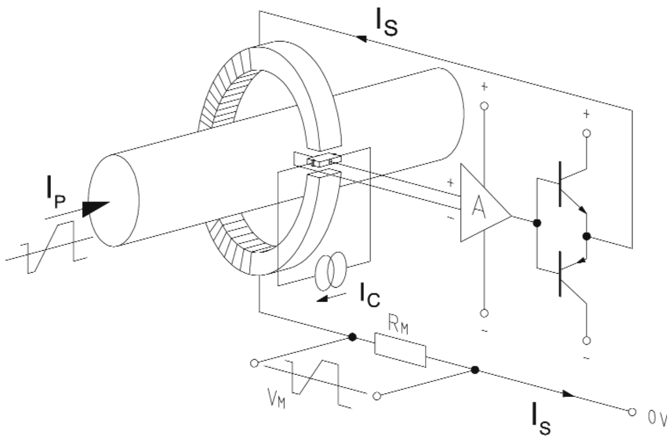


*Figure 1a: Operating principle of the closed loop transducer*

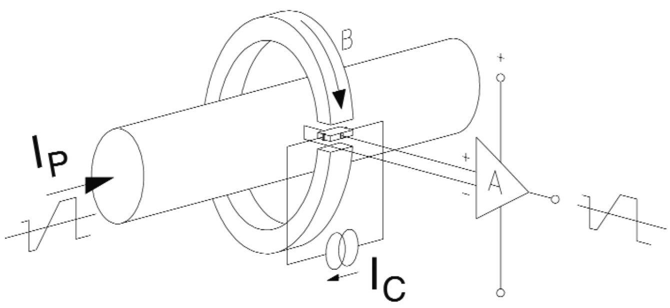


*Figure 1b: Operating principle of the Open loop transducer*

Fully integrated ASICs for open loop current transducers such as LEM's HXS series (picture 1) have been developed in the past. The performance is satisfactory: typically the critical specification parameters are:

- Gain drift: 350 ppm°C;
- Input related offset drift: 2 uT°C;
- Response time: 5 us;
- Output noise density: 7 uV/rtHz with a sensitivity of 40 V/T in a fixed bandwidth;
- Current consumption: about 15 mA

These 'first generation' ASICs have a rigid architecture where only gain (sensitivity) is adjustable and is stored in a memory which can only be written once, which limits the flexibility of their use.

Advances in silicon manufacturing technology and also in quality standards give a serendipitous combination of process changes that permit the design of a 'second generation' family of ASICs.

These advances are:

- Analogue elements which are fast and dense
- Digital elements which are dense enough to add useful functionality within a limited cost budget
- EEPROM memory which can be re-written as many times as needed

The three above features are available in processes such as the 180nm and 350nm nodes which are somewhat behind the state of the art, and so are at a reasonable cost.

There is also an apparently unrelated development, which is that quality standards such as the automotive AEC-Q100 require testing at 2 or 3 temperatures.

Of course these factors are accompanied by some disadvantages. The need for both high speed and low noise increases power consumption. The best transistors are 3.3V devices, but the market requires operation in a 5V environment.

However, putting these developments together has allowed us to design an ASIC in which we have targeted at least a 2x improvement in the critical parameters of the 1st generation listed above. At the same time we have been able to add features such as an Over Current Detection (OCD) output, and the final circuit configuration may be chosen at any time in the process, even by the end user of the current transducer using the ASIC.

**Result: A cost-effective Hall-cell based LEM ASIC with fast response time and low temperature drifts.**

Figure 2 shows a block diagram of the LEM ASIC.

To minimise the effect of offsets in the Hall cells conventional spinning techniques are used with an output at 1.5MHz and the 8 cells are placed in an optimised symmetrical arrangement . Using 8 cells improves the signal to noise ratio of the signal at the input to the electrical chain to a level similar to that of dedicated Hall cells made with III-V compounds such as Gallium Arsenide, though the low signal level at this point means that the following amplifier has to be a low noise level: it is physically large and consumes a high current, about 8 mA for the Hall cell and amplifier combination.

The signal is amplified with high gain-bandwidth amplifiers and is filtered before demodulation to limit the noise which is folded back into base-band. The filter uses the same elements as the oscillator which sets the spinning frequency, and so can have quite a narrow bandwidth despite the process variations. The OCD block input is taken before the demodulator and final output amplifier / filter which has 2 advantages: it accommodates signals outside the linear operating range of the output, and it has a fast response which is independent of the output filter bandwidth. The latter may be chosen for the best compromise between the response time of the signal channel and the noise level at the output. A timer block at the OCD output allows a hold time of up to 1ms, if needed, to ensure that a short overload may still be detected by an external micro-controller.

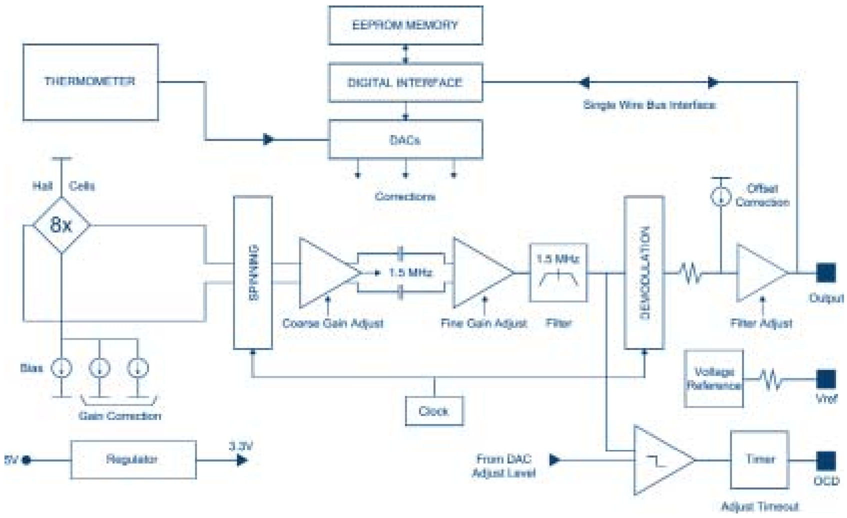


*Figure 2: Block diagram of the Hall-cell based LEM new ASIC*

In order to meet a quality commitment at the ppm level, testing of the packaged ASIC is done at cold and/or hot before the final test at ambient temperature. This allows drifts of gain and offset to be measured and an opposite correction to be stored in EEPROM. These data are combined with the output of an on-chip thermometer and digital to analogue converters to generate analogue corrections of the unavoidable gain and offset drifts in a standard silicon process. Indeed, several corrections may be stored for different ASIC configurations and correction needed automatically applied for the configuration chosen.

If the Vref pin of the ASIC is forced to the supply voltage the output pin becomes the I/O port of a single wire bus interface. This means that the final ASIC configuration may be decided at any time, even in the final application of the LEM current transducer.

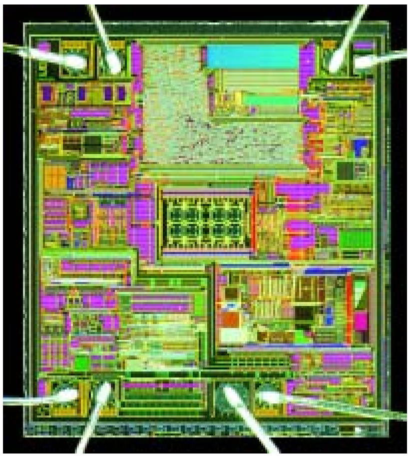

*Figure 4: New ASIC die, a complete O/L Hall effect current transducer on a single chip*

For example, two users may both want to measure currents in the same range. For one a fast response time may be the most important parameter while the other prefers a low output noise. Each may choose the output filter bandwidth according by configuring the ASIC according to his preference.

The magnetic sensitivity may be chosen between 5 and 200 V/T with 0.5% precision by sharing the 12 bits of data between exponential steps of 15% in the coarse gain adjustment and 32 steps of 0.5% in the linear adjustment.

The real challenge in design is to improve all the critical parameters, since generally they impose opposite constraints.

The measured specification parameters of the new LEM ASIC are given as following:

- Gain drift: typical 100, maximum 200 ppm°C
- Input related offset drift: typical 0.3, maximum 1.0 uT°C
- Response time: for < 2 us
- Output noise density: 6 uV/rtHz with a sensitivity of 40 V/T in a selectable bandwidth
- Current consumption: 19 mA
- Die area: slightly smaller than the first generation equivalent

Measured parameters from our standard validation set up which checks 9 circuits at a time are shown in Figures 3a and 3b. A die photograph is shown in Figure 4: the 8 Hall cells can be seen at the centre of the die.

**Conclusion**

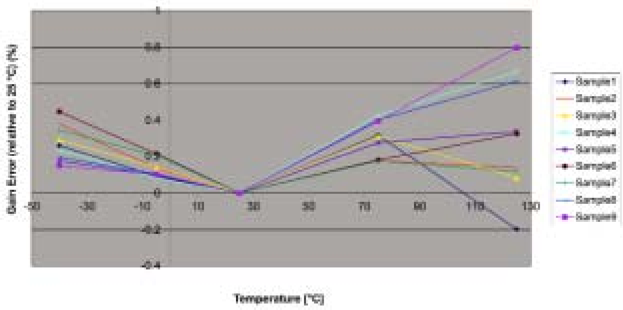


*Figure 3a: New ASIC gain drift*

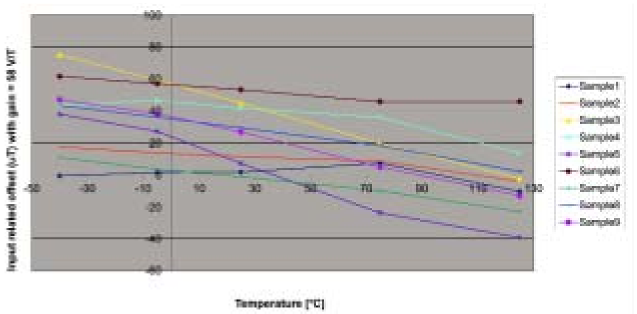


*Figure 3b: New ASIC offset drift*

The LEM ASIC described meets the target of improved precision for open loop Hall-effect based current transducers. Looking forward, we think that more improvements are possible, both by adding more features and by using new design techniques to achieve the same level of precision while reducing the calibrations needed.

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# Vacuum Brazing- a Way to Manufacture Heat Exchangers for the 21st Century

*It can be used to produce larger assemblies with complex geometries*

*Liquid cold plates can look deceptively simple, but what are the benefits of one technology over another and what are the respective manufacturing processes? How would one select a manufacturing partner for these products?*

*By Andreas Engelhardt and John Broadbent,*
*Thermacore Europe Ltd, Ashington, United Kingdom*

One way would be to select a vacuum brazing provider, offering thermal products (cold plates) as a limited part of their brazed product range, based on their extensive metal joining portfolio. Alternatively, why not talk to Thermacore, a thermal solutions provider with over 40 years' of experience in the design and manufacture of thermal management solutions and who have invested in vacuum brazing furnaces and associated processes in two locations, Northumberland in the United Kingdom and Pennsylvania in the United States, as part of the processes required to provide state of the art thermal management solutions.

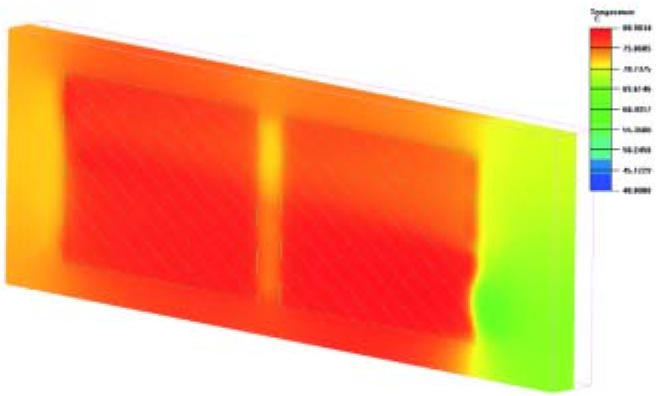

*Figure 1: Temperature Distribution across liquid cold plate surface*

**Why vacuum brazing?**
Vacuum brazing is a way of producing liquid cold plates and other complex heat exchanger products, offering significant benefits over other joining technologies:

- Flux free process leads to very clean parts
- Highly repeatable and controllable batch process
- Excellent thermal properties and the ability to deploy highly enhanced surface structures inside heat exchangers.
- Joints can be produced to near parent metal strength, leading to leak and void free parts with high proof pressures.
- Ability to produce internal joints, even in complex structures, increasing the part's overall strength.
- Ability to join large surfaces together
- Uniform material properties during and after brazing.
- High temperature resistance of joints

**Vacuum brazing as part of the product development process for thermal solutions**
In order to produce high performance thermal solutions, Thermacore design engineers begin with the use of industry standard CFD (Computational Fluid Dynamics) software as well as proprietary spread sheets developed over the last 40 years to determine thermal requirements, such as component temperatures, coolant temperature rise, pressure drops and flow rate optimisations.

But, as these results alone do not lead towards manufacturable products, engineers apply mechanical design rules, which have been developed through thousands of hours of design and manufacturing experience, to each individual product design. The application of this know-how allows Thermacore to convert high performance thermal designs into cost effective solutions, which meet or exceed the expectations of the customer. This vast reservoir of experience gained knowledge is equally applied to new design solutions, as well as on a consultancy service basis to "build to print" scenarios, where potential design flaws are highlighted and possible improvements are suggested.

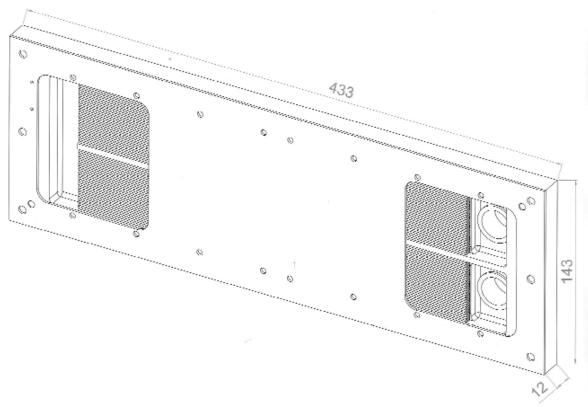


*Figure 2: CAD design of cold plate completed*

Once the design is completed, the component can follow the vertically integrated manufacturing route, with machining, vacuum brazing, heat treatment, test and stringent quality control, all under one roof.

Vacuum brazing is one of the key manufacturing processes, and part of brazing process family, where a filler material is taken above its melting temperature, which exceeds 450°C. This filler material is then fed between close fitting components and distributed by capillary action or in the case of vacuum brazing is already in place before the heating process begins. Once all the filler material is molten, the part is cooled down and the filler material forms a joint through atomic attraction and diffusion. During vacuum brazing, the parts are placed in a vacuum furnace, which provides the required heat and at the same time remove the need for flux and the risk of oxidisation during the process. Therefore the components will be clean and bright after brazing.

*Figure 3: Vacuum Brazing Furnace*

Depending on the requirements of the part and its complexity, a Helium leak check can be part of the standard procedure at this stage. Once leak tightness has been ensured and when required, the parts will undergo heat treatments to either T4 or T6 hardness stages. This will allow machining at similar feeds and speeds as those for untreated Aluminium. Depending on individual part geometries, additional processes such as straightening may allow more effective ways of machining the finished components when required.

**Typical Products**

Products which are typically vacuum brazed are liquid cold plates, flat tube heat exchangers and plate fin heat exchangers, but certainly not limited to these components. Generally vacuum brazing is employed as a process, where lightweight, high performance assemblies with increased internal surface areas are required. Additionally, vacuum brazing can be used to produce larger assemblies with complex geometries, benefiting from the low distortion introduced by the process itself. These structures can range from plank type assemblies with internal channels to electronic enclosures, with and without internal features such as cold walls.

All of the afore mentioned products benefit from the high internal cleanliness due to the fluxless process, and the lack of other substances involved in the process.  Wave guides are amongst the non-thermal products that are also regularly produced by vacuum brazing.

With any of the products mentioned above, early involvement of Thermacore engineers not only reduces the time to market, it may also significantly reduce the number of design iterations required to achieve the desired product quality. Thermacore carefully controls all its manufacturing process in order to achieve and maintain a 98% plus yield on proven out designs and products. The application of proven design rules leads towards an improved product from the onset of a project, a service, which is rarely found with normal contract brazing houses.

**Markets**

The markets segments that vacuum brazed assemblies can be found in are quite diverse. They can range from automotive products, such as oil cooler type assemblies, at the lower cost end of the market, towards highly complex assemblies, with reduced weights, for the aerospace or defence industries.

Recently, the power market and renewable energy technologies as well as the emerging market of electrical and hybrid electrical vehicles have shown a significant interest in vacuum brazed assemblies to cool their components. These include components such as batteries and dc-dc converters but are not limited to these. Generally, vacuum brazed assemblies can be found in markets, where good quality joints, lightweight assemblies and high thermal and mechanical performances are required.

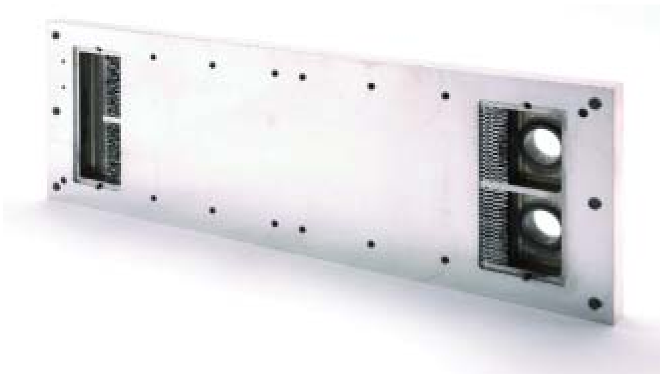

*Figure 4: Cold Plate modified for demonstration purposes*

**Summary**

Vacuum brazing is an attractive manufacturing method to produce lightweight and reliable assemblies and thermal products, such as heat exchangers and liquid cold plates. Vacuum brazed products are of a superior quality in comparison to other joining technologies such as conventional salt dip brazing and TIG welding. Additionally, there are no further requirements for internal cleaning of the assemblies and contamination risk of the system due to salts and others are non-existing. There is less distortion and a cleaner exterior due to the fluxless process. Superior thermal performance can be achieved through the ability of producing complex geometries and significantly increased heat transfer surfaces.

Thermacore can be considered as a one stop provider for numerous vacuum brazed products such as liquid cold plates, chassis and cold wall assemblies, as well as heat exchangers, but also other products produced through vacuum brazing. Additional services range from the design of the entire thermal solution to consultancy for existing designs. Pre and post braze machining of components and assemblies enable the delivery of complete components and thermal solutions. If you require any further information regarding vacuum brazed products and services, please do not hesitate to contact your Thermacore representative.

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# How to Design a Discontinuous Flyback Converter

*With the increase in recycled energy, solar power, and wind power, a significant number of new power designs are needed to provide support for these new initiatives. One of the most common power converters used to meet these new initiatives is the discontinuous-mode flyback converter.*

*By John Bottrill, Senior Applications Engineer, Texas Instruments*

The intent of this article is to walk a new designer through the process of designing one of these converters.

**Converter specifications**

To start your new design, identify the converter specifications. For this design example, use the following specifications:

- Output power ($P_{OUT}$) 100 watts
- Output voltage ($V_{OUT}$) 5 volts +/–50 mV
- Output current ($I_{OUT}$) 20 amps
- Output ripple at the switching frequency 50 mV
- Operating frequency ($F_{SW}$) 100 kHz
- Input voltage range 35 volts to 78 volts
- Input capacitor ripple voltage 0.5 volts

The power converter and its components are defined by the schematic in Figure 1.

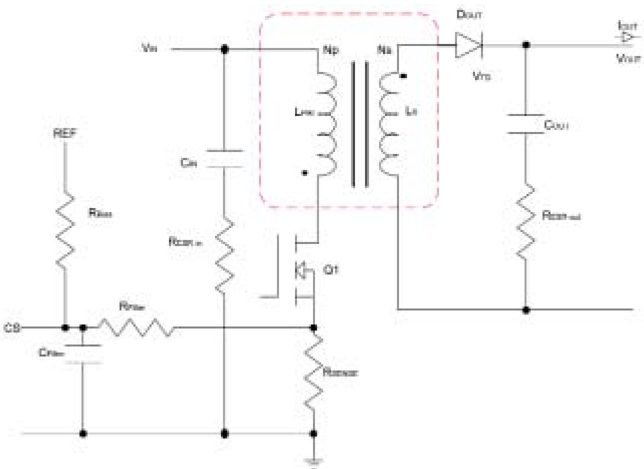


*Figure 1: Flyback converter design*

We start our design with the flyback transformer. First, establish the transformer's maximum duty cycle, which occurs at the maximum output load and minimum input voltage. Ideally, 50 percent duty cycle for both the transistor and diode are the best option, but in reality, you will need margin. The diode ($D_{OUT}$) conduction time needs to be slightly longer than the maximum transistor (Q1) on time. This prevents the drain of Q1 from ringing below ground during light-load minimum input voltage conditions.

Let the diode worst-case maximum conduction time equal 50 percent. Assume that the tolerance for the secondary winding magnetizing inductance ($L_{SEC}$) is +/– 5 percent. Assume that the diode ($D_{OUT}$) forward voltage $V_{FD}$ is 1 volt.

Now calculate the energy transfer needed per cycle (E_per_Cycle):

$V_{OUT}$ is defined in the specification as 5 Volts
$I_{OUT}$ is defined in the specification as 20 amps
$F_{SW}$ is the switching frequency defined in the specification as 100 kHz

$$\text{E\_per\_cycle} = \frac{(\text{Iout}\times\ \text{Vout+Vfd}\ )}{\text{Fsw}} = 1.2\ \text{mJ} \qquad \text{(Eq. 1)}$$

The energy transfer needed per cycle from Eq. 1 is 1.2 milli-joules.

At this point, two equations are needed. Both have to do with the energy/current in the output winding of the flyback transformer. Remember, in reality a flyback transformer is just a coupled inductor.

The integral of the total current through the diode on a per cycle basis must equal the total load current integrated over that same single-cycle time frame. Since the maximum diode conduction time ($T_{DIODE}$) is set at 50 percent of the cycle, and since the current through the inductor must be a triangle, using high school formulas for the area of a triangle, the peak of this current is a factor of four times the output current at a 50 percent conduction time. For this design it is 80 amps peak (Eq. 4).

The voltage across the transformer secondary winding ($V_{TRAN}$) (Eq. 2) is equal to the output voltage ($V_{OUT}$), plus the diode forward voltage drop ($V_{FD}$).

$$\text{Vtran} = \text{Vout} + \text{Vfd} = 6\text{V} \qquad \text{(Eq. 2)}$$

The maximum conduction time for the diode $T_{DIODE}$ is defined in Eq. 3.

$$\text{Tdiode} = \frac{1}{2\times\text{Fsw}} = 5\ \mu\text{s} \qquad \text{(Eq. 3)}$$

Now we can determine the peak diode current (IPK_DIODE) using Eq. 4.

$$\text{Ipk\_diode} = \frac{\text{Iout}\times 2}{\text{Fsw}\times\text{Tdiode}} = 80\text{A} \qquad \text{(Eq. 4)}$$

With the defined peak current for the output diode, the next step is to define the power per cycle in the secondary ($P_{IND\_SEC}$) using the specified output current $I_{OUT}$ and Eq. 5.

$$\mathrm{Pind\_sec} = \mathrm{Iout} \times \mathrm{Vtran} = 120\ \mathrm{W} \qquad \text{(Eq. 5)}$$

From Eq. 5 the maximum power needed from the secondary is 120 W. We can now determine the secondary inductance required ($L_{SEC\_MAX}$).

Eq. 6 defines the maximum inductance that the secondary inductance can have.

$$\mathrm{Lsec\_max} = \frac{2 \times \mathrm{Pind\_sec}}{\mathrm{Fsw} \times \mathrm{Ipk\_diode}^2} = 0.375\ \mu\mathrm{H} \qquad \text{(Eq. 6)}$$

Next, identify the inductance needed on the primary side. The power into the primary will be slightly higher than the power out. Assume 95 percent efficiency (Eq. 7) through the transformer. This means that the power into the primary is 126.3 W (Eq. 8). In this case, we define the selected current sense resistor RSENSE as having 0.5 volt cross it at peak primary input current (Eq. 9). You can define a half-volt drop across the FET (Eq. 10) at the same current. This sets the $R_{DSON}$ of the FET.

$$\mathrm{Iind\_eff} = 95\% \qquad \text{(Eq. 7)}$$

$$\mathrm{Pind\_pri} = \frac{\mathrm{Pind\_sec}}{\mathrm{Iin\_eff}} = 126.3\mathrm{W} \qquad \text{(Eq. 8)}$$

$$\mathrm{VRIsense} = 0.5\mathrm{V} \qquad \text{(Eq. 9)}$$

$$\mathrm{Vfet} = 0.5\mathrm{V} \qquad \text{(Eq. 10)}$$

These voltages drop the effective voltage across the primary winding ($V_{IND\_PRI}$). Knowing this voltage (Eq. 12), the input DC current ($I_{INDC}$) can be determined as in Eq. 13.

$$\mathrm{Vin\_min} = 35\mathrm{V} \qquad \text{(Eq. 11)}$$

$$\mathrm{Vind\_pri} = \mathrm{Vin\_min} - \ \mathrm{VRIsense} + \mathrm{Vfet}\ \ = 34\ \mathrm{V} \qquad \text{(Eq. 12)}$$

$$\mathrm{Iindc} = \frac{\mathrm{Pind\_pri}}{\mathrm{Vind\_pri}} = 3.715\mathrm{A} \qquad \text{(Eq. 13)}$$

For this example, we selected the UCC2813-1, a low-power economy BiCMOS current-mode pulse-width modulator (PWM) as the control IC for this analysis, partly because it has an internal duty cycle limit below 50 percent, and partly because of ease of use.

By design, The FET's duty cycle (Duty_FET) must be less than the conduction time of the output diode (Eq. 14). Set the maximum on tine for the FET (Eq. 15) to 45 percent (Eq. 14) of the total cycle time. This sets the peak current ($I_{PRI\_PK}$) the same way you set the secondary current. From this you can determine the maximum primary side inductance ($L_{PRI}$).

$$\mathrm{Duty\_FET} = 45\% \qquad \text{(Eq. 14)}$$

$$\mathrm{Ton\_FET} = \frac{\mathrm{Duty\_FET}}{\mathrm{Fsw}} = 4.5\ \mu\mathrm{s} \qquad \text{(Eq. 15)}$$

$$\mathrm{Ipri\_pk} = \frac{\mathrm{Iindc} \times 2}{\mathrm{Duty\_FET}} = 16.5\mathrm{A} \qquad \text{(Eq. 16)}$$

$$\mathrm{Lpri} = \frac{\mathrm{Vind\_pri} \times \mathrm{Ton\_FET}}{\mathrm{Ipri\_pk}} = 9.266\ \mu\mathrm{H} \qquad \text{(Eq. 17)}$$

Now that the maximum primary side inductance is determined (Eq. 17), the primary to secondary side inductance now can be used to determine the turns ratio (Eq. 18).

$$\mathrm{Np\_Ns} = \left(\frac{\mathrm{Lpri}}{\mathrm{Lsec\_max}}\right)^{0.5} = 4.971 \quad \text{set Np\_Ns} = 5 \quad \text{set Lpri} = 9\mu\text{H} \qquad \text{(Eq. 18)}$$

For ease of manufacturing, set the turns ratio ($N_P\_N_S$) to five and the primary inductance, $L_{PRI}$, which has been changed to 9 µH. This changes the secondary side inductance as well as the primary side (Eq. 19).

$$Ls = \frac{Lpri}{5^2} = 0.36\ \mu H \qquad \text{(Eq. 19)}$$

Now look at the primary current and define several items including the peak primary current (Eq. 22), the duty cycle, and the RMS current. The total charge going into the unit is defined in Eq. 20.

$$\mathrm{Qpri} = \frac{\mathrm{Iindc}}{\mathrm{Fsw}} = 37.152\ \mu\mathrm{C} \qquad \text{(Eq. 20)}$$

Next calculate the energy per cycle into the converter (Eq. 21). Then use the new primary inductance to calculate the peak primary current (Eq. 22) and the RMS current (Eq. 25).

$$\mathrm{Ein\_per\_cycle} = \frac{\mathrm{Iindc} \times \mathrm{Vind\_pri}}{\mathrm{Fsw}} \qquad \text{(Eq. 21)}$$

$$\mathrm{Ipri\_pk} = \left(\frac{2 \times \mathrm{Ein\_per\_cycle}}{\mathrm{Lpri}}\right)^{0.5} = 16.754\mathrm{A} \qquad \text{(Eq. 22)}$$

$$\mathrm{Ton\_pri\_L9\mu H} = \frac{\mathrm{Lpri} \times \mathrm{Ipri\_pk}}{\mathrm{Vin\_pri}} = 4.435\ \mu\mathrm{s} \qquad \text{(Eq. 23)}$$

$$\mathrm{Duty} = \mathrm{Ton\_pri\_L9\mu H} \times \mathrm{Fsw} = 0.443 \qquad \text{(Eq. 24)}$$

$$\mathrm{Iin\_ind\_RMS} = \left(\int_{0\,\mathrm{sec}}^{\mathrm{Ton\_FET}} \left(\frac{\mathrm{Ipri\_pk} \times \mathrm{t}}{\mathrm{Ton\_FET}}\right)^2 \times \mathrm{t}\ \mathrm{dt}\right)^{0.5} \times \mathrm{Fsw} = 3.77\mathrm{A} \qquad \text{(Eq. 25)}$$

Now identify the same factors on the secondary side using Eq. 27, Eq. 29, and Eq. 30.

$$\mathrm{Eout\_per\_cycle} = \frac{\mathrm{Iout} \times \mathrm{Vtran}}{\mathrm{Fsw}} = 1.2\mathrm{mJ} \qquad \text{(Eq. 26)}$$

$$\mathrm{Isec\_pk} = \left(\frac{2 \times \mathrm{Eout\_per\_cycle}}{\mathrm{Ls}}\right)^{0.5} = 81.65\mathrm{A} \qquad \text{(Eq. 27)}$$

$$\mathrm{Ton\_sec} = \frac{\mathrm{Ls} \times \mathrm{Isec_{pk}}}{\mathrm{Vtran}} = 4.899\ \mu\mathrm{s} \qquad \text{(Eq. 28)}$$

$$\mathrm{Duty\_diode} = \mathrm{Ton\_sec} \times \mathrm{Fsw} = 0.49 \qquad \text{(Eq. 29)}$$

$$\mathrm{Iout\_ind\_RMS} = \left(\int_{0\,\mathrm{sec}}^{\mathrm{Ton\_sec}} \left(\left(\frac{\mathrm{Isec\_pk} \times \mathrm{t}}{\mathrm{Ton\_sec}}\right)^2\right) \times \mathrm{t}\ \mathrm{dt}\right)^{0.5} \times \mathrm{Fsw} = 20\mathrm{A} \qquad \text{(Eq. 30)}$$

Note that even with this change to the inductances and its impact to duty cycle and peak currents, the diode conduction time ($T_{ON\_SEC}$) (Eq. 28) is greater than the transistor "on" time ($T_{ON_PRI_}$L9µH) (Eq. 23). Therefore, the ringing voltage on the primary side switch will not go below ground when the diode stops conducting at low input voltage and light loads.

We already determined the information necessary for the transformer. The volts second rating on the primary is 30 microsecond-volts with a primary to secondary turns ratio of five-to-one.

| Parameters | Primary | Secondary |
|---|---|---|
| Inductance | 9 µH | 0.36 µH |
| Ipeak | 16.75 Amps | 81.65 A |
| I RMS | 3.77 amps | 20 amps |

*Table 1: Inductance and current requirements for the flyback transformer*

This information can now be given to the magnetics designer along with the thermal environment and efficiency requirements.

Now we move on to the input capacitor. Assume that the source of the current is a DC current source and that the current coming out of the inductor is the current into the flyback primary at minimum input voltage. Set the change in voltage for the input capacitor as 1 volt total. Split this into the voltage change as a result of the ESR, and the voltage change as a result of difference in the net charge. Now establish the RMS current in the capacitor. Start by determining the input capacitor's RMS current (Eq. 31).

$$\mathrm{Qipcapt1} = \int_{0\,\mathrm{sec}}^{\left(\frac{1}{\mathrm{Fsw}}\right)-\mathrm{Ton\_pri\_L9\mu H}} \mathrm{Iindc}^2 \times \mathrm{t}\,\mathrm{dt}$$

$$\mathrm{Qipcapt2} = \int_{0\,\mathrm{sec}}^{\mathrm{Ton\_pri\_L9\mu H}} \left(\mathrm{Iindc} - \frac{\mathrm{Ipri\_pk} \times \mathrm{t}}{\mathrm{Ton\_pri\_L9\mu H}}\right)^2 \times \mathrm{t}\;\mathrm{dt}$$

$$\mathrm{IincapRMS} = (\mathrm{Qipcapt1} + \mathrm{Qipcapt2})^{0.5} \times \mathrm{Fsw} \;= 3.02\mathrm{A} \qquad \text{(Eq. 31)}$$

The specification has 0.5 volts of ripple voltage on the input capacitor. Therefore, we budget the voltage drop initially for 50 percent due to the capacitors ESR, and 50 percent due to the change in charge on the capacitor. For a first approximation of the charge (Eq. 32), use the input current during the off time of the primary switch. Eq. 33 yields the minimum necessary capacitance.

$$\mathrm{Qin\_FAPX} = \mathrm{Iindc} \times \left(\frac{1}{\mathrm{Fsw}} - \mathrm{Ton\_pri\_L9\mu H}\right) = 20.675\ \mu\mathrm{C} \qquad \text{(Eq. 32)}$$

$$\mathrm{Cip\_cap} = \frac{\mathrm{Qin\_FAPX}}{\frac{1}{2}\times 0.5\ \mathrm{V}} = 82.7\mu\mathrm{F} \qquad \text{(Eq. 33)}$$

The remaining capacitance voltage variation is due to the current through the capacitance's equivalent series resistance (ESR). The current into the capacitor is the input current, and the peak current out of the capacitor is the peak transformer primary current less the input current. This means that the effective differential current is equal to the peak primary current. Eq. 34 yields a maximum ESR of 15 milli-Ohms.

$$Resr\_IPCAP = \frac{\frac{1}{2}\times 0.5V}{Ipri\_pk} = 15m\Omega \qquad \text{(Eq. 34)}$$

This now defines the input capacitance CIN. The minimum capacitance must be at least 83 µF with a maximum allowed resistance of 15 milli-Ohms, and it must be rated for a 3.02 amps RMS current (Eq. 31) at 100 kHz. Allow for a 10 percent margin and an 85 volt voltage rating.

Now perform the same procedure to determine the output capacitor (Eq. 35).

$$\text{Qopcapt1} = \int_{0\,\text{sec}}^{\left(\frac{1}{\text{Fsw}}\right)-\text{Ton\_sec}} \text{Iout}^2 \times \text{t dt}$$

$$\text{Qopcapt2} = \int_{0\,\text{sec}}^{\text{Ton\_sec}} \left(\text{Iout} - \frac{\text{Isec\_pk} \times \text{t}}{\text{Ton\_sec}}\right)^2 \times \text{t dt}$$

$$\text{IoutcapRMS} = (\text{Qopcapt1} + \text{Qopcapt2})^{0.5} \times \text{Fsw} = 15.452\text{A} \qquad \text{(Eq. 35)}$$

The output ripple allowed is 50 mV. Splitting the ripple voltage between the ESR and the capacitance equally leads to Equations 36 through 38.

$$\text{Qoutcap} = \text{Iout} \times \left(\frac{1}{\text{Fsw}} - \text{Ton\_sec}\right) = 102\ \mu\text{C} \qquad \text{(Eq. 36)}$$

$$\text{Cout\_cap} = \frac{\text{Qoutcap}}{\frac{1}{2}\times 0.05\ \text{V}} = 4.1\ \text{mF} \qquad \text{(Eq. 37)}$$

$$\text{Resr\_OPCAP} = \frac{\frac{1}{2}\times 0.05\text{V}}{\text{Isec\_pk}} = .306\ \text{m}\Omega \qquad \text{(Eq. 38)}$$

This now defines the output capacitance. The output capacitor COUT minimum capacitance needs to be at least 4,100 µF (Eq. 37) with a maximum allowed resistance RESR-OUT of 0.3 milli-Ohms (Eq. 38). It must be able to handle a current of 15.5 amps RMS (Eq. 35). Use 17 amps to allow for a 10 percent margin in the current and a 6.0 volt voltage rating on the capacitor.

Figure 1 shows two resistors ($R_{BIAS}$ and $R_{FILTER}$). $R_{FILTER}$ works with $C_{FILTER}$ to remove transient spikes. However, because the CS upper limit of the UCC2813-1 is 0.9 volts, our design calls for a 0.5 volt upper limit. $R_{BIAS}$ is connected between the REF pin and $R_{FILTER}$. The $R_{BIAS}$ and $R_{FILTER}$ form a voltage divider such that, if the source of Q1 is at ground, the voltage at the CS pin is 0.4 volts. In a current limit situation, with an additional 0.5 volts across the $R_{SENSE}$ resistor, the 0.4 volts across $R_{FILTER}$ resistor drives the voltage on the CS pin to 0.9 volts, exceeding the trip point. This improves the converter's overall efficiency and reduces power lost in the $R_{SENSE}$ resistor.

Another option is to measure the current by a current transformer (Figure 2). Using this method of current sensing, you can lower the converter's power consumption.

**Conclusion**

In summary, when choosing the output capacitance, it may be necessary to put several capacitors in parallel to meet the ESR and RMS current requirements.

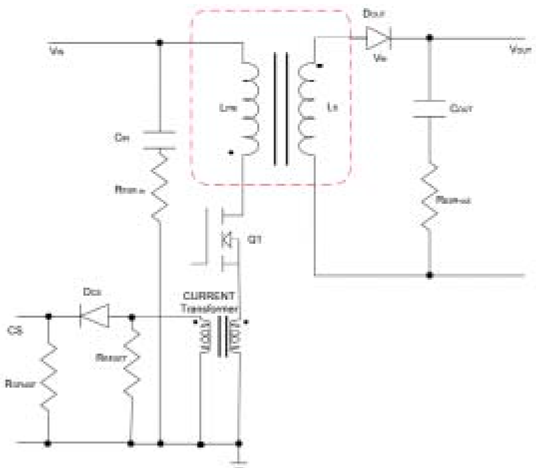


*Figure 2: Flyback converter with current transformer added*

The diode, $D_{OUT}$, has the same RMS current requirement as the transformer's secondary winding. The FET, Q1, and the current sense resistor, $R_{SENSE}$ (Figure 1), or the current transformer primary (Figure 2), has the same current requirement as the transformer's primary winding.

The single component with the highest losses is the rectifying diode on the output. It is possible to substantially reduce these losses when using a secondary side synchronous rectifier controller like the UCC24610, and modifying the circuit for synchronous rectification of the output current.

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John Bottrill is a Senior Applications Engineer at Texas Instruments, Manchester, New Hampshire. John supports customers and evaluates new ICs before release. In doing so, he has produced more than 20 technical papers and has two patents to his credit. He received his B. Sc. in Electrical Engineering from Queen's University at Kingston, Ontario, Canada. You can reach John at ti_johnbottrill@list.ti.com.


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# Integrated Approach to Wireless Charging Technology

## *Technology Gives Mobile Devices a Boost*

*Wireless Power technology is on the rise; in the last few years, many proprietary after-market solutions have become available for a variety of mobile devices. Industry as a whole recognized the need for a wireless power standard and adopted 'Qi'[pronounced Chee] as a universal standard to enforce common protocol and inter-operability through Wireless Power Consortium (WPC).*

*By Manjit Singh, Integrated Device Technology*

We are beginning to see some wireless power charging pads becoming available in the market, but due to the complexity of their design, they are being sold at retail price close to $100 US. To date, this has been cost prohibitive to major carriers such as AT&T, Verizon, and Sprint, and to OEMs that include Samsung, LG and Nokia. Such complexity and the resultant higher cost of wireless power transmitters dis-incentivized carriers and OEMs from including a charging pad as a standard 'in-box' accessory. Instead, an after-market product approach has been taken and the pricing point of the charging pad isn't very attractive to the end user. This article covers some guidelines and tips for engineers designing a WPC compliant wireless power transmitter that is cost competitive and low in terms of complexity.

**Introduction**

In today's age of infotainment, portable mobile devices such as smart phones, tablets and eBook readers, are using the stored energy in their batteries at such high rates that recharging the battery in middle of the day has become a necessity, not an option. Gone are the days when a mobile device, when fully charged, could operate for several days. User demand for audio &Video streaming, high definition gaming, GPS, and frequent web browsing, means that energy usage has outpaced the small advancements made in increasing battery energy density over the past few years.

Carrying around AC adaptors is impractical and inconvenient. As useful as they are, AC adaptors are bulky and they often come with proprietary connector types. The proliferation of mobile technology means for example a typical family of four may carry, on average, about seven mobile devices for a domestic flight. As such, carrying seven different AC adaptors is a significant burden. Not to mention the issues involved in dealing with different voltage ratings and connectors for different countries or regions. Finally, it has to be said that the aesthetics of AC adaptors are not ideal and do not complement the highly stylized portable devices they are designed for.

Wireless Power Charging, as a technology based on induction, is not a new concept; in fact it fascinated Nikola Tesla (1856 – 1943) in his heyday! What is new today is the need for wireless power charging for mobile devices whose battery size and capacity isn't keeping up with the use-model of the battery. While end-users take their lunch break, it makes sense, and is almost a necessity, that their mobile device 'power snacks' wirelessly too. This has not happened yet because the cost of the wireless power transmitter has been prohibitive for both OEMs and infrastructure vendors. Because of the high cost of constructing a transmitter, carriers and OEMs have had to price a charging pad at around $80 to $100 US. This is largely due to the IC solutions currently available on the market; a typical wireless power transmitter using the available technology consists of nine ICs and more than 80 passive components.

**Wireless Power Charging System**

A typical wireless power charging system consists of a transmitter and receiver that are coupled inductively through two sets of coils as shown in Figure 1.


*Figure 1: A wireless power charging system using IDT's IDTP9030 and IDTP9020 devices*

On the transmitter side, an inverter (half-bridge in the example) converts a DC input voltage into an AC current signal. A changing AC current in the transmitter coil induces a voltage in the receiver coil following Faraday's law of induction and Biot-Savart's law.

Biot-Savart's Law dictates the amount of magnetic field generated by the transmitter coil current at a given distance or coupling; Whereas Faraday's law dictates the induced voltage on the receiver coil due time varying flux resulting from magnetic field of the transmitter coil.

The net result is that the incoming AC signal is converted into DC by a synchronous full-bridge rectifier on receiver as a loosely regulated rectified voltage. Further, this rectified voltage is converted into a tightly regulated DC voltage through a DC-DC stage (an LDO or a switching regulator).

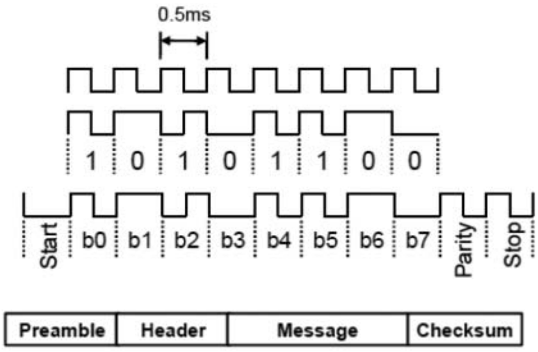



*Figure 2: WPC protocol*

**Communication link (from RX to TX)**
In the WPC communication protocol, the receiver sends communication packets through a back-scatter modulation method. The receiver modulates the load seen by the transmitter through reflected impedance to send communication bits over the same power link that exists between the two coils. A 2 KHz digital communication signal on the receiver side translates into a primary coil current/voltage having the same envelope.

Communication throughput per the WPC protocol is 2Kbps and it utilizes a differential Bi-Phase encoding scheme. Each packet has a structure and format to it (Preamble, Header, Message, and Checksum):

**Pre-amble:** A stream of 1's condition the transmitter and allow it to start detecting communication packets coming from the receiver.
**Header:** Indicates what type of packet is the current packet and what the payload/message that is to follow after this.
**Message:** The actual payload/message of the packet. The size of the message is a function of the type of packet.
**Checksum:** At the end of each packet, the checksum byte allows the transmitter to detect errors in the packet just received.

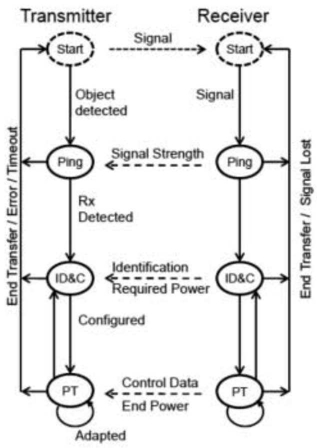



*Figure 3: Control Protocol*

**Control Protocol**
WPC has a control protocol that has four phases: Selection, Ping, ID & Configuration, and Power Transfer.

Each phase has certain required packets that the receiver must send to the transmitter to continue the power transfer. Some of the packets involved in each phase are shown in the table 1.

| Header* | Packet Types | Message Size |
|---|---|---|
| *ping* phase | | |
| 0x01 | Signal Strength | 1 |
| 0x02 | End Power Transfer | 1 |
| *identification & configuration* phase | | |
| 0x06 | Power Control Hold-off | 1 |
| 0x51 | Configuration | 5 |
| 0x71 | Identification | 7 |
| 0x81 | Extended Identification | 8 |
| *power transfer* phase | | |
| 0x02 | End Power Transfer | 1 |
| 0x03 | Control Error | 1 |
| 0x04 | Rectified Power | 1 |
| 0x05 | Charge Status | 1 |

*Table 1: Packets involved in each phase*

**Signal Strength Packet:** Is the very first packet a receiver is required to send to indicate to the transmitter not to remove power signal. It also indicates the relative strength of the signal received by the receiver. Received signal strength can be a power, voltage, current or combination of these.

**ID and Configuration Packet:** Is the second packet the receiver sends to identify itself in terms of class of receiver, configuration information, any additional proprietary or optional packets to follow etc.

**Control Error Packet:** In power transfer state, the receiver conveys to the transmitter its power needs via control error packets. The value is a signed integer between -128 to +127. Negative values instruct the transmitter to 'decrease' the power whereas positive control error value indicates 'increase' the power.

**Rectified Power Packet:** In power transfer state, receiver conveys the amount of power it is delivering to the load from rectifier via this packet. It is an unsigned integer value between 0 and 100. A 0 rectified power value implies receiver isn't providing any power to the downstream load whereas 100 implies receiver is delivering full power the load.

**Designing a wireless power transmitter using IDTP9030**
Integrated Device Technology's IDTP9030 is the world's first single chip solution for wireless power transmitter. It seeks to offer a low cost solution with the highest level of integration. It integrates several value-add features such as Foreign Object Detection (FOD), two-way communication, and multi-mode operation. The IDTP9030, plus a few additional passive components, allows the construction of a fully functional wireless power transmitter. The IDTP9030 has a high efficiency half bridge inverter to do DC-AC conversion of input DC voltage into AC coil current. It also has an on-board modulator/demodulator block that detects, demodulates, and decodes WPC compliant communication packets. There is an embedded micro controller with RAM/ROM that executes incoming decoded packets and adjusts the operating point to adjust transmitted power to the receiver.
When configured in dual mode operation, the IDTP9030 automatically detects the type of receiver (WPC or proprietary) and adjusts its behavior based on the protocol used by the receiver.

TX-A1: 'Magnetically Guided' type transmitter Comparison

*Figure 4: Typical evaluation kit (top) and one from IDT (bottom)*

A typical TX-A1 transmitter manufactured with currently available ICs can be a very complex and expensive solution. Shown in Figure 4 is a comparative example between a typical evaluation kit (top) and one from IDT (bottom).

A fully functional IDTP9030 based TX-A1 type transmitter can be constructed with 30 components, including a single IC. In comparison, the same transmitter from the other evaluation board requires 90 components including five ICs. Utilizing a highly integrated transmitter IC translates to a much simpler finished design which is lower cost, has a significantly smaller footprint, and lower complexity.

This type of approach will enable carriers and their OEMs to introduce wireless charging to their end customers at lower cost and as sleek charging pads. Moreover, an ultra low cost transmitter incentivizes infrastructure vendors to rapidly design and deploy wireless charging pads into consumer end products such as furniture, tables, night lamps, and docking stations.

**www.idt.com**

# Enabling More Effective Battery Charging Over USB Interconnects

*USB ports are clearly a convenient place for portable devices to draw power from*

*Developed in the mid 1990s, USB has gone on to become the most widely used data interface on the planet. Its huge popularity has certain additional upshots which are also now being realised. Market pressures are beginning to make it attractive as the principal way to power electronics hardware. As of January 2011, the European Commission (EC) introduced a policy that means all smartphone/data-enabled phone handsets sold in Europe need to have the ability to be charged via a standard micro USB connector. This will help consumers to escape from the irritation of having to rely on various proprietary cables to charge each individual portable electronics item they possess.*

*By Graham Brown, Applications Engineer,*
*Future Devices Technology International (FTDI)*

USB offers the means with which to charge multiple portable devices through a single 'universal' power source, resulting in far greater convenience. There are challenges with its employment in this role, however. Previously the charging capability of USB was fairly limited. The amount of current available from a standard USB Host port was really only suited to powering computer peripherals, such as keyboards, mice and card readers. USB 2.0 supports a charging current of up to 500 mA, which can translate into a prolonged charging process for some batteries. At the same time, the public at large is requiring shorter recharge periods.

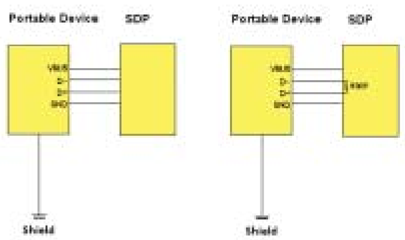



*Figure 1: Difference between a DCP and SDP*

In this environment, the USB Charging Specification Version 1.2, was announced in early 2011, offering new powering modes that increase flexibility when it comes to replenishing devices' batteries. The document introduces the concept of a Dedicated Charging Port (DCP) which enables a maximum current of 1.8 A to be supported. This nearly quadruples the current that a Standard Downstream Port (SDP) USB 2.0 connection can carry, resulting in considerably quicker charge up time.

**All about the DCP**

The USB interface is made up of four shielded wires. These are:

- VBUS which is used to power the connected peripheral
- D- which is the negative data terminal
- D+ which is the positive data terminal
- GND which is the ground connection

In a DCP, both the D+ and the D- ports are shorted together with a 200 Ohm resistor, so that data transfer is prevented. It indicates to the connected peripheral that the port is fully focussed on the charging function and does not provide Host functionality. It is vital that any portable device that is to be connected with a USB port can differentiate between it being a DCP or an SDP. This will allow it to take advantage of the larger charging current that is available.

**DCP Identification**

Figure 2 shows an example of a charging circuit in line with version 1.2 of the USB charging specification. It includes a large number of discrete components and requires the systems' microcontroller to take care of the identification procedure. This means that a proportion of microcontroller's valuable processing capacity cannot be devoted to the core application, thereby impinging on the system's overall performance. Furthermore, a relatively large bill of materials is called for, as well as many hours to write the necessary code and to implement the circuit design in a way that makes it fully effective.

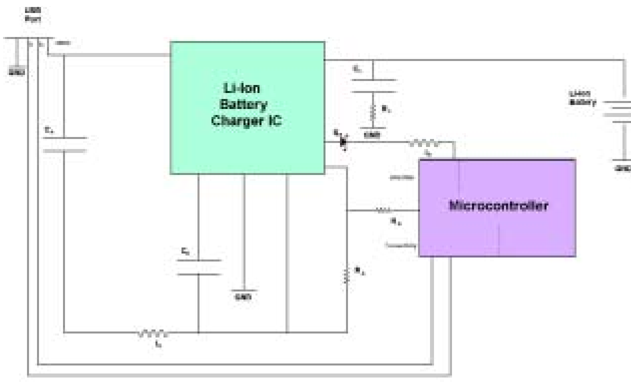



*Figure 2: Conventional USB Battery Charging Schematic*

FTDI has endeavoured to simplify USB charging, so that development time, system complexity and utilisation of engineering resource are all minimised for the greatest return on investment. To this end it has introduced the X-CHIP series of USB controller ICs, which has a feature set that supports the new concepts of USB battery charging. Circuitry inside each IC enables the portable device it has been incorporated into to detect when it becomes connected to a DCP. Once a DCP is detected, the X-CHIP asserts a signal on one of its CBUS pins to enable charging to begin.

Figure 3 describes a battery charging application based around the X-CHIP. The circuit will charge a battery when connected to either a USB Host port or a DCP. The CBUS pins can be used to control the charging rate of the battery depending on the power source which has been detected and its associated current limit. The charge rate of the battery is defined by the resistance connected to the PROG pin of a Linear Technology LTC4053 battery charging controller.

**The CBUS pins are:**

- The BCD# is an open-drain active-low output signal. It is asserted to indicate when the X-CHIP has been connected to a DCP.
- The PWREN# is open-drain active-low output signal. It indicates that the X-CHIP has been enumerated by the USB Host controller. It is used to select the resistance value on the PROG pin in order to enable 500 mA charging.
- The SLEEP# is a push-pull active-low output signal. It indicates when the X-CHIP has been put into USB suspend mode. It is used to shut down the LTC4053 when the device is powered from a USB Host and the Host has put the X-CHIP into suspend mode.

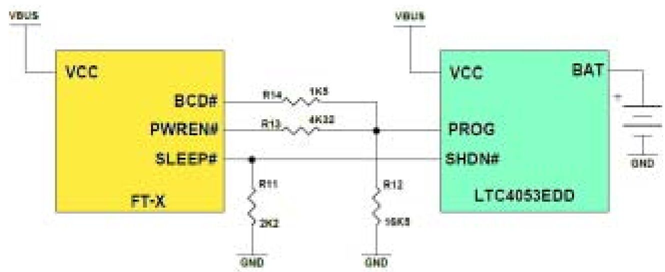



*Figure 3: Simplified USB Battery Charging Schematic*

In Figure 3, the resistance of the PROG pin of the LTC4053 is set by resistors R12, R13 and R14. The BCD# is used to configure the resistor network on the PROG pin to set approximately 1 A charging current.

The BCD#, PWREN# and SLEEP# outputs have been designed to minimise the external circuitry required for charging applications. Normally external MOSFET devices are required to select the range. As already mentioned, the X-CHIP asserts its BCD# signal to indicate the detection of the DCP. This open-drain output short circuits R14 to ground and the PROG pin of the LTC4053 will therefore have a resistance of 16.5 kΩ in parallel with 1.5 kΩ to ground. This results in a charging current of approximately 1 A being initiated. When the X-CHIP is connected to a standard USB Host controller, this pin is not asserted and the device operates as a traditional USB interface chip. Since the BCD# signal is open-drain without an internal pull-up, it can be used to pull resistor R14 to ground without the need for utilising any external MOSFETs.

During start-up of the device, the CBUS pins will default to an input with weak pull-up until the MTP ROM is read. This will occur for approximately 14 ms and the CBUS pins will then take their selected function and behave as described elsewhere in this article.

**Conclusion**

Thanks to their widespread use, USB ports are clearly a convenient place for portable devices to draw power from, potentially delivering as much as 10 W to a variety of different devices through a single interconnect. Furthermore, the push to standardise on USB charging by various countries (including China and EU member states) is allowing consumers to employ fewer charging cables. This will increase convenience while reducing the quantity of electronic waste entering the environment each year (which was being caused by customised adapters). Lastly, by using an integrated approach rather than relying on discretes it is possible to create far more optimised charging circuits in terms of space, components and engineering resource. In the end, USB is not only the most popular wired, digital interconnect, but a key system element for providing power and charging the batteries of electronic products.

**www.ftdichip.com**

# Enabling Device Connectivity for Remote Power Management

*Reduced maintenance expenses, and higher uptime are quickly realized.*

*Many businesses and service providers rely heavily on geographically dispersed equipment. But when a device "locks-up" or fails, the options for recovery are limited.*

*By Martin Poppelaars, VP EMEA Sales Europe, Lantronix*

Being able to get to the equipment remotely can save expense and allow for quick problem mitigation. One simple but effective method of fixing many problems is to cycle power or reboot. If the device is at a remote POP site, Telco central office, co-location facility or even an equipment room, gaining access to perform the reboot on the device can present a challenge.
A majority of enterprises use uninterruptible power supplies (UPS) to keep their equipment operational. Multiple devices are connected via a single UPS to power outlets, which poses its own dilemma.

If an individual router fails, for example, the UPS does not have the ability to power cycle an individual power outlet. There are typically two recovery choices. One option is a radical approach whereby an operator can command the UPS to simultaneously power cycle both itself and all its attached devices. The second choice is to dispatch a technician to power cycle the problem router at the remote location. Both options have clear drawbacks in terms of time and expense.

**The pitfalls of dropped connections**
The direct or indirect revenue stream dependent on remote equipment is jeopardised with the long list of problems caused by a failed network.

Firstly, many third party technician service calls to locked-up network equipment are solved with a reboot operation. Yet a third party service call averages about (use local currency).

In addition to this, the average downtime from locked-up equipment averages 1.5 hours. From this, service level penalties and lost revenue go up exponentially, depending on the size of the enterprise.

The knock on effects of this, of course, are lost revenue, customer dissatisfaction, decreased productivity and service level agreement penalties. The importance of attaining the fast and easy recovery of locked up devices, therefore, should be paramount. But where to begin?

**Intelligent Power Distribution**
Service providers and other businesses whose revenue is dependent upon the quantity of remote devices they manage need to know the maximum number of devices the available power resource will support. A critical factor that defines what equipment can be installed is the available power. Yet, configuring the maximum number of devices for a power supply is not a straightforward process.

With the expectation of an always on, always working Internet economy, installation of new equipment is needed to handle the exploding data loads. Adding more equipment, however, is constrained by the availability of power resources and complicated by the manufacturer's nameplate specification, which is generally inaccurate and cannot be used for power planning.

The solution for adding new equipment to existing power supplies is to perform power measurement verification. If, however, equipment units are co-located at multiple sites, then performing on-site measurement verifications becomes costly and time-consuming. There is also the consideration that technicians with the skills to perform power verification are very limited. Remote Power Management devices can expedite this process, performing the needed measurements and verification remotely.

**The need for remote management**
Remote Power Management combines intelligent power distribution, management and measurement into a single device. Using this solution, network and system administrators, service providers and hosting companies are able to power On/Off and reboot attached servers or individually control the power to attached devices from a remote location. This is achieved via in-band or out-of-band communications through a Console Server, Remote power manager, Remote KVM™ or directly over an IP network.

The Remote Power Manager provides the ability to immediately power cycle or reboot the network without interrupting all the equipment attached to the UPS.

Remote Power Managers, in conjunction with a console server or Remote KVM, can also initiate a graceful shut down for a wide variety of servers, and provide remote equipment monitoring to ensure that software is running correctly.

Another important function that Remote Power Managers can provide is power sequencing. During a power-up, each of the power outlets can power on sequentially, which distributes the load and eliminates the risk of a blown fuse or circuit breaker trip due to inrush currents. Highly useful in a networked data centre, power sequencing gives system administrators the option to turn on certain devices before others.

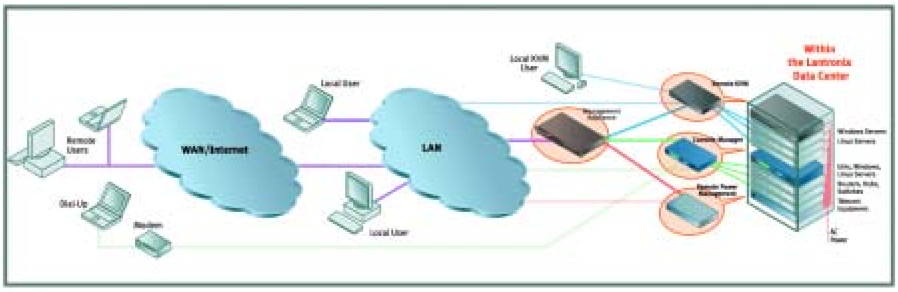
A further way Remote Power Managers help to maximize data centre utilisation is through environmental monitoring. Remote Power Managers can also include temperature and humidity sensing allowing for the remote monitoring of critical environmental conditions.

### How Remote Power Management Technology Works

Remote power management can be done by securely connecting directly to the power manager for individual device control or through a management appliance that facilitates the control of large numbers of devices. User interfaces with clear and understandable screens and/or commands are essential for smooth operation.

### Security

Direct TCP/IP access to each Remote Power Management device on the network is the fastest and most direct method to reboot an individual server or router, but also presents the greatest security risk to the network. If not properly secured, this could allow nefarious individuals to power down or up devices without proper authorization.




### User Interface

There are typically two types of user interfaces that are supported. A graphical user interface (GUI) allows an operator to control the power to devices directly.

The command line interface (CLI) allows script files to be constructed and sent directly for execution. Remote Power Managers execute the commands sent to them via scripting or direct from the user and provide appropriate feedback.

Network control hardware such as routers, DSU/CSU, network servers and uninterruptible power supplies often require In-Band management. For remote access to critical network hardware, SNMP management, IP-based management tools and other In-Band management approaches are needed. But when the network in a remote location is not functioning, SNMP and In-Band management tools are of no use.

A good alternative to sending a technician on-site is to install an Out-of-Band management system. Out-of-Band management provides dial up access to the RS-232 console, craft, or AUX ports on network control hardware. With this access, systems administrators can communicate with routers, DSU/CSU, file servers, or any other network hardware equipped with an asynchronous RS-232 control port, with a modem and phone line. This allows for remote diagnosis and resolution of problems which require more than a power cycle.

To prevent such an attack, the Remote Power Manager solution must provide encrypted security solutions for network traffic. True access security is provided only when utilising one of the commonly used security protocols, such as SSL, TLS, and SSH security protocols. SSH and TLS/SSL represent the strongest security protocols available for communicating and managing a Remote Power Management device via TCP/IP network. Both of these protocols provide for authentication and the strongest of encryption of the entire session.

### Conclusion

Maintaining "five nines" of uptime in the data centre is imperative for today's distributed networks. Remote Power Management offers a solution to quickly return a network to operational status after a failure or a system reconfiguration. In doing so, businesses can achieve maximum uptime by isolating individual locked-up components and independently rebooting the failed device. In other cases, it allows for remote out of band access to the console port for problem resolution.

In being able to offer this level of remote access, monitoring, and control of equipment, the results of quicker problem resolution, reduced maintenance expenses, and higher uptime are quickly realized.

**www.lantronix.com**

# High-Speed Switching IGBTs for Induction Heating

Toshiba Electronics Europe has announced two new additions to its family of compact and integrated IGBTs for induction heating and other current resonance inverter switching applications. As with previous models, the 600V, 50A GT50JR21 and GT50JR22 combine an IGBT and a reverse recovery freewheeling diode into a single, monolithic device.


Ideal for use in cooking appliances, the new devices are supplied in a TO-3P(N), TO247-equivalent package and offer a high maximum junction temperature rating of 175ºC. Maximum current rating for both parts is 50A. Typical saturation voltage (at IC = 50A) is just 1.5V for the GT50JR21 and 1.65V for the GT50JR22.

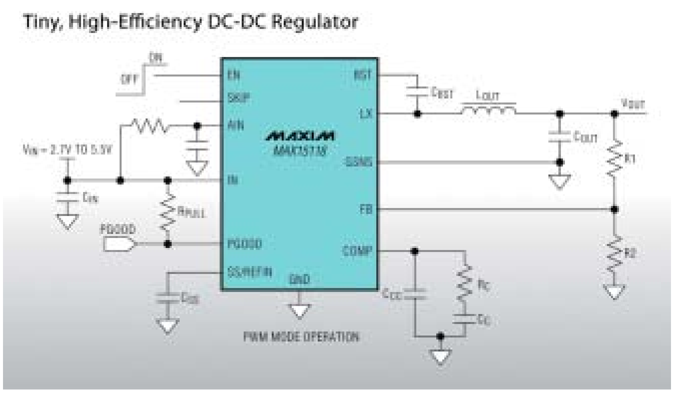
Typical IGBT turn-on time (ton) and turn-off time (toff) with a collector current of 50A are just 0.26µs and 0.31µs and 0.25µs and 0.37µs respectively. Consequently, the GT50JR21 is suitable for low frequency switching and GT50JR22 is suitable for higher frequency switching. The collector power dissipation for each IGBT is 230W at 25ºC.

**PCIM Booth 12-301**

**www.toshiba-components.com**

# DC-DC Regulators for Space-Constrained Applications

Maxim Integrated Products (NASDAQ: MXIM) introduces the MAX15058 / MAX15108 / MAX15112 / MAX15118, the industry's smallest current-mode, synchronous DC-DC converters that deliver up to 3, 8, 12, and 18A, respectively, of output current. These DC-DC regulators integrate MOSFETs to simplify designs and provide the highest efficiency in a tiny wafer-level package (WLP). Operating in fixed pulse-width modulation (PWM), they are suitable for telecom, networking, server, and base-station applications. Configured in a pulse-skip mode, they will reduce power during light load conditions found in notebook and single-cell battery applications.




These DC-DC regulators are highly efficient and deliver up to 94% and the MAX15108 delivers up to 95% conversion efficiency at full load. This reduces overall power loss in the system.

The MAX15058/MAX15108/MAX15112/MAX15118 operates from a 2.7V to 5.5V input voltage and provide ±1% output-voltage accuracy over load, line, and temperature. The devices are fully specified over the -40°C to +85°C extended temperature range.

**www.maxim-ic.com**

# Full-Bridge PWM Microstepping Motor Driver IC

Allegro MicroSystems Europe designed the A4975 a full-bridge motor driver IC for one winding of a bipolar stepper motor in a microstepping mode.


Internal pulse-width-modulated (PWM) current control combined with an internal three-bit nonlinear digital-to-analogue converter allows the motor current to be controlled in full-, half-, quarter- or eighth-step (microstepping) modes, while nonlinear increments minimise the number of control lines necessary for microstepping. The benefits of microstepping include increased step resolution and reduced torque variations and resonance problems at low speed.

The outputs of the A4975 are rated for continuous output currents up to ±1.5 A and operating voltages up to 50 V. The device includes synchronous rectification control circuitry which lowers IC power dissipation during PWM operation and reduces the need for external Schottky diodes.

Internal circuitry determines whether the PWM current-control circuitry operates in a slow (recirculating) current-decay mode, fast (regenerative) current-decay mode, or mixed current-decay mode in which the "off" time is divided into a period of fast and slow current decay.

**www.allegromicro.com**

# Boost Converter for Stop-Start Automotive


International Rectifier has introduced the automotive-qualified AUIR3240S battery power switch for the combustion-engine shut-off and restart function (Stop-Start system) that can help reduce fuel consumption in automotive vehicles by up to 15percent.

The AUIR3240S is a highly integrated boost converter designed specifically for the Stop-Start system that halts the engine when a vehicle is stopped in traffic. This system requires a “board net stabilizer” using a power switch that disconnects the starter and main battery from the auxiliary electrical systems during engine start. The AUIR3240S is capable of driving several MOSFETs in parallel to achieve very low on-state resistance (Rds(on)) with current consumption below 50µA. The device provides 15 V on the output with a wide input voltage (4-36 V). The AUIR3240S also features diagnostic on the output current and a thermal sensor interface for very robust designs.

**PCIM Booth 11-111**

**www.irf.com**

# High Accuracy Programmable DC Power Supply Generation

Magna-Power Electronics, a leader in high power programmable DC power supplies, has released its next generation product line featuring major performance upgrades. The new generation, spanning every product model from 2 kW to 2000 kW+, addresses a wide-range of new demanding application requirements.


Key new features introduced are:

High Accuracy Programming and Monitoring: Enhancements to the product controls and calibration procedures enabled an over five-fold improvement in accuracy. Accuracy specifications are now ±0.075% of full-scale voltage/current programming and ±0.2% of full-scale voltage/current monitoring.

Electronic Output Bleeder Stage: Standard output bleeder resistance was replaced with near constant power electronic loading.

Integrated EMI Filter: Iintegrated EMI filters are now a standard on the entire product line, enabling improved EMI/EMC performance. All products ship with CE conformity.

The new generation is now available and the built-to-order lead-times are as short as 2 weeks, consistent with Magna-Power Electronics newly reduced delivery schedules. All products are designed and manufactured in Flemington, NJ USA.

**www.magna-power.com**

# Single-Phase Power Metering SoC for Smart Grid

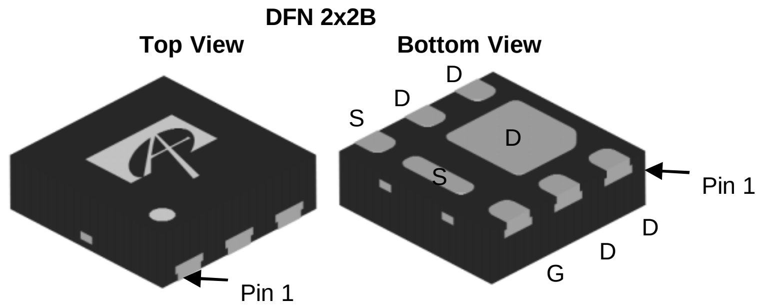

Integrated Device Technology, Inc announced the world’s most advanced single-phase power metering SoC for smart grid applications. This new device features the industry’s widest dynamic range and an unprecedented level of integration, enabling smart meter manufacturers to improve accuracy, while simplifying their designs and lowering overall system cost.

The IDT 90E46 is a single-phase SoC for smart meter designs, which integrates an energy metering analog front-end with a real-time clock, temperature sensor, LCD driver, and ARM Cortex M0 microprocessor. The metering device is the latest member of IDT’s award-winning family and offers the industry’s widest dynamic range of 5000:1, which enables meter manufacturers to merge various meter types into one, thus simplifying the design and manufacturing process for meter makers and reducing the storage and management complexity for utilities.

**www.idt.com**

# MOSFETs in DFN 2x2 Package Offer Space Savings

Alpha and Omega Semiconductor Limited introduced a series of new solutions in a DFN 2mm x 2mm package. This broad portfolio of new products offers exceptional performance while enabling affordable form factor solutions used in hand held applications. The ultra small package is optimized for portable wireless solutions such as in tablet PCs, eReaders, smart phones, digital cameras, MP3 players, and ultrabook computers. The ultra low on-resistance of these MOSFETs reduces conduction losses which translate into lower power consumption and longer battery life. The compact footprint and ultra-thin 0.6 mm profile of the DFN2x2 power package enables more efficient solutions in space constrained applications. AON2410, AON2409, AON2408, AON2407, and AON2406 are the best-in-class 20V and 30V devices on the market today in a DFN2x2 package and are used for load and battery switches in portable applications. AON2403, AON2405, and AON2406 provide ultra low on-resistance values down to guaranteed spec at 1.5V rating helping the designers to drive their circuit with lower supply voltage, which in turn lowers the power consumption and improves battery life.




**PCIM Booth 12-669**

**www.aosmd.com**

# Power Measurement Software for Stand-by Testing Standards

A new power measurement software package for the Yokogawa range of precision power analysers provides a complete solution for the testing of standby power in accordance with the latest IEC62301 Ed.2.0 (international) and EN50564:2011 (European) standards.


The software, designed for use with the Yokogawa WT210, WT500, WT1800 and WT3000 power analysers, is targeted at manufacturers of domestic electrical appliances and related equipment, who need accurate measurements to ensure that their products operate at optimum energy efficiency with minimum standby power consumption.

The new standards will help to ensure that power efficiency is incorporated into all the key stages of the product manufacturing process, and Yokogawa's world-class measurement solutions will, in turn, help the industry to develop products with lower standby power consumption in compliance with the IEC and EN standards.

**PCIM Booth 12-329**

**www.tmi.yokogawa.com**

**www.yokogawa.com**

# Introduction of Planar Transformers

Wurth Electronics Midcom Inc. introduces the newly developed planar transformer product series.
The series is optimized for frequencies ranging from 200kHz to 700kHz, with 500VDC isolation and 250W power handling capabilities. Developed to be fully customizable to individual customer needs, the planar SMD transformers comes in multiple turns ratio options with optional Aux winding for maximum flexibility. The parts have a low-profile height of 10mm and an operating temperature range of -40°C to +125°C.

The patent-pending design offers a multitude of advantages compared to traditional bobbin-wound products including reduced size and weight, high efficiency, low leakage, consistent parasitics and excellent thermal characteristics. The innovative use of pre-formed flatwires yields significant cost reductions compared to existing stacked layer and multilayer PCB designs.

**SMT Booth 9-202**

**www.we-online.com**

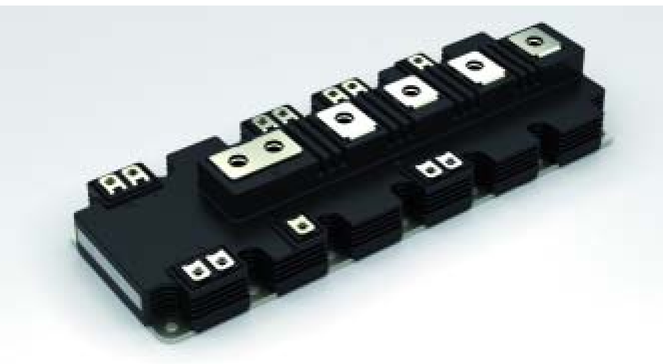
# Surface Mount Inductor

Renco Electronics announces their latest addition, RL-8100 Series, purports to build on Renco's already successful line of surface mount inductor products. Standing at only 2mm tall, the RL-8100 series boasts an ultra-compact design that offers simple pick and place from its tape and reel packaging. Although compact, the RL-8100 doesn't lack toughness. With an operating temperature range of -40°C to +130°C, the RL-8100 series displays high heat resistance as well as new, magnetically shielded construction. Rugged durability, combined with a small frame and economic price make the RL-8100 ideal for use in laptops, smartphones and other personal computing devices.


**www.RencoUSA.com**

# Product Line for 3L Applications

Mainly driven by the photovoltaic and UPS market, the NPC circuit topology (3L topology) is considered to be used in more and more applications. Danfoss Silicon Power offers the right solutions with low internal stray inductance for these specific products. The customer can choose between various standard housings with flexible pin out configuration. Starting with the small E1 with a max. 3L rating of 100A/650V, the complete range of E-type modules can be build up as 3L modules. Maximum power will be reached by using the Danfoss P3 module with a power rating of 1200A/650V or 600A/1200V. The type of circuit is not limited to a standard NPC configuration only: The customer can choose between a bidirectional switch NPC (BSNPC) circuit too or decide for a Vienna bridge with thyristors inside for soft start applications for example. Selecting the right chips from all leading chip manufacturers opens a lot of various possibilities to find the ideal and most cost-effective solution for a customer's requirement.



**PCIM Booth 12-325**

**http://siliconpower.danfoss.com**

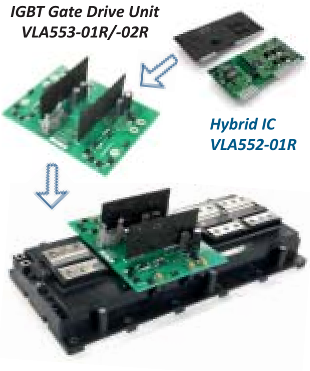
# Automotive Gate Driver ICs Deliver Increased Efficiency and Reliability

Engineers in the automotive space are faced with the challenges of delivering inverter designs with increased efficiency, higher drive current and greater immunity to noise, especially in hybrid electric vehicles (HEV) and electric vehicles (EV). To help designers meet these challenges, Fairchild Semiconductor developed the FAN7171 high-current, high-side gate driver IC and the FAN7190 high-current, high- and low-side gate driver IC.
Part of a family of automotive high voltage ICs (HVIC) gate drivers, the FAN7171 and FAN7190 are ideal for electric and hybrid electric DC-DC power supplies and power inverters, diesel and gasoline injectors and valves as well as MOSFET and IGBT high-side driver applications.


The FAN7171 and FAN7190 HVIC devices deliver an integrated inverter solution with higher efficiency, more drive current and more robustness in harsh automotive applications.
The FAN7171 is a monolithic high-side gate driver IC that can drive high speed MOSFETs and IGBTs that operate up to +500V, while the FAN7190 can drive MOSFETS and IGBTs that operate up to +600V. Greater drive capability enables higher power systems with an increase in power efficiency.
Both devices have a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction. Better noise immunity, with a negative voltage swing (VS) down to -9.8V at 15V VBS, allows for improved design reliability and increased durability in challenging noise environments.

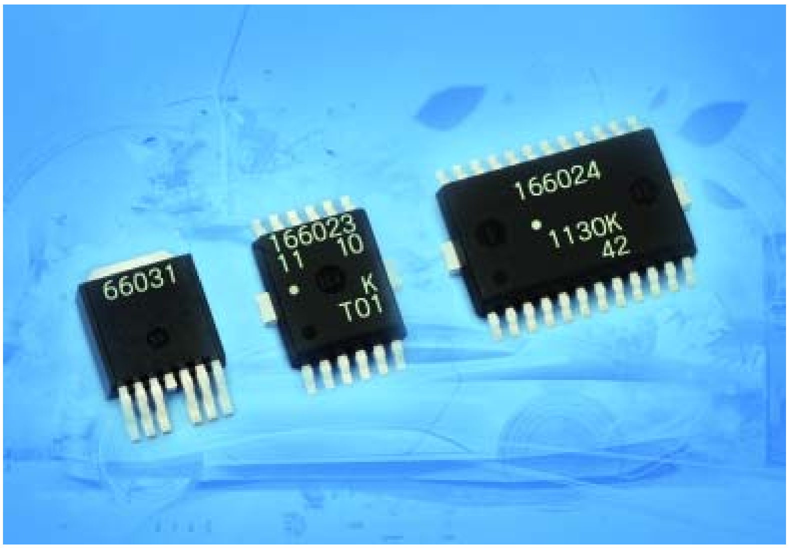
**PCIM Booth 11-320**

**www.fairchildsemi.com**





## Intelligent Power Devices with Enhanced Protection Functions for Automotive Body Applications




Renesas Electronics, a premier provider of advanced semiconductor solutions, today announced 14 new intelligent power devices (IPDs), including the ìPD166023, designed for automotive applications driving exterior lamps such as headlamps and fog lamps as well as seat heaters and motors.

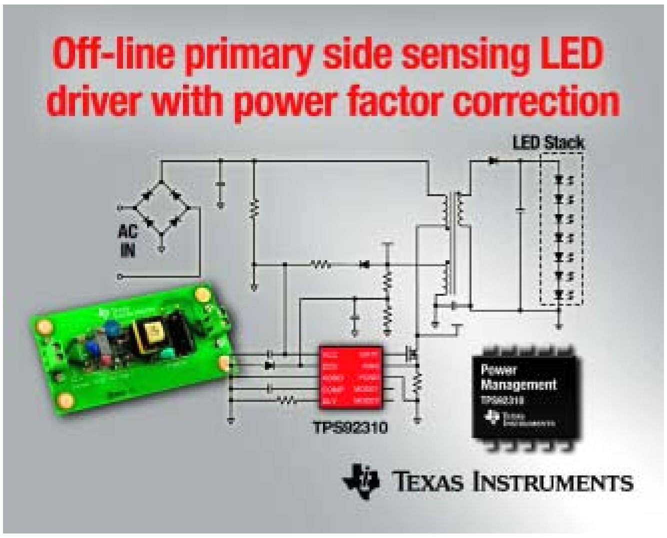
An IPD is a power IC device that incorporates in a single package, or on a single chip, a power semiconductor switch (power MOSFETs) and its control circuit featuring interface to microcontroller (MCU) as well as protection functions and self-diagnostic. Renesas has been mass producing IPDs for automotive body applications for many years. The new IPD products expand this existing lineup and increase performance level to address strong market demand.

**PCIM Booth 12-364**

**www.renesas.eu**

## Dual Mode Off-Line Controller for Non-Dimmable LED

Texas Instruments Incorporated introduced a off-line primary side sensing controller to its portfolio of non-dimming LED drivers. The new TPS92310 AC/DC constant current driver with power factor correction (PFC) reduces cost and shrinks-to-fit in high-power LED retrofit bulbs, including A19, PAR30/38 and GU10. For more information, samples and an evaluation board, visit http://www.ti.com/tps92310-preu .




The TPS92310 is the first in a family of primary side, regulated controllers with PFC.  In May, TI will offer the TPS92311 with similar features and an integrated, 600V power FET with avalanche energy capability, further reducing solution size and component count. The TPS92310 and TPS92311 join TI's portfolio of off-line LED lighting controllers that include the National LM3445, the industry's first TRIAC dimmable LED driver with both full-range and flicker-free dimming. For more information on all of TI's lighting products, visit http://www.ti.com/lighting-pr.

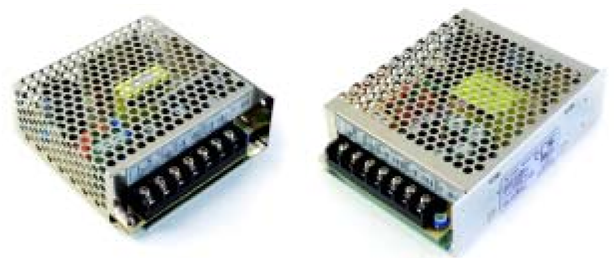
AC input voltage supports all common line voltages (100V, 120V, 230V, 240V, 277V), including U.S. commercial. True primary side sensing and regulation provides accurate LED current regulation, eliminating optocoupler, secondary error amplifier and associated passive components.

**PCIM Booth 11-225**

**www.ti.com**

# 30 and 60 W Dual Output Industrial Power Supplies

CUI Inc announced a new series of enclosed dual output internal switching power supplies. The VGD series is offered in two configurations, 30 and 60 W. It is ideal for a wide range of applications including industrial control, networking, automation, and test & measurement equipment.



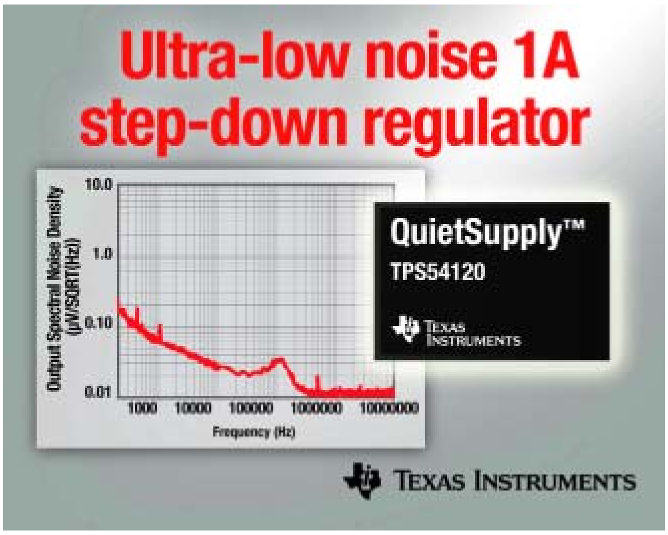
The VGD series offers a universal input (85-264 Vac) and dual output voltages of either 5V/12V or 5V/24Vdc. Protections include short circuit, overload, and over-voltage. All models are approved to UL, cUL, and Intertek 60950-1 safety standards and include a built-in EMI filter.

"The VGD series provides customers with the ability to generate two separate voltages in a singular package, minimizing the need for an external DC-DC converter," stated Kraig Kawada, CUI's VP of Product Management. The VGD series is available through Digi-Key with prices starting at $19.80 per unit for 100 pcs. Please contact CUI for OEM pricing.

**www.cui.com**

## Step-Down Supply Reduces Switching Noise by 99 Percent,

Texas Instruments Incorporated introduced a new class of voltage regulators designed to deliver the industry's lowest-noise 1-A switching power supply without sacrificing efficiency and power performance. The TPS54120, the first in TI's family of QuietSupply™ regulators, reduces switching noise by up to 99 percent, compared to other power conversion devices, and helps maximize the performance of precision data converters and amplifiers and sensitive clock distribution circuits used in applications, such as telecommunications, test equipment, and high-end audio and video equipment. Key features and benefits of TPS54120; 99-percent noise reduction: 9 μVRMS at 100 Hz to 100 kHz, and 17 μVRMS at 100 Hz to 1 MHz.




Performance: High power supply rejection ratio (PSRR) of 83 db at 10 kHz, 70 dB at 100 kHz

Design flexibility: Synchronizable to external clock from 200 kHz to 1.2 MHz

Wide input voltage range of 4.5 V to 17 V, adjustable output of 0.8 V to 6.0 V

The TPS54120 is available in volume now from TI and its authorized distributors in a thermally enhanced 4-mm x 4-mm, 20-pin QFN or TSSOP package, and has a suggested resale price of $1.95 each in 1,000-unit quantities.

**PCIM Booth 11-225**

**www.ti.com**

## Pico Zenigata LED Line Up with 15 – 72.5 lumens

With the Pico Zenigata LED series, Sharp completes its portfolio for high-performance LEDs. With just a single LED, the types of the GM2BBxxQK1C series achieve luminous flux levels of up to 24.5 lumens and an efficiency of up to 125 lm/watt. Luminous flux and efficiency of the other two series were improved accordingly: above all the GM2BBxxQKAC (2 LED dies) reaches up to 46.7 lumens with an effective power of up to 120 lm/W; the GM2BBxxQK0C (3 LED dies) radiate up to 72.5 lumens at an efficiency level of up to 120 lm/W. All three series are available with a typical CRI value of 83. The high colour rendering (HCR) LEDs achieve the high CRI level through a combination of blue LED dies with a special mixture of green and red phosphor. Even without secondary optics, the 'Pico Zenigata' LEDs from Sharp provide suitable light for energy-efficient lighting.

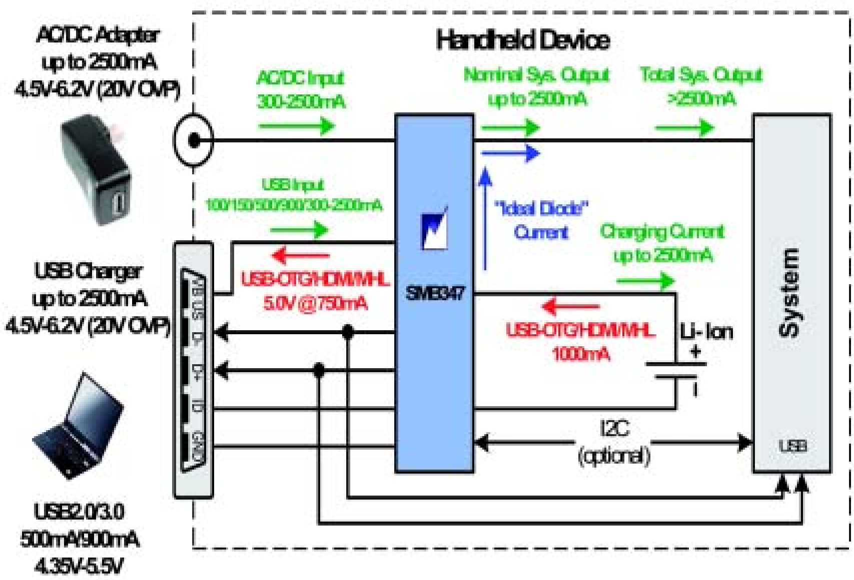
**www.sharpleds.eu**

### ADVERTISING INDEX

# Smart and Flexible 2.5A Li+ Charger, Tiny Solution for Big Batteries

***High-Efficiency, Programmable Flexibility, Universal USB/AC/DC Inputs & Robust Safety Features Deliver a Complete, Cost-Effective Solution***

### *Fastest, Safest and Most Flexible Charging Solution*




### *SMB347 Features*

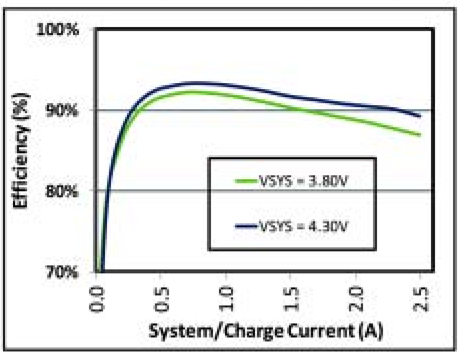
- Dual Inputs - AC/DC/USB2.0/3.0
- Dual Output CurrentPath™ for low/dead battery with 'ideal diode'
- +3.6V to +6.2V Input (+20V OVP)
- USB BC1.1/1.2 Source Detection
- Programmable Input Limit to 2.5A
- Automatic Input Limit Detection*
- Programmable Charge Current to 2.5A
- Integrated 5V USB-OTG Boost Output
- TurboCharge™* for 40% Faster Charging
- Robust Safety: JEITA/IEEE1725 Support
  - Over-Current/Over-Voltage
  - Thermal Monitor
  - Input Detection and Fault Status
- <10uA standby current
- I²C Programmable (Volatile and Non-Volatile)
- 2.5mm x 3.0mm CSP Packaging

* Patented

### *Programmable Switch-Mode Battery Charger Family*

| | SMB347/346 | SMB328A/B | SMB137B/136 | SMB329B | SMB338P |
|---|---|---|---|---|---|
| Input Voltage Range (OVP) | 4.0 to 6.2 (20) | 4.0 to 6.3 (20) | 4.0 to 6.0 (18) | 4.0 to 6.2 (20) | 4.0 to 6.2 (18) |
| # of Inputs/Outputs | 2/2 | 1/1 | 2/2, 1/2 | 1/1 | 1/1 |
| Maximum Charge Current (mA) | 2500/1250 | 1200 | 1500 | 1150 | 1250 |
| Battery Thermal Protection | HW JEITA | HW JEITA | SW JEITA | √ | |
| USB Charging Spec | rev 1.1/1.2 | | rev 1.0 | rev 1.0 | |
| Package (mm) | 3.0x2.5 CSP | 2.2x2.0 CSP | 3.0x2.5 CSP | 2.2x1.9 CSP<br>4x4 QFN | 2.2x1.9 CSP |

### *>90% System Efficiency*

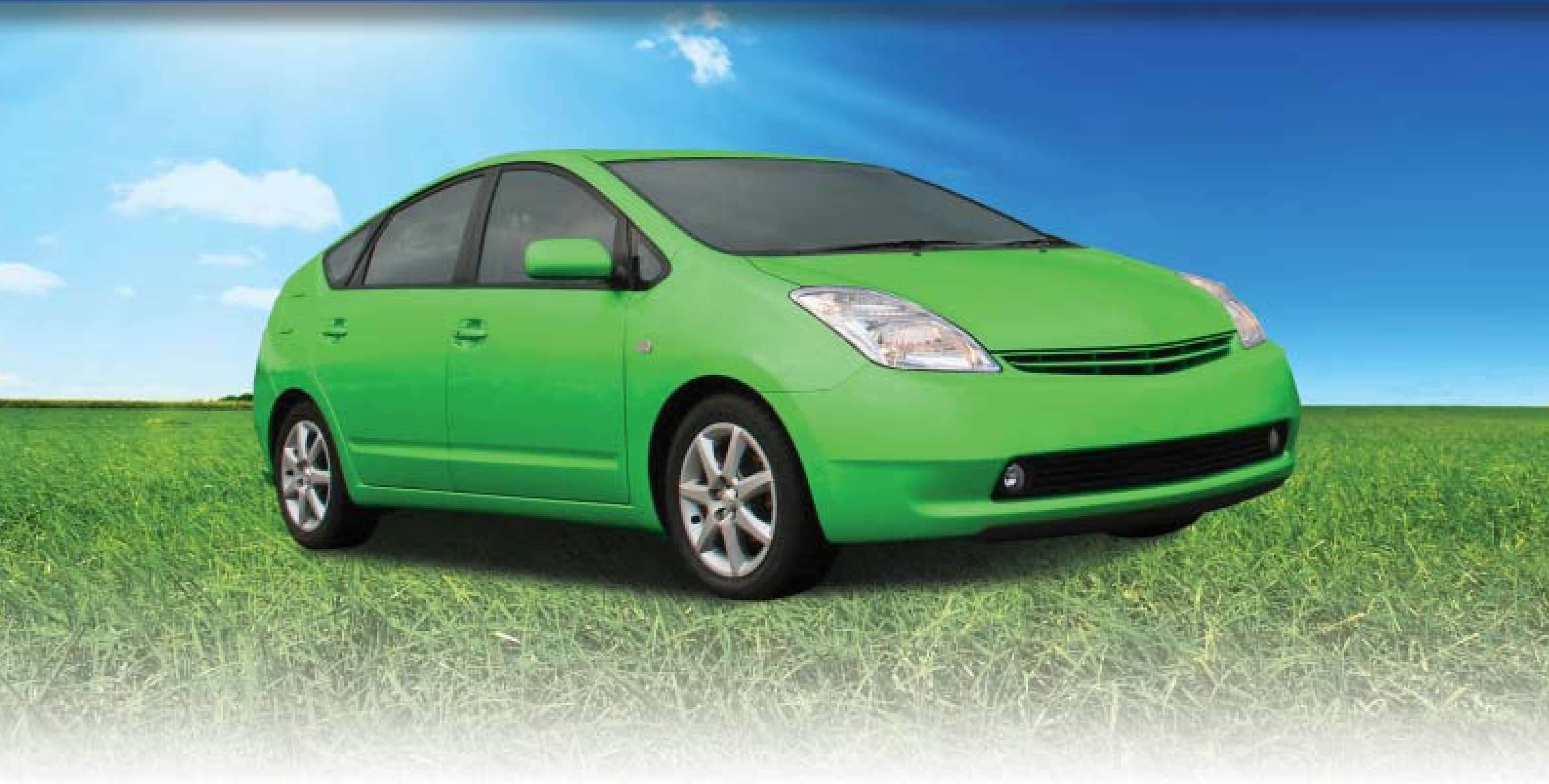



*For more information see:*
***www.summitmicro.com/SMB347***

**SUMMIT MICROELECTRONICS**

*Programmable Power for a Green Planet™*

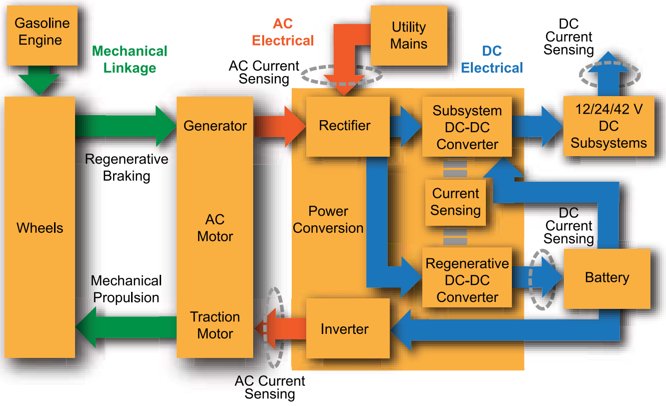
# Innovative Integrated Current Sensor IC Products



## Hybrid Vehicle Current Sensing

Consumers are embracing environmentally friendly "green cars" as a result of the rising cost of fossil fuels and a growing concern for the health of the environment. Hybrid electric vehicles (HEV), quickly becoming the most popular green car, employ complex power electronic circuitry to control the flow of electric energy through the vehicle. In a single electric motor HEV, the motor acts as a drive motor in parallel with the internal combustion engine in the drivetrain, or as a generator to charge the battery during regenerative braking.

A typical HEV also contains various sub-systems that require electrical current sensors for maximally efficient operation; including AC motor and DC–DC converter applications. Read the entire article explaining recent advances in Hall-effect current sensor technology and the use of unique, high bandwidth, enhanced resolution current sensors in HEV applications by visiting **www.allegromicro.com/promo1111**




### *Applications include*

- **Main Inverter**
- **Fuel Pump**
- **Power Steering**
- **Main Battery Charge Current**
- **Oil Pump**
- **DC-DC Converters**
- **Air Conditioner Compressor**
- **AC Line Charge Current**
- **Circulation Fan**
- **Electronic Hydraulic Braking**

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