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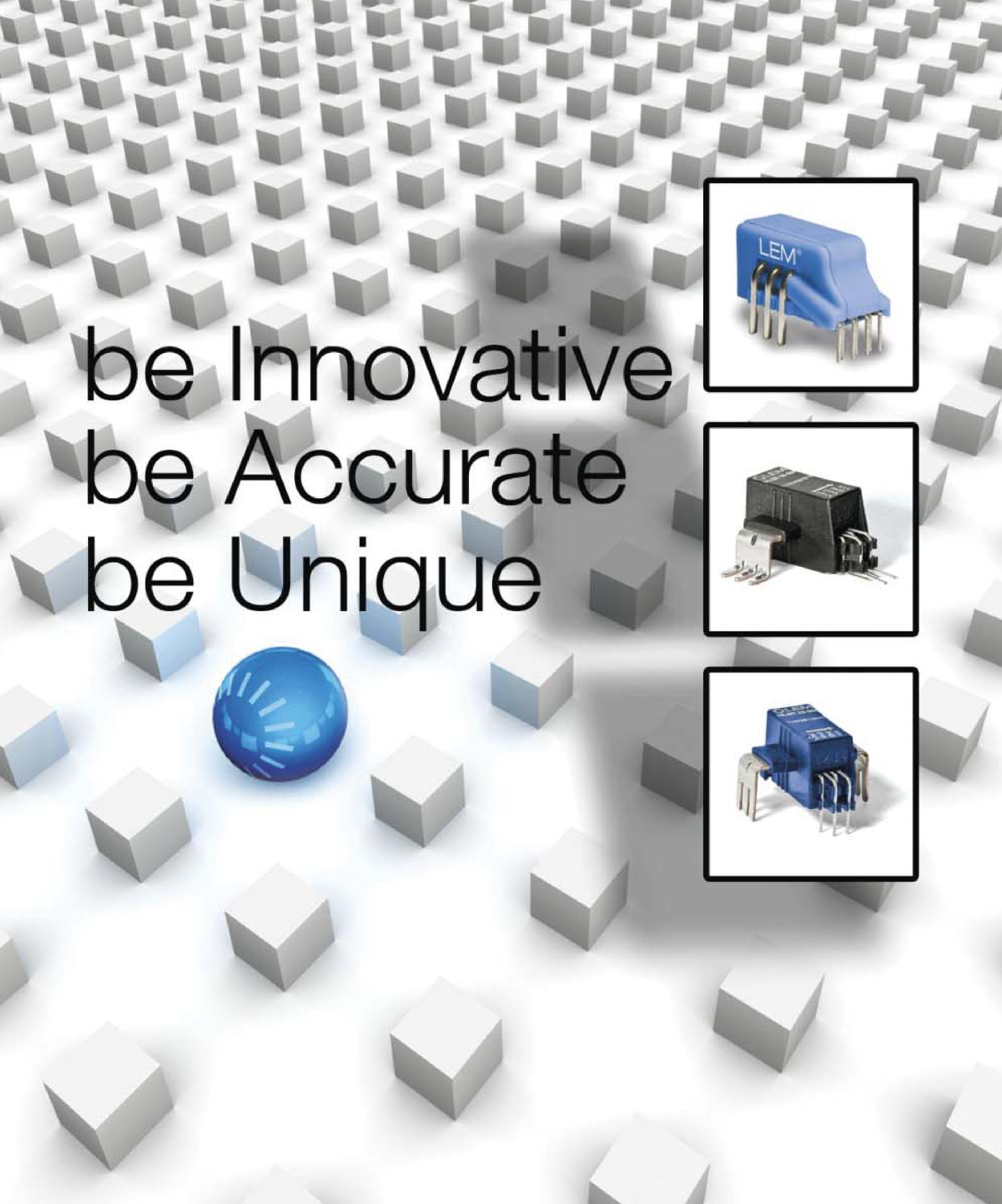
Bodo´s Power Systems®

Electronics in Motion and Conversion

November 2013

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Events

productronica 2013,
Munich, Germany, November 12th – 15th
http://productronica.com/de/home

sps ipc drives 2013,
Nuremberg, Germany, November 26th-28th
http://www.mesago.de/de/SPS/home.htm

Power Electronics,
Moscow Russia 2013, November 26th-28th
http://www.primexpo.ru

Cips 2014,
Nuremberg, Germany, February 25-27
http://www.cips-conference.de

Embedded World 2014,
Nuremberg, Germany, February 25-27
http://www.embedded-world.de

EMC 2014,
Duesseldorf, Germany, March 11-13
http://www.mesago.de/en/EMV/home.htm

Clean "Green" Energy

Wikipedia paints a confident picture of Germany and Europe developing renewable energy sources, with a good path for the future (see http://en.wikipedia.org/wiki/Renewable_energy_in_Germany). The German Government reports that in 2011 renewable energy (mainly wind turbines and biomass plants) generated more than 123 TWh (billion kilowatt-hours) of electricity, providing nearly 20% of the 603 TWh of electricity supplied. In 2012, this increased to 21.9% of overall demand, with wind turbines and photovoltaic providing half of that. Along with a vast majority of her compatriots, Chancellor Angela Merkel believes that, „As the first big industrialized nation, we can achieve such a transformation toward efficient and renewable energies, with all the opportunities it brings for exports, developing new technologies and jobs".

The installed capacity of wind power in Germany in 2011 was 29 gigawatts (GW), producing about 8 percent of total electrical power. According to the European Wind Energy Association (EWEA) in a normal wind year, installed wind capacity in Germany will now meet about 10.6% of electricity required. There are currently more than 23,000 wind turbines in Germany, with plans to build more. The installed capacity of PV was 32 GW in 2012, generating 28 GWh, over 5% of electrical usage. On a Saturday in May 2012, solar energy sourced a record 22 GW into the grid, or 50% of the country's midday electricity demand.

Since 2011 with a particular focus on offshore wind farms, Germany's federal government has been working on a new plan for increasing the commercialization of renewable energy. Developing network capacities capable of transmitting the power generated in the North Sea to large industrial consumers across the nation is one of the major challenges. Information on renewable energy is widely available and accessible, and helps us understand the developments taking place, and the demands on a smarter grid.

In view of the rising cost of energy, it is obvious that a reduction in consumption should be part of the plan for the future. The move to LED lighting will make a significant contribution, and buildings must become more efficient in thermal insulation.

Considering nuclear disasters that have happened in recent years, the last being Fukus-

hima, we realize that the cost of cleaning the site and returning to normalcy is unknown. Japan, after more than two years, has finally officially asked for help from international experts to get Fukushima under control. Cooling water for the damaged reactors becomes radioactive and must be stored in tanks. In over a 1,000 tanks such cooling water continues to be used and stored. Knowing the isotopes and their half-life, we can calculate the years required to cool the site. We can expect several hundreds of years of contaminated water which will need to be stored, and needing 1,000 tanks in two years' time gives us an indication of how many tanks will be needed in the future - about 500 tanks a year for a hundred years! Do we have any idea what the overall costs to Japan or the world will be to solve Fukushima? Nuclear accidents make for a very costly source of energy, possibly the highest of all, both in financial and social metrics.

Communication is the only way to progress. We delivered twelve issues last year and will continue this year, each month, on time, every time. With this November issue, we've now published 124 technical articles amongst 756 pages total. As a media partner, Bodo's Power Systems serves readers across the globe. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com.

My Green Power Tip for November:
Schleswig-Holstein, where I live, meets about half of its electric demand through wind energy, as do three other states in Germany. Get your government to move towards renewables. Over time our kids will benefit.

See you at the productronica or sps ipc drives conferences.
Best Regards

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EPE2014 Call for Papers

After the huge success of the 2013 edition, we invite and encourage you to submit a synopsis to EPE2014 ECCE Europe, that will take place in Lappeenranta from 26 to 28 August 2014.
Please note the following deadlines: Receipt of synopses 15 November 2013, Notification of provisional acceptance 1 March 2014 and Receipt of full typescript for final review 1 June 2014
Do not miss this 2014 opportunity to meet with colleagues from academics and industry. Do not miss this unique opportunity to visit Finland and meet with its innovative industry.
The Call for papers with all details is available on-line:

http://media.lut.fi/media/EPE2014-Call-for-papers/#/1

World's First 6-inch GaN-on-SiC Wafers for RF Power Transistors

RFMD, a global leader in the design and manufacture of high-performance radio frequency solutions, introduced the world's first 6-inch GaN-on-Silicon Carbide (SiC) wafers for manufacturing RF power transistors for both military and commercial use. The company is converting all GaN production and development to 6-inch diameter wafers using its existing high-volume, 6-inch GaAs foundry to reduce platform cost for the growing GaN device market.
GaN technology supports broad frequency bandwidths and high breakdown voltages in a small area. A 6-inch GaN wafer offers 2.5-times more useable area over competing 4-inch GaN wafer platforms currently available, resulting in 2.5 times more RF power devices per wafer. Larger area-per-wafer and subsequent lower cost per unit area (in dollars per square millimeter) is key to enabling affordable, high performance power monolithic microwave ICs (MMICs) for military and commercial applications. RFMD expects to complete qualification of its 6-inch GaN platforms in 2014.

www.rfmd.com

10th Anniversary of Innovative SACX® Alloy Launch

It was 10 years ago this fall when Alpha launched its innovative new lead-free, low-silver (Ag) solder alloy – ALPHA SACX®. This new alloy enabled the conversion from SnPb alloys to lead-free alloys in response to the RoHS regulations introduced in the European market. In addition to facilitating this transition, SACX® offered the soldering performance of SAC305 at 30% lower cost, thus helping to shield electronic assemblers from Ag cost volatility. In addition, it produced tougher solder interconnects versus alloys without Ag, and significantly improved resistance to drop shock compared to higher Ag alloys.

Leading global electronics manufacturers in many markets, including contract manufacturers, mobile devices, automotive, computer, telecom/telecom infrastructure, audio visual/gaming systems, white goods, equipment controllers, general lighting and LED lighting have relied on SACX® and SACX Plus® to assemble their electronic devices which touch the lives of millions upon millions of people around the world.
ALPHA SACX Plus® 0107, 0307 and 0807alloys are available worldwide as bar, solid wire, solder paste, cored wire, spheres and preforms, and are perfect together when used in combination. As with all Alpha wave solder alloys, our proprietary Vaculoy® manufacturing process is used to maximize alloy purity. For more information about ALPHA SACX Plus®, go to:

www.alpha.alent.com/Products/Soldering-Alloys

Coilware and LED Manufacturing – Focusing on Energy Efficiency

Light-emitting diodes, or LEDs, are an energy-efficient alternative that offers unlimited design possibilities. However, LED manufacturing is associated with several challenges. productronica 2013,
the International Trade Fair for Innovative Electronics Production that takes place in Munich from November 12 – 15, 2013, deals with both topics with a special show on coilware and a highlight forum on the third day of the fair.
Whether it comes to electric motors, transformers, generators or magnetic-field sensors, winding coils is an art. Coilware manufacturing is „magnetic field design" at the highest level: Depending on the application, low material consumption, limited waste, high fill factors and high energy efficiency can be
critical for success. Volume and weight reduction in the case of high-energy components increase the amount of heat to be dissipated without affecting performance – a challenge that can only be solved with perfectly coordinated material, design and processing technology.

www.messe-muenchen.de

www.productronica.com

Market for Power Semiconductors Plunges in 2012; Infineon Maintains Leadership

Global revenue in the power semiconductor business dropped by nearly 16 percent in 2012 as sluggish consumer demand, falling pricing and other factors conspired to undercut the market, according to a upcoming report from the Power Management and Analog IC Service at IHS Inc..

Following healthy growth during the previous year, market revenue in 2012 for power semiconductor discretes and modules fell to slightly less than $15 billion, down from nearly $18 billion in 2011.

The module segment of the market contracted by 27 percent, a much steeper decrease than for discrete power semiconductors, which declined by about 12 percent.

Infineon powers up. Despite the market slowdown in 2012, Infineon remained the leading supplier of power semiconductor discretes and modules. The company held an 11.8 percent share of global market revenue, almost unchanged from 12 percent in 2011. Infineon led No. 2 player Toshiba Corp. by 4.7 percentage points.

www.ihs.com

Awarded $2 M by US Department of Energy to Develop New Transportation Technologies

GaN Systems Inc has partnered with Arkansas Power Electronics International (APEI) in a successful bid for funding from the $45M US DoE programme aimed at developing new vehicle technologies to improve fuel efficiency and reduce transportation costs. The APEI-led team, also including Toyota Motor Engineering and Manufacturing North America Inc, the University of Arkansas National Center for Reliable Electric Power Transmission and the US National Renewable Energy Laboratory, has been awarded $2 Million as one of the 38 different projects the DoE is funding across the US.

The team will develop new electric motor traction drives for hybrid electric vehicles based on gallium nitride (GaN) and silicon carbide (SiC) power semiconductors. These new technologies will replace traditional silicon semiconductors in automotive power electronics to herald a new generation of highly efficient and lower cost systems.

Girvan Patterson, CEO of GaN Systems comments: "We're delighted to be part of the APEI team and to be collaborating on such an important programme. The DoE initiative is a very exciting opportunity for the industry. HEVs are full of power electronics for functions like battery management, auxiliary power, braking, instrument clusters and many more. Over the next few years we will see dramatic improvements in all these systems which will be designed into vehicles such as Toyota's next generation Prius. "

www.gansystems.com

Upcoming ECPE Events

ECPE is delighted to present the draft program of the next ECPE Workshop 'Power Electronics Packaging' on 12-13 November 2013 in Baden-Dättwil, Switzerland.

ECPE Workshop 'Power Electronics Packaging'
12 - 13 November 2013, Baden-Dättwil, Switzerland
Chairmen: Prof. M. Johnson (University of Nottingham), Jürgen Schuderer (ABB Switzerland Ltd.), Thomas Harder (ECPE e.V.)

Moreover we would like to draw your attention to the following ECPE Events:
ECPE Tutorial 'EMC in Power Electronics'
15 - 16 October 2013, Grenoble, France
Chairmen: Dr. E. Hoene (Fraunhofer IZM), Prof. J.-L. Schanen (G2ELAB)

CIPS 2014 - 8th International Conference on Integrated Power Electronics Systems
25 - 27 February 2014, Nuremberg, Germany
Conference Chairs: Prof. L. Lorenz (ECPE e.V.), Prof. E. Wolfgang (ECPE e.V.), Prof. D. Silber (University of Bremen)

The CIPS 2014 - 8th International Conference on Integrated Power Electronics Systems will be held in conjunction with the ECPE Annual Event 2014.

Furthermore we would like to point out the table top exhibition which will take place in the same area as the poster-session and the coffee and lunch breaks. Besides industrial companies demonstrating their products, the universities and research institutes are also welcome to present their latest results on Power Electronics Systems. For registration please visit the conference website at www.cips-conference.de

The up-to-date ECPE Calendar of Events 2013 with all ECPE Workshops and Tutorials is available on the ECPE website:

www.ecpe.org

Submit Poster Abstracts for IPC APEX EXPO 2014 in Las Vegas

IPC — Association Connecting Electronics Industries® invites researchers, technical experts and industry leaders to submit abstracts for poster presentations at IPC APEX EXPO®, the industry's premier conference and exhibition for printed board design and manufacturing, electronics assembly and test, March 25–27, 2014 at the Mandalay Bay Convention Center, Las Vegas, Nevada.

Technical poster presentations are being sought on all relevant electronics topics, including design, materials, assembly, processes and equipment. Recognized by the Trade Show News Network (TSNN) as one of the top 250 trade shows in the United States, IPC APEX EXPO provides presenters with profile-raising exposure to thousands of key engineers, managers and executives of the industry's leading companies. 3:30 pm–4:30 pm on Wednesday, March 26.

.An abstract of up to 300 words summarizing technical and previously unpublished work covering case histories, research and discoveries should be submitted by December 22, 2013, at:

www.IPCAPEXEXPO.org/CFPosters

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Joint Wind Expo Concept 23rd to 26th of September 2014

The first WindEnergy Hamburg, the leading international wind energy expo, will be held in one year's time in Germany's second largest city. The Hamburg Fair site will be the meeting point for experts from all parts of the world from 23 to 26 September 2014. Twelve months before the start, the trade fair companies of Hamburg and Husum have presented details on the profile of their joint event for the leading international market, and an outline of HUSUM Wind, which is likewise to be run jointly by the two companies – it will be held from 2015 onwards, reflecting the national wind market with its wide range of players and special requirements.

WindEnergy Hamburg – the leading international event for the industry
WindEnergy Hamburg as the leading international wind fair gives the global industry an ideal platform for dialogue and presentation – located in Germany, which is at the forefront of wind energy technology. Hamburg is the capital of the wind industry, and is the perfect international setting with cosmopolitan flair.

HUSUM Wind – the main industry fair for the German market
The leading international wind industry fair WindEnergy Hamburg will be followed on 15 to 18 September 2015 by HUSUM Wind, the main industry fair for the domestic market.

http://www.husumwind.com

TRANSFORM in Abu Dhabi – Pole Position for Transformers

From 26 to 28 November 2013, Transform will be taking place in Abu Dhabi. Ten European premium suppliers from the transformer industry invite you to attend a series of high-quality presentations and an exclusive exhibition. Visitors can expect a professional platform with well-known specialists sharing first-hand information on the latest industry developments and trends.

Transform is held every two years at a different location and has become the main trade conference for decision makers at international transformer manufacturers, utilities and industrial companies. In 2013, guests can look forward to a unique experience at the Formula 1 race track in Abu Dhabi and a great social program. Don't miss this chance to learn about the latest innovations and future technologies in power transformers and to discuss these in depth with leading specialists.

Maschinenfabrik Reinhausen (MR), Essex & LS Cable, GEA Renzmann & Grünewald, HSP & Trench Bushing Group, Krempel, Nynas AB, OMICRON electronics, PFISTERER Kontaktsysteme, Röchling Engineering Plastics and ThyssenKrupp Electrical Steel all look forward to seeing you in Abu Dhabi.

www.transform.net

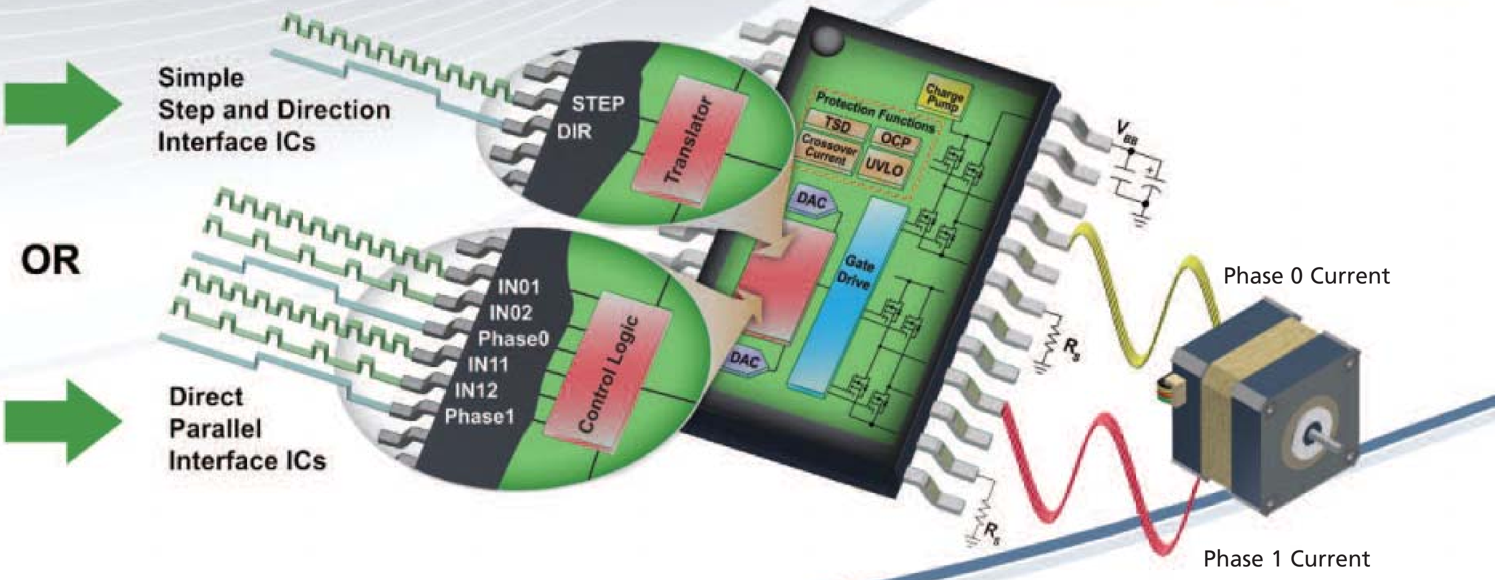
Strategic Investment from Avago Technologies

Amantys announced that Avago, a leading supplier of analogue interface components for communications, industrial, and consumer applications, has invested $5m in power electronics innovator Amantys as part of a strategic investment agreement between the two companies. Commenting on the investment, Amantys Chairman Pete Magowan said: „Attracting Avago as a strategic investor is a significant endorsement of the progress at Amantys and a great match for exploiting our vision for the future of the power electronics industry. "The company can now accelerate critical IGBT driver development programmes to enhance our roadmap of innovative, cost effective gate drive solutions."

As part of the investment, Martin Weigert, Avago's GM Industrial Fibre Products, will join the Amantys board as a non-executive director.

www.amantys.com

Allegro Stepper Motor Driver ICs



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	A4989	12 to 50	< 10	Step/Dir	2
Integrated Driver ICs	A3988	8 to 36	1.2	Phase I0/I1	4
	A4986	8 to 35	2	Phase I0/I1	2
	A4987	8 to 35	1	Phase I0/I1	2
	A3977	8 to 35	2.5	Step/Dir	2
	A3979	8 to 35	2.5	Step/Dir	2
	A4982	8 to 35	2	Step/Dir	2
	A4984	8 to 35	2	Step/Dir	2
	A4985	8 to 35	1	Step/Dir	2
	A4988	8 to 35	2	Step/Dir	2
	A4990*	7 to 50	1.4	IN_{1-4}/INH	2
	A4979	7 to 50	1.5	Step/Dir or Serial	2
	A3981*	7 to 50	1.4	Step/Dir or Serial	2
	A4992*	7 to 50	1	Step/Dir or Serial	2

* AEC Q100 qualified

Allegro MicroSystems offers a full line of stepper motor driver and pre-driver ICs. These devices feature easy to use two wire step and direction translator interfaces as well as industry standard parallel or serial control. Microstepping positioning is available with resolutions from full step to 16 microsteps per step. Safety features include thermal shutdown, undervoltage lockout and over current protection.

Two package options are available, a TSSOP (with leads), and a QFN (without leads) which has the smallest PCB footprint. Both packages have an exposed pad for enhanced thermal performance.

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Copiers	CNC milling machines	Headlamp leveling
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	Robotics	

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Win an MPLAB Starter Kit for Digital Power from Microchip

Bodo's Power is offering you the chance to win an MPLAB Starter Kit for Digital Power (#DM330017). This starter kit allows the user to easily explore the capabilities and features of the dsPIC33F GS Digital Power Conversion family. It is a digitally controlled power supply board that consists of one independent DC/DC synchronous Buck converter and one independent DC/DC Boost converter. Each power stage includes a MOSFET controlled 5W resistive load. The kit features an On-Board In-Circuit Debugger /Programmer via USB, LCD display for voltage, current, temperature and fault conditions and an on-board temperature sensor.

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The Digital Power Starter Kit provides closed-loop Proportional-Integral-Derivative (PID) control in the software to maintain the desired output voltage level. The dsPIC® DSC device provides the necessary memory and peripherals for A/D conversion, PWM generation, analog comparison and general purpose I/O, preventing the need to perform these functions in external circuitry.

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Package Considerations for High Frequency Power Conversion Devices

Power conversion at switching frequencies 10 MHz and above requires both high-speed transistors and high frequency capable packaging. eGaN® FETs, the first enhancement-mode gallium-nitride-on-silicon field effect transistors, have demonstrated their ability to improve high frequency power conversion compared with the aging power MOSFET by providing unmatched device performance as well as packaging [1].

By Alex Lidow, CEO and Co-founder, Efficient Power Conversion Corporation

This article will discuss the newest generation of eGaN FETs, the EPC 8000 series. This latest family of eGaN FETs further pushes the frequency capability of power conversion and targets higher frequency emerging applications such as envelope tracking.

Influence of Package on Performance

As power device technology evolves, improved device packaging must be also developed. To look at the impact of packaging on performance a 1 MHZ, 20 A, 12-1.2 V point of load (POL) converter with an EPC2015 eGaN FET is considered and shown in figure 1.

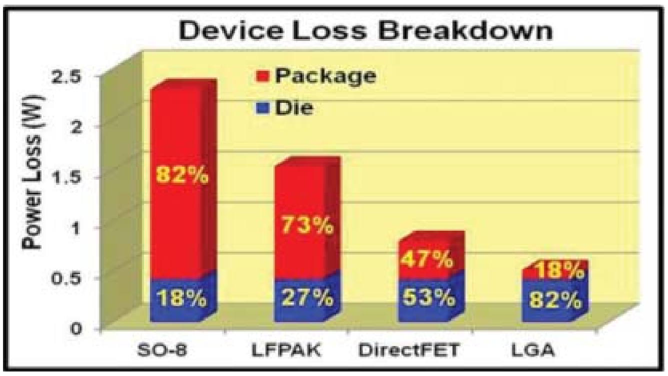

Figure 1: Device loss breakdown by package type

For an ultra-fast eGaN FET in a SO-8 package, only 18% of the switching losses are the result of the die, while 82% of the losses are introduced by the parasitics introduced by the package [2].

Evaluating an eGaN FET in a LFPAK package, an improvement to the SO-8 [3], 73% of the loss is still contributed by the package because the large common source inductance (CSI) limits the speed of the device [4].

The DirectFET [5], designed to minimize CSI, can improve performance over its predecessors and reduce the package related losses to 47% of the total loss. To fully utilize the improvements offered by gallium nitride a better package is required.

eGaN FET LGA Packaging

For the eGaN FET (Figure 2), a higher voltage lateral power device, all of the connections are contained on the same side of the die. This allows for the die to be mounted directly to the PCB, minimizing the total parasitics to the internal bussing and external solder bumps. To further decrease parasitics, the drain and source connections are arranged in an interleaved land grid array, providing multiple parallel connections to the PCB from the die.

The result of this improved packaging is a significant reduction in package related losses, with only 18% of these loss being contributed by the package and 82% from the die.

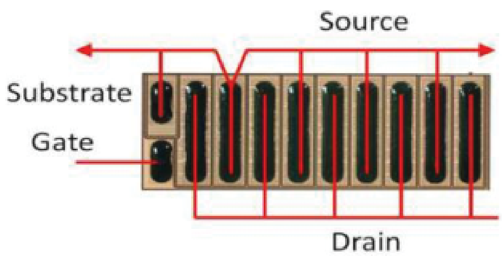

Figure 2: eGaN FET LGA connections layout

As transistor technology looks to move higher in switching frequency, the package becomes even more critical, positioning the eGaN FET to increase operating frequencies not possible with traditional MOSFETs. This is accomplished by providing improved device performance combined with an unmatched low parasitic package.
eGaN FETs for Higher Frequencies

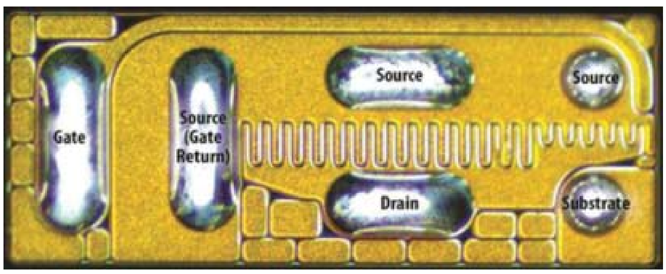

Figure 3: Gen 3 eGaN FET pin-out

The ultra-high speed switching capabilities of gallium nitride transistors have now been taken to the next level with the introduction of the third generation of eGaN FETs, the EPC8000 series [6]. In the EPC8000 family, the packaging is designed to extend the switching capability to beyond 10 MHz. Figure 3 shows the improved eGaN FET package. The key improvements made with this design are:

1. Separate gate return (source).
A separate gate return (This source terminal is dedicated to only the gate drive) for the gate circuit limits the common source inductance to inside the device itself. This reduction in common source inductance is critical to high frequency performance.

2. Low inductance gate.
The wider solder bar for the gate circuit significantly reduces the inductance of the gate circuit, thereby enhancing the speed of the connection to the gate driver.

3. Low internal parasitic Inductances.
The internal routing has been designed with high frequency applications in mind, and therefore internal parasitic inductances have been minimized for both the drain and gate circuits.

Design Example:
The EPC8000 family of devices targets compact, low power, high frequency applications. One example of this type of application is envelope tracking which requires a power supply to track the envelope of the signal transmitted to a radio frequency power amplifier (RFPA). Envelope tracking can significantly increase efficiency in the RFPA and, given the rapid expansion of wireless data transmission, This application will continue to grow.

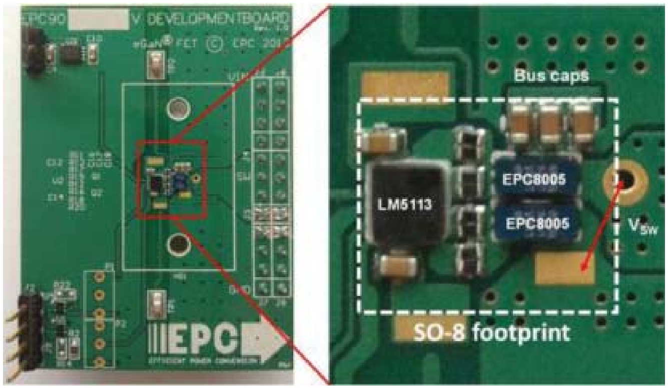

Figure 4: EPC9025 evaluation board with EPC8005 eGaN FETs and LM5113 gate driver

To demonstrate the EPC 8000 eGaN FET family in an envelope tracking application, a 42 V to 20 V, 40 W buck converter operating at 10 MHz with the 65 V, 275 mΩ EPC8005 is shown in figure 5. The board was designed using an optimal layout technique [7] to ensure the least amount of parasitic inductance and the highest efficiency. Figure 4 shows a photograph of the EPC9025 evaluation board fitted with EPC8005 devices and an LM5113 gate driver IC. It should be noted that the area occupied by the converter is smaller than the footprint of a SO-8 package.

The converter was tested at both 10 MHz and 5 MHz operations, and the efficiency is given in Figure 5. The plots show an 87% peak efficiency while operating at 10 MHz and 92% while operating at 5 MHz. The inductor used in the 5 MHz operation is the same as in the 10 MHz operation, and selecting a more optimal inductance could lead to even further improvement.

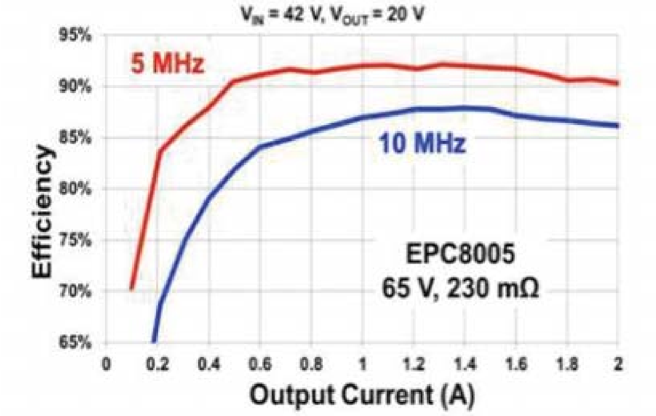

Figure 5: Efficiencies of EPC9025 operating at 5 and 10 MHz

Conclusion
Applications will continue to emerge requiring higher speed FETs, and the package becomes an essential component for achieving high performance at high frequencies. Therefore, as power transistors are designed with higher and higher switching speeds, particular attention must be paid to the package, the pin configuration and board layout. The innovative design of the eGaN FET packages allows designers to fully utilize GaN technology, offering unmatched high frequency performance.

Sources:

[1] Lidow, A., J. Strydom, M. de Rooij, Y. Ma, GaN Transistors for Efficient Power Conversion, 1st ed. El Segundo: Power Conversion Publicaitons, 2012.
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Electronics Industry Digest

By Aubrey Dunford, Europartners

SEMICONDUCTORS

Worldwide sales of semiconductors reached $ 25.53 billion in July 2013, the highest total of 2013 and an increase of 5.1 percent over July 2012, so the WSTS. Global sales in July were 2.6 percent higher than the previous month. Sales in the Americas increased 21.5 percent compared to July 2012, marking the region's largest year-over-year increase in more than two years. Regionally, July sales increased on a sequential monthly basis in Japan (7.9 percent), the Americas (5.4 percent), Asia Pacific (1.2 percent), and Europe (0.3 percent). Compared to the same month in 2012, sales in July increased sharply in the Americas (21.5 percent), solidly in Asia Pacific (7.2 percent), and modestly in Europe (1.1 percent), but fell steeply in Japan (-18.6 percent), largely because of the devaluation of the Japanese yen. Measured in Euros, European semiconductor sales were € 2.179 billion in July 2013, an increase of 0.2 percent versus the previous month and a decline of 3.0 percent versus the same month a year ago.

The worldwide semiconductor market is expected to grow 3 percent from 2012 to 2013, at $ 298 billion, so ABI Research. 2013 will see some growth as the wider economic environment improves but major market growth is not expected until later in 2014/early 2015.

Exar, a supplier of analog mixed-signal components and data management solutions, announced the appointment of Andreas Koller as VP of Sales for EMEA. Koller will be based near Munich, Germany and report to Steve Bakos, Senior VP of Sales and Marketing.

Worldwide semiconductor manufacturing equipment billings reached $ 7.55 billion in the second quarter of 2013, so SEMI. The billings figure is 3 percent higher than the first quarter of 2013 and 27 percent lower than the same quarter a year ago. Worldwide semiconductor equipment bookings were $ 9.17 billion. The figure is 5 percent lower than the same quarter a year ago and 18 percent higher than the bookings figure for the first quarter of 2013.

OPTOELECTRONICS

Plastic Logic, involved in flexible display technology, nnounced its participation in the new European-wide research project, Liquid Crystals for Robust Applications (LiCRA). The LiCRA project aims to build on European leadership in organic thin film transistor (OTFT) backplane and LCD technology, in order to create a scalable manufacturing process for a truly robust LCD. The project will focus on several key areas of innovation required to enable the manufacturing of LCDs on plastic film. Plastic Logic is collaborating on the LiCRA project with Merck KGaA, The University of Stuttgart's Institute for Large Area Microelectronics, Etkes and Sons, micro resist technology and LOFO High Tech Film. Plastic Logic will further develop its active matrix OTFT backplane technology, which has already been industrialised in its Dresden factory. The results of the project will be published in summer 2015.

PASSIVE COMPONENTS

Molex has entered into a definitive agreement to be acquired by Koch Industries, one of the world's largest private companies. Under the terms of the agreement, Koch Industries will acquire all of Molex's outstanding shares, for $ 38.50 per share in cash, for a total equity value of approximately $ 7.2 billion. At the close of the transaction, Molex will become a standalone subsidiary of Koch Industries and will continue to be operated by the company's current management team.

Würth Elektronik opens an electronic design & application center In Munich. The design center offers the engineers from various nations and specialist fields who work there space for ideas to develop new passive and active components. The focus areas are both wireless power transfer and energy harvesting applications as well as developing new power modules. In addition the first customer-specific passive components will be developed by Würth Electronics Midcom at the new location.

OTHER COMPONENTS

Aeroflex, a provider of microelectronic components, and test and measurement equipment, announced the sale of its Aeroflex Test Equipment Services ("ATES") business to Trescal for approximately $ 18.7 M. ATES provides calibration and repair services of non-Aeroflex test and measurement equipment in the United Kingdom. French group Trescal operates in 62 calibration laboratories and employs over 1,500 people across the world. Trescal services 25,000 customers in various sectors such as defense, aerospace, aeronautics, automotive, power generation & utilities, electronics manufacturing, communications and medical & chemistry. In 2012, Trescal pro forma sales reached € 157 M.

Measurement Specialties, a manufacturer of sensors and sensor-based systems, announced the acquisition of Sensotherm Temperatursensorik, a German supplier of platinum (Pt) thin film RTD temperature sensors for € 5.2 M. Measurement Specialties expects the transaction to contribute over $ 1.7 M in annual EBITDA and approximately $ 4.4 M in annual sales. Western Digital has entered into a definitive agreement to acquire Virident, a provider of server-side flash storage solutions. Virident will be acquired for approximately $ 685 M in cash. Virident solutions enable enterprises to tackle performance-intensive datacenter applications with PCIe-based enterprise flash storage solutions for virtualization, database, cloud computing, and webscale applications. The pending acquisition extends WD's presence in enterprise SSDs, which IDC predicts will grow from $ 2.5 billion in revenue in 2012 to $ 7 billion in revenue by 2017.

This is the comprehensive power related extract from the « Electronics Industry Digest », the successor of The Lennox Report. For a full subscription of the report contact:

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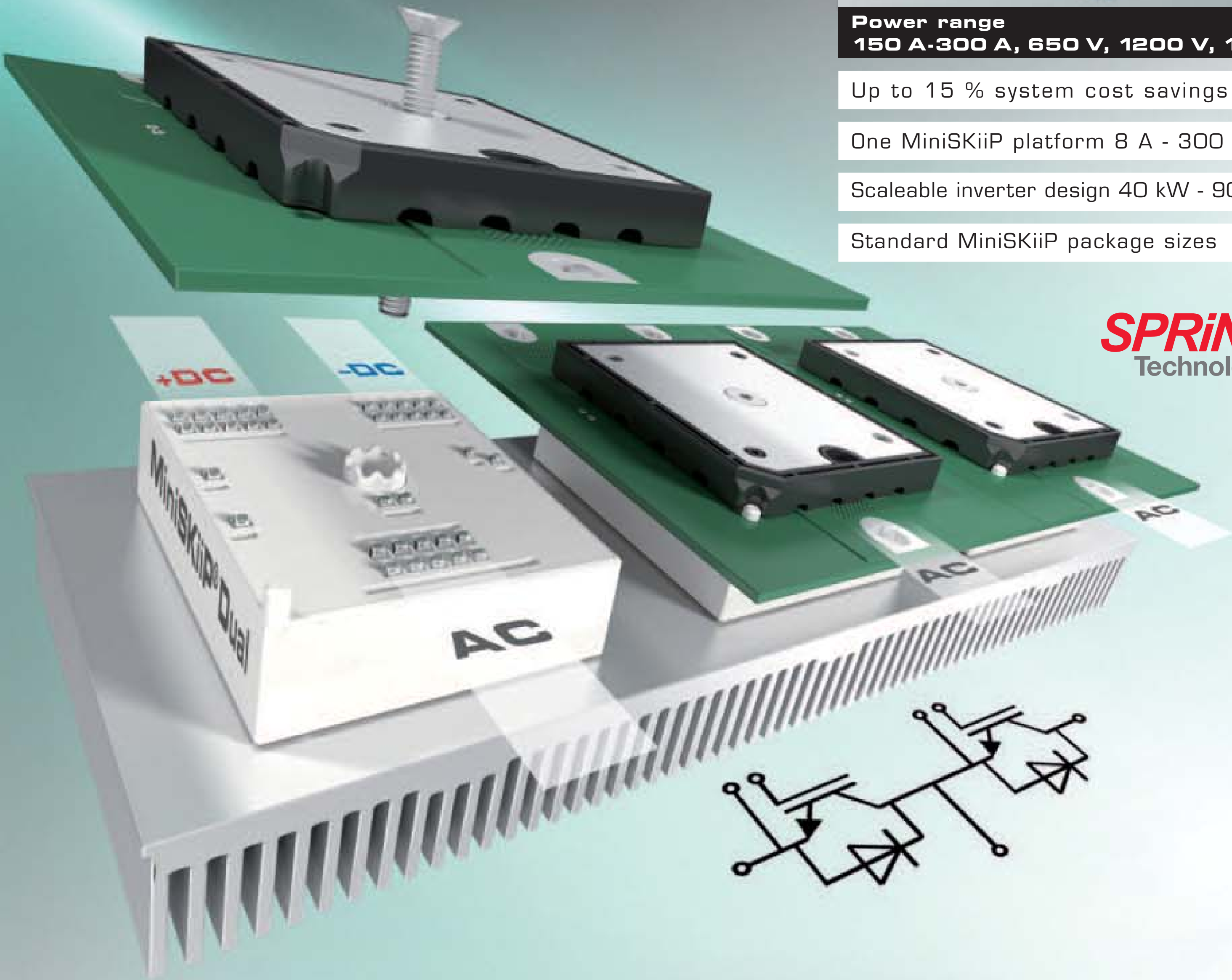

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More than Moore and Granular Powering

By Jeff Shepard, President, Darnell Group

Darnell Group has embarked on a groundbreaking analysis of the next frontier in power conversion, so-called "granular power." Granular power refers to deeply-embedded dc-dc converters that power individual microprocessor cores or similar partitions in large-scale integrated circuits such as SoCs, SiPs, FPGAs, and so on. Solving the complex technical challenges needed to implement granular power will not only provide efficient power for large-scale ICs, it will dramatically impact the power paradigm of a variety of portable devices including tablets and handsets which have dozens of power rails.

It is well-known that large digital ICs have hit a "power wall" The power wall problem is exacerbated with leakage power which increases with CMOS scaling. With modern CMOS processes, leakage is a significant part of total power (whereas dynamic power historically comprised the majority of total power). Leakage power is exponentially dependent on temperature, creating a thermal runaway problem: increased temperature increases leakage power, and increased total power (switching + leakage) increases temperature. Leakage power is exerting pressure to decrease junction temperature, exacerbating the power wall problem.

The effects of the power wall are already apparent in modern processors: Even though native transistor switching speeds have continued to double every two process generations, processor frequencies have not increased substantially over the last 8 years. The utilization wall is getting exponentially worse, roughly by a factor of two, with each process generation. The emergence of three-dimensional (3D) CMOS integration will further exacerbate this problem by substantially increasing device count without improving transistor energy efficiency.

Consequently, multiple innovations in power delivery and chip design are required to take full advantage of future improvements in IC technology. Near-term innovations (within the next few years) involve "More-than-Moore" (MtM) scaling. MtM scaling will attempt to extend the same design principles that have driven digital device scaling for decades over to analog/power, and to integrate those technologies on-die within a SoC/SiP. The ultimate goal of MtM power is to increase system-level power efficiency and capabilities through the integration of both digital and analog/power into compact systems.

As defined by Sarda Technologies, "Granular power delivery, consisting of fast power gating and fast dynamic voltage scaling of each load, can significantly improve energy efficiency. Granular power delivery uses a dedicated VR for each load – i.e., each component in a system or core (or clusters of cores) in a multi-core processor or system-on-chip (SoC). An analogy is to replace the garden hose with a drip sprinkler system. Each VR supplies only as much power as is needed by either power gating or dynamic voltage scaling. Systems use multiple components – processors, SoCs, FPGAs, memories, radios, etc. – and each component requires multiple voltage levels – for different cores, I/O, etc. Individually optimizing the power delivery to each of the 10-20 loads in a tablet or ultrabook or 50-100 loads in a server or router dramatically improves system energy efficiency and performance."

Next-generation VHF power switches, such as the GaAs devices under development at Sarda (as well as GaN devices under development elsewhere), are expected to be a key to implementing MtM power. In addition to the significant device design, fabrication and packaging difficulties; power gating and dynamic voltage and frequency scaling (DVFS) have been identified as key challenges to the development of commercially-successful MtM powering systems.

Power gating simply turns off the power to loads not actively being used at the moment. Processor cores, banks of memory, mass storage, I/O ports, etc. can all be selectively powered down. Although it is a common technique for power management, it suffers from some serious limitations. The performance degradation and power consumption costs become significant due to the time it takes to power back up the load. Multi-core SoCs use microarchitectural predictive control techniques to determine if a core is likely to be idle for a relatively long duration. The overhead due to wake-up latency and frequent mis-predictions can have a significant negative impact on power-performance.

Dynamic voltage and frequency scaling (DVFS) reduces the voltage of a circuit to its minimum energy point (MEP). DVFS alters the circuit's performance and power consumption on the fly by changing its supply voltage (V) and frequency (f) to provide a cubic reduction in dynamic power, which is proportional to C V2 f (where C is the effective load capacitance). By reducing the voltage by a small amount, dynamic power is reduced by the square of that factor. However, reducing the voltage means that transistors need more time to switch on and off, which forces a reduction in the operating frequency. For a given circuit, the MEP is not a fixed voltage.

It can vary widely depending on its workload and environmental conditions (e.g., temperature) due to opposing trends in the dynamic and leakage energy per clock cycle as the supply voltage scales down. Significant reductions in power consumption (up to 100x) are achieved by decreasing the supply voltage from ~1.1V at high load powers when performing active operation down to ~0.3V (close to the transistor's threshold voltage) when idling. DVFS seeks to reduce power consumption when cores are idle, boost single-threaded performance in the presence of large workloads, and remap voltage and frequency settings to improve performance and energy utilization.

The effectiveness of power gating and DVFS depend upon its granularity and transient response. Per-chip DVFS, where a single VR supplies all cores, is widely used today but constrains all the cores to scale their voltage / frequency uniformly and simultaneously. Per-core DVFS, which requires a dedicated VR for each core, provides the greatest flexibility in controlling power. Architectural simulations show 20-30% power savings with fast, per-core DVFS. Per-cluster DVFS, an intermediate point between the extremes of per-chip and per-core DVFS, clusters together several cores in a common voltage / frequency domain. All cores on a domain use a common voltage / frequency setting. This approach takes advantage of the natural granularity of the division into cores and shared cache.

Trends in current multi-core systems suggest the following: (1) Future high-throughput systems are likely to pack together a large number of simple cores hosting many more applications. (2) Even though per-core, independent voltage control is currently impractical, future systems with a multitude of cores can be expected to have a small number of independent voltage / frequency domains. As such, cores that differ in power-performance capabilities will exist. This clustered approach to DVFS domains is a way forward for multi-core ICs.

DVFS reduces voltage and frequency on the fly to reduce the total power during such periods. Reducing frequency can usually be done quickly, whereas for changing voltage the regulators have to settle their output voltage. Changes in voltage must, thus, be carefully scheduled in advance to align ramping up voltage with activity in the chip.

The semiconductor and electronics industries have hit the energy efficiency wall. The consequence is diminishing performance improvement with each new generation of products and commoditization (which is increasingly apparent in systems ranging from smart phones to servers). MtM, DVFS, power gating and a variety of other developments will be necessary to address this changing and challenging situation.

Moore's Law cycle of "scaling" reduces the transistor size, which lowers its operating voltage and, in turn, decreases power consumption per transistor. Consequently, each new generation of ICs has historically doubled transistor density and increased their operating speed within the same power budget.

The problem is that CMOS IC scaling is no longer providing the required energy efficiency improvement, because the decrease in the transistor's threshold voltage has stopped to keep leakage current under control. This, in turn, has prevented the supply voltage from scaling. Given the strong dependence of the dynamic energy on supply voltage, as more transistors are integrated on a fixed-sized chip with every generation the chip power increases rapidly.

Sarda is only one of several start-ups as well as established power management companies seeking solutions to MtM powering challenges. The first commercial products are already on the horizon from multiple vendors. Darnell's analysis will provide critical insights into emerging powering technologies, potential competitors, customer needs, pricing requirements and other factors that will drive this revolution in power conversion.

The report is scheduled for release in the first quarter of 2014. For additional information, or to become a sponsor, contact Jeff Shepard at Darnell Group, jshepard@darnell.com or +1-951-279-6684.

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Expanding the Dynamic Range of Current Measurement

ASIC-based current transducers can expand the dynamic range and increase the sensitivity and reliability of current measurement. In power electronics, the accuracy with which electrical current is measured is not solely based on the selection of a suitable transducer.

By Erik Lange, Marketing & Applications Engineer, LEM USA, Inc.

Level-shifting and intermediate scaling in the circuit between the microcontroller and the transducer can introduce offset and gain whilst, in closed-loop designs, the use of burden resistors can affect the accuracy of the current measurement. The conversion of analogue current measurement into a digitised format is another area in which accuracy can be compromised.

These factors often mean that the measuring device needs to operate over an expanded range. This range typically combines the normal operating range, of between 80% to 125% of the nominal current, and an additional 300% of the nominal current to provide protection against over-current events. The result of measuring this expanded range is that a limit is placed on the dynamic range which can be used for control.

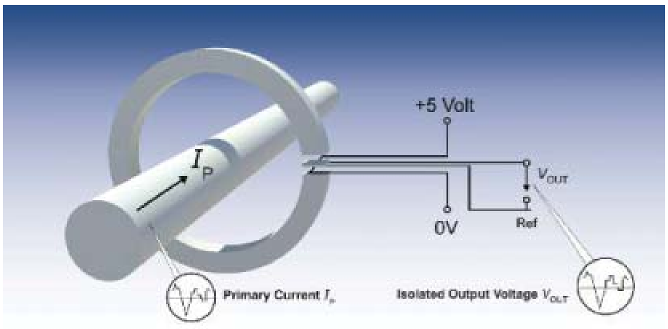

Figure 1: Open-loop, Hall-effect current transducers using an ASIC in the gap of the core

Externalising over-current detection

The challenge of expanding the dynamic range can be addressed by using open-loop Hall-effect current transducers which use an ASIC-based approach to current detection. Figure 1 shows the placement of the ASIC in the gap in the core of an open-loop Hall-effect current transducer.

This construction enables techniques such as Hall-cell spinning, as shown in Figure 2, which is used to reduce offset. In addition, it also provides programmable sensitivity and Over-current Detection (OCD) as a separate, programmable output. By externalising OCD, the transducer is freed from measuring the peaks which are required for protection and enables its full measuring range to be used to measure the application's dynamic operating range.

Typically, the OCD can be programmed to set trip thresholds of 250% or 300%, however the LEM HO series of open-loop Hall-effect current transducers allows a trip threshold of 570% of the nominal rating of the transducer. This means that the externalised OCD can detect currents which are higher than the transducer's rated measurement range, enabling a transducer rated at 8A to be programmed for an OCD threshold of 45.6A.

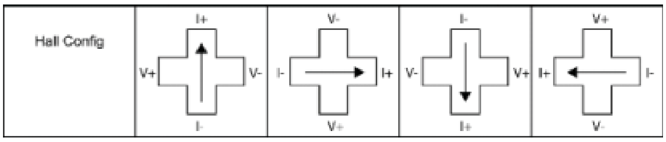

Figure 2: Hall-cell spinning reduces offset

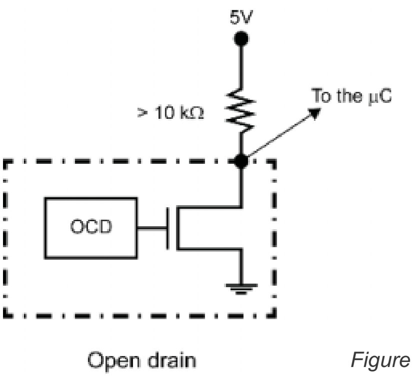

Figure 3: Over-current detection

A further benefit of the OCD pin is that it can be used to replace a dedicated over-current detection crowbar circuit which usually consists of a comparator and a number of resistors. By eliminating these discrete components, the OCD pin offers the additional benefit of reducing component count and board space.

Expanding dynamic range measurement

ASIC-based current transducers are available in 5V or 3.3V versions. For 5V transducers, the dynamic range is typically 0.625V/nominal current. This allows for a bidirectional transducer, measuring AC, to have a zero current point of 2.5V out. Current in either direction of flow increases or decreases the output voltage of the transducer from the 2.5V start point, or zero primary current. This means that for a 10A application, where 10A is equal to a 100% load, the transducer would have a nominal rating of 10A and provide protection with a peak rating of 30A. However, with a rating of 0.625V/10A the sensitivity of a transducer such as the LEM HXS 10-NP/SP4 provides a 300% reading of 30A which equates to a 4.375V output.

The availability of 5V or 3.3V current transducers also minimises the need for level-shifters or scaling between the transducer and the analogue-to-digital converters which typically operate on a 5V or 3.3V supply.

Magnetic Multiplication

A technique called 'magnetic multiplication' is used in transducer construction so that multiple wraps of conductor material are applied, in series, around bus bars inside the transducer. The conductor's magnetic fields are therefore defined by the number of wraps. This is useful when the rating of the current transducer is higher than that of the application's primary current, because using more of the transducer's dynamic range helps to minimise offset and linearity errors. The following examples show how this works in an AC and a DC application.

Figure 4: Transducers incorporating multiple bus bars and an OCD pin

Bidirectional AC measurement

With the OCD pin externalising the task of over-current detection, the transducer's entire dynamic range can be used for control. The example used in the previous 10A application can also be applied to a 15A transducer such as the LEM HO 15-NP.

The current is wrapped, in series, around three separate bus bars. With a rating of 125% at the upper end of the nominal range, a maximum current of 37.5A.t would be achieved. At 100%, or 10A duty, the transducer detects 30A.t.

The original sensitivity of 53.33 mV/A for the LEM HO 15-NP will result in a sensitivity of 160mV/A. This provides a sensitivity which is greater, by a factor of 2.56, compared to the 62.5mV/A sensitivity of a standard transducer with a nominal 10A rating. The lower currents are lifted out of the noise floor allowing more of the available dynamic range to be used. In this example of AC measurement, both sides of the 2.5V zero current point are used by the application.

Unidirectional DC measurement

In a unidirectional DC application, the dynamic measuring range can be expanded significantly by using the reference voltage, Vref. Starting with a LEM HO 8-NP ASIC-based transducer, the primary current is wrapped three times, in series, to provide a maximum of 37.5A.t, or 125% of the current's application. When the Vref is pulled or programmed to 0.5V, or 0A, the application can use the transducer's full sensitivity of 100mV/A. At 37.5A.t, the peak voltage output is 4.250V, giving a range of 3.75V for an adjustment of 12.5A or 300mV/A. This means that a DC application which would typically have operated at 62.5mV/A can now operate at 300mV/A.

The combination of Vref shifting and the externalised OCD enables significantly finer current control. Take the example of a 5V application operating with 12-bit resolution, in which a bit represents 1.22mV. The output voltage range would be between 0.50V and 4.250V, with a current of 0A to 12.5A and a range of 3072 bits. In a 10A application, without Vref and OCD, the 0 to 12.5A operating range would be represented by a voltage of 2.5V to 3.28V, with a range of 0.781V which represents 640 bits. The Vref shifted/OCD method provides bit resolution of 4.1mA or 19.5mA without the ASIC-based features.

Typically, ASIC-based transducers at the lower-current end of the series, such as the LEM HO 8-NP, have a broader range available than higher-current versions. In contrast, the higher-current LEM HO 25-NP does not support such a broad range of measurement when the Vref is pulled to 0.50V.

Thermal management

As an ambient temperature of 85°C could possibly result in de-soldering of a transducer, the final design should be thoroughly checked for the operating temperature at the core, solder joint and bus bars.

When a smaller transducer is operating over the full dynamic range, the conductors will generate heat in the single-digit Watt range and the bus bars will have sub milli-Ohm resistance. However, when currents approach 150A, even the 200µOhms of the LEM HLSR 50-P will begin to generate 4.5 Watts.

The operating temperature range of ASIC-based transducers is typically rated at 105°C to 125°C. In ASIC-based transducers with integral bus bars, the maximum temperature of the bus bars may be slightly lower, at 120°C. Taking heat dissipation into account when designing the board layout enables the heat generated by the transducers to be managed. To assist in heat dissipation, the PCB traces and copper surrounding the transducer pins should be maximised, rather than minimised to allow sufficient heat to be dissipated and air movement can also be considered as part of the thermal management of the design.

Conclusion

The benefits offered by ASIC-based transducers with OCD are not limited to enabling an expanded dynamic range. Transducers such as the LEM HO series can also help to reduce component count and, as a result, deliver higher reliability. They can also enable higher resolution from the analogue-to-digital converter and improve the signal-to-noise ratio as well as providing higher sensitivity which increases the gain as the volts-per-amp increase.

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Highly Efficient UPS Topologies with Regenerated Switching Losses

High efficiency is a must for solar applications. Now other applications are emerging with equally challenging demands for efficiency. With the experience gained in high-efficiency solar applications, it is possible to exploit synergetic effects for next-generation UPS topologies. And in contrast to the solar market, system costs have been a focus topic from day one in this sector.

By Michael Frisch, Vincotech GmbH, Biberger Str. 93, 82008 Unterhaching (Germany) and Temesi Ernö, Vincotech Kft., Kossuth Lajos u. 59, H-2060 Bicske (Hungary)

Switching losses have to be reduced to achieve higher switching frequencies and enjoy the size and weight benefits that passive components do not offer. Enhanced efficiency reduces the required battery capacity and cooling effort. Highly efficient circuits are clearly the smartest way to go for compact designs and highest power density. And the best news is that highest efficiency can be achieved at no extra cost – by means of parasitic inductance and intelligent integration into the UPS environment.

Regenerating switching losses

Low inductance allows engineers to use fast switches, but ultra fast freewheeling diodes are necessary to maintain low turn-on losses.

The objectives here are to:

- Increase inductance at turn-on.
- Achieve ultra low inductance at turn-off.
- Regenerate the energy stored in the parasitic inductance: EL = ½*L * I2.

The way to achieve this new switching behavior is to use the parasitic inductance $L_{parasitic}$ at turn-on and bypass it during turn-off. To this end, the snubber diode Dtran (see Figure 1) consigns the parasitic inductance's stored energy to the integrated capacitor Ctran during turn-off.

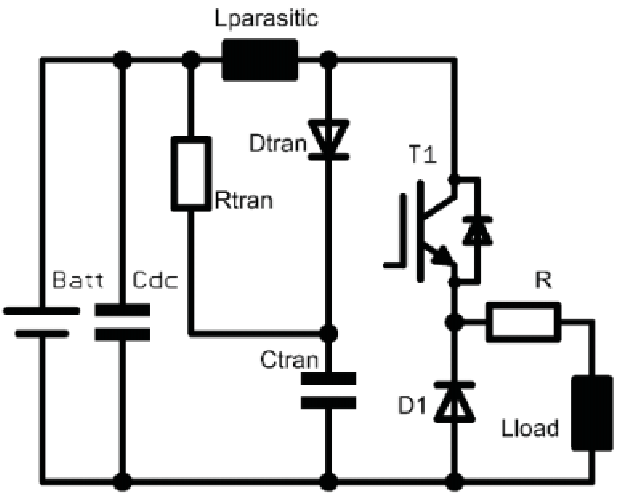


Figure 1: Asymmetrical inductance with feedback to the main DC link

The stored energy circulates in $L_{parasitic}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. With this circuit, we are able to spare the semiconductor switching losses. However, some energy has to be dissipated in passive components. One way to increase efficiency is to regenerate the stored energy using a DC-DC circuit (see Figure 2).

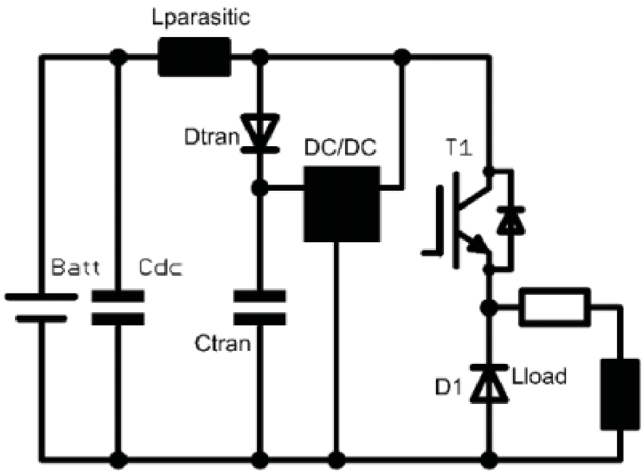


Figure 2: Asymmetrical inductance with regenerated stored energy

This proposal has been verified by comparing different parasitic inductances in a conventional power module setup and in an asymmetrical setup with integrated snubber capacitors.

Test conditions:
R_G = 2Ω (+/- 15 V), V_{DC} = 600 V, I_{OUT} = 400 A
Component: Infineon HS3 / 1200 V / 400 A

Turn-off

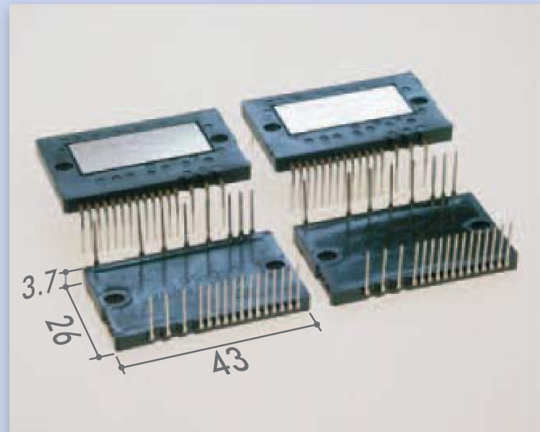
It is expected that the reduced inductance with integrated capacitors will decrease voltage overshooting at turn-off. The turn-off characteristic at a symmetrical inductance of 50 nH (see Figure 3) indicates voltage overshoots >1000 V and ringing with the DC capacitor.

Turn-off at low temperatures is the most critical case. An overvoltage >180% was measured at 25°C, which limits usage to 650 V. Safe turn-off is no longer possible given overcurrent conditions. In our test, the module failed at 720 A / 600 V / TJ=25°C.

• Trench-FS IGBT • High thermal cycling capability • Low spike voltage & oscillation free • Excellent turn-on dI_C/dt control by R_G

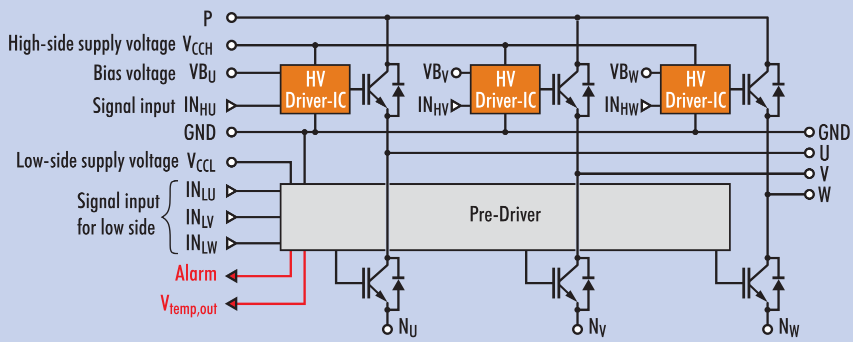
Low Power IPM

- ▸ For 600V/15A , 20A , 30A
- ▸ Built-in High Voltage Driver-IC



▸ Built-in protection functions

- + Under voltage protection (→ self shutdown & Alarm)
- + Short circuit protection (→ self shutdown & Alarm)
- + Type A: Temperature monitoring (→ $V_{temp,out}$)
- + Type C: Temperature monitoring (→ $V_{temp,out}$) and Overheating protection (→ self shutdown & Alarm)



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The same test with asymmetrical inductance (see Figure 4) confirms this expectation. The peak voltage is just 720 V, and the snubber diodes suppress any ringing

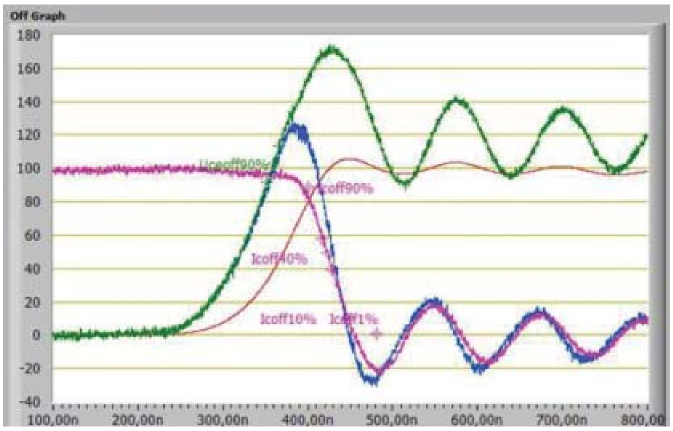

Figure 3: IGBT turn-off characteristics with symmetrical inductance; L[ON] = L[OFF] = 50nH

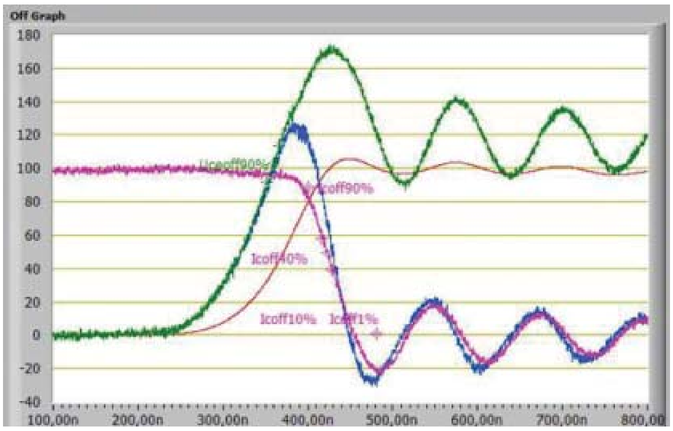

Figure 4: IGBT turn-off characteristics with asymmetrical inductance; L[ON] = 50 nH, L[OFF] = 5 nH

Turn-on

The freewheeling diode conducts when the IGBT is turned on with an inductive load. The reverse current is added to the output current in the IGBT during the diode's reverse recovery (see Figure 5).

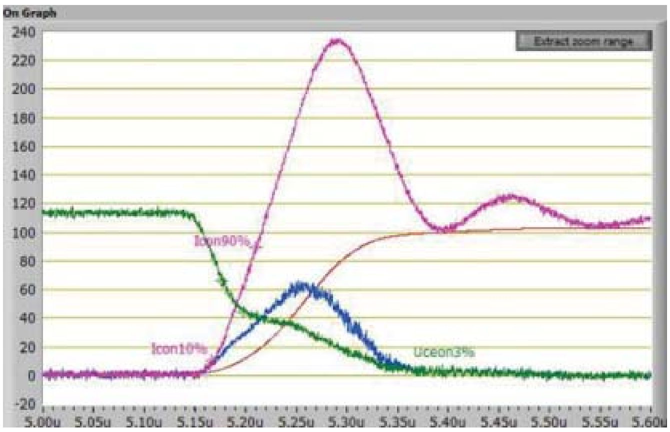

Figure 5: IGBT turn-on characteristics with symmetrical inductance; L[ON] = L[OFF] = 50 nH

Asymmetrical inductance is similar, but the integrated capacitors do have some influence on the freewheeling diode's reverse recovery (see Figure 6). At turn-on, the current of the transistor T1 is increased by the reverse recovery current through the diode D1. The current is reduced at the end of the recovery phase, but additional energy is stored in the parasitic inductance Lparasitic. This causes an overvoltage at the transistor's collector. Some of the stored energy will flow into the capacitor, which reduces the reverse current in the diode and the forward current in the transistor. This significantly diminishes switching losses.

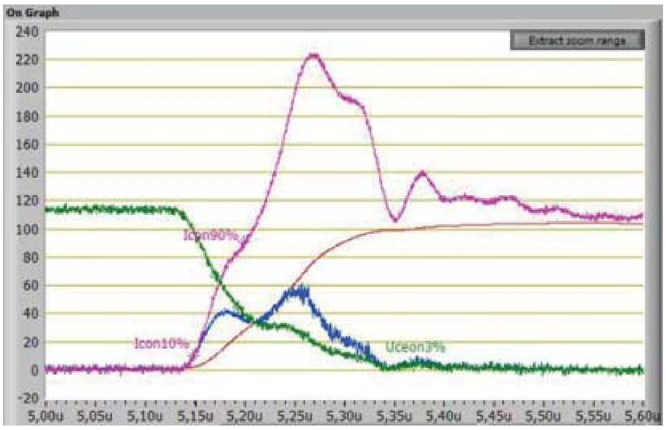

Figure 6: IGBT turn-on characteristics with asymmetrical inductance; L[ON] = 50 nH, L[OFF] = 5 nH

Inductance may be further increased with the asymmetrical inductance circuit, and thereby take advantage of the reduced turn-on loss. The table 1 compares a circuit with a symmetrical inductance of 50 nH and two asymmetrical configurations with 50 nH (on) / 5 nH (off) and 90 nH (on) / 5 nH (off):

	Classic Lon/Loff = 50nH	Asymmetrical I Lon/Loff = 50nH/5nH	Asymmetrical II Lon/Loff = 90nH/5nH
E_{OFF}	27.78 mJ	25.66 mJ	25.77 mJ
E_{ON}	16.92 mJ	15.487 mJ	12.44 mJ
E_{REC}	31.78 mJ	28.27 mJ	26.70 mJ
total	76.48 mJ	69.42 mJ (-10%)	64.91 mJ (-15%)

Table1: Symmetrical inductance of 50 nH and two asymmetrical configurations with 50 nH

The new asymmetrical setup's switching losses are lower. It is not just the turn-off losses that are reduced; all switching losses decrease.

This achieves several benefits:

- Superior switching performance with standard components:
  Reducing switching losses with standard components is entirely possible, so the new circuit improves efficiency without requiring investments in special components.
- Reduced EMI:
  The increased turn-on inductance reduces the peak current in the transistor, a major source of EMI.
- No bus bars required:
  Inductance in the DC input is now welcome and will further reduce losses at turn-on. Expensive laminated bus bars for a low inductive connection with the DC capacitor bank are no longer required. And that could well be this new design's greatest benefit.
- Reduced voltage swing of the onboard capacitors.
  The onboard capacitors are not discharged during turn-on, so voltage swing and dissipation in the capacitors are reduced.

Three-level UPS concept with regeneration

There is one problem left to solve before all these benefits can be enjoyed. The energy stored in the onboard capacitors has to be regenerated to maximize efficiency. This requires a symmetrical BUCK circuit. The same circuit is used in UPS systems to charge the battery. The idea here is to also use the battery charger to regenerate switching losses without extra effort and cost (see Figure 7).

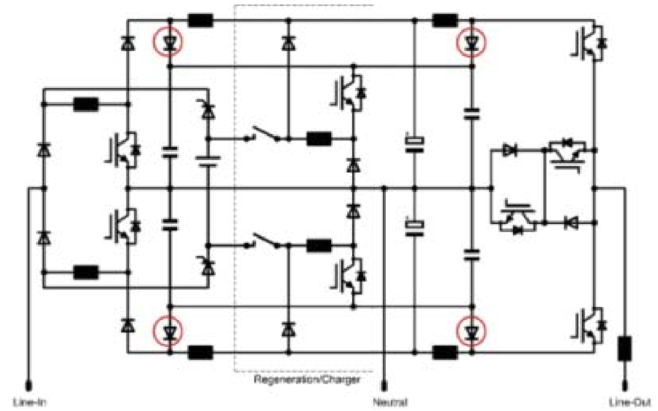

Figure 7: UPS configuration (only 1 phase shown) with battery charger used for switching loss regeneration

How this works:

- The energy stored in the parasitic inductance (PFC-DC and inverter-DC inductance) is transferred to the onboard snubber capacitors.
- The snubber capacitors of the input PFC and output inverter are connected.
- A diode prevents the capacitors from discharging reverse recovery current at turn-on.
- The snubber's stored energy is regenerated to the main DC voltage or used to charge battery.

All onboard capacitors are connected in the full-fledged three-phase UPS system (see Figure 8). A single central BUCK circuit charges the battery or regenerates the energy stored in the onboard capacitors back to the external DC link capacitor bank.

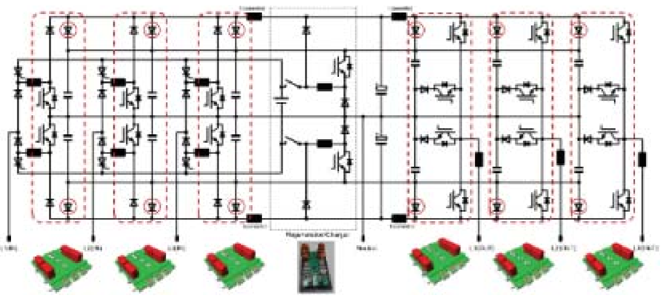

Figure 8: Three-phase UPS configuration with a shared battery charger / switching loss regenerator

This achieves several benefits:

- The parasitic inductance reduces the switch's turn-on losses without requiring an external low inductive DC connection.
- Reduced turn-off and turn-on losses:
  The onboard capacitor takes the parasitic inductance's stored energy at turn-off and after the BUCK diode's reverse recovery during turn-on.
- No extra effort:
  The snubber capacitor's stored energy is regenerated to the main DC voltage or charges the battery.

Power module definition

The combination of all these ideas has culminated in the following power module specifications.

- 200 kVA output power at 20 kHz
- Asymmetrical parasitic inductance with energy regeneration.
- Three-level topology

Power module concept

The UPS concept is supported by dedicated power modules for input power factor correction (PFC) and the output inverter.

Input PFC module (see Figure 9)

- 2x 650 V / 600 A power rating
- Asymmetrical parasitic inductance with onboard snubber capacitors (5nH turn-off inductance) and DC-DC regeneration circuit
- Symmetrical boost topology.

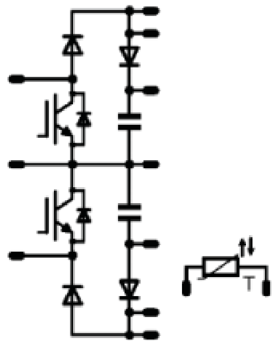

Figure 9: Symmetrical boost circuit with onboard capacitors and interface for the regeneration of switching losses

Output inverter module

- 1200 V / 600 A power rating
- Asymmetrical parasitic inductance with onboard snubber capacitors (5 nH turn-off inductance) and DC-DC regeneration circuit
- Split outputs in the high- and low-side circuit to decouple the corresponding switches
- Mixed voltage NPC (MNPC) topology

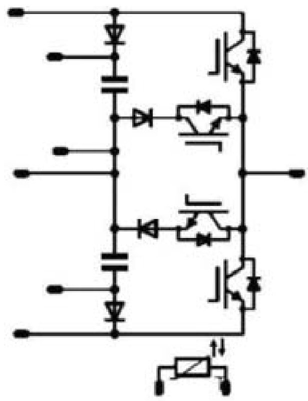

Figure 10: Output three-level inverter module with onboard capacitors and interface for switching loss regeneration

Power module

The power module is equipped with DC snubber diodes and capacitors. Power feeds are connected via the screw terminals beside the capacitors. The contact holes alongside the module provide a low inductive interface for all DC voltages and connections for all switches.

The following configurations are possible with this low inductive access to all IGBTs are:

- The three modules' transient DC path may be connected to access full capacity for all switches.
- Paralleled modules:
  The transient interface supports each switch's low inductive paralleling.
- Extended capacitance:
  The ultra low inductive capacitance can be increased with additional capacitors connected at the low inductive interface. Each conversion stage gets full access to the entire onboard capacitance with the low inductive connection of the DC voltage between all modules (all three phases, input and output).
- Connected switching loss regeneration:
  Resistors or a symmetrical BUCK circuit may be connected to the transient interface to regenerate the energy stored in onboard capacitors.

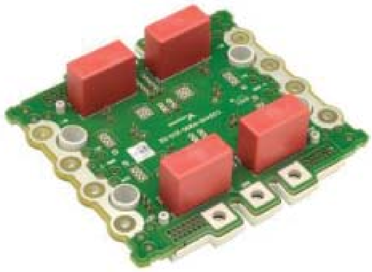

Figure 11: Power module mechanics with power connection and low inductive interface

Conclusion

Switching loss regeneration with asymmetrical inductance achieves great benefits without extra effort and cost. It can even serve charge batteries in UPS systems.

- No laminated bus bars are required for external interconnection. The parasitic inductance is used to reduce turn-on loss, while circumventing the voltage overshoot problem at turn-off.
- The snubber diode reduces voltage swing and losses in the onboard capacitors
- Reduced EMI and reduced pulse load for the external DC link capacitors:
  The snubber diodes suppress any ringing, and the increased turn-on inductance decreases the pulse current in the DC link.
- Increased efficiency and superior switching performance with standard components
- No extra effort for the regeneration circuit as it is also used for battery charging

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Short-Circuit Detection is Possible for Power Drive Systems with Long Motor Cables

Long motor cables add high parasitic inductive and capacitive loads to the system. These parasitics lead to reflections on the collector-emitter voltage and the collector current, which have a considerable duration due to the length of the cable.

By Marc Buschkühle and Christian R. Müller, Infineon Technologies AG and Benno Weis, Siemens AG

In this article, the influence of a long cable on the switching characteristics is investigated experimentally and it is shown that short circuits can still be detected in spite of these significant parasitic effects.

High inductive and capacitive loads in power drive systems

In power drive systems, a common way to reduce the emission of electromagnetic interference (EMI) is to use shielded motor cables. Due to its shielding, the motor cable reduces the radiated EMI but, on the other hand, adds parasitics. As a consequence, a significant additional charging current flows from the inverter into the cable during switching operations. Two major challenges are encountered, as the charging current is superimposed on the load current:

1) Thermal management of the power semiconductors
2) Protection circuit of the system

The article focuses on the influence of the charging current on the short-circuit detection using a 200 m long shielded cable. The target is to switch off the short circuit within 5 µs. Compared to the standard turn-off time frame of 10 µs, the system reaction must be twice as fast.

The device under test (DUT) was an 25A EasyPIM™ 2B power module. A nominal DC link voltage of V_{CC} of 600 and an increased voltage of 850 V were selected as operating conditions. The collector current I_C was adjusted in steps from low current ratings up to 100 A, which is 400% of the rated chip current.

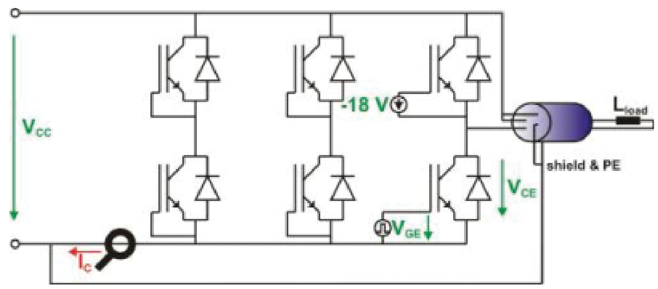

Figure 1: Schematic view of the experimental setup together with the applied and determined voltages

A 4-wire cable was used to connect an inductive load between the positive DC link voltage and the power terminal of one AC output. Fig. 1 shows the schematic of the electrical setup with the relevant sixpack topology of the power module. The collector emitter voltage (V_{CE}) and the gate voltage (V_{GE}) of one lower system were measured directly, and the collector current (I_C) was measured by a current probe integrated in the measurement setup.

Experimental results and interpretation

The measurement focused on investigating the charging current (I_{Osc}) as a result of the cable parasitics. Due to the position of the current probe and the load inductance in the measurement setup, the charging current can only be clearly measured when the device is turned-on. Thus, the device was operated in the double-pulse mode and the charging current I_{Osc}, which is superimposed on the common turn-on waveform of the IGBT, was determined.

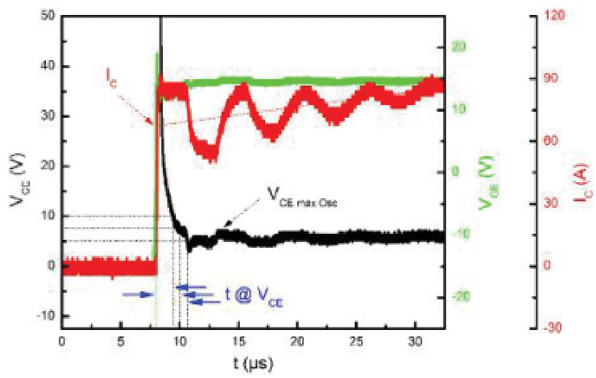

Figure 2: Turn-on characteristics of the 1200 V IGBT, i.e. the lower system in the setup

The turn-on characteristic of the IGBT is shown in Figure 2. V_{CE} decreases rapidly when the IGBT is turned-on. After the DUT is switched on, reflections in the range of a few volts are visible on the collector-emitter voltage. The reflections decay with the turn-on time. Reflections with an amplitude of more than 15 A occur in the collector current. These reflections are superimposed on the diode-recovery peak current (I_{rec}).

V_{CE} and I_C differ significantly from typical waveforms and may limit the short-circuit detection of the IGBT.

A schematic drawing of a simplified equivalent circuit diagram of the measurement setup is shown in Figure 3. The cables parasitic generate characteristic impedances in parallel to the load inductance and

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the free-wheeling path. When the voltage drop across the load inductance L_{load} changes rapidly, a charging current in the characteristic impedance can be observed; in the case of a switching event, not only the charging current itself, but also its reflections after twice the propagation time are observed. Therefore, the collector current through the IGBT is given by: $I_C = I_{load} + I_{Osc} + I_{rec}$, with load current I_{load}. Due to the fact that I_{rec} is significantly lower than I_{Osc}, it can be neglected.

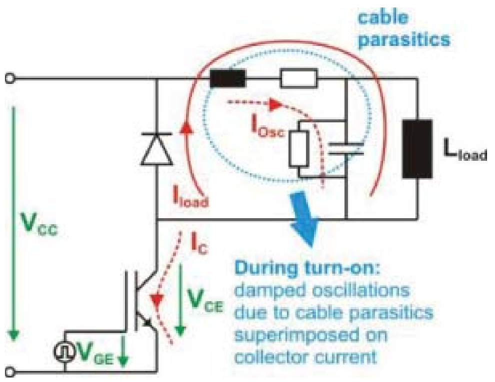

Figure 3: Schematic drawing of a simplified equivalent circuit diagram of the measurement setup

The fast short-circuit detection is realized with a V_{CE} -desaturation-detection circuit, the drop of V_{CE} is monitored, and the reaction time of the system is extracted. To determine this reaction time, the time interval is measured between the turn-on pulse at the gate terminal, i.e. $V_{GE} = 0$, and the instant in time that V_{CE} drops below a certain value, e.g. $V_{CE} \leq 10$ V.

A desaturation-detection circuit can be realized if this reaction time is well below the short-circuit withstand time of the IGBT. At high currents, this reaction time is expected to be longer, as it takes longer for V_{CE} to drop.

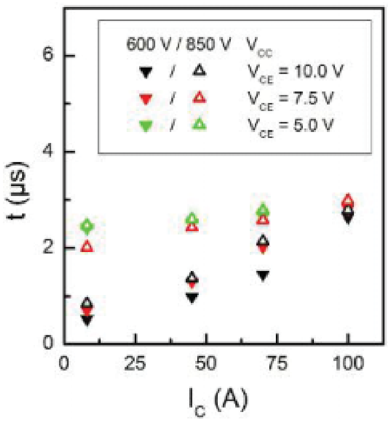

Figure 4: Reaction time of the system versus the collector current at different V_{CE}-desaturation-detection levels for V_{CC} = 600 and 850 V

The reaction time of the system versus the collector current is shown for V_{CC} = 600 and 850 V is shown in Figure 4. For a desaturation-detection level of V_{CE} = 7.5 and 10.0 V, the reaction time of the system increases from 0.8 µs - at a low collector current - to 2.6 µs at a high collector current with V_{CC} = 600 V. At a dc voltage of V_{CC} = 850 V and for the detection level of V_{CE} = 10.0 V the same behavior is observed. However the reaction time is less than 0.3 µs longer. In contrast to this, the reaction time is always longer than 2 µs for V_{CE} = 7.5 V at V_{CC} = 850 V.

Independent of the DC link voltage, a desaturation-detection level of V_{CE} = 5.0 V always provides reaction times longer than 2.5 µs and for 400% of the nominal current, V_{CE} did not drop below 5.0 V at all. Therefore, V_{CE} = 5.0 V does not allow a reliable distinction to be made between normal operation and when a short circuit occurs.

The maximum value of the collector-emitter voltage ($V_{CE\ max\ Osc}$) after the turn-on process of the 1200 V IGBT has finished is shown in Figure 5. For V_{CC} = 600 V, $V_{CE\ max\ Osc}$ is in the range of 6.0 V for low collector currents, and reaches a value of 7.5 V at 400% of the nominal current. At V_{CC} = 850 V, $V_{CE\ max\ Osc}$ is consistently above 7.5 V; however, even for I_C = 100 A, it still remains below 10.0 V.

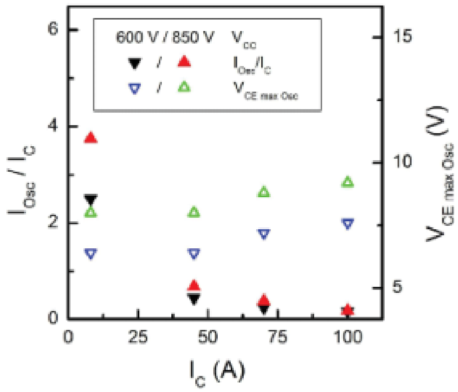

Figure 5: The maximum amplitude of I_{Osc} in relation to I_C and maximum V_{CE} after the 1200 V IGBT has been turned on for V_{CC} = 600 and 850 V.

These results show that even for very high collector currents, a reaction time of less than 3 µs can be achieved. To implement reliable short-circuit protection, the desaturation-detection level should be at least 7.5 V (V_{CC}=600 V) or 10 V at V_{CC} = 850 V.

The maximum amplitude of I_{Osc} in relation to I_C is also shown in Figure 5. It can be seen that for low collector currents, the charging current is at least twice the load current. With increasing collector current, the ratio between I_{Osc} and I_C decreases and the charging current becomes less dominant.

These results illustrate that the charging current leads to a massive additional load for the IGBT. Especially for low collector currents, the losses of the IGBT increase significantly. As a consequence, the thermal management of the inverter and the IGBT have to consider these additional losses.

Conclusion

The protection of fast switching IGBTs is strongly influenced by cable parasitics. Especially for very long cables, a significant charging current is added to the load current and oscillations are observed in the collector-emitter voltage. These effects can significantly limit the efficiency of protection measures, such as desaturation detection. Although the influence of the cable parasitics is considerable, it is experimentally shown and concluded that it is theoretically possible to detect a short circuit in less than 5 µs.

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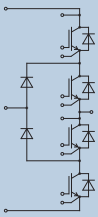
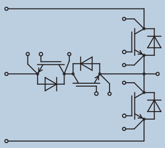
- EconoPACK™ 4 NPC1 topology for high switching frequencies (approx. $f_{sw} \geq 12$ kHz)

NPC1 topology
- 650V IGBT4
- Optimized for $f_{sw} \geq 12$ kHz
- Portfolio
  - F3L200R07PE4
  - F3L300R07PE4



NPC2 topology
- 650V/650V IGBT4
- 650V/1200V IGBT4
- Optimized for $f_{sw} < 12$ kHz
- Portfolio
  - F3L400R07PE4_B26
  - F3L300R12PT4_B26
  - F3L400R12PT4_B26



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Specialized DC/DC Converters Enable Simple and Efficient Switching in IGBT Applications

Modular DC/DC converters with dual asymmetric outputs provide the positive and negative voltages as well as the galvanic isolation necessary for IGBT applications.

By Matthew Dauterive, Field Application Engineer;
RECOM Engineering GmbH & Co. KG, Gmunden, Austria

As renewable energy takes center stage, efficiently harvesting this energy becomes increasingly critical. One main reason for efficiency increases in recent years has been the significant improvement in IGBT performance. IGBTs rapidly switch high voltages (1000V or more) with extremely low switching losses, making them logical choices when designing inverters and boost converters in power conversion circuits.

In Figure 1, two typical functions of IGBTs in power conversion circuitry are employed. Since DC voltage from the photovoltaic array is unstable and not maximized, a boost converter employing maximum power point tracking (MPPT) is used to acquire the maximum DC voltage from the photovoltaic array further improving performance.

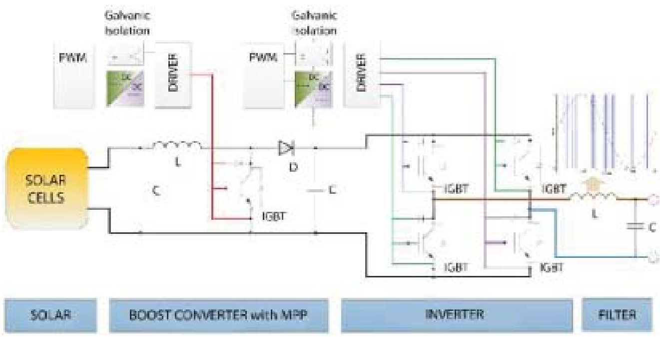

Figure 1: Photovoltaic Power Conversion

However, this voltage is often useless in DC form. To make it compatible for transmission, it is converted into an AC waveform by using two pairs of bridge-connected antiphase IGBTs. These IGBTs are switched with a PWM signal creating the signal in Figure 1. After passing over an LC filter, it is smoothed and becomes an AC sine wave which can then be injected into a power distribution network.

IGBTs are not only used in power harvesting but in loads as well. Motors control a majority of the world's electricity, and variable-frequency-drive motors are often the most economic choice. In a typical application (Fig 2.), IGBTs are used to adjust the frequency of the AC signal in a variable-frequency-drive 3-phase motor. The six-pulse voltage-source inverter drive consists of a bridge rectifier, DC link, and inverter. The 6 IGBTs in the inverter produce the adjustable frequency pulse input to the 3-phase motor.

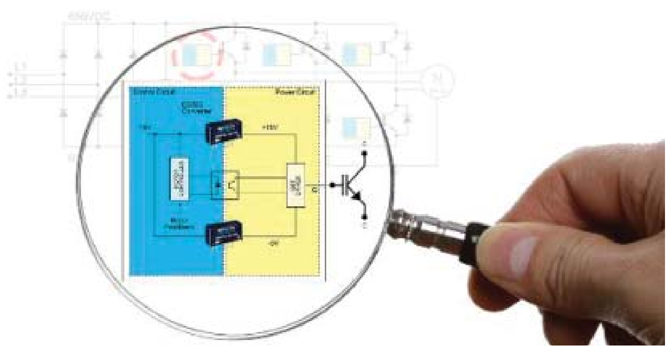

Figure 2: IGBT Driver Circuitry

For IGBTs to be an efficient solution, they must be properly driven. Since IGBTs switch at high frequencies up to 300 kHz, typical control circuitry is inadequate. Luckily, drivers were developed in order to allow IGBTs to rapidly switch with minimal losses. Since the driver is connected to the power circuit floating at high voltages, it is isolated from the low voltage control circuit. An optocoupler isolates the feedback, and the power supply to the driver is galvanically isolated over DC/DC converters. Two separate voltages are used to meet the special conditions when driving an IGBT.

To minimize switching losses, an IGBT switches extremely fast, and the slew rate depends on how fast the gate is charged. Practically, it has been seen that +15VDC is sufficient to reliably switch on an IGBT, but if the IGBT switches too quickly, the current overshoots, producing a destructive current spike. This not only wreaks havoc with regards to electromagnetic noise, but it also damages the IGBT and its surrounding circuitry. To dampen the spike, it is necessary to increase the switching time of the IGBT by increasing gate resistance. However, if switching time is increased, then so are the switching losses – and there is part of the dilemma.

The turn-off behavior of the IGBT further complicates the matter. Again, the switching rate is determined by the gate capacitance. The faster the gate is discharged, the faster the device turns off. In order to further speed up the discharge of the gate to reduce switching losses, a negative voltage is applied. Logically, -15V is considered so one dual-output ±15V DC/DC converter can be used for both positive and negative rails. However, when the device is switched off too hard, a large destructive voltage spike is created. It is believed that such spikes decrease the life expectancy of IGBTs. Therefore, it becomes necessary to moderate turn-off rates by decreasing the magnitude of the negative voltage on the gate. Practically, -9VDC is considered to be a nice trade-off. Although switching time is slightly increased leading to larger switching losses, the resultant voltage spikes become manageable.

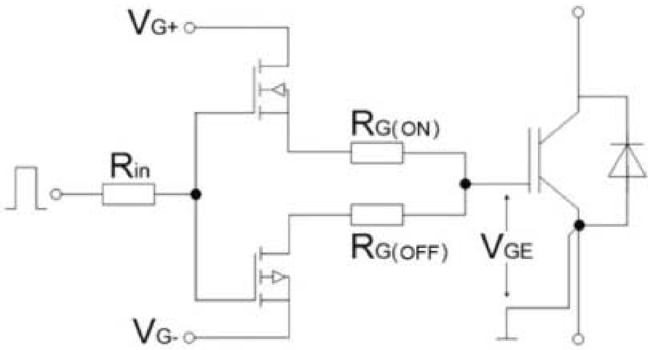

Figure 3: IGBT Control Circuit

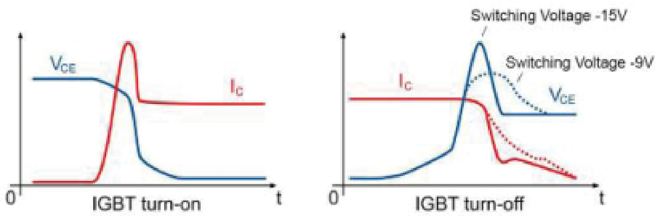

Figure 4: IGBT Switching Characteristics

So there is the full dilemma – either use one ±15 or ±9VDC dual-output converter and settle for the compromise in either switching losses or destructive voltage spikes, or use two separate DC/DC converters to provide the optimized 15VDC and -9VDC which increases component count and design costs. However, there is a third option: use an asymmetrical, dual-output DC/DC converter specially designed for IGBT applications – which is exactly why converters such as RECOM's R05P21509D have been brought to the market.

The asymmetrical output voltage of these DC/DC converters make them ideal for supplying the rails which optimize the driving characteristics of IGBTs, but additional information should be considered before selecting the right DC/DC converter. Not only are these converters responsible for supplying the asymmetrical rail voltages, they also provide galvanic isolation which protects the control circuit from high voltages in the power circuit. And without adequate isolation, the entire application fails. But what is adequate isolation?

The level of isolation is often used to describe the isolation of DC/DC converters. Good engineering practice dictates that twice the DC link voltage is a sufficient isolation level. IGBT applications may have a DC link voltage of slightly more than 1000VDC, so it seems that 2000VDC should be enough. But it is important to remember the switching spikes at turn on and turn off. Furthermore, the parasitic capacitances in the circuit are discharged because of the high slew rate of the IGBT, and the actual voltage levels at switching are much higher. A major hurdle in measurement technology is attempting to measure these spikes in a real application. The inductance of measurement probes actually compromises the measurement making it nearly impossible to accurately measure these spikes. Since determining the necessary level of isolation is not an exact science, it is a good idea to

go as high as reasonably possible. For example, a typical application running with a DC link voltage of 1000VDC should use an isolation level of 6000VDC in order to provide continued isolation and extend the lifetime of the system.

While the level of isolation is obviously critical, the type of isolation determined by the construction of the transformer is equally important. Functional isolation relies solely on the transformer wire coating in the DC/DC converter. Once this coating cracks, the isolation of the system fails catastrophically. A better design using basic isolation physically separates input wires from output wires so that even if the wire coating fails, there is still adequate distance between input and output circuits. Since IGBTs often switch at very high frequencies, the isolation is heavily taxed. Therefore, it is recommended that basic isolation is used in order to further extend the lifetime of the system.

When the right DC/DC converter is chosen, IGBT drive circuitry is simplified. Additionally, the life of the application can be extended by making the right choice of switching voltages in order to dampen switching spikes. Moreover, isolation type and level are critical in order to maintain isolation throughout the life of the application. RECOM has recently released a family of IGBT converters which meet these demands for IGBT switching applications. Information about these products can be found on RECOM's website at:

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SiC MOSFETs Improve PV and UPS Inverters and Industrial Power Supplies

Since the release of the first generation of SiC MOSFETs in 2011, these wide bandgap power devices have taken a major step forward in the commercial market place, including the introduction of a second generation MOSFET product family.
This new generation device's improved performance, as well as the fact that there are now multiple sources of SiC MOSFETs available in the market, has changed the economics for several applications, notably photovoltaic (PV) and uninterruptible power supply (UPS) inverter design, as well as industrial power supplies.

By Paul Kierstead, Cree

The second generation of SiC MOSFETs available in 2013 from Cree and others now includes devices rated at 1200V/ 320†, 160, 85, and 25mOhm, along with devices rated at 1700V / 1Ohm and 40mOhm. These higher-rated next generation MOSFETs not only enable their use in applications ranging from 60W to 1MW (primarily in industrial power supply, solar inverter, UPS inverter, and motor drive markets), but they are also the industry's most efficient 1200-1700 V power transistor technology available in terms of measured device losses. SiC MOSFETs exhibit a fraction of the switching losses associated with commonly used silicon IGBTs. Conduction losses are also reduced in most applications. The latest generation of SiC MOSFETs has improved on the already substantial (factor of 7-10 lower losses) technical advantages over silicon devices, while device costs have been reduced by nearly half in 2013. The result has been several recent public announcements of mass production using these new SiC MOSFETs by manufacturers of solar inverters and industrial power supplies. This article compares different economic and performance trade-offs for applications using the SiC MOSFET relative to other conventional solutions.

In PV inverters, SiC MOSFETs are rapidly being designed in, but whereas a few years ago, the reason to specify SiC devices was part of a push to increase efficiency, the latest generation of SiC MOSFETs is being used primarily to cut inverter costs. SiC MOSFET energy efficiency and high switching frequency capability are allowing increased power density, reduced cost of thermal management and smaller, lighter, less expensive magnetic components. For example, Figure 1 illustrates a commercial 11kW PV inverter released in 2013 using SiC MOSFETs[1]. These PV inverters typically operate with a boost stage, a power or inverter stage, and an auxiliary power supply, and SiC MOSFET technology impacts each of these segments. (UPS inverters face similar needs, although with some differences in terms of requirements to deliver feedback to the grid, and handle over-current pulses.). Using SiC MOSFETs with very low switching losses allows designers to keep efficiencies high with relatively simple topologies such as two-level instead of three-level, fewer components, and standard gate drive products.

Figure 1: 11kW PV inverter released in 2013 using SiC MOSFETs[1]

Inverter Boost Stage:
In a typical inverter boost stage, a 200 to 400VDC solar panel input (for PV) is boosted to an output voltage of 450 to 1,000VDC. The power electronics design engineer's goal is to keep the system efficiency as high as possible, but at the same time achieve as low cost as possible through size, weight and component reduction. Work published at the 2013 PCIM[2] and in Bodo's Power Systems[3] detailed the use of SiC MOSFETs and diodes in the boost stage to cut costs by 10-20% compared to conventional technologies, and at the same time gain extremely high efficiency (+ 99%) for a 10kW interleaved topology operating between 60 and 100 kHz. Compare that to efficiencies in the mid 98% range at no more than 20 kHz for typical silicon boost designs. SiC MOSFETs provide better efficiency at much higher frequencies, which enables the key cost reduction in magnetics. The initial boost work published at 10kW has since been scaled to 50kW as shown in Figure 2, and is targeted for future publication. The 50 kW boost shown in Figure 2 is only 7 kg, and a volume of only 450mm x 250mm x 155mm. The SiC 50 kW boost shown in Figure 2 is up to half the weight and half the volume of a typical silicon implementation. Throughout the 5-50kW range, the performance and economic benefits to using SiC MOSFET and diode technology are similar.

Si IGBT technology is typically limited to the 20 kHz range due to their switching losses, even when using high speed IGBT devices (IGW40N120H3). Moving to SiC MOSFET technology allows the frequency to scale up to between 60 and 100 kHz, with improved or constant efficiency depending on the optimization chosen for the particular design. This higher frequency operation, in turn, enables the inductor costs to be cut substantially, resulting in as much as a 20% overall bill of materials (BOM) cost reduction for the boost stage.

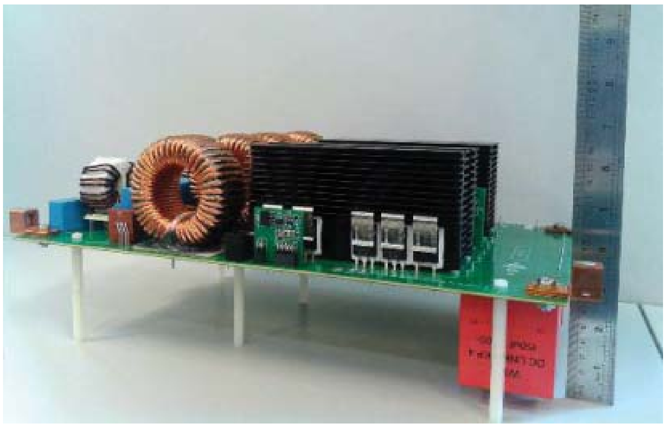

Figure 2: Initial boost work published at 10kW has since been scaled to 50kW

Additionally, the operating temperature, weight and efficiency of the system are dramatically improved by specifying the SiC MOSFET over conventional Si technology, with power density typically possible to be over one kW/kg for lower power (up to 100 kW) systems which is three times higher than many commercial Si-based systems today in the same power range. Improved kW/kg translates directly to BOM cost reduction, and reduced shipping, installation and maintenance costs. As illustrated in Figure 3, the normalized results using SiC MOSFETs in a 10 kW boost reference design, relative to the Si IGBT technology results in significant reductions in cost (~20% less), weight (~50% less), and operating temperature (20-30% less). Exact results will vary depend the design engineer's implementation of SiC MOSFETs, but clearly the system cost can be cut significantly.

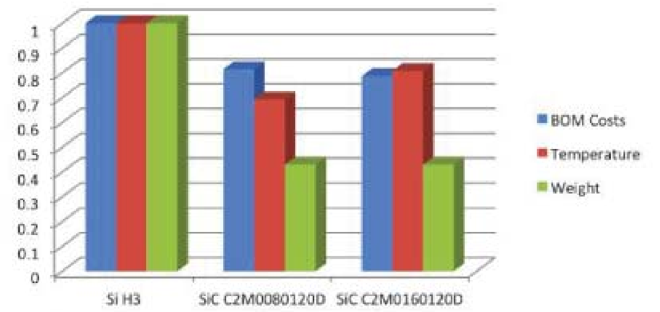

Figure 3: Normalized results using SiC MOSFETs in a 10 kW boost reference design

Inverter Power Stage or Inverter Stage:
In the inverter stage, unlike the boost stage, the operating frequency is generally lower to minimize EMI. However, a typical high-frequency PV inverter power stage using SiC MOSFETs can be targeted to 48 kHz, whereas Si-based PV inverter power stages are typically limited to operation at 16kHz or less. Thus, although inductor costs are reduced, it is a less significant reduction than is possible in the boost stage.

For the power stages, either two-level, T-type or similar topologies are available for SiC-based inverters. Unlike Si-based inverters, switching losses are typically reduced by a factor of seven or more, thus scaling to 48+kHz allows the design engineer to maintain acceptable (~ 98% +) power inverter stage efficiencies regardless of topology. Hence, the choice of topology then becomes driven by cost, rather than performance concerns. For example, SiC enables equal or better performance in a simple two-level hard switched topology than more complicated multi-level topologies while providing equivalance advantage of higher switching frequency. For central inverters, the DC link voltage is also being pushed up to 1,500 V with 1,000 V output, and this move also favors SiC for simpler topologies due to the very low switching losses of 1,200 and 1,700 V SiC MOSFETs. In general, using SiC MOSFET technology enables a reduction in inductor costs, and the topology can be chosen based on other cost factors, such as number of components, drivers, and so on, so as to achieve the maximum high-frequency performance for the minimum cost. In addition, lower part counts and simpler designs can contribute to improved system reliability and lifetimes.

In the power stage, there is one additional way SiC MOSFET technology can lower costs. In addition to the savings realized by reducing the inductor size by raising the frequency to 48+ kHz in a simple PV inverter stage topology like two-level or T-type, it is further possible to eliminate the external anti-parallel SiC Schottky diode. By using the SiC MOSFET's third quadrant operation4, the body diode is only on during dead time, thus the channel of the MOSFET, allowing for symmetric conduction, lowers conduction losses by 55-60% relative to the body diode operation alone. In this manner, both inductor costs and SiC diode costs are reduced for a typical 48 kHz power stage.

Figure 4: 60 W auxiliary power supply evaluation board

In UPS inverter stages, in contrast to PV inverter stages, a larger pulse requirement is needed, which would ordinarily require surge larger SiC power MOSFETs be designed into the primary switch positions. However, unlike PV systems, UPS applications may have inverter stages that go well above 48 kHz operation (up to 80 kHz in many cases), enabling even more savings in the inductor segment of the inverter stage. The additional inductor cost saving can offset the marginal increase in SiC device cost.

Auxiliary Power Supply:

To illustrate the savings possible in the auxiliary power supply stage, a 60 W reference board has been made available [5] demonstrating the advantages of using a 1700 V, 1 Ohm SiC MOSFET in a simple single-switch flyback topology as compared to a conventional silicon-based two-switch flyback topology. The simpler single-switch flyback topology made possible with SiC MOSFET technology results in the architecture having fewer components, lower costs (only one driver instead of two drivers, for example), better efficiency (enabling cooler, more reliable operation while completely eliminating the heat sink cost), and, of course, lower magnetic costs due to the higher frequency operation. Additionally, voltage clamps or snubbers can be eliminated, since the SiC MOSFET has 1700 V of breakdown voltage (with a comfortable margin) compared to Si-based FETs, which are typically limited to 1500 V.

Figure 4 shows a 60 W auxiliary power supply evaluation board, which illustrates these advantages. Note the SiC MOSFET is shown on a heat sink, but in many actual designs, the heat sink may not be needed. It is important to point out these auxiliary power supply advantages are not only limited to UPS and PV inverters, but can be applied to motor drives as well.

Summary:

Applying SiC MOSFET technology in the boost, inverter power, and auxiliary power supply stages, can result in anywhere from a 5% - 25% reduction in overall inverter costs for PV and UPS inverters, depending on the architecture chosen and volume considerations. Additionally, the inverter weight can be reduced substantially (~50%), as SiC MOSFET technology can achieve a 1kW/kg power density for lower power systems up to 100 kW. This weight reduction allows for even more savings in shipping and installation costs, in addition to the BOM reduction.

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Combined Capacitor and Choke for Motor-Run Applications

Economic and efficient control of bidirectional motors

A design for the control of bidirectional AC motors features the EPCOS LCap, a combined motor-run capacitor and choke in a single rugged package. Thanks to LCap's narrow tolerances over time, compact size and reduced assembly complexity, it is designed for use in economical and energy-saving drive controls for washing machines, dryers, garage door openers, gate openers, power shutters and more.

By Mischa Baur, Product Marketing Manager, AC-DC Capacitors, TDK

Standard bidirectional asynchronous induction motors used in appliances such as economy washing machines have two windings: the primary winding and the auxiliary. A motor capacitor is needed to start the motor in the required direction by shifting the phase to the necessary winding. Conventionally, electromechanical switches have been used to control the motor (on-off, direction of rotation).

Electromechanical switches, however, have obvious drawbacks. They produce noise, have a higher breakdown risk, and they have a shorter average operating life than electronic components. There is a large demand for electronic control solutions to replace electromechanical designs (relays) with the objective of increasing operating life and reliability, reducing power consumption and making the drives quieter.

Premium appliances such as top-of-the-line washing machines and dryers with sophisticated programs employ variable speed drives that are controlled by frequency converters. These solutions achieve a very high degree of variable motor control and energy efficiency. The electronics, however, are complex and require a large number of electronic parts. The complexity and costs of the subsequent assembly processes are correspondingly high

Reliable and elegant solution

Together with TDK, STMicroelectronics developed and qualified an elegant and economical electronic control system for bidirectional AC motors (Figure 1). The design consists of the following circuit components:

STM microcontroller unit (MCU)

STM triacs (ACST, BTA and High Tj Triacs series) to switch the power to the required winding

EPCOS LCap combined motor-run capacitor and choke to produce the phase shift for the auxiliary winding and protect the switches from overcurrents, respectively.

Compared to circuits that use electromechanical switches, the design offers several benefits:

- Higher efficiency because triacs are operated by a single pulse, thus eliminating wasted power consumption from a continuous flow of current through the relay coil
- Increased reliability because triacs have a longer operating life than relays
- Reduced EMI thanks to spark-free operation
- Noise reduction through the elimination of mechanical relays
- Suitable for use in single-speed bidirectional drives for applications such as garage door and gate openers or power awnings and shutters

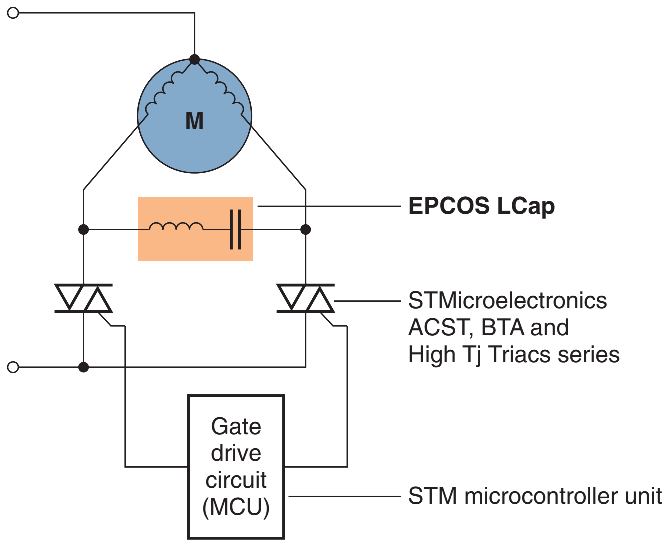

Figure 1: Electronic motor control

The latest generation of triacs is well suited for this application. They offer fast switching and are driven by gate currents as low as 5 mA. Moreover, the triacs, for example, have a very high surge current capability (ITSM). A single 16-A triac can withstand a surge current of 140 A for 20 ms and a repetitive dI/dt of 100 A/µs. The phase angle can be easily controlled, which would be hard to achieve with mechanical relays.

Effective overcurrent limiting with integrated choke

A choke is needed in the electronic circuit with two triacs to protect the switches in the event of current overload. EMI in the circuit, for example, can force both switches to the "on" state, which would discharge the capacitor without any current limitation. The current overload resulting in such an event can damage the switches. To prevent this, an inductor is inserted in series with the capacitor to limit the current supplied by the capacitor during the period of current overload.

A triac current of more than 1000 A (Figure 2) is possible for the first peak lasting 25 µs when both triacs are forced to the "on" state simultaneously (red curve). This value is typical for a bidirectional asynchronous 230 V, 50 Hz induction motor with a rated power of 150 W that is driven by a circuit with two triacs using a 10 µF phase shift capacitor. This high current exceeds the maximum value allowed for the triacs.

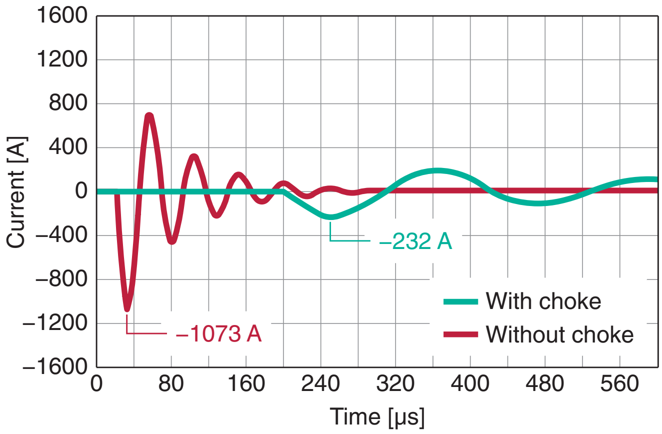

Figure 2: Peak current with and without a choke in series with capacitor

A series choke effectively limits the current peak. The dI/dt rate will be shifted to values that triacs can withstand without damage. As shown in Figure 2, an inductance of 80 µH reduces the first peak current to

Figure 3: EPCOS LCap

less than 250 A (green curve) with a duration of 110 µs, keeping the current within the safe operating area. Tests at the STMicroelectronics laboratories have shown best results when using an EPCOS LCap, an integrated capacitor and choke that combines the phase shift capacitor with the current limiting choke in one package.

During washing mode, the drum is rotated in both directions by turning on each triac alternately. One of the two windings of the induction motor is supplied directly by the mains voltage. The other is supplied through the motor-run capacitor providing a phase shift and a high voltage across the capacitor, which can reach a peak value of 650 V. Only one triac is turned on during spin mode, since the drum rotates at maximum speed in one direction only.

Two components, one package

The EPCOS LCap, which combines the motor-run capacitor and choke in one package, offers a number of performance and logistics benefits compared to a solution with discrete components:

	EPCOS LCap - B32350- -		TRIAC [1-]
Motor power - W - 230 V, 50 Hz-	Capacitance F-	Inductance - - H-	Type
120	4	5	ACST610-8 BTA06-800TWRG BTB12-600TWRG High Tj Triacs
190	10	80	ACST1235 ACST1035 BTA12-800CW High Tj Triacs
250	50	100	ACST1635-8FP BTA16-800CWRG High Tj Triacs

[1)] From STMicroelectronics

Table 1: Typical combinations of LCap and triacs

- Low ESR
- Long-term stability with narrow tolerances
- Highly rugged and maintenance-free
- Compact size
- Two connections instead of four
- Reduced assembly time

Capacitor	
Rated capacitance [µF]	3 to 50
Rated voltage [V AC]	230 to 450
Tolerance [%]	± 5
Choke	
Rated inductance [µH]	5 to 100
Tolerance [%]	± 10

The EPCOS LCap is available in a wide range of rated capacitances and inductance values. Types with further values, for example, for small motors are available on request.

Table 2: Key data of the EPCOS LCap combined motor-run capacitor and choke

The integrated capacitor and choke in one package offers tighter tolerances than a discrete solution because the air-core coil choke typically exhibits higher tolerances as a result of mechanical influences that can physically change the winding. In addition to LCap's ideally matched electrical characteristics, the combined component offers measurable benefits for assembly in production lines. Moreover, the lower component count means that fewer assembly operations are necessary, resulting in improved failure rates. Thanks to these advantages, LCap technology is already being used successfully by global market leaders for economical and easy-to-mount solutions.

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Trade-offs When Selecting Automotive Dc/Dc Converters

In automotive designs using dc/dc converters, strict conducted and radiated emissions have to be met. Emissions in the Radio LW, MW, SW and FM bands are more tightly controlled to avoid interfering with the vehicle's radio reception, Figure 1.

By Dan Tooth, Texas Instruments

The most tightly controlled being the FM band, which can have an average conducted emissions limit that is almost three-times lower than in the MW or SW bands. (Note – the MW band is sometimes referred to as the AM band).

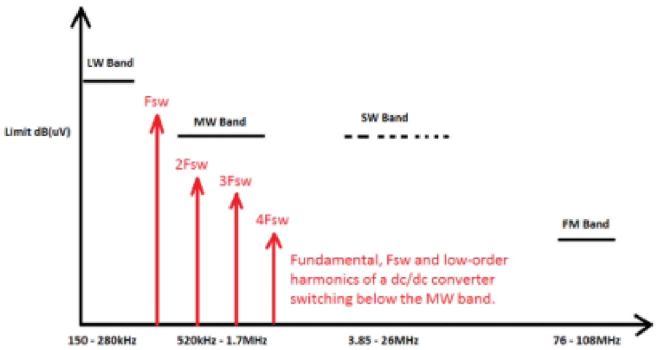

Figure 1 – Typical Conducted Automotive Emissions Requirements, highlighting the Radio Bands. Also the positions of a Fundamental Switching Frequency, Fsw and its low order Harmonics.

Also, the ambient temperature in automotive applications is expected to reach 85°C. When the temperature rise due to power losses within a dc/dc converter IC are added to the ambient temperature, junction temperatures can reach 125°C. These two different yet related requirements are often a focus for the automotive electronics design engineer.

Dc/dc converters produce switching frequency noise at their switching frequency fundamental (Fsw) plus harmonics of Fsw. In addition they produce much higher frequency noise which can fall within the FM band, due to parasitic resonances excited in the dc/dc converter circuit. To avoid producing switching frequency noise in the MW band, you can select a switching frequency that lies just above it, at 2MHz ± 10%, where the emissions are permitted to be higher. This is straightforward when the input voltage (Vin) is low, e.g. 5V or 3V3, because the duty cycle and hence converter on-time (Ton) remain long enough to stay above the minimum on-time (Ton(min)) of the dc/dc converter IC. Ton = Vout / Vin x 1 / Fsw. However, when the dc/dc converter in question is connected to the vehicle battery, Ton becomes very short. For automotive applications, the maximum Vin the converter is required to support varies, but can be 18V for continuous operation, 24V for 2 x battery and up to 32V for load-dump transients. (As the input voltage increases, Ton of the step-down dc/dc converter decreases. If the Ton is required to be less than the IC's Ton(min) then this leads to pulse-skipping [1] behavior, Figure 2 and increased RF emissions in unpredictable lower frequency bands. To avoid this behaviour, the switching frequency must be decreased, which results in Ton increasing for a given duty cycle D = Ton x Fsw).

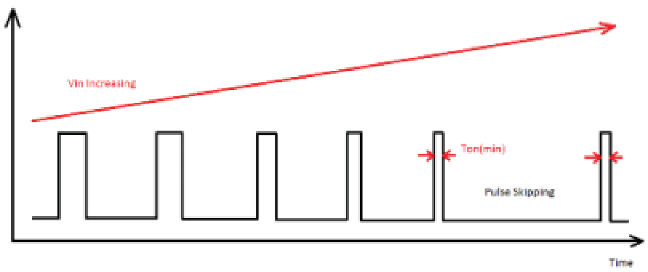

Figure 2 – Increasing Vin leads to Decreasing Ton, Until Ton(min) of the IC is reached and pulse-skipping behavior is Encountered.

Another approach is to set the switching frequency of the converter connected to the battery below the MW band. The four or five-times reduction in switching frequency compared with switching at a frequency above the MW band makes Ton(min) of the IC no longer an issue. With a longer Ton, the dV/dt of the switch-node waveform can also be reduced, exciting less ringing of the resonant parasitic tank circuits and less emissions in the FM band. Figure 1 shows that the fundamental, Fsw, is located at a frequency where the emissions are permitted to be higher. The 2nd and 3rd harmonics of Fsw do fall into the MW band, but they are lower in amplitude compared with the fundamental. The input filtering is manageable – Texas Instruments designed a two-stage input filter comprising an inductor and a bead inductor, that passed the automotive test limits when tested according to CISPR25 at an independent test facility [2].This was for TPS54360-Q1 with a 3.5A load.

The high ambient temperature which automotive electronics have to be designed for (>85°C) can create issues with ICs getting too hot. Synchronous dc/dc converters (two integrated MOSFETs in the IC) have all the losses in one IC pkg. Non-synchronous dc/dc converters (one integrated MOSFET plus an external Schottky diode) spread the losses between two packages, with a corresponding bigger thermal area. Furthermore, when computing MOSFET power losses it is important to use their on-resistance value, Rds(on), at a realistic junction temperature of 125°C, not room temperature. Calculating or measuring conduction losses at room temperature is not realistic and could easily lead to disappointment when the ambient is moved up to 85°C. At high temperature then MOSFET Rds(on) is significantly higher, (by 0,5%/°C). Conversely, the forward voltage of a Schottky diode decreases with temperature, reducing losses. The conduction losses in a MOSFET are proportional to the rms current squared, whereas in a diode they are proportional to the average current.
Switching power loss, Psw, in the top MOSFET is approximately Psw = Vin x Iout x Fsw x Tr where Tr is the rise time of the voltage on the switching node. (The switching loss in the bottom MOSFET is small and ignored in this discussion). From that equation, and all other things being equal, switching above the MW band compared to below it gives a four or five times increase in switching losses, simply because the switching frequency is four or five times higher. To calculate the total power dissipation in the IC, then switching losses have to be added to conduction losses.

In summary, a synchronous buck converter has two sets of MOSFET conduction losses plus one of switching losses dissipated in one IC package. A non-synchronous buck converter has one set of conduction and switching losses in the IC and one set of conduction losses plus a small switching loss in the external diode.

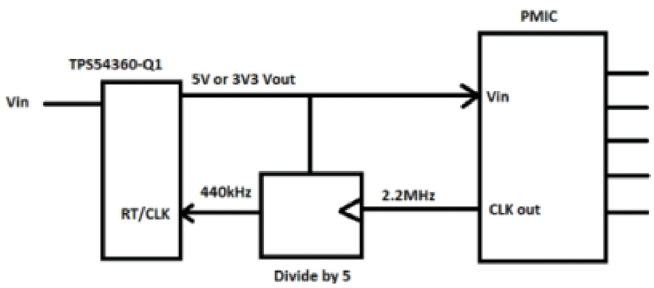

Figure 3 – Two dc/dc Converters with Clock Synchronization at Different Frequencies via a Divide by Five. TPS54360-Q1 is switching below the MW band and the PMIC above it.

In an automotive power topology and given the tradeoffs discussed, then a low input voltage power management IC (PMIC) can be used, switching at 2.2MHz(typ), plus an upstream converter, TPS54360-Q1, as shown in Figure 3. TPS54360-Q1 was operating off the car battery and is switching just below the MW band. The switching frequencies of the converters can be phase-locked by dividing-down the 2.2MHz PMIC clock by a divide by five circuit [3]. The output of the TPS54360-Q1 can be set to either 3V3 or 5V, but the current is lower for the same output power when 5V is used and so it is preferred.

The TPS54360-Q1 is part of a new family of non-synchronous (MOSFET + external diode) automotive dc/dc converters with a max Vin of 60V, or 42V for TPS54340-Q1 and are rated at 3.5A. TPS54540-Q1 and TPS54560-Q1 are higher current 5A versions. (The term “non-synchronous dc/dc converter” only refers to the fact it has one MOSFET and a diode and is not referring to their ability (or not) to accept an external switching frequency clock synchronization signal.) The ICs have a low drop-out voltage, which means that they retain Vout voltage regulation when the Vin has decreased so that it is only a few hundreds of milli-Volts above Vout and the duty cycle is high, D = Vout / Vin. Their SOIC plus power-pad package means the pin-pin and pin-pad metal-metal spacing is large at 0.8mm, to increase reliability under tough high humidity environmental conditions. As expected, their cost is very competitive as they are non-synchronous buck converters, which are lower cost than synchronous buck converters. These new ICs can all be synchronized to an external clock.

Conclusion

Synchronous buck dc/dc converters switching above the MW band are not a panacea. Non-synchronous dc/dc buck converters like TPS54360-Q1 family, switching below the MW band have many desirable qualities in automotive applications. Thermally, the losses are spread between two packages; the IC and the external diode, plus the switching losses are lower. The conducted EMI in the MW band can be managed by locating the switching frequency just below it and in the FM band by managing the switch node dv/dt. A simple two stage input filter can meet the conducted emissions requirements.

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Industry's First Reliable All-SiC Power Module for High-Efficiency Power Conversion Solutions

Nowadays, applications like solar and wind inverters, Uninterruptible Power Supplies (UPS), motor drives, welding and induction heating as well as high power auxiliary converters are becoming more and more energy-hungry. Therefore, the use and demand for power modules will increase accordingly. In addition, application efficiency or lower losses at high-switching frequencies become most important.

By Christopher Rocneanu, Field Application Engineer MEV Elektronik Service GmbH and Dr. Mrinal Das, Marketing Manager at Cree Inc.

Due to the low dynamic losses, high frequency capability and the very good thermal conductivity of wide band gap power semiconductors, especially SiC, the results are very promising.

MEV Elektronik Service GmbH is multiplying its efforts to offer the best solution for the customer, especially in the field of wide band gap semiconductors. At the beginning of 2013, we started to cooperate with CREE Inc., the worldwide leader of SiC and GaN wafers and devices. Not only do we offer modules or power semiconductors but also design and provide a complete solution for the customer.

In the high power field, MEV Elektronik offers two All-SiC-Modules at the moment. At the beginning of this year, CREE Inc. introduced the CAS100H12AM1, the industry's first fully qualified All-SiC module in a half-bridge configuration. The half bridge has an RDS(on)=16 mΩ (5x CPMF-1200-S080B in parallel), 1200V blocking voltage and a current rating of 105A @ TC=100 °C. It comes with an AlSiC baseplate in order to provide an ideal temperature match for higher reliability and lighter weight. Additionally, the module has a Si3N4 AMB (Active Metal Braze), with stable power and thermal cycling. The SiC technology enables designers to utilize the high-frequency capability of SiC MOSFETs and reduce the switching losses at the same time.

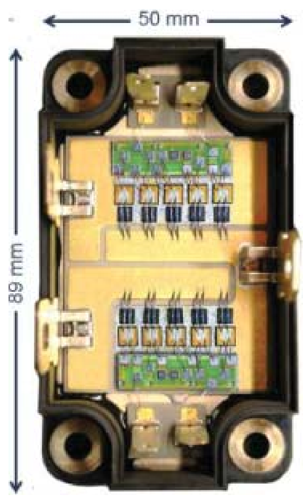

Figure1: Half-bridge configuration with 5x 80 mΩ (CPMF-1200-S080B) MOSFETs and 5x10A diode (CPW2-1200-S010B) in parallel. The MOSFETs are rated at 150 °C max. junction temperature and the diode is rated at 175°C max. junction temperature. The module is fully qualified and available at MEV Elektronik Service GmbH ex stock.

As already mentioned, the big advantages of the SiC-MOSFET are the low losses. Due to the unipolar structure of the MOSFET the current shuts off rapidly with no tailing phenomena. Moreover, as can be seen in Figure 2a) and b), the SiC MOS physics predicts a reduction of EON with an increase of temperature.

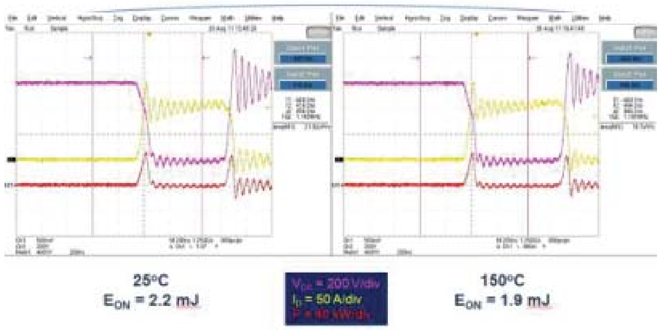

Figure 2: Turn-on Energy at a temperature of 25°C and 150°C

At the PCIM 2013, CREE Inc. recently released an All-SiC SixPack Module, alleviating conventional design constraints. The module (CCS050M12CM2) is configured in a three-phase topology and contains the 2nd generation of SiC-MOSFET and the 5th generation of SiC-Schottky diode chip technology from CREE. The newest generation of CREE's chips fully utilizes the enhanced performance and decreases the cost per chip due to the reduced die size. The module has a blocking voltage of 1200V, ID=50A @T=100°C, RDS(on)= 25 mΩ @ Tj=25°C and is rated at 150 °C maximum junction and case temperature. All in all the module has 6 times lower switching losses than an IGBT 4 module. Additionally, it has a high thermal conductivity design and is available ex stock MEV in an industry standard package from MEV Elektronik Service GmbH.

The biggest advantage of an all-SiC module is the derating which is due to the improved thermal behavior and lower switching losses compared to an IGBT module. Figure 3 shows the current vs. VCE, VDS respectively.

At the rated current the losses match, but due to safety reasons you rarely run the IGBT at the maximum rated current (especially at TC≥80°C). If the current is reduced to 15A, then VDS≈0.6V and VCE≈1.2V, which is due to the fact that the MOSFET has a linear curve and the IGBT has an exponential curve.

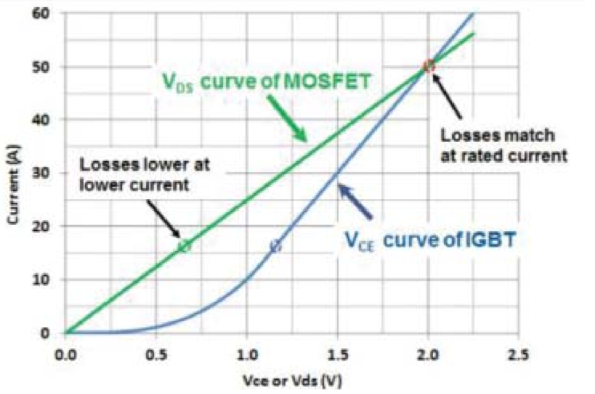

Figure 3: Comparison between 50A IGBT4 and 50A SiC MOSFET in module at TJ=150°C

Figure 4 shows the comparison between the CCS050M12CM2 and a Si-IGBT solution. The turn-on energy of the SiC MOSFET is roughly 30% of the IGBT. It can be seen that the Si IGBT has a high over-shoot, while the SiC-MOSFET has none. This is due to the fact that the Si-Diode is a pin-diode and the SiC-diode is a Schottky. With a Schottky diode the reverse recovery event is just capacitive. Thus, it is temperature independent and has a very small value.

For turn-off, the IGBT has Eoff= 11.2 mJ compared to Eoff= 3.2 mJ for the SiC-MOSFET. This is due to the tail current phenomenon which does not occur on unipolar devices like the SiC-MOSFET.

If you take a closer look at the curve you will find a lot of ringing. This is a normal behavior for SiC-devices and due to the high switching speed. To decrease the ringing, the SiC-MOSFET was switched with an external RG,ext.= 20 Ω, while the Si-IGBT had a RG,ext.= 5 Ω.

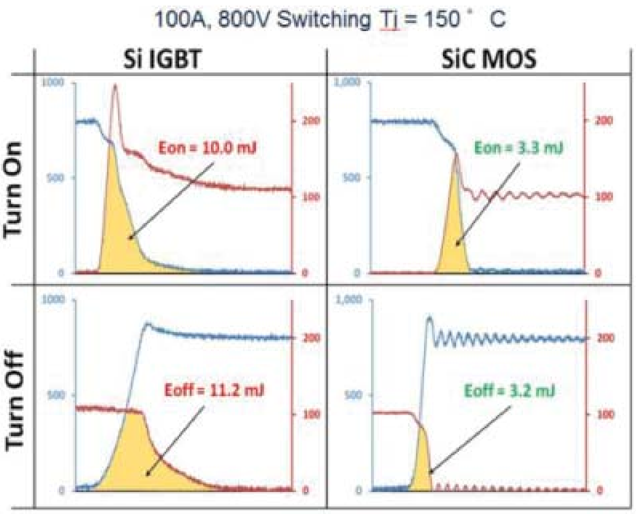

Figure 4: Turn-on and turn-off energy for CCS050M12CM2 and Si-IGBT Six-Pack

Even though the external gate resistance is 4 times higher, the total conduction losses are 3 times smaller with the SiC-MOSFET. Design considerations for SiC devices regarding ringing and EMI will be the topic in another article soon. Additionally, MEV is organizing seminars on SiC together with CREE. If you are interested or need further information please contact MEV.

Figure 5: Evaluation gate driver board

For evaluation purposes CREE Inc. developed an evaluation gate driver board. It is an easy-to-use, cost effective gate driver which is available ex stock MEV Elektronik.

But MEV does not only offer standard SiC-Modules. Since the beginning of 2013 we have a very strong and close partnership with Powersem GmbH to design, develop and sell customer-specific SiC power modules. We will use Cree's SiC dice and Powersem will package them in accordance with customer specifications.

MEV Elektronik will act as worldwide representative and technical sales force of Powersem and will design the modules according to the customer's requirements, offer technical support, logistics and after-sales service. Flexibility, pooling of competencies and customer-specific design will help the customers to meet their goals and achieve optimal performance in their products and solutions.

No matter whether you want an asymmetrical half bridge with NTC or half bridge with two 80 mΩ dies in parallel with or without a freewheeling diode, as long as it makes sense from a technical point of view, we can and will do it.

Several packages are available from Powersem. SiC-Eco 1 and SiC-Eco 2 are compatible with the industrial standard package. They are available in various heights (9 mm and 17 mm). Additionally, customers can use the SiC-Slim with a height of 6mm. For all packages, the customer can choose whether to solder (Gold Pins also available) or press-fit which is especially suitable for automotive applications. One advantage of press-fitting is the low resistance between the layers. A variety of customer-specific modules can be seen here:

http://www.mev-elektronik.com/data/download/PSM_Datenblatt_SIC-Modules_7_jz.pdf

"MEV Elektronik Service GmbH has been supporting SiC-technology for a long time,"says Mr. Chadda CEO of Powersem. "With their focus on technical project support and their experience in the area of wide band gap power devices, MEV is a very important partner for us. MEV Elektronik will act as a worldwide technical distributor of customer-specific SiC-modules. Furthermore, they will get prompt feedback from the customer's site as well as being able to fully support the customer in designing the optimal module with regard to performance and capability."

This partnership enables us to fully exploit the advantages of Cree's market-leading SiC technology, use the experience and expertise of Powersem' s package capability and at the same time commit ourselves to the needs of our customers, even the small- and medium- sizedones.

http://www.mev-elektronik.com

Miniaturisation of High Voltage, High Capacitance Multilayer Ceramic Capacitors

There is a constant battle to reduce size and weight of electronic components. Moore's law supposes that for computing hardware the number of transistors on an integrated circuit doubles every 2 years. Assuming that available space for these components does not increase - in fact it is generally desirable that this space decreases - it follows that the component size must dramatically reduce to compensate.

By Matt Ellis, Senior Application Engineer of Syfer Technology

The techniques and practicalities of handling and mounting discrete components, as distinct from those for semiconductor wafer processing, means that there is a baseline to size reduction which is rapidly approaching. There have, however, been constant improvements in manufacturing and materials technology over the past few decades allowing for miniaturisation of Multilayer Ceramic Chip Capacitors (MLCCs). Significant they may have been, but none the less not quite to the extent found in semiconductor manufacture. Volume manufacturers have pioneered these developments with the current commercially available pinnacle being the sand grain like 01005 EIA case size - surface mount capacitor only 16 thousandths of an inch by 8 thousandths. One such manufacturer has claimed a further improvement with a metric 0201 size, 0.2mm x 0.1mm or 0.008” x 0.004”.

The focus of this miniaturisation has broadly been in the field of base (or noble) metal electrode technology. Improvements in tape casting and other processes have facilitated these improvements but they generally only apply to low voltage components, a quick search of the main manufacturer's ranges reveals that the typical maximum available voltage, even in the now commonplace 0402 case size, is only 100Vdc with some suppliers pushing up as high as 250V in class 1 dielectrics. For higher voltage, large capacitance value and high power applications there is still a need for larger size components although miniaturisation can still provide significant benefits.

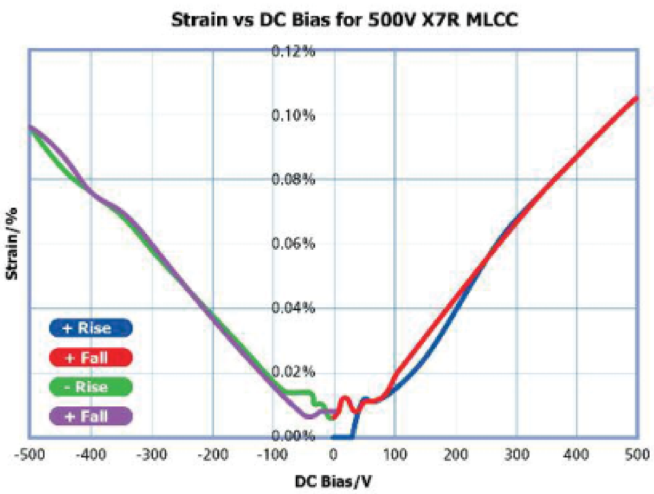

Figure 1: Graph showing strain vs DC bias for X7R MLC Capacitor

The space and aerospace industries are the primary beneficiaries of component weight reduction; according to NASA it costs $10,000 to put a pound of weight (454g) into space, that's $22 a gram so any drop in weight can lead to significant savings. The drive towards greener technology means that weight saving in any transportation system is also of benefit. With the increase in development and production of electric and hybrid electric vehicles the use of high voltage, and high voltage high capacitance, MLCCs is on the rise. Despite this demand miniaturisation has not occurred at anything like the pace of smaller low voltage components and it could be argued that, especially in the field of SMPS leaded capacitors, that technology has remained static. There are reasons for this; designers can be tied to MIL specifications which dictate a certain part, or range of parts, but there are also technical issues to overcome as well.

The limits of capacitor design are defined by their failure modes and there are many failure modes which limit the extent to which mid to high voltage MLCCs can be developed. There are extrinsic failure modes, such as mechanical and thermal cracking, but we will look at the intrinsic ones which are in the hands of the manufacturer. The limiting factor for MLCCs has changed over time, early types were limited mainly by the quality and purity of the dielectric materials themselves with point defects and contamination limiting the maximum number of layers and the minimum thickness of those layers. Generally speaking the higher the capacitance the lower the reliability as there is a greater total area of electrode overlap and therefore the likelihood of a point defect. As dielectric materials, together with materials preparation and processing, improved the limiting factor became the dielectric strength of the material itself. Once this problem had been overcome one could imagine that thicker and larger parts could be manufactured without fear of dielectric breakdown or point failures. Not to be as a new failure mode appeared - electro-mechanical stress cracking. Commonly referred to as piezoelectric effect it can also follow electro-strictive behaviour (figure 1) and has been the failure mode to limit MLCC advancement for some time now. It affects most class II barium titanate based dielectrics and becomes an issue for case sizes 1210 and upwards, with voltages above 200V. The crack typically runs through the centre of the component along one or two dielectric layers (figure 2).


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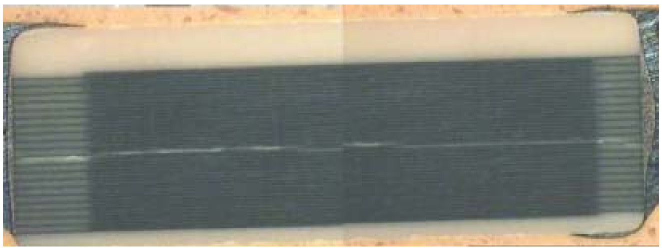


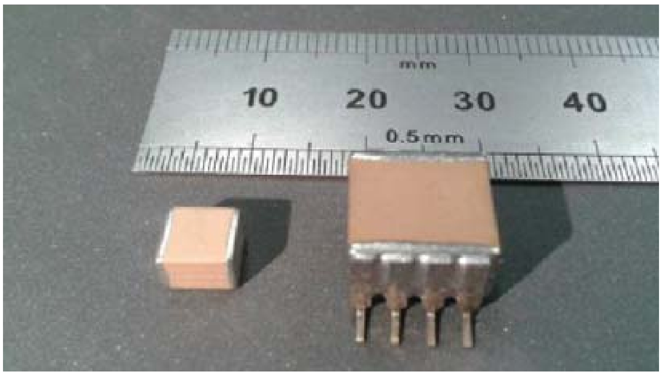
Figure 2:
Typical "Piezo" crack failure through centre of MLC Capacitor

In order to increase the available capacitance for a given footprint, the common solution is to 'stack' capacitors together with lead frames. However, it is not only labour intensive, and therefore costly, but can also lead to different reliability issues. Other solutions could involve special dielectric formulations, but these are usually a trade-off for the dielectric constant and will affect the ultimate capacitance value available.

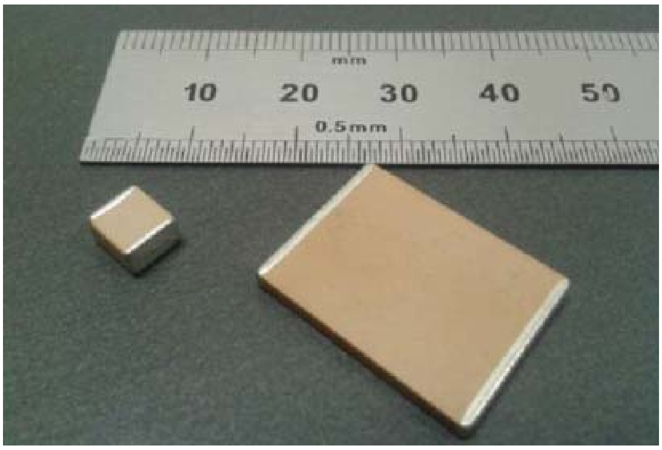
The Syfer Technology solution to the limitations imposed by electromechanical failure is to invent StackiCap™ - a single chip design to provide high CV in compact packages and offer the greatest volumetric efficiency and CV per unit mass of any high voltage X7R ceramic capacitor available.
After a series of trials and iterations this novel product and unique manufacturing process has a ground-breaking patent pending - GB Pat. App. 1210261.2.

Exploiting the manufacturing and process benefits of being a single unit, whilst allowing the capacitor to exhibit the electrical and physical behaviour of multiple, thinner, components, StackiCap™ employs an inbuilt stress relieving layer. This layer is made up of a combination of already utilised material systems and is formed during the standard manufacturing process. The layer is positioned in the place/s where mechanical stress is the greatest allowing for mechanical decoupling of the multiple component layers. At this time 2, 3 and 4 "stack" versions have been trialled (figures 3, 4 and 5).

StackiCap™ technology can also reduce board area significantly, even when replacing existing non-stacked alternatives. Often designers are restricted in the X-Y planes but not Z, so in extreme cases an 8060 size can be replaced with a single StackiCap™ 2220 (figures 6 and 7).



Top: Figure 6: StackiCap™2220 vs 3640 2 stack MLC.
Bottom: Figure 7:StackiCap™2220 vs 8060 MLC.



StackiCap™ capacitors are suitable for a wide range of applications

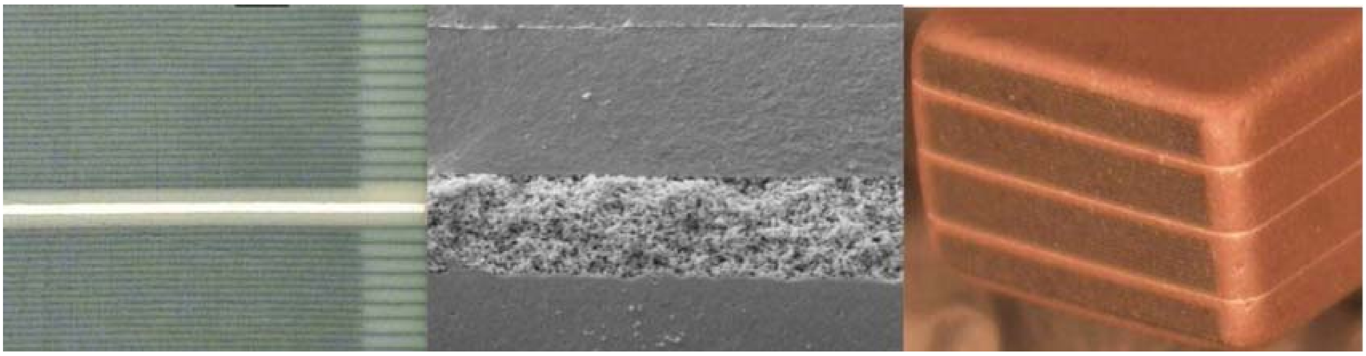


Figure 3: (left), 4: (centre) and 5: (right) showing stress relieving layer under Optical magnification, SEM Magnification and at macro level pre termination

As no lead frames are required, standard tape and reel packaging, with pick and place capability, is available. In addition Syfers' Flexi-Cap™ polymer flexible termination is included as standard. The potential benefits are significant. For example the space and weight saving for a 1kV 330nF stacked leaded component against the equivalent in StackiCap™ technology (2220 1kV) would be 0.56cc volume down to 0.12cc, a factor of 4.5 with weight of 3.2g down to 0.63g, a reduction factor of 5. In NASA terms this example this would give a $56 saving per component just in payload costs – and this type of component is often used a number of times in each application so the size, weight and resultant cost savings can mount up quite significantly.

such as switch mode power supplies for filtering, tank and snubber; DC-DC converter; DC block; voltage multipliers etc. and will provide huge benefits in applications where size and weight is critical. The range currently comprises case sizes 1812, 2220 and 3640 for commercially availability with case sizes 5550 and 8060 under development. This range is fully compliant with the RoHS Directive.

www.syfer.com

Quality Improvement of Reverse Recovery Characteristics

Measurement of High Voltage Thyristors for Series Connection Application

Nowadays high voltage thyristor stacks based on series connected assemblies are widely used in soft starters for high power motors and high voltage controlled rectifiers in industrial applications and transportation, in HVDC line converter units for the electric power industry. Thyristors in such series connected stacks have some special requirements, the most important of which is the possibility for all thyristors in stack to operate in simultaneity during switching-on and reverse recovery process.

By Vetrov I.Yu., Pallaev R.B., Poleschuk A.V., Presnyakov D.A., Stavtsev A.V., Surma A.M.

Development of a special equipment for testing of high voltage thyristors (and series connected assemblies) in the reverse recovery modes close to typical ones in operating hardware is quite relevant as well. Further, we describe such equipment used at Proton-Electrotex for testing of thyristors adapted for series connection.

System for precision measurement of reverse recovery characteristics of high voltage thyristors and series connected assemblies on their basis
The basic diagram of testing equipment power part is shown on Figure 1 and includes the following master units.

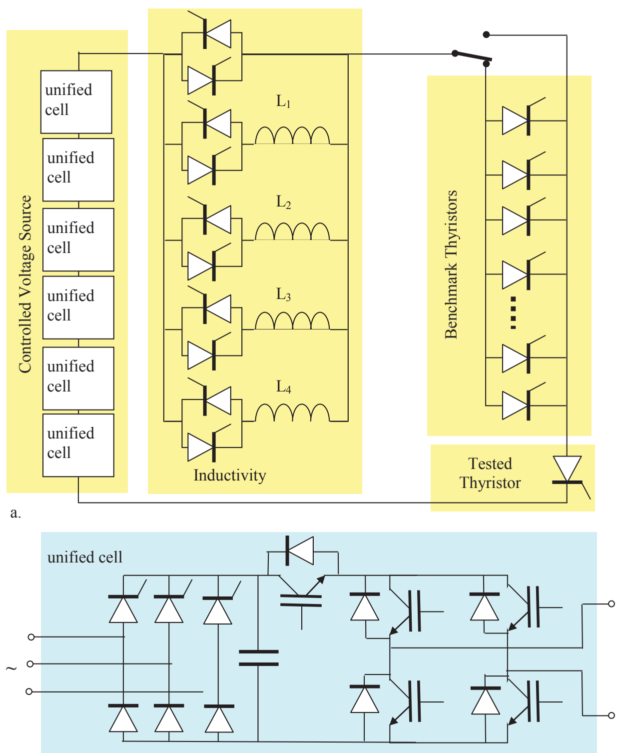


Figure1 a: Basic diagram of testing equipment power part
Figure1 b: Unified cell diagram of controlled voltage source

Controlled voltage source unit. The Unit contains a set of series connected consistent cells. An output voltage of each cell Vcell can be set in the range 0…500V with the 100V interval. When the unit is on, each cell can generate three voltage levels - «+Vcell»; «0»; «-Vcell», the voltage levels switch at a desired time.

Removable inductive coils unit. This unit enables to choose among five variants of a test loop inductance, which makes possible to vary the rate of anode current in wide range during switching-on and reverse recovery of the thyristor under test.

Reference thyristors unit. This unit, as shown below, ensures precise selecting of the tested thyristors in the groups with low spread of reverse recovery characteristics suited for mounting in series assemblies.

During the testing of separate high voltage thyristors or series connected couples as a part of the controlled voltage source, up to six cells are being switched on, which enables to run tests under conditions close to the nominal voltage and the maximum current load of thyristor. During the tests with high reverse voltage, the thyristors can be connected with damping RC circuits.

The unit can be used for thyristor stack testing with voltage in the range 6-10kV, for which quantity of cells in the controlled voltage source can be increased.

A Unit control system enables to generate five time intervals (phases) with controlled length, during each of those the voltage source cells are enabled with certain voltage level as it is shown on Figure 2. During the test of reverse recovery characteristics, the following phases are usually considered.

Phase 1: Increase of tested thyristor anode current with controlled rate of rise. Rate of rise depends on the total positive voltage of the controlled source cells and the selected inductive coil.
Phase 2: Maintenance of anode current on a desired level. The controlled source cells operate in the pulse-width modulation (PWM) mode which enables to maintain required anode current with a small oscillation against the given level.

Phase 3: Stabilization of anode current prior to reverse recovery process. The total voltage of source cells has low positive or zero value, that ensures the change of anode current with low speed to make precise level of anode current, which commences reverse recovery process.

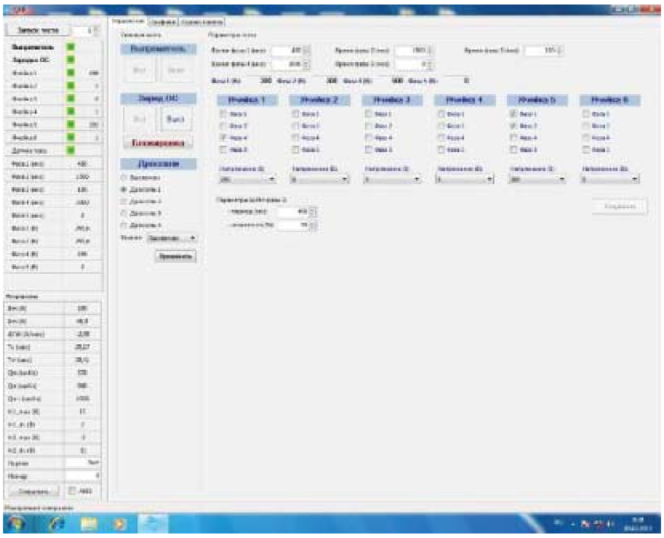


Figure 2: Control system window for testing mode selection

Phase 4: Reverse recovery process. The total voltage of source cells has negative value corresponding to given value VRDC for the tested thyristor. Controlled rate of anode current fall is defined by the given inductive coil.

Phase 5: Second applying of direct voltage with required peak value to the tested thyristor. This phase is handled to prove meeting the requirements for turn-off time (tq) standard of the tested thyristor.

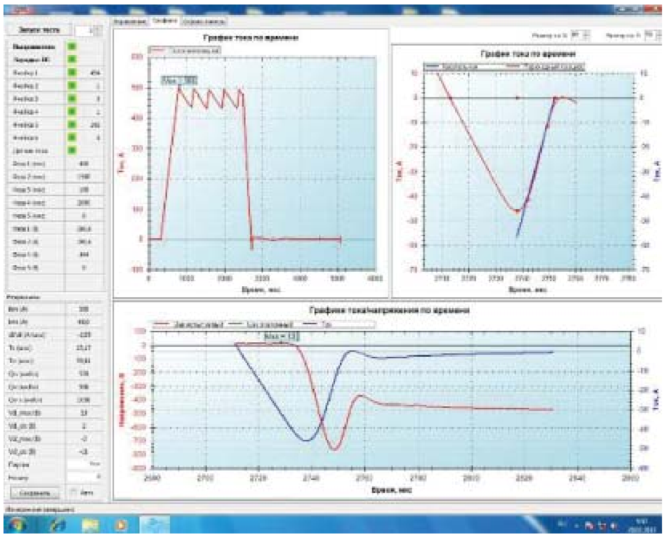


Figure 3: Data collection and processing system window

During the test, the computerized system collects and processes the sensor signals of thyristor anode current and voltage and displays waveforms of current and voltage along with numerical values of the main characteristics: reverse recovery time (trr) and its phases (ts и tf), reverse recovery surge current (IrrM), approximated (Qrra) and integrated (Qrri) reverse recovery charges (Figure3).

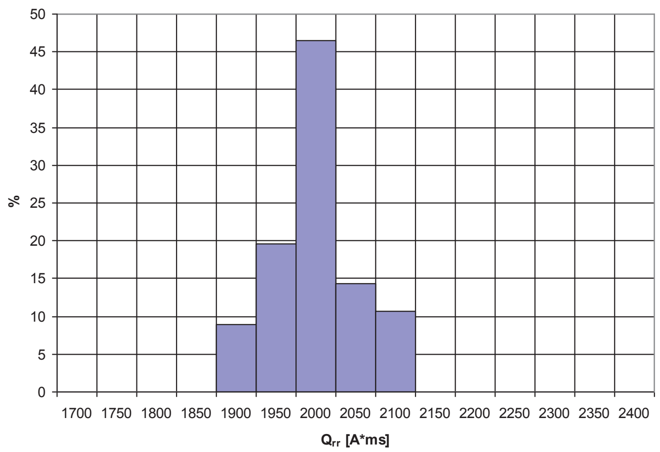


Figure 4a: Typical statistical distribution of reverse recovery charge in lots of high voltage thyristors (as example thyristor T273-1250 -44 with average current 1250 A, voltage 4400 V)

The typical statistical distribution of reverse recovery charge for high voltage thyristors adapted for series connection is shown on Figure 4a. RMS deviation value Qrr normalized to the mean equals about 2.5% in big lots of such thyristors. Herewith the contribution of measurement accuracy and actual variation of Qrr in measured value defined by controllability of technological process is approximately the same.

It is possible to avoid the impact of measurement error and organize more precise group selection for series connected assemblies by parallel testing with reference thyristors. This method is based on high sensitivity of anode voltage distribution in the reverse recovery process of couple series connected thyristors to the difference of Qrr values for these devices. Thus, typical dependence of maximum pulse voltage VrrM variation, which occurs during the reverse recovery of couple series connected thyristors as a result of difference in the reverse recovery charges is shown on Figure 4b. It is clear that in the case of low values of reverse recovery charge difference this dependence is close to linear. This enables, using reference thyristors with

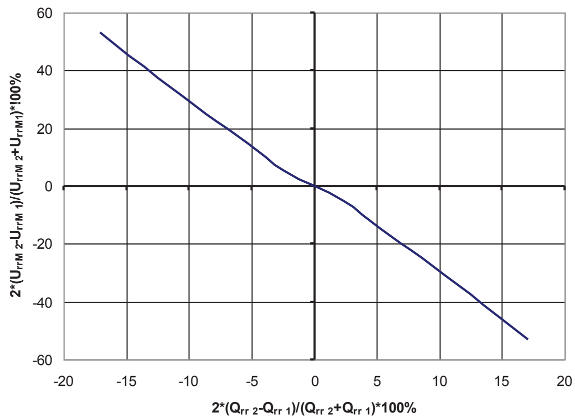


Figure 4b : Typical dependence of maximum pulse voltage VrrM variation during reverse recovery of the couple series connected thyristors as a result of difference in reverse recovery charges.

Qrr values gradually increasing by 2-3%, to group the tested thyristors by this characteristic with precision higher than 0.5%. Such grouping precision enables to obtain simultaneous reverse recovery of the thyristors in series connected assemblies even without snubber RC circuits. As an example, recovery of the couple of high voltage thyristors T653-630-65 (average current 630A, voltage 6500V) is shown on Figure 5.

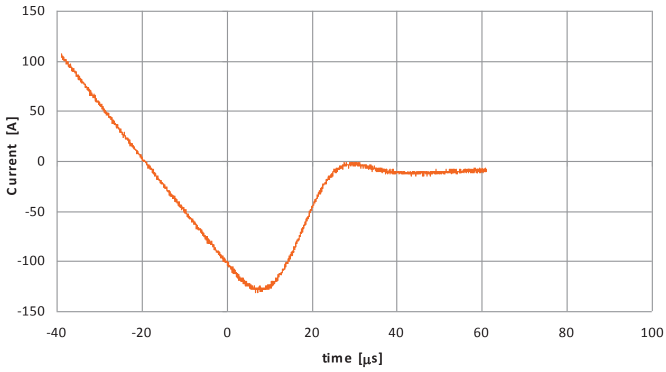


Figure 5a: Simultaneous reverse recovery of the couple series connected high voltage thyristors anode current waveform

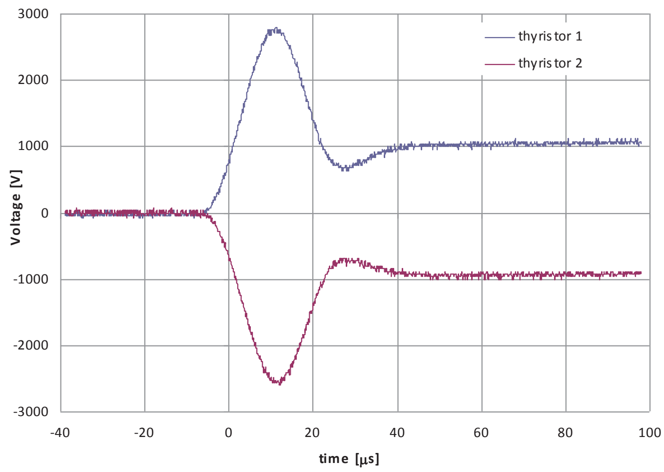


Figure 5b: Simultaneous reverse recovery of the couple series connected high voltage thyristors anode voltage waveform

Conclusion

Application of measurement equipment complex described above in production of high voltage thyristors adapted for series connection enables to improve quality and reliability of high voltage thyristor switches based on series assemblies for power electronics in industrial applications, transportation and the electric power industry.

www.proton-electrotex.com

Line Filter – The Last Barrier in the Switch Mode Power Supply

Switch mode power supplies result in conducted interference because they generate radio interference voltage on the mains side. This can interfere with other equipment supplied with mains power. Line filters help to suppress the generated radio interference voltage. These can easily be designed from passive components such as current-compensated line chokes and X / Y capacitors. This article concerns the design of a single-phase line filter.

By Stefan Klein, Application Engineer, Technical Marketing, Würth Elektronik eiSos

Parasitic currents at the switch mode power supply input

Parasitic currents result in radio interference voltage via impedances. Figure 1 shows the main current flow of parasitic currents in a switch mode power supply.

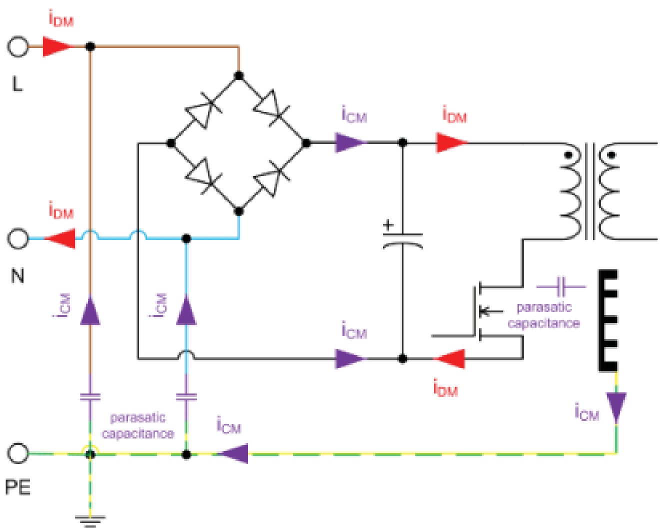


Figure 1: Parasitic currents at the switch mode power supply input

Initially, a high frequency active current „iDM“ flows on the mains side with the pulse frequency of the switching regulator which results in differential mode interference. Caused by fast switching processes of semiconductor components, usually MOSFETs, high frequency oscillations occur in combination with parasitic effects. In principle, the differential mode current flows from the mains power line „L“ over a rectifier bridge, then over the primary winding of the isolating transformer, over the MOSFET and over the neutral conductor „N“ back to the mains. The MOSFET is mounted on a heat sink for the cooling. In turn, this is connected to the protective earth conductor „PE“. Capacitive coupling between the heat sink and the drain of the MOSFET occurs here and produces common mode interference. A capacitively coupled common mode current „iCM“ now flows over the earth line „PE“ back to the switch mode power supply input where it is coupled again via parasitic capacitance both on the mains power line „L“ as well as on the neutral line „N“. The common mode current „iCM“ now flows as shown in Figure 1 over both mains power lines, via the rectifier bridge to the MOSFET, where it is again parasitically coupled via the heat sink to the earth line „PE“.

Expected interference spectrum

The rectified mains voltage is applied at the drain-source section. The peak level of the rectified mains voltage corresponds to:

$$V_{\mathrm{p}} = 230\mathrm{V} \cdot \sqrt{2} = 325\mathrm{V} \qquad \text{(E-1)}$$

A switch mode power supply with pulse frequency of 100 kHz has been used as an example. For this pulse frequency, the timing signal corresponds to „T“ 10 µs. The pulse duration is 2 µs. Based on this, the duty cycle can first be determined:

$$V = \frac{t_{\mathrm{on}}}{T} = \frac{2\mu\mathrm{s}}{10\mu\mathrm{s}} = 2{,}5 \qquad \text{(E-2)}$$

Assuming that the current through the rectifier bridge is trapezoidal, the EMC spectrum without line filter and without further Fourier transformation can be approximately determined. The first break point of the envelope of the spectrum is needed first:

$$n_{\mathrm{co1}} = \frac{1}{\pi \cdot D} = \frac{1}{\pi \cdot 0{,}2} = 3{,}\!; \sqrt{5} \qquad \text{(E-3)}$$

The first corner-over frequency of the envelope of the spectrum enclosing amplitude density is analogous to this:

$$f_{\mathrm{co1}} = n_{\mathrm{co1}} \cdot f_{CLK} = 1{,}592 \cdot 100\mathrm{kHz} = 159{,}2\mathrm{kHz} \qquad \text{(E-4)}$$

The first harmonic amplitude can be determined from this:

$$c_n = \frac{29K_p}{n_{co1}9\pi} = \frac{29125\mathrm{V}}{n592\pi} = 020\mathrm{H} \qquad \text{(E-5)}$$

Based on the assumption that the parasitic coupling capacitance „CP“ between the switch mode power supply and ground is 20pF, the first harmonic common mode current can now be determined:

$$I_{\mathrm{cm1}} \; o \; \frac{f\,\mathrm{o}5C_{1\mathrm{o}n}5C_{\mathrm{p}}5c_n}{=(2c\,\mathrm{o}5C_{1\mathrm{o}n}5C_{\mathrm{p}})^{\pi}+1} \; o \; \frac{f\,L\,5125{,}f\,\mathrm{kHz}5f\,c\,\mathrm{pF}51nc\,\mathrm{V}}{p(2c\,L\,5125{,}f\,\mathrm{kHz}5f\,c\,\mathrm{pF})^{\pi}+1} \; o \; 0{,}2\mathrm{mA}$$

(E-6)

The radio interference voltage is measured using mains simulation and an EMC test receiver. Due to the parallel connection of the 50 Ω input impedance of the EMC test receiver and the 50 Ω output impedance of the mains simulation, total impedance „Z“ of 25 Ω is produced. The measured radio interference voltage „Vcm“ can now be calculated:

$$c_{\mathrm{cm}} = 1 \cdot I_{\mathrm{cm1}} = 25\,\Omega \cdot 2{,}I\,,\;\; \mathrm{A} = 0{,}0I\,5\mathrm{V} \qquad \text{(E-7)}$$

Converted to dBµV, this gives:

$$c_{(\mathrm{pc\,\mu m})} = 20 \cdot \mathrm{lom}\left(\frac{2{,}2\mathrm{F9m}}{1\mathrm{\mu m}}\right) = 9I{,}2I\ \mathrm{dB0V} \qquad \text{(E-8)}$$

The result of the calculation is that high conducted emission can be expected. For example, the product family standard EN 55022 can be used here for assessment of the interference emission. In the frequency range of 0.15 MHz to 0.5 MHz, it defines a permissible interference level of 66 dBµV to 56 dBµV of the quasi peak. Figure 2 shows the result of the measurement of the conducted radio interference voltage of this switch mode power supply without line filter.

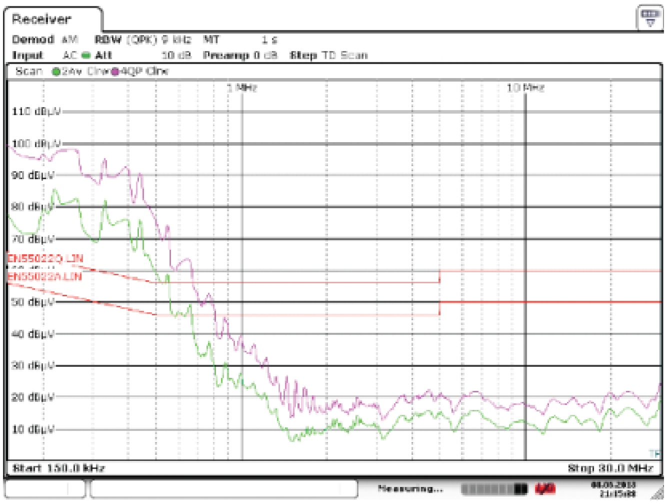


Figure 2: Radio interference voltage of a switch mode power supply without line filter

The measurement shows that a line filter is absolutely essential.

Design of a line filter

Figure 3 shows the schematic design of a simple single-phase line filter. Würth Elektronik provides various models of line chokes, such as the WE-CMB series, for the construction of line filters. A line choke basically consists of a MnZn ring core on which there are two geometrically separated windings wound in opposite directions. Figure 4 shows the design of the WE-CMB. In this case, the WE-CMB acts like a filter coil which counteracts the current and reduces its amplitude. A common mode choke with as low as possible SRF in the lowest frequency range should be used because the switch mode power supply used here switches with very low pulse frequency. Low SRF causes high attenuation in the lower frequency range.

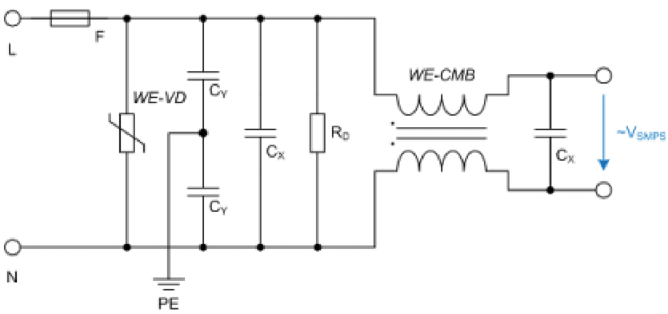


Figure 3: Single-phase line filter

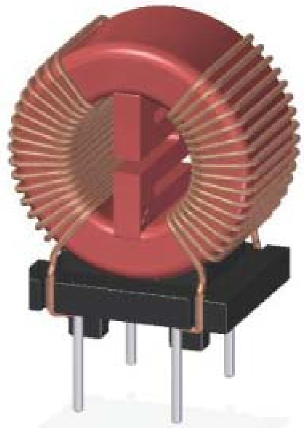


Figure 4: Design of the WE-CMB

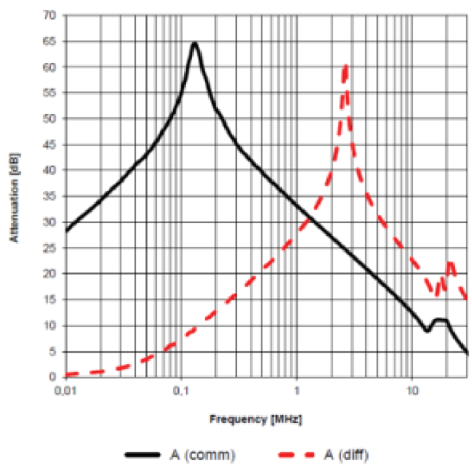


Figure 5: Attenuation of the WE-CMB XS 39 mH

A suitable WE-CMB of the XS design of 39 mH has been selected for this. Figure 5 shows the characteristic curve of its attenuation in the 50 Ω system.

A distinction is always made in the attenuation between the common mode (black line) and differential mode (red, dashed line) suppression. In common mode operation, the WE-CMB line choke reaches its maximum attenuation at 150 kHz. However, the attenuation drops with increasing frequency. Other X / Y capacitors are required because the line filter should suppress interference up to 30 MHz. An X capacitor is placed both before as well as after the line filter to block differential mode interference from the mains side and the switch mode power supply. With its leakage inductance, the WE-CMB in combination with the X capacitor forms a low pass filter which reduces the differential mode interference and subsequent common mode interference. Two X capacitors with a value of 330 nF have been selected here as an example. Their SRF is approx. 2 MHz.

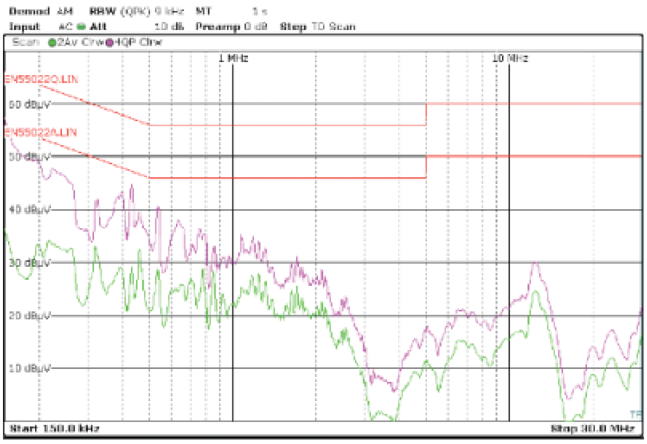


Figure 6: Radio interference voltage with line filter

For safety reasons, a resistor must be placed on the mains side in parallel with the X capacitor to discharge the capacitor if the switch mode power supply is disconnected from the mains. A varistor should also be placed before the line filter so that transient overvoltages from the mains are short-circuited. Würth Elektronik disk varistors from the WE-VD series are ideally suitable for this. Overload protection must also not be missing. This should always be placed before the varistor. The protection trips in the case of a short-circuit by the varistor. Y capacitors are required for further suppression of the common mode interference. In combination with the WE-CMB, they form a corner frequency „f0" which is defined by the „Thomson" oscillation equation:

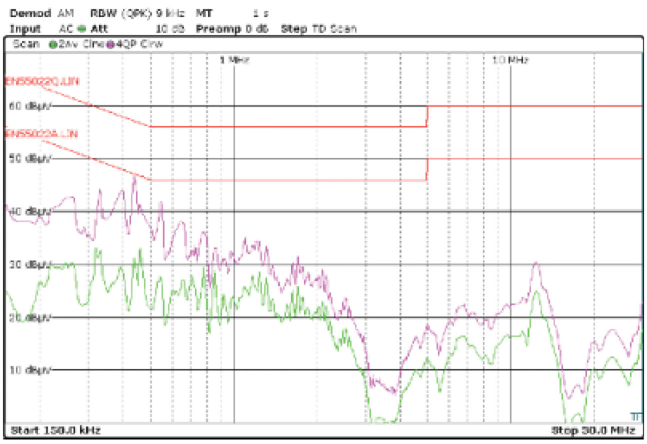


Figure 7: Radio interference voltage with optimised line filter

$$f_0 = \frac{1}{2\pi\sqrt{L*C}} \qquad \text{(E-9)}$$

Attenuation of 40 dB is required to achieve below the permissible interference level of 66 dBµV (at 150 kHz). This corresponds to a decade in the logarithmic representation. One tenth of the pulse frequency is used as factor for the corner frequency or further calculation of the Y capacitors. The oscillation equation is now converted and used to determine the X capacitance:

$$0_Y = \frac{1}{(2\pi f\frac{f_{CLK}}{10})^2 f L_{CMC}} = \frac{1}{(2\pi f\frac{100\text{kHz}}{10})^2 \cdot 39\text{mH}} = *,\sqrt{}\text{pF} \qquad \text{(E-10)}$$

As two Y capacitors are needed, the calculated value is divided by two. Y capacitors conduct common mode interference from the switch mode power supply back to the protective earth. As, depending on the device type, only leakage currents of 0.25 mA to ≤ 3,5 mA are permissible, no capacitance with a value greater than 4.7 nF should be used. Two Y capacitors with an E 12 value of 2.2 nF have been selected for this reason. Figure 6 shows the result of the measurement with this line filter.

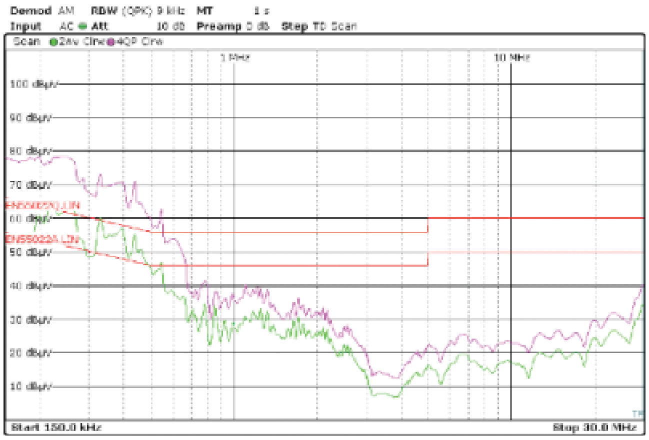


Figure 8: Radio interference voltage with line filter without WE-CMB

The EMC test of the radio interference voltage is passed with filter. The smallest signal to interference ratio of 10 dB of the quasi peak is present at the lowest frequency of 150 kHz. Quasi peak and average peak are far below the permissible interference level in the other frequency range.

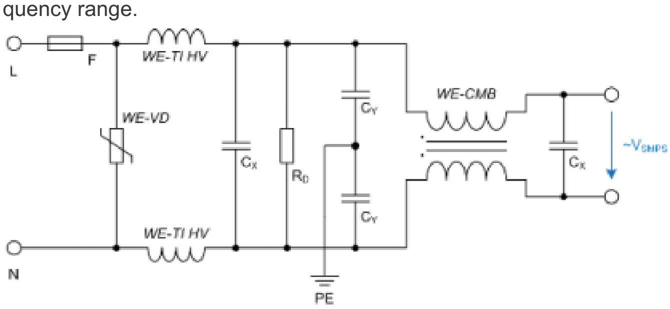


Figure 9: Line filter with WE-CMB and WE-TI HV

Optimisation of the line filter

It is also possible to further increase the signal to interference ratio in the lower frequency range. Two X capacitors with 330 nf are replaced with two 1.5 1,5 µF X capacitors for this. Figure 7 shows the measurement of the optimised line filter.

The change of the capacitance causes a reduction of the radio interference voltage of approx. 15 dB in the lower frequency range. A greater signal to interference ratio has been achieved and a good line filter designed.

Error due to dispensing with line choke

It is often tried at the beginning to only use X and Y capacitors to suppress interference in order to dispense with a common mode choke. However this is contrary to the principle of the line filter of counteracting the interference current by adding a high-impedance filter element. The radio interference voltage using the same filter without common mode choke has been measured as an experiment. Figure 8 shows the measurement.

As expected, the interference emission in the lower frequency range increases strongly without the WE-CMB line choke. At 200 kHz, the quasi peak shows a value of approx.78 dBµV and the average peak shows a value of 60 dBµV. The permissible interference level is exceeded up to 600 kHz both by the quasi peak as well as by the average peak. A line filter without line choke is inadequate!

Additional differential mode filter

If the differential mode suppression using the WE-CMB and the X capacitors is not sufficient, an additional differential mode filter consisting of two coils connected in series helps. Figure 9 shows the design.

The Würth Elektronik coils WE-TI HV and WE-PD2 HV or the WE-SD series are ideally suitable for the differential mode suppression. The WE-UKW series is recommended in the case of high frequency interference. The „Thomson“ oscillation equation can be used again here to calculate the coils. If attenuation of 40 dB / decade would be required from each coil, the calculation should be made with a corner frequency of one tenth of the pulse frequency.

The already used X value of the X capacitors can be used for the calculation of the coil:

$$L_{\mathrm{DM}} = \frac{1}{\left(2\pi\cdot\frac{f_{\mathrm{CLK}}}{10}\right)^2\cdot C_{\mathrm{X}}} = \frac{1}{\left(2\pi\cdot\frac{100\mathrm{kHz}}{10}\right)^2\cdot 330\mathrm{nF}} = 767\ \mu\mathrm{H} \qquad \text{(E-11)}$$

As the coils for the differential mode current are in series, the calculated value is divided by two. The next larger inductance value of a WE-TI HV would be 470 µH. It should be ensured for the selection of a differential mode coil that its rated current „IR“ is far above the rated current of the switch mode power supply input.

Result of the line filter

In conclusion, a line filter for switch mode power supplies without a common mode choke is not sufficient. Individual capacitors are not sufficient to completely suppress the interference emission. Additional longitudinal coils before the line filter help if further suppression of the differential mode interference is required. Using a line filter, all interference levels are below the permissible limit value and the switch mode power supply can pass an EMC test.

Literature

Würth Elektronik eiSos GmbH & Co. KG „Trilogy of Inductors“, Application manual for EMC filters, pulsed power supplies and HF circuits, 4th extended and revised edition, Dr. Thomas Brander, Alexander Gerfer, Bernhard Rall, Heinz Zenkner

www.we-online.de

Extending the MOSFET Gate Drive Conductors

Using a Dual Stripline PCB Layout Configuration

In many applications there will be a need to place one or more rails in a Power XR application at some distance from the controller. This article will introduce and examine from both a theoretical and practical standpoint a layout design technique that will allow the MOSFETs to be as much as 5 inches from the driver.

By Ron Berthiaume, Exar

The Exar XRP77XX series family integrates internal gate drivers for all 4 PWM channels. These drivers are optimized to drive both high-side and low side MOSFETs for synchronous rectification operation.

Normally these drivers are required to be close to the MOSFETs they are driving due to their high current and high speed rise and fall times.

THEORY

When the MOSFETs are moved away from the driver (more than 1 inch) the parasitic capacitance and inductance of the layout can become dominate resulting in inadequate performance of the power system. In order to eliminate these parasitic issues, this article describes a layout approach that allows the power stage to be as much as 5 inches from the driver and still work as expected. The basis of the operating theory is that the drive to the MOSFETs is a pulse of current and that if one views the drive conductors as a pulse transmission line with a capacitive termination (gate and Miller capacitance) then the parasitics can be minimized.

A Dual Stripline (also called a broadside coupled stripline) was chosen in order to have the magnetic field produced from the current pulse that charges and discharges the MOSFET capacitance be cancelled by the proximity effect of the opposing currents. This lowers the trace inductance of the Dual Stripline. In addition radiated noise is lowered since the gate traces are enclosed by the ground plane.

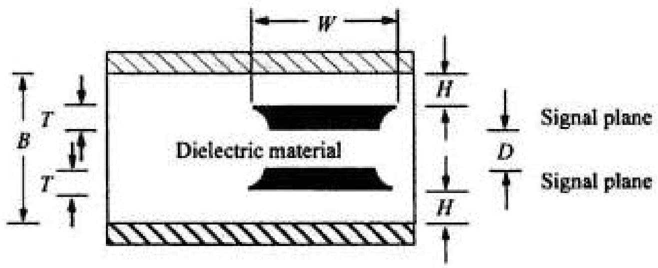


Figure 1a: Dual Stripline Configuration (Cross Section View)

Figure 1a shows a Dual Stripline transmission line design that has been created to match the drive capability of a 3 ohm drive stage similar to what is in an XRP7714. In the four layers shown in Figure 1a, the top and bottom (cross hatched area) conductors are a power plane or ground, but from an AC perspective both can be considered ground. The two inner conductors on the signal planes are the gate and source leads to the MOSFET. These signals come from the internal driver of the XRP77XX.

IMPLEMENTATION

Here are some basic guidelines for the design of a Dual Stripline as shown in Figure1a
Close traces, the "D" dimension lowers the intrinsic inductance, Lo.
Increasing the trace width, W will decrease Lo.
Increasing copper thickness, T will increase Lo.
Increasing length will not change Zo but will increase the amount of parasitic capacitance and inductance that the driver will see. This will add to the losses in the driver.

Designs can accommodate some discontinuities (e.g. vias, unequal traces) to allow for getting a layout routed. These runs are not as critical as many digital signals.

The capacitance is affected by the distance to the ground plane, H and thickness of the trace, T. The thinner the dielectric, the higher is the capacitance. Also the higher the PCB dielectric constant (K) the greater is the capacitance.

TESTING

Tests were done on a printed circuit board (PCB) using Exar's XRP7714 digital controller.
The Figure 1b is a block diagram of the XRP7714 and MOSFET connections using the Dual Stripline configuration.

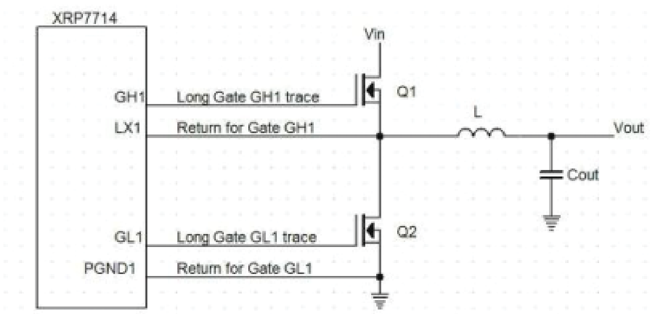


Figure 1b: Block diagram of the XRP7714 and MOSFET connections using the Dual Stripline configuration

From a PCB layout viewpoint, each return etch should follow under the gate drive etch on an adjacent signal layer. For the high side MOSFET gate drive (GH1 and LX1) this should be easier to implement. However, for the low side gate drive (GL1 and PGND1) care must be taken to ensure that PGND is not connected in multiple places, which could reduce the benefit of a Dual Stripline configuration.

The two Figures below show the internal Layer 3 layout (Figure 2) and internal Layer 4 layout (Figure 3) of an XRP7714 PCB layout that uses the Dual Stripline configuration as discussed above.

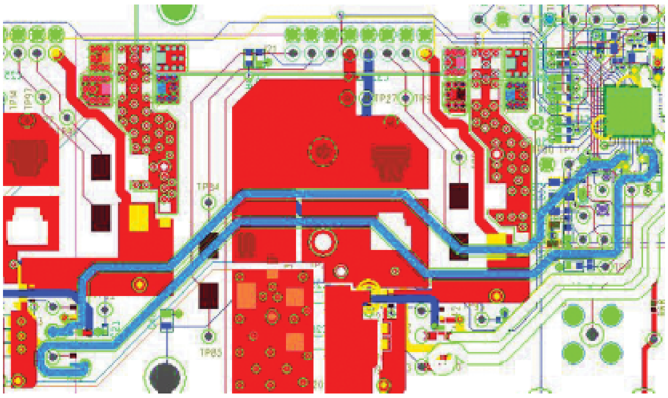


Figure 2: Gate conductors shown in Blue on Layer 3

Figure 3: PGND an LX Return conductors shown in Blue on Layer 4

TEST RESULTS

To verify that the Dual Stripline configuration is performing as intended, three separate tests were conducted. The voltage waveform at the phase node (LX) was measured with a 250 MHz bandwidth oscilloscope and with differential probes directly at the pins of the MOSFETs. In these tests, the input voltage was 12 VDC and the output voltage was 3.3 V with a 12 Amp load.

Test 1 used a DrMOS type power stage so that the gate driver is optimized for the MOSFET while the parasitic inductance and capacitance are minimized since all of the devices are on the same silicon. The DrMOS has an internal driver so that the trace length from the controller to the FETs is not a factor.
Test 2 used discrete MOSFETs being driven by the XRP7714 drivers with a short distance between the XRP7714 pins and the MOSFET gate pins.
Test 3 used the Dual Stripline configuration with the PCB layout shown in Figure 2 and Figure 3 with a distance of 5 inches between the XRP7714 pins and the MOSFET gate pins.

				Ringing	
Test	**Configuration**	**Rise time**	**Fall Time**	**Overshoot**	**Duration**
		(ns)	**(ns)**	**(%)**	**(ns)**
Test 1	DrMOS	5	4	45	40
Test 2	Discrete FET; short distance	6	5	100	50
Test 3	Discrete FET; 5" distance	6	5	100	50

Table 1 Summary of the Test Results

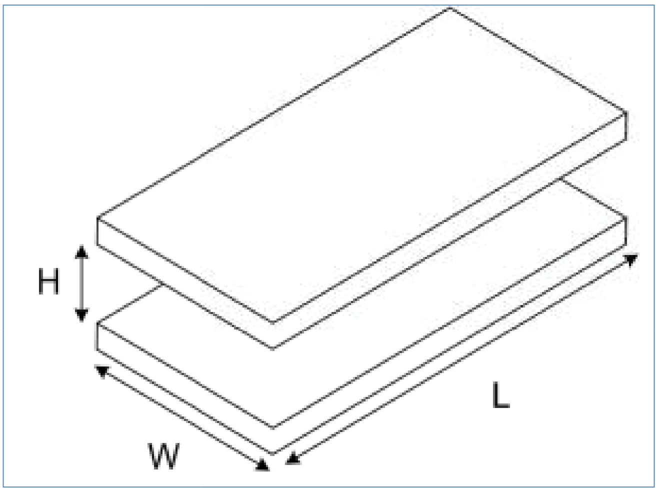
The reduced ringing in Test 1 with the DrMOS is attributable to the lower parasitics associated with close coupling of the gate drivers and power MOSFETs.

When comparing the results from tests 2 and 3, it can be seen that phase node performance has not been degraded at all by using the longer gate drive traces. Furthermore, it is evident that this technique even compares reasonably well to the optimal integrated drivers on the DrMOS set up.

Lastly, measurements were also made of the gate drive signals for the Dual Stripline configuration to verify that the distance hasn't prevented the gate driver from exerting proper control over the gate at the point of phase node current commutation. Measurements also showed that the low side gate remains considerably lower than 1.8V when both the high to low and low to high transitions of the phase node occur, ensuring cross conduction cannot occur.

Conclusion

Correct layout is always a vital part of any good switch mode converter design. Experience dictates that adding additional distance between the gate drivers and power MOSFETs in such a design would be a violation of typical design principles. However, this article has shown that when attention is paid to the traces between gate drivers and the FETs, and a few simple Dual Stripline guidelines adhered to, a distance of up to 5" is achievable with virtually no impact on the overall performance of the converter. This in turn allows designers to take full advantage of the higher level of integration offered by the XRP77xx series of programmable multi-channel controllers without having to sacrifice the geographic flexibility afforded by individual POL solutions.



Where:
H = Dielectric thickness between the signal planes
d = Dielectric thickness between the signal planes
W = Width of the trace
T = Thickness of the trace
Zo = Characteristic impedance (Ω)
Co = Intrinsic capacitance of the trace (pF/unit distance)
Lo = Intrinsic inductance of the trace (nH/unit distance)
K = Dielectric constant of PCB material

Figure 4: Broad Side Trace Configuration

A brief discussion on impedance, capacitance and inductive calculations

An industry accepted formula for the characteristic impedance (Zo) and capacitance (Co) of a Broad Side Trace configuration is shown below. The formulas don't take into account the affect of the outside ground planes. Their affect will further decrease the inductance so they will be beneficial, and the calculated inductance could be thought of as the worst case. This formula is an approximation based on simplifying assumptions as shown and should be used with the understanding that this is only valid over a range of values, and should be used as guidelines as none will give exact results. There are textbook and Web-based impedance calculators available online that do not consider the valid range of parameters, so user beware!

$$L_{trace-pair} \approx \frac{\mu_0 \mu_r h}{w}$$

It is interesting to note that almost all multilayer PCB with ground planes and power planes will introduce a stripline configuration since the signal trace is usually between two ground planes. The unique attribute of the Broad Side Trace and Dual Stripline is that the signal trace and its associated current return trace should be above and below each other as the trace makes its way across the PCB.

$\mu_{o=}$	3.192E-08	H/Inch
μ_r	1	-
W	40	mils
H	6.4	mils
K	1	-
L	5.11	nH/in
C	1.73	pF/in
Zo	54.29	

Table2: Design Example

$$C = 0.0882 \cdot K \cdot \frac{W}{d}\left(1 + \frac{d}{\pi \cdot W}\left(1 + 2.3 \cdot \log\left(\frac{2 \cdot \pi \cdot W}{d}\right)\right)\right) \ in \ \frac{pF}{cm}$$

$$Zo = \sqrt{Lo * Co}$$

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Metallized Film Capacitors

Considerations for selecting the most suitable types

The expected life cycles of electronic products are continuously increasing, so that today life cycles of up to 10, 15 or 20 years are expected. Of course, each electronic component used in such a product should have at least the same lifetime-expectancy.

By Dieter Burger, Managing Director dbTec electronics GmbH the European sales-office of HJC, Taiwan

In power electronics, metallized film capacitors are being used on the AC-side in EMI-filter or AC-filter applications, e.g. as X2- or Y2- noise suppression capacitors.
On the DC-side, film capacitors are being used e.g. as Pulse-, Snubber-, PFC- and DC-link capacitors.
This article discusses the main stress factors for the life of metallized film capacitors, and the aspects which must be considered to select the most suitable types.

Important considerations for the selection
Depending on the application, the right capacitance-value, voltage withstanding characteristics and current carrying capability must be considered.
There are applications with relatively high ripple-currents, e.g. for X2-capacitors in an AC-filter of a PV-inverter, or for DC-link capacitors.

Rationale:
Assuming a constant frequency f and capacitance C, the increase of tan δ (loss factor) in a metallized film capacitor is caused by an increase of the ESR (equivalent series resistance):
$\tan\delta = ESR \times 2\pi f \times C$

Not only can an unspecified loss of capacitance have fatal consequences in the application. It is also important to keep the tan δ (ESR) within an acceptable change during the life cycle to limit the power loss and the temperature-rise of the film capacitor.

Temperature increase of the capacitor (ΔT):
$\Delta T = P/G$
$\Delta T = T_{housing} - T_{ambient}$
Increase in the housing temperature of the capacitor (°C), maximum 15°C above rated temperature
$P = I_{rms}^2 \times ESR$
Power loss of the film capacitor (mW)
G = Thermal conductivity (mW/°C)

The capacitor's permissible ripple current I_{rms} and its thermal conductivity G must be specified by the capacitor-manufacturer.
Following these formulas, the power loss P and the temperature-increase of the capacitor raise by the same factor by which the ESR increases. Therefore, an uncontrolled or unknown increase of the ESR during the life cycle can't be accepted.
Considering the specified maximum increase of the ESR (tan δ) during the life cycle, the circuit ripple current Irms must be reduced, so that by limiting the power loss, the temperature-increase of the capacitor is limited accordingly.

Regarding the allowed temperature-increase, it must be considered that the internal temperature in the hottest point inside the capacitor (hotspot) is about Tamb + 1.5 to 2 times the ΔT between the housing and the ambient. If the ambient temperature is below 70°C, generally a 15°C temperature increase is acceptable.

The temperature increase of a film capacitor is:
a) proportional to the power loss
b) which is proportional to the tangent delta and to the square of the current.

Consequently if e.g. a doubling of the tangent delta is specified during the lifetime, then the ripple current through the capacitor must be reduced by √2 to maintain the initial power loss. If an increase of the tangent delta is specified by times 5 during the lifetime, the ripple current must be reduced by square root of 5 to maintain the initial power loss.
The above considerations underline that it is essential for a design engineer to know the maximum change of the ESR during the life cycle of his product.

End of Life of a film capacitor
The following end of life criteria are proposed for film capacitors in power electronics:
$\Delta C/C \leq 10\%$
$\Delta \tan\delta / \tan\delta$ (at 1kHz and 10kHz): ≤ 200%

The end of life is defined as the point in time from which onwards the capacitor does not fulfil its initial specified values.

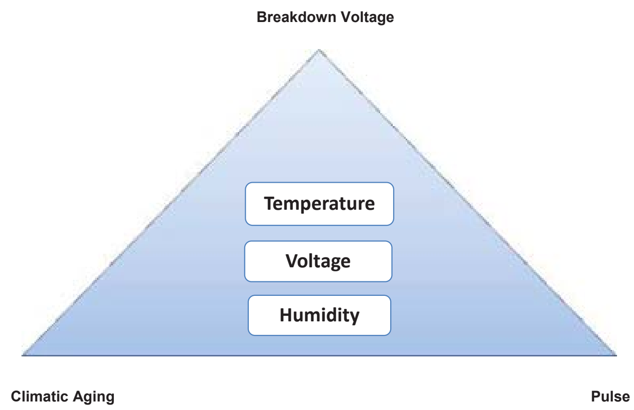


Figure 1: Determining factors for the life of a metallized film capacitor

Which facts contribute to an increase of the ESR during the life cycle?
The increase of the ESR expresses the aging of a metallized film capacitor. This is fundamentally determined by the aging of the dielectric, the electrodes and the endspray contacts. The speed of this aging process is accelerated by temperature, voltage and humidity.

Reasons for a capacitance-loss
- Self-healing effects
- Reduction of the electrode metallization by corona-discharges or by humidity-corrosion.

Figure 2: Film metallization with significant humidity-corrosion

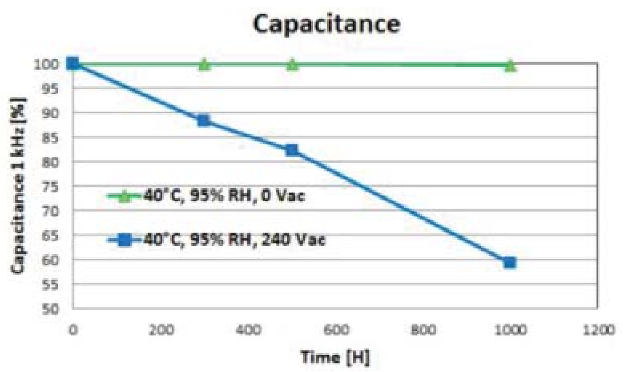


Figure 3: Mean values of the capacitance-loss over the time from HJC's standard X2-capacitors which fulfill the current IEC 60384-14.

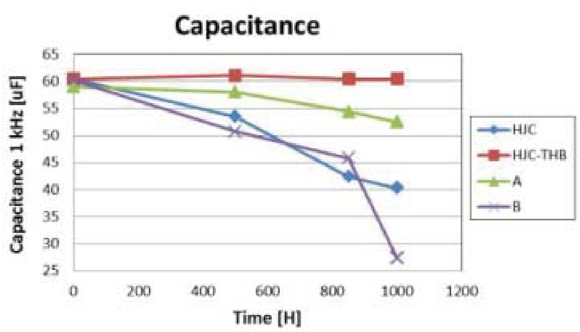


Figure 4: Capacitance loss during a test with 85°C, 85% RH and 700VDC for 4 DC-link capacitors with 60µF/70Vdc (HJC = HJC standard version EPB606K700VDC, HJC-THB = HJC humidity-robust version THB-EPB606K700VDC, A and B = corresponding standard version of competitors.

Reasons for an increase in tan δ (ESR):
- Aging of the dielectric.
- Reduction of the metallization by corona-discharges or humidity-corrosion.
- Humidity corrosion in the endspray-contacts.
- Break of the endspray-contacts due to excessive stress (heat) from pulse-currents caused by dU/dt's.

Prove for the sensitivity of metallized film capacitors for humidity:
Due to market pressure for miniaturization and cost-savings, film capacitors are being produced with increasingly thinner dielectric films and metallization layers. The result of this tendency is greater sensitivity of the capacitors to environmental conditions.

However, most specifications of metallized film capacitors don't take into account the sensitivity of film capacitors for the simultaneous stress by voltage and humidity. The same is true for the current IEC standard for AC- and DC- metallized film capacitors:

Current IEC standard regarding the humidity resistance:

X- and Y- capacitors:
IEC 60384-14 4.12 (Damp heat)
→ 40°C, 90-95% humidity, 21 or 56 days (→ without voltage!)

DC capacitors:
IEC 60068-2-78 (Test Ca, Damp heat)
→ 40°C, ~ 95% air humidity, 21 or 56 days (→ without voltage!)

As both tests are without voltage, it just can be considered as storage tests.

Current IEC standard regarding the endurance-performance:

X- and Y- capacitors:
IEC 60384-14 4.14 (Endurance):
→ 1.25 U_{rated} (X-capacitors) or 1.7 U_{rated} (Y-capacitors) at upper category temperature for 1000 hours (through a 47ohm resistor), once every hours increase to 1.5 Urated for 0.1seconds. (→ without humidity!)

DC capacitors:

IEC 61071 Capacitors for power electronics – 5.15 (Endurance Test): "The purpose of the endurance test is to demonstrate the performance of the capacitor under the conditions which will actually occur in service."

→ Same as for X- and Y- film capacitors, to verify the endurance performance the standard IEC 61071 just refers to simultaneous stress by temperature and voltage, but without humidity!

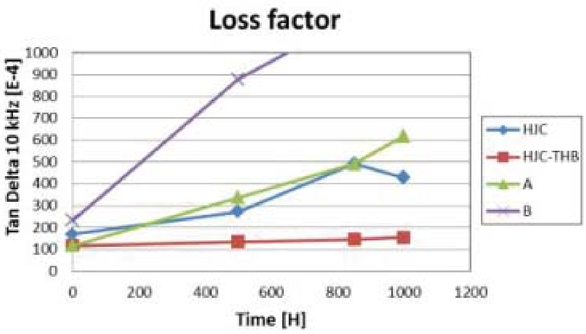


Figure 5: Mean values of the loss factor increase at 10 kHz of the same types in the same test

However, it can be easily verified that humidity in combination with voltage leads to an accelerated capacitance-loss and increase of tan δ (ESR):

The test-result show that conventional X2-capacitors can pass the test 4.2 (damp heat test) from the latest issue of the standard IEC 60384-14 with excellent results (green curve). However, the same capacitors may exceed their specified capacitance-values already after about 250 hours (blue curve), if in addition to the temperature of 40°C and humidity of 95% there will be also applied the mains-voltage.

The chemical process of humidity-corrosion in the metallization occurs faster when humidity and voltage are present at the same time. This is true for both, AC- and DC- film capacitors.

The curves in Figure 4 and 5 demonstrate the need to verify the capacitor's robustness when temperature, voltage and humidity are applied simultaneously. Humidity can enter a film capacitor either during its production-process or later in the application due to an untight packaging (box and potting).

Accelerated lifetime-test:

Whether a sufficiently robust film capacitor has been selected can be verified by using an accelerated life cycle test with the following parameters:

- 85°C, 85% humidity, nominal voltage U_N, 1000 hours.

Whereby the following criteria apply:

$\Delta C/C \leq 10\%$

$\Delta \tan\delta/\tan\delta \leq 200\%$ at 1 kHz, and at 10 kHz or 100 kHz.

This test is called either THB-test (Temperature, Humidity, Bias) or "85/85-test with voltage".

Next to the verification of the humidity-robust construction of the film capacitor, it is essential to verify if its failure-mode shows a Fail-safe characteristics.

Conclusion:

Metallized film capacitors stand out from other capacitor types due to their numerous technical advantages. However, a metallized film capacitor is not a static component, like almost all electronic components it is subject to aging processes.

For a designer of a power electronics board it is essential to know the aging-characteristics of the selected film capacitors. Therefore he needs to know what is the maximum capacitance-loss and increase of the ESR during the life cycle of his product. It is a weakness from most current datasheets of film capacitors that the electrical data are given for new capacitors, but the aging-effects are just specified for the influence of temperature and voltage. It can be easily verified that film capacitors may show an accelerated aging under the simultaneous influence of temperature, voltage and humidity. As long as the current IEC standards for AC- and DC film capacitors are not updated accordingly, the robustness of the selected film capacitor against a climatic aging should be verified within the homologation process. A suitable test (THB-test or 85/85-test with voltage) has been proposed in this article. The manufacturer of the film capacitor should be able to specify what will be the maximum capacitance-loss and increase of the tangent delta in this accelerated lifetime-test.

Further information can be found under:

www.dbtec-electronics.com

Oscilloscope Reinvented

The convergence of power stage modeling and signal processing within the HIL gives its oscilloscope function a high-bandwidth probeless access to all signals within the test setup. This convergence opens up unheard-of possibilities for automatic testing and reporting.

By Subhashish Bhattacharya NC State University,
Toni Gualtieri, Predrag Nikolic and Dusan Majstorovic Typhoon HIL Inc.

Introduction

It is estimated that the cost of quality in power electronics (PE) industry amounts to 2-4% of its overall revenue. The lion's share of those resources is spent on control systems quality assurance, quality control and mitigation of the controller-related field problems.

Now, the question is if there is a way to test power electronics control systems more efficiently than with the current methodologies?

Before we can answer this question let us look into the state of the art PE laboratory first.

Unique Challenges of PE Testing

Figure 1a illustrates a typical high power test stand with the PE controller under test and the oscilloscope highlighted. The oscilloscope in a typical PE test stand has to process a large number of input channels, with a large dynamic range and a multitude of probes with, sometimes, extreme insulation requirements. The large dynamic range means that a very deep memory oscilloscope is needed and the high number of probes is both costly and time consuming to deal with.

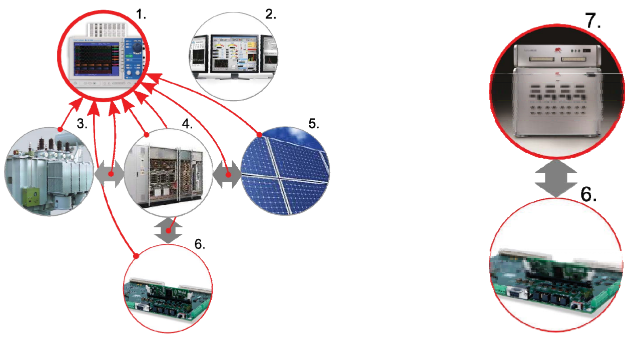


Figure 1. Testing power electronics controls; a) the power electronics lab setup, b) the HIL setup: 1. a deep memory oscilloscope with a large number of channels, 2. test setup control, supervision and protection, 3. a grid side transformer, power supplies, etc., 4. a power electronics converter, 5. An energy source/load, 6. controller hardware/software under test and 7. a HIL with HIL Connect.

To make things more "interesting", the testing involves elaborate safety procedures while the interpretation of the results is often done manually, i.e. skilled technicians interpret the downloaded measurements, store them, and write reports about their findings.

Figure 1b proposes an alternative approach which all but removes the need for testing the PE controller in a high power laboratory. The "trick" is to package the 5 elements from Figure 1 into a compact, desktop device that emulates the power stage with high fidelity and time resolution, and at the same time includes a powerful oscilloscope, as well as test control, supervision, analysis and automation functionalities.

PE Testing the HIL way

Once the power stage is digitized inside the HIL device, there is no need to worry about physical properties of the signals (all that remains is the low voltage custom interface between the PE controller and the HIL, element 8 in Figure 2). Suddenly, with high energy components out of the picture, PE testing becomes a signal-processing problem, which is much easier and less costly to solve.

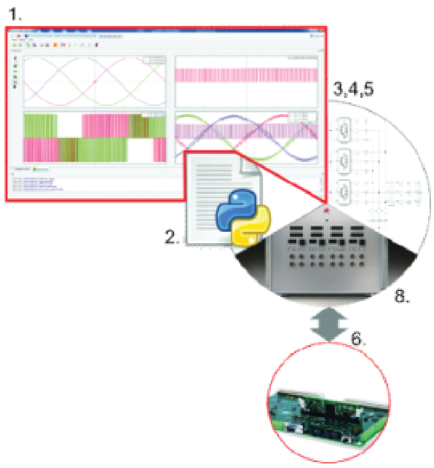


Figure 2: PE Testing the HIL way 1. a deep memory oscilloscope with a large number of channels, 2. Python script test control and supervision , 3-5. digitized PE hardware, 6. controller hardware/software under test and 8. a HIL Connect custom physical interface between the physical controller and the HIL system.

The HIL oscilloscope

The convergence of the power stage model and signal processing within the HIL gives its oscilloscope a high bandwidth, probeless access to all HIL internal signals.

32
analog channels
bits of resolution
digital channels
Mpts of storage

Figure 3: HIL scope key parameters

The oscilloscope's 32 Mpts of storage are directly connected to the HIL processor data bus which enables probeless data access of the HIL scope. The signal processing and display functions are implemented in SW and have found a place on the PC. The cycle time, steps 1-4, from Figure 4 depend on the size of the acquired data sample size (400 Bytes to 128 Mbytes), and is in the 20ms-10s range.

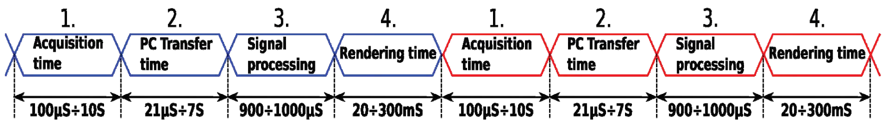


Figure 4. HIL Scope time diagram

In addition to featuring the rich oscilloscope mode from Figure 5, the HIL Scope can also operate in capture mode, in which the data is stored in the PC for post-processing. In this mode, the scope can also be controlled via the Python script for easy integration into the automated PE controller testing procedure.

Figure 5: Feature-rich HIL Scope GUI.

Testing made simple and cost effective

The control system test architecture from Figure 2 all but removes the personnel and material risk of the high power laboratory, and replaces it with the comfortable, risk-free development of Python scripts that:

Fully control the test procedure on both, the HIL and the controller

- under test
- collect and analyze the test data
- automatically generate test reports

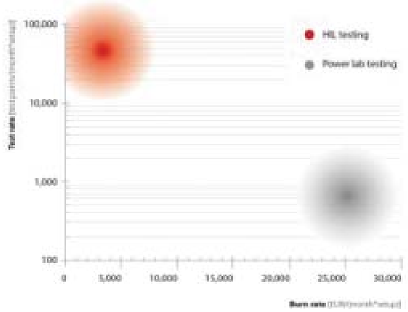


Figure 6: Performance advantage of HIL test setup.

Figure 6 compares variable cost per test points between the "average" high power laboratory and the HIL test setup. Although exact numbers may vary, the speed and efficiency of unsupervised 24h/365 day automatic test system with the test analysis and reporting functionality of the HIL provides orders of magnitude lower cost per test point than the power laboratory. Additionally, to further increase the capacity of the HIL test setup, all that is needed is additional HILs, while in case of the power laboratory, it is additional space, additional personnel, and additional high power equipment.

Conclusion

By digitizing the power laboratory by means of HIL technology i.e. by "removing" high energy physics from PE controller development and testing, we have reasons to expect a measurable reduction of quality cost, improved quality and shorter time to market.

www.typhoon-hil.ch

Surface Mount EMI Filters for Hi-Rel Applications

Syfer Technology, with EPPL listing, has a range of devices appealing particularly to designers in the medical implantable and space sectors as well as industrial, automotive, aerospace and telecom applications. The increasing use of SMD filters over conventional panel mounted filters has simplified assembly methods, reduced production costs and enabled smaller volumetric efficiencies to be gained giving a greater choice of options to the designer - particularly shorter lead-times for development samples.

Syfer Technology continues to refine existing ranges, explore new ones and bring on board new materials, like lead free dielectrics.
For example, the E01 and E07 ranges of feed through MLCC 'C' filters now have extended working voltages from 25Vdc to 200Vdc, and in certain cases up to 500Vdc. This will significantly broaden the market for these devices. These surface mount EMI filter 3 terminal chip devices are designed to offer reduced inductance compared to conventional MLCC's when used in signal line filtering. The filtered signal passes through the chip's internal electrodes with the 'noise' filtered to the grounded side contacts, resulting in reduced length noise transmission paths. Available in C0G/NP0 & X7R dielectrics, in case sizes 0603 to 1812. Current ratings are 300mA to 3A with voltage ratings of 25Vdc to 200Vdc (500Vdc in some case sizes).
FlexiCap™ termination is used throughout the range and all versions are available with either tin or tin/lead finishes.

www.syfer.com

Low Loss, High Density SiC MOSFET Power Modules

Richardson RFPD, Inc. announced availability and full design support capabilities for eleven new low loss, high density silicon carbide (SiC) MOSFET power modules from Microsemi.
The new modules feature high speed switching, low switching losses, low input capacitance, low drive requirements, minimum parasitic inductance, increased reliability, and low profiles—allowing designers to shrink system size and weight, while reducing overall system costs.
The extended temperature ranges of the new devices meet next-generation power conversion system requirements for higher power densities, operating frequencies and efficiencies. The new modules are ideally suited for a range of high power, high voltage industrial applications requiring high performance and reliability, including high power switch mode power supplies, motor drives, uninterruptible power supplies, solar inverters, and oil exploration.

The devices are in stock and available for immediate delivery. To find more information, or to purchase these products today on the Richardson RFPD website, please visit the Microsemi SiC MOSFET Power Modules webpage.

www.richardsonrfpd.com

Voltage Regulator Delivers Digital Dynamic-Loop-Compensation

Ericsson has introduced a new 3E DC-DC regulator (Enhanced Performance, Energy Management, and End-user Value), the BMR461, that is the first 12 x 12 x 8mm 12A digital point-of-load (POL) module to combine Dynamic Loop Compensation (DLC), low-bias current technology, advanced energy-optimization algorithms to reduce energy consumption, and a land-grid-array (LGA) footprint that guarantees excellent thermal, mechanical and electrical performance.

Dynamic Loop Compensation:

The BMR461 Dynamic Loop Compensation is based on 'state-space' or 'model-predictive' control, which guarantees stability while also achieving the optimum dynamic performance without requiring any external components.

Optimized Efficiency

The BMR461 features several algorithms that optimize efficiency across a wide range of operating conditions. Compared to the conventional technology that is currently implemented in analog and digital-hybrid POL regulators, the device's combination of energy optimization algorithms and low bias technology requires up to five times lower current, and therefore further improving overall efficiency.

PMBus Control

Designed for high performances, the BMR461 recognizes 84 PMBus commands and includes a non-volatile memory allowing board-power-designers to upload their own configuration files. The BMR461 also includes easy synchronization through automatic pin detection and without the need for reconfiguration

Reliable Footprint

The BMR461 footprint is based on a matrix Land Grid Array (LGA) composed of 32 solder-pads and has been developed to meet OEM manufacturing requirements in terms of pick-and-place, solderability and co-planarity, or future evolutions such as high power devices with 12x12 footprints as well as additional features that require more interface pads.
A development board – called the ROA17003 – is also available to assist power system designers

www.ericsson.com/powermodules

Best-In-Class DrMOS-IIIS Power Modules

Alpha and Omega Semiconductor launched the AOZ5019, a third-generation high efficiency power module with an EZPair package. This new generation supersedes the previous generation in a smaller package and with a higher frequency. The AOZ5019 is offered in a 23-pin 3.5mm x 5mm QFN package that integrates a dual gate driver and two optimized MOSFETs which combined produce a high efficiency DC-DC synchronous buck power stage and allows switching frequencies up to 1.5MHz. The new device enables high power density voltage regulator solutions ideal for notebook PCs, servers, and graphic cards applications.

The AOZ5019 utilizes AOS's proprietary state-of-the-art trench MOSFET and packaging technologies which improves the efficiency, thermal performance, and package size over the previous generation solution. For example, the efficiency is 1% higher at a heavy load condition compared to leading competitor, the package size has been reduced to 3.5x5mm, and effective thermal pad area has been improved by three times compared to discrete solutions.

www.aosmd.com

Dual Full-Bridge Motor Driver IC for Automotive

The A4990 from Allegro MicroSystems Europe is a new dual full-bridge driver IC designed to operate one bipolar stepper or two brush DC motors in automotive and harsh environment industrial applications.
Each full bridge in the new device uses DMOS power devices with integrated freewheeling diodes. Peak motor current can be limited to provide higher efficiency and reduce motor heating.
The new driver IC is targeted at both the automotive and the industrial markets. Key automotive applications include HVAC actuators, EGR (exhaust gas recirculation) valves, and idle speed control. It is also designed for harsh environments where stepper or DC actuators are needed: for example, in satellite dish or solar panel positioning systems.
The A4990 enables stepper motors to be driven with full current in either direction in each phase, allowing two-phase "on" full-step operation. DC motors can be driven both clockwise and anticlockwise, and in brake mode. A single input turns all bridges off, allowing all motors to coast. All control modes can easily be achieved using three, four or five outputs from a standard parallel interface of a microcontroller.
The A4990 is designed for typical applications requiring up to 800 mA and 28 V, and has 3.3 V and 5 V compatible inputs. The peak motor current can be limited by sense resistor selection to provide higher efficiency, reduced motor heating and longer motor life.
The outputs are protected from short circuits to supply and ground, and low-load current detection is included. Chip-level protection includes overtemperature shutdown and overvoltage and undervoltage lockout.

The A4990KLPTR-T is supplied in a 20-lead TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matt-tin leadframe plating.

www.allegromicro.com

300mA LDO Regulators have Low Quiescent Current

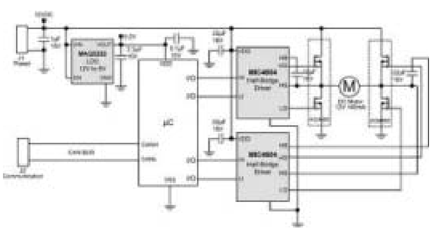
Advanced Power Electronics Corp. (USA), a leading Taiwanese manufacturer of MOS power semiconductors and ICs for DC-DC power conversion applications, has announced a new series of low drop-out linear regulators that include current and thermal shutdown protection features. APE8800A-HF-3 positive linear regulators have a very low quiescent current of about 30µA, an output voltage accuracy of ±2%, and can supply a guaranteed 300mA of output current with a drop-out voltage of only 250mV.

APE8800A-HF-3 regulators are able to operate with low ESR ceramic output capacitors as small as 1µF for stability. As well as current limit protection, the APE8800A-HF-3 also offers an on-chip thermal shutdown feature providing protection against overload or conditions where the junction temperature may exceed the specified thermal shutdown temperature.
The regulators are available with several fixed output voltages from 1.2V to 5V, and are packaged in low-profile, space-saving RoHS/REACH-compliant halogen-free 5-lead SOT-23-5 and TSOT-23-5 packages.

http://www.a-powerusa.com/docs/APE8800A-3.pdf.

85V Half Bridge MOSFET Drivers with Integrated Bootstrap Diode

Micrel, Inc. introduced the MIC4604, a 85V Half Bridge MOSFET driver that features an integrated 85V Bootstrap diode and one of the widest programmable gate drive ranges



(5.5V to 16V) in the industry. These features make the MIC4604 an ideal solution for the industry's most demanding battery operated motor applications including power tools and power DC/AC inverters. The MIC4604 is currently available in volume with pricing starting at $0.69 for 1K quantities in a SOIC package option. Samples can be ordered at: http://www.samplecomponents.com/scripts/samplecenter.dll?micrel.
As an example, in battery powered motor drive applications, there is no need to boost the voltage to exceed the typical minimal gate drive of 9V offered by othersolutions; the MIC4604 allows operation from supplies as low as 5.5V. In addition, the 85V operating voltage offers plenty of margin which protects against voltage spikes that are present in motor drive and power supply applications, making the MIC4604 an ideal solution for low voltage and high voltage applications.

www.micrel.com

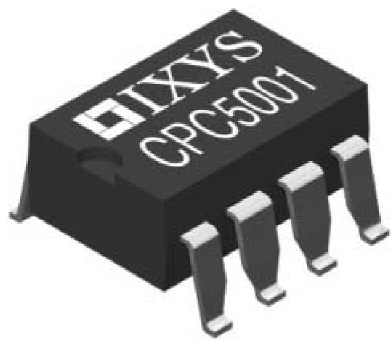
5 Watt USB Switching Power Adapter in Ultra-Compact Case

CUI Inc has announced an ultra-compact 5 W wall plug adapter with integrated USB connector, the EPSA050100U-I38-EJ. With a footprint of just 41 x 30 mm (1.61 x 1.18 inches), the adapter is among the industry's smallest ac-dc power supplies to integrate USB. The small form factor makes it ideally suited for a wide range of consumer applications, including media players, e-readers, GPS, and other mobile devices.
The EPSA050100U-I38-EJ has Level V energy-efficiency compliance for green design requirements and is equipped with a no-load power draw of less than 0.1 W.
Rated with an output of 5 Vdc at 1 A, the high density EPSA050100U-I38-EJ operates at ac input voltages ranging from 90~264 Vac.
Safety marks include UL/cUL, PSE, and LPS (limited power source).
The 5 W power adapter meets EN55022 Class B limits for conducted and radiated EMI and provides protections for over-voltage, over current, and short circuit conditions.
The EPSA050100U-I38-EJ is now available through distribution with prices starting at $6.05 for 100 pieces. OEM pricing is available on request.
A data sheet is available from:
http://www.cui.com/product/resource/epsa-5w-usb.pdf.

www.cui.com

Dual, One-Channel Each Direction Digital Optical Isolator

IXYS Integrated Circuits Division Inc., a wholly owned subsidiary of IXYS Corporation, announced the immediate availability of a new device for its family of high speed communication ICs, the CPC5001 Dual, One-Channel Each Direction Digital Optical Isolator.
The CPC5001 is a non-inverting logic-signal isolator with buffered-logic inputs and open-drain outputs. Channel 1 propagates a signal from Side A to Side B, while Channel 2 sends a signal from Side B to Side A. The CPC5001 supports 5M baud data rates for digital communications over an optical barrier while providing 3750 Vrms of galvanic isolation.
Available in an 8-pin DIP or 8-pin surface mount package, it functionally replaces two logic buffers and two single-channel optical isolators. Internal band gap references regulate the input LED drive currents to 3 mA to reduce peak power requirements.
The CPC5001 Dual High-Speed Digital Optical Isolator is ideal for clock, data, interrupt and reset signals in isolated line receiver and bus receiver applications. The device may be used in Power-over-Ethernet (POE) applications, providing buffering and isolation of signals between the host controller and the Power Supply Equipment (PSE) controller. Additional applications include SPI bus interface, power supply high side interface and isolated signal monitoring and control. The CPC5001 is certified to UL 1577 and EN/IEC 60950.

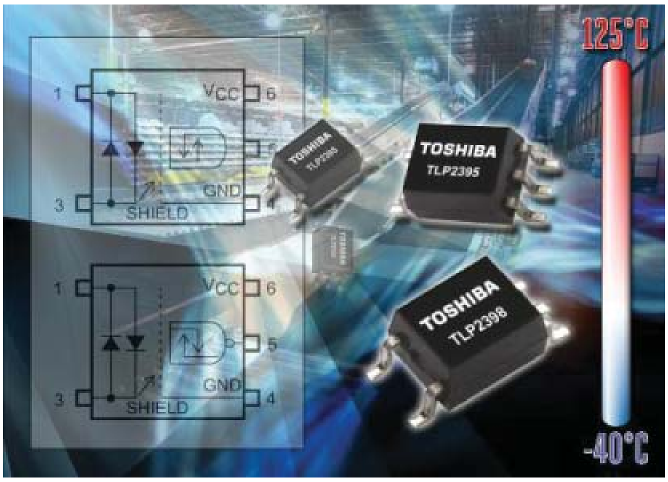


www.ixys.com

Dual Polarity Input Photocouplers for Industrial Designs

Toshiba Electronics Europe (TEE) has announced two dual-polarity, high-speed photocouplers that can support both sink and source logic input signals. The TLP2395 and TLP2398 will help to significantly reduce component count and power consumption in industrial systems ranging from programmable logic controllers (PLCs) to instrumentation.

Requirements to support both sink and source logic inputs in modern PLC and instrumentation systems means that bridge circuitry is commonly employed upstream from the photocouplers used in high-speed



digital interfaces. Now, however, by combining two LEDs in a reverse parallel configuration, the TLP2395 and TLP2398 eliminate the need for these bridge circuits. As a modern PLC can have multiple photocouplers - and, therefore, multiple bridge circuits - the devices will significantly reduce circuit size, power consumption and cost.

Both the TLP2395 (logic buffer output) and the TLP2398 (inverter output) photocouplers will accommodate a wide 3V to 20V power supply voltage range, which helps to reduce the need for DC-DC conversion circuitry. Each device also offers guaranteed operation at temperatures ranging from -40°C to 125°C.

Toshiba's devices support a data transfer speed of 5Mbps and combine a propagation delay of less than 250ns with a pulse width distortion below 80ns. As a result they are ideal for RS232C, RS422, RS485 and other commonly used industrial communication interfaces. A low input current drive of 2.3mA and a supply current of just 3mA contribute to application efficiency.

The two couplers are supplied in SO6 surface mount packaging that integrates two GaAlAs LEDs coupled with a high-gain, high-speed photodetector. Despite board mounting dimensions of only 7.0mm x 3.7mm x 2.3mm, guaranteed minimum creepage and clearance distance is 5mm and guaranteed minimum input-output withstand voltage is 3.5kVrms. An internal Faraday shield ensures common-mode transient immunity of ±20kV/µs.

www.toshiba-components.com

Leading Efficiency for DC-DC Synchronous Buck Applications

International Rectifier has introduced the 25V FastIRFET™ family of innovative power MOSFETs for DC-DC synchronous buck applications including advanced telecom and netcom equipment, servers, graphic cards, desktop, ultrabook and notebook computers.

The FastIRFET™ family features IR's latest generation silicon in an industry standard PQFN package that delivers benchmark power density for discrete DC-DC converters. The family includes the IRFH4201 that offers on-state resistance (RDS(on)) as low as 0.7 milliOhms, and the IRFH4210D and IRFH4213D monolithic FETKY® devices designed to reduce ringing and further improve system efficiency.

The advanced 25V FastIRFET™ MOSFETs offer industry leading power density for discrete high performance DC-DC switching applications. The devices complement IR's integrated SupIRbuck®, PowIRstage® and power block platforms to offer designers a broad array of high performance DC-DC options.

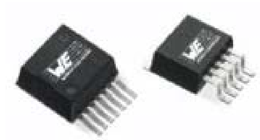
Optimized for 5V gate drive applications, IR's FastIRFET™ devices work with any controller or driver to offer design flexibility while delivering higher current, efficiency and frequency capability in a small footprint. The devices are available in industry standard 5x6 and 3.3x3.3mm PQFN packages that feature an environmentally friendly, lead-free and RoHS compliant bill of materials.

Datasheets are available on the International Rectifier website at:

http://www.irf.com

Power Modules for Point-of-Load DC/DC-Converter

Würth Elektronik eiSos has been a European leader in the development, manufacturing and sales of passive and electromechanical components for many years. Four years ago, the company also began offering active components for the electronics market. The first product group comprised TVS diodes; LEDs soon followed. The family of MagI³C Power Modules now represents the first active components for power electronics.



Würth Elektronik will launch its step-down regulator Power Modules product range with five modules offering variable output voltage and two modules with output voltage. Both types will provide auto-reset for overvoltage and overcurrent as well as thermal shutdown.

Modules with variable output voltage (MagI³C-VDRM) have an input voltage range of 6 V to 42 V and an output voltage range of 0.8 to 24 V. Adjustable switching frequency (200 kHz to 800 kHz) and a programmable soft-start provide additional flexibility.

www.we-online.com

Automotive DirectFET®2 Power MOSFET Delivers Increased Power Density

International Rectifier has launched the AUIRF8736M2 DirectFET®2 power MOSFET for heavy load automotive applications including electric power steering, braking systems and pumps that require superior power density in a compact footprint.

Leveraging IR's benchmark COOLiRFET™ silicon technology, the 40V AUIRF8736M2 offers a 40% improvement in on-state resistance (Rds(on)) compared to previous generation devices to help minimize conduction losses. The dual-side cooling Medium Can DirectFET®2 power package delivers excellent thermal performance and low parasitic inductance.

The AUIRF8736M2 combines the performance of the COOLiRFET™ silicon with the DirectFET®2 package, delivering a 40% Rds(on) improvement in the same footprint, or equivalent performance to a Large Can device in a 50% smaller package.

The device is qualified according to AEC-Q101 standards, features an environmentally-friendly 100% lead-free package and RoHS compliant bill of materials, and is part of IR's automotive quality initiative targeting zero defects.

www.irf.com

Ultimate Field Deployable Shielded Cat 6A Cable

Belden Inc. has introduced a range of rugged high performance shielded Cat 6A cables for use in studios or in tactical field deployable audio/data installations. Designed as the ultimate field deployable product, these exceptionally robust cables can be used in the harshest of environments, yet deliver reliable performance for maximum uptime.

Belden CatSnake Cat 6A tested cables deliver superior performance thanks to the 100% coverage of the pairs as these are individually shielded with Beldfoil aluminium/polyester foil and an overall braided shield.

The Belden CatSnake Cat 6A cables are extremely robust and have exceptional flexibility and flex life. This makes them ideal for use in high traffic areas, such as in broadcast studios or in any type of tactical, field deployable audio/data installation. Moreover the compact, round cable design eases transportation and deployment.

These cables have been tested for repeated bending according the EN 50289-3-9-5, and exceed the required 100 bends (radius 40mm, weight 8kg) while maintaining electrical performance.

Belden's shielded CatSnake features Beldfoil shielded twisted pairs with 24 AWG stranded bare copper conductors and polyolefin insulation and is RJ-45 compatible.

For simulating the coiling and uncoiling on a reel, the CatSnake Cat 6A has been subjected to a Track Chain test. Even after 1 million bendings (radius 100mm, length 5m, speed 3.5m/s) the cable performed according the electrical performance stated in the data sheet.

www.beldensolutions.com

Charge Any Portable Device over USB in a Car with a Single IC

Maxim Integrated's automotive DC-DC converter with cable drop compensation integrates a smart USB charge emulator to enable fast and reliable charging for portable devices (PDs).

Recognizing and then charging any portable device (PD) directly from a vehicle battery can now be done over USB with a single IC, the MAX16984 automotive DC-DC converter with USB charge emulator from Maxim Integrated Products, Inc.

Previously, PDs like smartphones and tablets could not charge reliably from OEM stock USB ports in vehicles. Long embedded USB cables cause a voltage drop and reduce charging current, resulting in a PD to not properly charge. Low-cost portable USB car chargers introduce RF interference. Now, the MAX16984 brings intelligent USB charging into an automobile and solves these problems. This single-chip solution integrates all the functions of the traditional three-chip solution. The MAX16984 combines a low EMI 5V automotive-grade DC-DC converter capable of driving up to 2.5 A with dynamic voltage adjustment, which is essential for charging contemporary PDs over long automotive embedded cables; a USB Battery Charging Specification v1.2-compliant charge emulator, which conducts the necessary handshake between the PD and upstream host instructing the PD to increase its charge current; and integrated ESD diodes and USB over voltage protection switches, which provide robust industry-le ading fault protection. The result is the fastest and most reliable PD charging with the smallest solution size. The MAX16984 is ideal for automotive radios and navigation modules, embedded telematics and connectivity modules, and USB-dedicated charging ports.

www.maximintegrated.com

Advertising Index

Rugged, Reliable MOSFETs for Industrial Applications

Part Number	V_{DS} (V)	$R_{DS(on)}$ Max. VGS=10V (mΩ)	I_D (A)	Q_G (nC)	Package
IRF7739L2	40	1	270	220	DirectFET-L8
IRFB7430	40	1.3	409	300	TO-220
IRFH7004	40	1.4	259	129	PQFN 5X6 mm
IRFS7440	40	2.5	208	90	D^2PAK
IRFS3006-7	60	2.1	240	200	D^2PAK-7
IRFS3006	60	2.5	195	200	D^2PAK
IRFH5006	60	4.1	100	67	PQFN 5x6 mm
IRF7749L2	60	1.3	108	220	DirectFET-L8
IRFB3077	75	3.3	210	160	TO-220
IRFH5007	75	5.9	100	65	PQFN 5x6 mm
IRF7759L2	75	2.2	83	220	DirectFET-L8
IRFP4468	100	2.6	195	360	TO-247
IRFH5010	100	9	100	65	PQFN 5x6 mm
IRF7769L2	100	3.5	124	200	DirectFET-L8
IRFS4010-7	150	4	190	150	D^2PAK
IRFS4010	150	4.7	180	143	D^2PAK
IRFH5015	150	31	56	33	PQFN 5x6 mm
IRF7779L2	150	11	67	97	DirectFET-L8
IRFP4668	200	9.7	130	161	TO-247
IRFH5020	200	59	41	36	PQFN 5x6 mm
IRFP4768	250	17.5	93	180	TO-247
IRFH5025	250	100	32	37	PQFN 5x6 mm
IRF7799L2	250	38	35	110	DirectFET-L8

Features

- Low on resistance per silicon area
- Optimized for both fast switching and low gate charge
- Excellent gate, avalanche and dynamic dv/dt ruggedness

The IR Advantage

- Best die to footprint ratio
- Large range of packages
- Available from 40 V to 250 V

Applications

- DC Motor Drives
- Uninterruptible Power Supplies (UPS)
- DC-DC Converters
- Power Tools
- Electric Bikes

Your FIRST CHOICE for Performance

For more information call +49 (0) 6102 884 311
or visit us at www.irf.com

International Rectifier
THE POWER MANAGEMENT LEADER