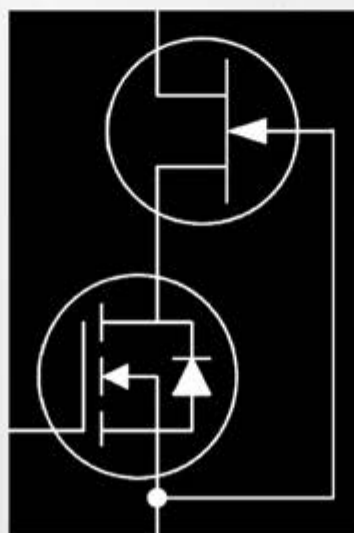
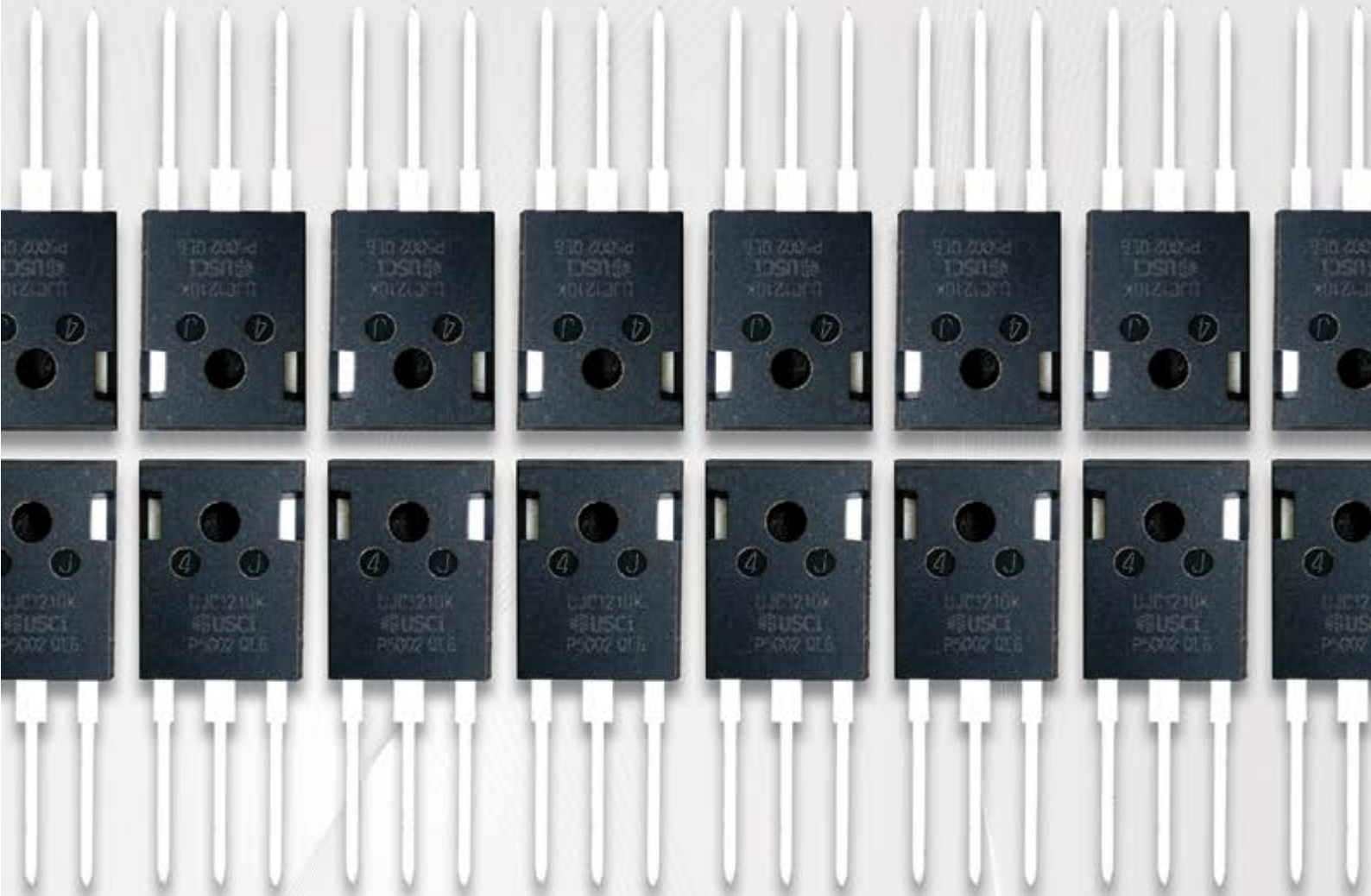


Bodo's Power Systems®

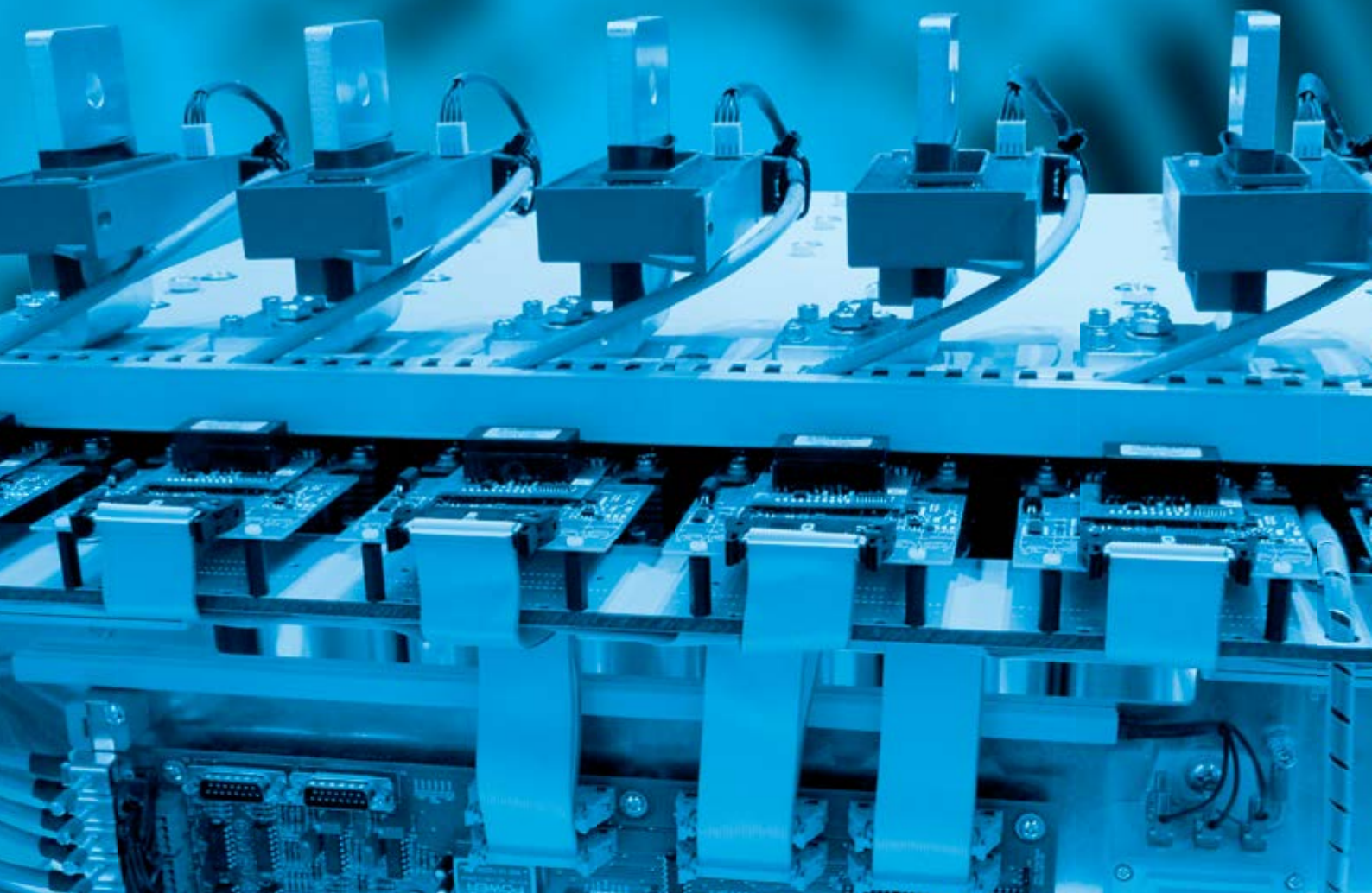
Electronics in Motion and Conversion

September 2015



 **USCi**
SiC Cascodes:
Paralleling
Made Easy

The VARIS™ concept – flexible power based on a modular concept



VARIS™ – the modular inverter system

The modular and flexible design of VARIS™ offers compelling benefits. The desired power can be easily achieved via parallel connection of the modules. You are also free to choose your preferred cooling type. And the use of standard components makes VARIS™ both cost-efficient and sustainable. Talk to the House of Competence, because VARIS™ fears no comparison.



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medical and industrial



Read online and search for key subjects from all articles in Bodo's
Power Systems by going to Powerguru: www.powerguru.org



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The Gallery





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Avago optocouplers are certified according to IEC 60747-5-5
The international safety standard for insulation and isolation



Avago's optocoupler portfolio includes gate drive optocouplers for driving IGBTs, digital isolators for system control and data communication and isolation amplifiers for current and voltage sensing applications. Optical isolation has been a proven technology since 1975.

Some of the benefits of using optocouplers are EMI Immunity, better protection against ESD (Electrostatic Discharge), reinforced isolation and high CMR of up to 40 kV/ μ s. To be really on the safe side, use Avago optocoupler technology from EBV – Avago's leading distribution specialist and the number one in EMEA semiconductor distribution.

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The World is One Market

Design and research are done everywhere in the world, as is manufacturing. The traditional work-bench countries now perform design and research. The electronic industry has taught us to view the world globally. At one time, chip design was done in the US, Europe and Japan. Asia mostly did packaging. And this is still true for Malaysia and the Philippines, where we find companies specialized in chip packaging. Chip design locations have for some time included China, South Korea and India. As electronic technology is at the forefront of progress, such globalization reflects well on progress in standards of living – and a challenge for us to provide educational opportunities for bright youngsters around the world.

Only education can help the world progress. At the moment there is far too much warfare, and addressing issues through armed conflict is too often the choice. There are so many victims killed or perishing in their attempt to reach a safe country. The United Nations needs to intensify their efforts to help these people, and governments must speed up their integration, and we must change our attitudes towards minorities and the poor. In fleeing conflict, they have made a long difficult trip to survive, to reach some material stability, and recover their dignity. As the human rights outlined in the constitution of the USA are well defined, this could be the platform for behavior in every country. The worldwide marketplace should not be the only global entity.

In the second half of the year we have important conferences and shows addressing the production of semiconductors - like SEMI-CRON and productronica. These conferences highlight improvements in semiconductor



manufacturing that we have come to rely upon. And they have spread out geographically to various continents, serving a portfolio of companies and products.

We have delivered nine issues this year. All technical articles are archived on my website and are also retrievable at PowerGuru. Bodo's Power Systems reaches readers across the globe. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodoschina.com

My Green Power Tip for September:

Start collecting wood for the fireplace, keep it dry, and use it to heat your home – it is a renewable resource. Or just help by reducing your consumption of coal, oil, electricity or gas.

Little by little we can make our resources last longer.

Regards



Events

EPE ECCE 2015, Geneve, Switzerland,
September 8-10 www.epe2015.com

Electrical Fuses 2015 Dresden, Germany,
September 14-16 www.icefa2015.com/

EU PVSEC 2015,
Hamburg, Germany, Sept. 14-18
www.photovoltaic-conference.com

E DPC 2015, Nuremberg, Germany,
Sept. 15-16 www.mesago.de/en/EDPC

HusumWind 2015, Husum, Germany,
September 15-18 www.husumwind.com

Power Fortronic, Bolonia, Italy,
September 17 <http://fortronic.net/power>

ECCE 2015,
Montreal, Canada, September 20-24
<http://2015.ecceconferences.org/>

LED LpS Event, Bregenz, Austria
September 22 – 24 www.LpS2015.com

KEEP UP WITH THE TIMES



LF xx10 Current transducer range Pushing Hall effect technology to new limits

To save energy, you first need to measure it! To maximise energy savings, you need to measure the current used accurately!

By using the most advanced materials available, LEM's new LF xx10 transducer range breaks new ground in accuracy for Closed Loop Hall effect transducer performance. LEM ASIC technology brings Closed Loop Hall effect transducer performance to the level of Fluxgate transducers and provides better control and increased system efficiency, but at a significantly lower price.

Available in 5 different sizes to work with nominal currents from 100 A to 2000 A, the LF xx10 range provides up to 5 times better global accuracy over their operating temperature range compared to the previous generation of Closed Loop Hall effect current transducers.

Quite simply, the LF xx10 range goes beyond what were previously thought of as the limits of Hall effect technology.

- Overall accuracy over temperature range from 0.2 to 0.6 % of I_{PN}
- Exceptional offset drift of 0.1 % of I_{PN}
- Fast response time less than 0.5 μ s
- Higher measuring range
- 5 compact sizes in a variety of mounting topologies (flat or vertical)
- Immunity from external fields for your compact design
- 100 % fully compatible vs LEM previous generation
- -40 to +85 °C operation

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At the heart of power electronics.



FTCAP Sign Global Distribution Agreement

Richardson Electronics, Ltd. announced a global distribution agreement with Fischer & Tausche, FTCAP GmbH, a leading manufacturer of custom and standard catalog aluminum electrolytic and film capacitors. The agreement aligns with FTCAP's focus on identifying new opportunities and solutions for customers' most challenging applications. For more than 65 years, FTCAP has developed and manufactured aluminum electrolytic and film capacitors in small to medium-sized batch quantities. FTCAP offers a broad selection of standard catalog items as well as custom solutions developed in close collaboration with customers.

Richardson Electronics is a global channel partner for world-class electron devices, power electronics, and RF & microwave components.

"As an established and reliable capacitor manufacturer with innovative capabilities, we are excited to partner with FTCAP in order to meet

customer requirements," said Greg Peloquin, Executive Vice President of Richardson Electronics' Power & Microwave Technologies group. "FTCAP offers a variety of high quality product solutions using tried-and-true technology gained from many decades of experience." "Similar to our company, Richardson Electronics has been an industry leader in providing innovative and high-quality products for more than 65 years," stated Dr. Thomas Ebel, Managing Director of FTCAP. "Richardson Electronics' extensive global network will present our innovative technology, products and services to customers and their most demanding design needs."

www.rell.com

www.ftcap.de

Second Successful Alpha Academy Seminar

Alpha presented its latest assembly solutions at the second Alpha Academy seminar on Tuesday 23rd June hosted by Barbieri, its Premium Distributor partner for Italy. The event follows on from the highly successful Alpha Academy seminar held in October last year, and was attended by over 20 people from a number of key companies across a broad range of professions including production managers and process engineers.

The seminar included presentations on the latest Alpha products and assembly solutions which were a direct result of customer feedback.

Alpha's Donato Casati and Sandro Crivellaro presented the latest



information on ALPHA® Exactalloy® Preforms, Low Silver Alloys and the topic of Total Ionic Contamination.

The seminar also included presentations from two guest speakers from Datapaq, a manufacturer of temperature profiling systems, data loggers and temperature analysis software for industrial heating systems and Prevent srl, a PCB Manufacturer that provides expert lab analysis.

Alpha's Donato Casati and Barbieri's Davide Barbieri commented, "The event has been hugely successful and we have received very positive feedback from the attendees. The technical focus of the seminar was extremely popular as it provided attendees with useful takeaways for their daily jobs. This has encouraged us to continue with the Alpha Academy seminars, with two further seminars planned for October and February."

Alpha and Barbieri have enjoyed a long and successful partnership, with Barbieri supplying Alpha products across Italy for 33 years. This year, Barbieri has become part of Alpha's unique group of Premium Distributors.

For more information on future Alpha Academy seminars in Italy please contact Donato Casati dcasati@alent.com

www.alpha.alent.com

Testing Access Barriers: Precision Power Scope is the Key

Yokogawa's PX8000 Precision Power Scope is playing a key part in production tests being carried out by Magnetic Autocontrol Group of Schopfheim, Germany: a major global supplier of vehicle and pedestrian access barriers for installations as diverse as access barriers at Frankfurt Airport, the Paris Metro ticket control systems and the Kuala Lumpur Petronas Twin Towers.

Each year, Magnetic Autocontrol produces more than 15,000 barriers for the world market. The products are based on a modular system using a range of standard components which can easily be customised according to user requirements. For orders from outside Germany, often only subassemblies or components are shipped from the factory at Schopfheim. These are then further processed and assembled by the company's global branches to produce the finished end products. This process significantly reduces the transport and

storage costs resulting in increased efficiency in the overseas sales activities.

In principle, the operation of these barriers is similar to the direct drive of a 3-phase control system. The heart of the system consists of one or more motors along with a control unit. Depending on the application and customer requirements, different interfaces are selected including USB, RS485 or Ethernet Ports as well as inputs from card readers, key switches or loop detectors. The number of drives can vary, from one for a standard barrier, up to four for a pedestrian gate.

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 Stand B.e31
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AC/DC CONVERTERS

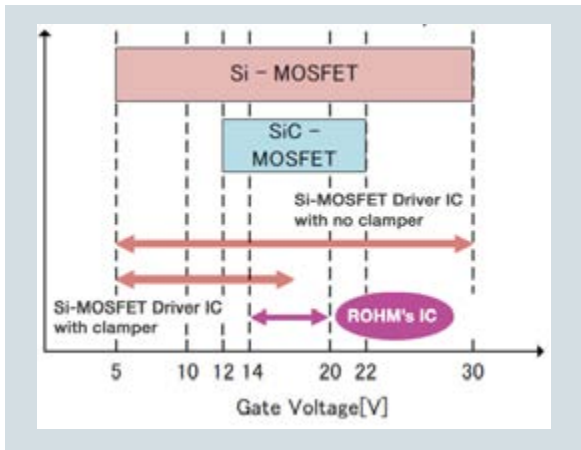
- High Voltage
- High Robustness
- High Integration

ROHM Semiconductor offers a wide line-up of AC/DC Controllers for external MOSFET as well as fully integrated converters with internal MOSFETs.

Highlight: AC/DC Converter IC for SiC-MOSFET Driving

Why using SiC MOSFET for AC/DC?

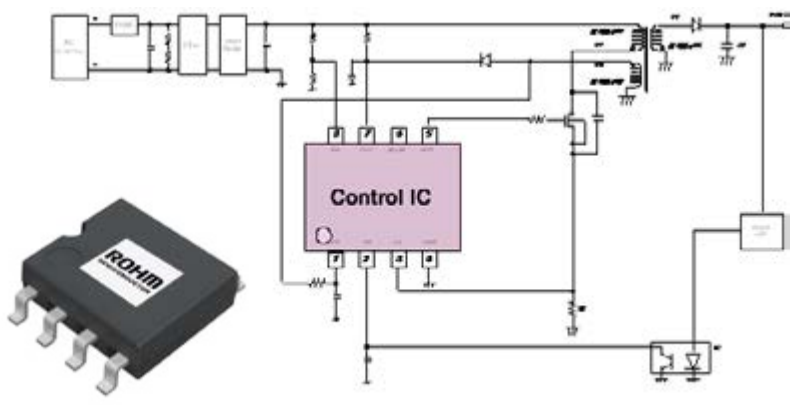
- High Voltage Operation possible with Low RON & Qg
- Less components (no high voltage clamper, no gate clamper, less cooling)
- Compact solution



BD7682FJ Key Features

- Quasi – Resonant DC/DC converter
- Integrated Gate Driver optimized for driving of SiC MOSFET
- Low VCC current (19µA @VCC = 18.5V)
- Burst function at light load
- Max. Frequency Controlled (120kHz)
- VCC Over/Under Voltage Protection
- Brown IN/OUT Function
- DC/DC Soft Start
- 250 nsec Leading-Edge Blanking
- Over Load Protection (128 ms Timer)

Optimum System for Driving SiC MOSFET



Distribution Partner for China and Taiwan's Power Supply Markets

GaN Systems Inc., a leading developer of gallium nitride power switching semiconductors, has appointed Shenzhen APL to distribute its Island Technology® high-power GaN devices in China and Taiwan. SZ APL is headquartered in Shenzhen (www.szapl.com) with additional offices in Shanghai, Beijing, and Taipei. The company has extensive experience in power electronics components distribution to major Tier1 customers in the automotive, industrial and enterprise segments.

Announcing the deal, Girvan Patterson, President, GaN Systems said: "We are delighted to have signed SZ APL as a distributor, as it has both significant knowledge of power electronics and strong relationships with Tier1 Chinese and Taiwanese customers. Demand for our GaN power switching transistors is growing very rapidly as manufacturers seek to design smaller, lighter and more power-efficient products in order to gain competitive edge. We are expecting multiple consumer and enterprise products designed with our GaN devices to be launched in the region in early 2016, with other applications from our industrial and automotive customers to follow later next year." Henry Ruan, President SZ APL comments: "We are very excited about our partnership with GaN Systems, which allows us to offer our customers the world's best GaN power transistors to meet the challenges of next-generation power electronics. Prior to signing our

distribution agreement with GaN Systems, discussions with our Tier1 customers confirmed GaN Systems as their first choice manufacturer of GaN E-HEMTs, so we are very pleased to be able to offer its product range – the broadest on the market - to our customers throughout China and Taiwan."

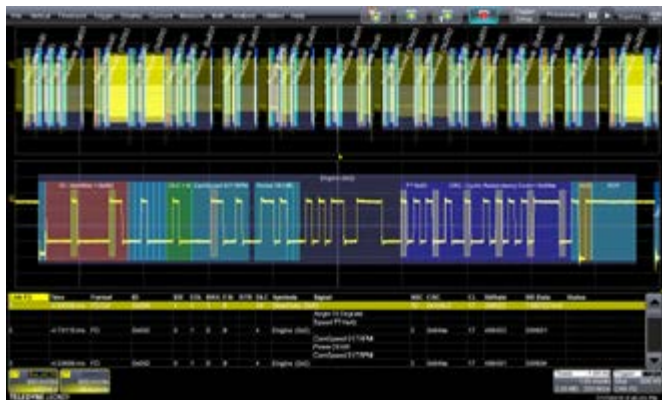
Charles Bailley, GaN Systems' Senior Director, Sales and Marketing, Asia adds: "SZ APL has many key relationships with major Tier1 customers in China and Taiwan, as well as a strong focus and understanding of power electronics and power ICs. During 2015, we have significantly increased our customer penetration in China and Taiwan and look forward to working with SZ APL to continuously add further major design wins."

GaN Systems is the first company to have developed and produced a comprehensive portfolio of GaN E-HEMT power devices with current ratings from 7A to 250A, in both 650V and 100V ranges. GaN Systems' Island Technology® die design, combined with the extremely low inductance and thermal efficiency of GaNPX™ packaging and DriveAssist™ technology, provides their GaN E-HEMTs with 45x improvement in switching and conduction performance over silicon MOSFETs and IGBTs.

www.gansystems.com

Strengthens Industry Leading CAN and CAN FD Solutions

Yokogawa's PX8000 Precision Power Scope is playing a key part in production tests being carried out by Magnetic Autocontrol Group of Schopfheim, Germany: a major global supplier of vehicle and pedestrian access barriers for installations as diverse as access barriers at Frankfurt Airport, the Paris Metro ticket control systems and the Kuala Lumpur Petronas Twin Towers.



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teledynelecroy.com

Developer Forum Battery Technologies Takes Place in Hamburg

At the 9th Developer Forum Battery Technologies – November 3-4, 2015 at Lindner Park-Hotel Hagenbeck in Hamburg, Germany – organized by Batteryuniversity, participants will acquire information about the latest trends and development potential in the area of lithium-ion batteries, possibilities for optimal utilization of their capacity and for determining the 'state of health', strategies for maximizing safety with stationary storage systems and much more.

Whether it's electric bikes, power tools, household appliances, electric vehicles, portable computers or home storage – in the meantime,

there is hardly any area of our daily life where lithium-ion batteries are not yet used. Nowadays, anyone who works as a system developer must therefore, in all probability, at least become familiar with the basics of this technology.

Detailed information and registration form can be found at:

www.entwicklerforum-akkutechnologien.de

Danish Wind Export Association at Husum Wind 2015



The Danish Wind Export Association is your shortcut to Danish companies who are among the world's best in their respective areas within the wind industry. At Husum Wind 2015, 28 of these companies are showing their newest products and services in hall no. 3B18

www.dk-export.dk

Power & Microwave Technologies at AMPERE 2015

Richardson Electronics, Ltd. announced its sponsorship and participation at the 15th International Conference on Microwave and High Frequency Heating (AMPERE 2015) at Cracow University of Technology, Poland, 14-17 September 2015. The Association for Microwave Power in Europe for Research and Education (AMPERE) is a European non-profit association devoted to the promotion of microwave and radio frequency heating techniques for research and industrial applications. The association has worldwide membership comprised of industrialists, academics and consultants.

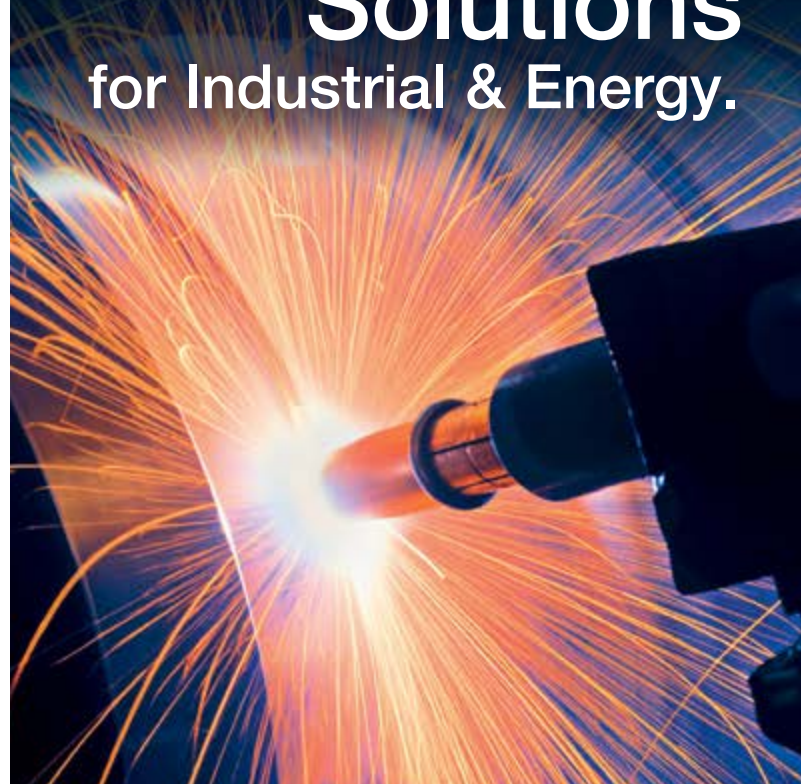
The company's in-house coil manufacturing and testing capabilities enable strict quality control and repeatability, resulting in faster lead times and competitive pricing.

Richardson Electronics sales engineers and technical specialists will be at the booth, offering support and solutions for attendees' design challenges and issues for systems operating at a kilohertz through gigahertz with power capabilities from a few watts to megawatts of power.

<http://ampere.pk.edu.pl/start/>

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Superior Solutions for Industrial & Energy.



Aluminum electrolytic capacitors for high ripple currents



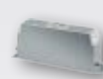
Common-mode chokes for high currents



PFC products for energy efficiency and power quality



Varistors and surge arresters for over-voltage protection



EMC and sine-wave filters for currents up to 8 kA



High reliability power capacitors



X and Y capacitors for EMI suppression



Output chokes up to 1500 A



UHV ceramic capacitors for highest reliability



High reliability SMT power inductors



Pulse transformers for LAN interfaces



CeraLink™ capacitors for embedding in IGBT modules

Win a Microchip MPLAB® Starter Kit for PIC24F from Bodo's Power!

The MPLAB® Starter Kit for PIC24F (DM240015) Intelligent Integrated Analog is a comprehensive development kit featuring the PIC24F "GC" family of 16-bit microcontrollers. This family features advanced integrated analog which reduces BOM cost, lowers noise, and has faster throughput.

The board demonstrates these features of the PIC24FJ128GC010 Microcontroller: direct LCD drive, 16-bit Sigma-Delta ADC, 12-bit Pipeline ADC, 10-bit DAC, Op-Amps, CTMU, DMA, USB, and XLP low power consumption.

The demonstration code includes: LCD display including scrolling text with icons, Sine wave audio output, Light Sensor, Temperature Sensor, Resistive Sensor, Watch Crystal based Time display, mTouch™ User Input Control with Visual Feedback, Bar Graph display of sensor and microphone input, and data logging of 16-bit ADC data to USB drive. The board also features an analog connector designed to insert into a breadboard for easy access to analog peripherals, and an expansion area for adding RF connectivity.

The board features an analog header, allowing clean analog signals to be accessed, preserving signal integrity. To complement the header, the board also features on-board sensors such as light sensor, potentiometer, microphone, temperature, and capacitive touch.

Additional features include USB Host and Device support, RF expandability, audio output via headphone jack, and on-board debugger/programmer.



Features:

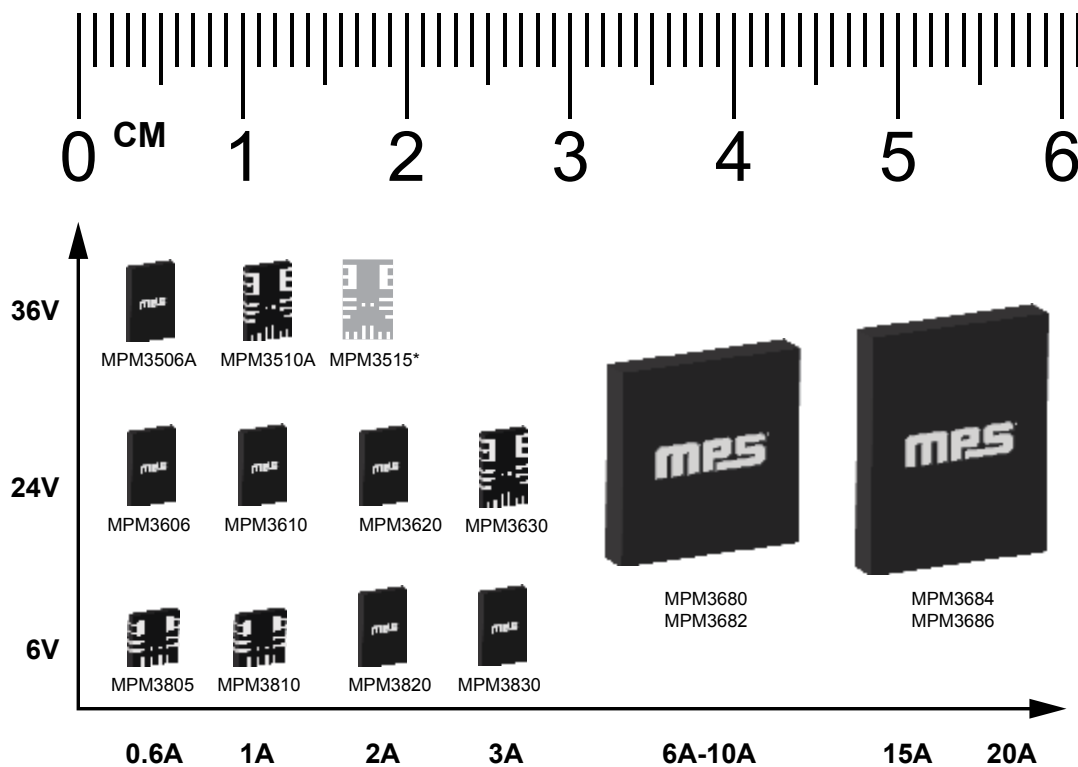
- 16-bit Sigma-Delta Analog to Digital Converter
- 12-bit Pipeline 10 Msps Analog to Digital Converter
- 10-bit 1 Msps Digital to Analog Converter (2)
- Operational Amplifiers (2)
- Comparators (3)
- Voltage References (3)
- Charge-Time Measurement Unit (CTMU)

For the chance to win a MPLAB® Starter Kit for PIC24F Demo Board, log onto <http://www.microchip-comps.com/bodo-mplab-pic24f> and enter your details into the online entry form.

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*Coming soon



Beyond the Chips – Higher Complexity of Energy-Efficient Solutions Demands System Understanding



By Adam White, Senior Vice President Global Sales of Infineon's Power Management and Multimarket Division

Semiconductors, the cornerstone of today's fast-moving global electronics industry, are essential to the way we live our lives in the 21st century. Computers, communica-

tion equipment, consumer products, mobile devices, automobiles, aircraft, medical equipment, lighting, industrial automation systems and renewable energy (to name but a few) are all dependent on these devices for the delivery of effective, reliable, efficient performance.

In fact, it is really no exaggeration to say that semiconductors – and not least those technologies targeting energy-efficient power management and motion control – are critical to both the ongoing advancement of the human race and our responsible stewardship of this planet's environment and its precious resources. We, at Infineon, believe that we are making life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everybody.

Recent history tells us that the birth of the semiconductor can be traced back to 1954 with the launch of the first transistor. Until then, many scientists had been skeptical that semiconductors could ever be realized in true commercial quantities. But, to our great benefit, history has proved otherwise, with the now famous 'Moore's Law' (that the number of transistors per unit area on an IC doubles every year) remaining true for over sixty years!

And while Moore's Law is typically quoted in relation to processing power it can be argued that it is linked to the larger economics of semiconductor manufacture as a whole. More specifically, that ever more sophisticated chips will be developed while maintaining or driving down unit pricing. And this rule is as applicable to a power semiconductor or an LED driver IC as it is to a microcontroller or a logic device.

One thing that has changed since the birth of the semiconductor, however, is the nature of application design. In the past, the electronics industry was largely built around a few very large OEMs who had the luxury of employing extensive in-house engineering teams. These teams would typically design everything from the 'ground-up' – creating discrete designs optimized for their target application. However, over the years the industry has become more fragmented – with much smaller design teams (often working for specialist design houses) developing products that are then built by contract electronics manufacturing companies before being delivered to the brand owner.

At the same time, pressure to reduce both time-to-market and cost has intensified significantly. This is particularly true of the consumer electronics and mobile phone sectors, with technologies and end user devices changing faster than once a year. And even an industry such

as the automotive sector, which would typically expect to have longer development cycles, is seeing those cycles shortened thanks to the pace of technological development and the growing expectation of an ever-more sophisticated buying public.

One effect of these industry changes is to increase the focus of design teams on their 'core competencies' where they can add competitive advantage, with the expectation that other elements of the overall system will be 'bought in'. As a result, there is a trend away from sourcing individual semiconductor components to overall solutions – say AC/DC power modules, battery management solutions or complete BLDC motor drive schemes – that can quickly and easily be incorporated into a design.

To meet the evolving needs of the electronics sector, semiconductor manufacturers must also evolve. No longer is it enough for these companies to simply develop and manufacture ICs. They must also develop an understanding for their customer's 'systems' – may that be a train, wind turbine, car, or washing machine. At Infineon we have coined the phrase 'from product to system' – or P2S for short – to describe our own individual approach to satisfying the system requirements of time-pressured design teams. Focusing on the three central needs of modern society – energy efficiency, mobility and security – the P2S strategy combines system know-how, application understanding and strong, mutually beneficial customer relationships.

One illustration of the P2S approach can be seen in the comprehensive offering that Infineon has developed for cordless power tools. Bringing together technologies for charging, battery management and BLDC motor drive and control – including MOSFETs, gate drivers, microcontrollers, sensors and AC/DC controllers – this offering extends to reference designs, demonstration boards and a complete solution for a 1kW cordless power drill. The latter provides significant design flexibility and ease of use as the demo can be separated into three parts, namely a power PCB, a control PCB and a capacitor PCB.

Finally, it is worth noting that the strategy to provide customers with access to as many solutions as possible was also one of the drivers behind Infineon's recent acquisition of power semiconductor manufacturer International Rectifier. As well as expanding the product portfolio, extending the manufacturing footprint, supporting a stronger regional presence and delivering greater distribution strength, this acquisition accelerates the strategic evolution 'from product thinking to system understanding'. This includes extending system know-how in efficient power management and expanding Infineon's expertise in a variety of technologies including next-generation gallium nitride compound semiconductors.

www.infineon.com

Silicon Carbide: our sole focus, your superior solution.



The only standard gate-drive SiC device – anywhere.



Our name says it all. At United Silicon Carbide, Inc, we are solely devoted to bringing you the best and most efficient Silicon Carbide (SiC) power devices available in the marketplace. This month USCi is releasing an advanced silicon carbide cascode product line. These devices deliver the performance of silicon carbide with the ease of use of low voltage silicon.

United Silicon Carbide's cascode products co-package xJ series high-performance SiC JFETs with a cascode optimized MOSFET to produce the only standard gate drive SiC device in the market today. These normally off devices exhibit ultra-low on resistance and gate charge, but also the best reverse recovery characteristics of any device of a similar current rating. These devices are excellent for switching inductive loads in bridge configurations with boot strap or floating high side drive.

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ELECTRONICS INDUSTRY DIGEST

By Aubrey Dunford, Europartners



SEMICONDUCTORS

Worldwide sales of semiconductors reached \$ 28.2 billion in May 2015, an increase of 5.1 percent from May 2014 and of 2.1 percent from April 2015, so the WSTS.

Year to-year sales have now increased for 25 straight months, and month-to-month sales increased for the first time in six months. European semiconductor sales reached \$ 2.873 billion in May 2015. In particular, sales of discrete semiconductor devices were up 3.7 percent from April, diodes up 5 percent and optoelectronics up 6.7 percent.

Worldwide semiconductor revenue is forecast to reach \$ 348 billion in 2015, a 2.2 percent increase from 2014, but down from the previous quarter's forecast of 4.0 percent growth, so Gartner. The outlook for the major applications that drive the semiconductor market, including PCs, smartphones, and tablets, have all been revised downward.

Semiconductor companies are spending more than ever to stay competitive. In 2015, the total amount spent is forecast to be \$ 68.7 billion, up 9 percent from 2014, so Semico Research. This breaks the previous record set in 2011 at \$ 63.8 billion. Globalfoundries has completed its acquisition of IBM's Microelectronics business. The deal strengthens the company's workforce, adding decades of experience and expertise in semiconductor development, device expertise, design, and manufacturing and more than 16,000 patents and applications. The acquisition includes an exclusive commitment to supply IBM with some of the world's most advanced semiconductor processor solutions for the next 10 years.

Transphorm, an early stage semiconductor company focused on redefining power conversion, announced a \$ 70 M investment round led by global investment firm KKR. Transphorm believes that there is a large market for its products as its ultra-efficient power devices and modules can eliminate

more than 40 percent of all electric conversion losses by using gallium-nitride (GaN). Its power conversion devices and modules simplify the design and manufacturing of motor drives, power supplies and inverters for solar panels and electric vehicles.

Exagan, a French start-up involved in gallium-nitride (GaN) semiconductor technology that enables smaller and more efficient electrical converters, has raised € 5.7 M in first-round financing that will be used to produce high speed power switching devices on 200mm wafers. Following Exagan's recent announcement of an agreement with X-FAB to produce devices on 200mm wafers, the financing will help support its mission of becoming Europe's primary supplier of GaN-based power switches.

Exagan, based in Grenoble with a branch office in Toulouse, was spun off by Leti and Soitec in 2014 and licenses materials and technology from both organizations.

OPTOELECTRONICS

Merck, a German company for high-tech products in healthcare, life science and performance materials, laid the cornerstone for a new OLED materials production plant in Darmstadt. Production of high-purity OLED materials for use in displays and lighting systems is scheduled to start in July 2016.

OTHER COMPONENTS

The German expert organization Dekra is taking over the testing company AT4 wireless in Malaga, Spain. With this, Dekra is completing its range of testing services for wireless communication and electromagnetic compatibility (EMC). Dekra is thereby securing key expertise for the future trends Industry 4.0 and Automotive 4.0. AT4 wireless has a workforce of 285 employees and has laboratories in Spain, Chile, USA and Taiwan.

Metrawatt International has announced the purchase of Seaward Group. Seaward is a manufacturer of electronic test and measurement instruments used in the appliance testing, bio medical, renewable energy, electronics manufacturing and utility markets.

DISTRIBUTION

Mouser Electronics has entered into a global distribution agreement with Dave Embedded Systems — a supplier focused on the design, manufacturing and sales of miniaturized Systems on Modules (SOMs) and other hardware and software embedded solutions for Linux, Windows and Android platforms.

UK-based Ismosys and Germany-based ActiveREP, both long established independent sales and marketing organisations, have signed a strategic partnership which will allow them to maximise their mutual resources for the benefit of their partners and customers they serve.

The partnership will be launched initially focusing on the CUI product line where Ismosys is already engaged as a representative throughout Europe.

Richardson Electronics announced a new distribution agreement with StarPower Europe, the European subsidiary of a power module company headquartered in Jiaxing, China. This global agreement supports the expansion of StarPower's products to new customers and opportunities outside of China. StarPower Europe recently announced building a European development centre in Nuremberg, Germany.

This is the comprehensive power related extract from the «Electronics Industry Digest», the successor of The Lennox Report. For a full subscription of the report contact:

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Biricha Lecture Notes on Analog and Digital Power Supply Design

Part 2.C Peak Current Mode PSU Compensator Design

In the previous article we discussed how to design a compensator under voltage mode control. In this article we are going to look at how to compensate a peak current mode controlled Forward type converter. Peak current mode control has some advantages over voltage mode control including inherent current limiting, better line regulation and easier current sharing across multiple power stages [1].

For now we will look at hard switched non-isolated converters only and the design method presented here can be applied to all Forward type converters under peak current mode control without an opto-coupler. We will discuss isolation and other topologies in later articles.

By Dr Michael Hallworth and Dr Ali Shirsavar, Biricha Digital Power Ltd

Peak current mode operation

Before we begin our compensator design, let us first look at how peak current mode control (PCMC) works.

The operation of the converter, at first glance, is quite simple. The circuit for a PCMC Buck converter is shown in Figure 1.

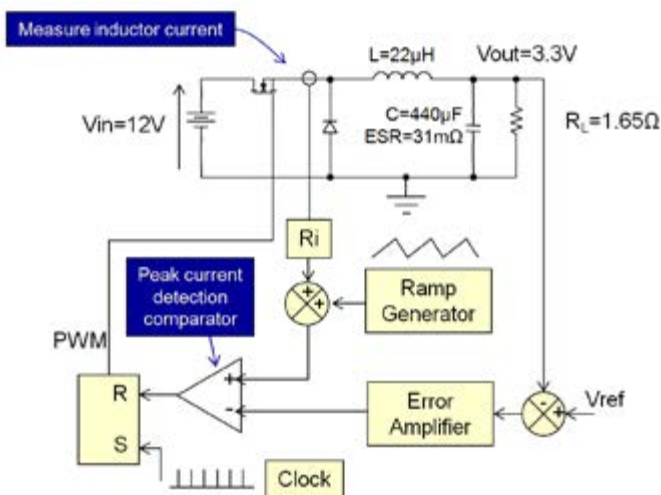


Figure 1: PCMC of a Buck Converter

As you can see, the switch in this Buck converter is being controlled by a set-reset flip-flop/latch. At the beginning of our switching period, the clock pulse sets the output of the SR latch high. This turns on the switch at the frequency of the clock which is therefore our switching frequency.

With PCMC, we typically measure the switch current. The peak of this, is the same as the peak of the inductor current scaled by the current sense gain R_i . If there is a power transformer, then of course

this will also scale the current. As you can see from Figure 1, this is fed into a peak current detection comparator. The other input to the comparator is the demand value of the peak of our current.

In other words we are comparing the current that we want (our demand current) with the current that we are actually getting (our measured current). As soon as the actual measured current becomes equal to the current that we want, the output of the comparator goes high, resets the latch and therefore turns off the switch. During the next cycle our demand current may change, and that would mean that we will turn off the switch as soon as the actual current hits the new demand value. Thus we are controlling the peak of our inductor current.

But how do we set the demand value of our current? Looking at Figure 1 again – we can see that we also have a voltage loop formed by the error amplifier and its compensating components. The output of this part of our circuit creates the demand value of our current. In short, we compare our actual output voltage with our demand output voltage and the error or the difference between these two (after voltage loop compensation) sets our demand value of current. Our job therefore is to calculate the poles and zeros and thus the component values of this compensator.

Sub-harmonic Oscillations and Slope Compensation

One final part we have not discussed in Figure 1 is the Ramp Generator block. If we set our input voltage to minimum and our load to maximum and look at the PWM on the oscilloscope and see the PWM duty cycle trace going from thick pulse to thin pulse to thick pulse repeatedly then our converter would be experiencing sub-harmonic oscillations. This is one of the headaches of current mode.

Without getting into too much detail, the problem is that in current mode, there is effectively a complex conjugate pair of poles at half the switching frequency F_s [2] and therefore at this frequency we will have a resonant bump; this is shown by the dashed green line in Figure 3. As the duty increases so does the Q of this double pole,

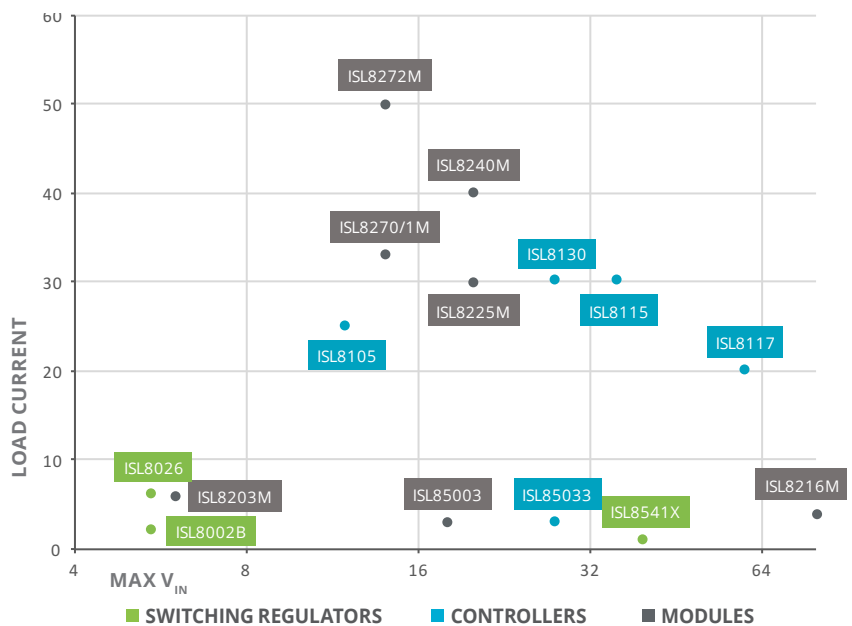
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this makes the sub-harmonic oscillations worse. Furthermore, if the gain crosses the 0dB axis at half the switching frequency your power supply will be unstable.

In order to avoid this, all we need to do is add a ramp to our measured current so that, if these oscillations were to occur, the switch would turn off a little bit earlier than it would otherwise (shown by dashed red area in Figure 2). This will damp any subharmonic oscillations and cause them to decay. This is the job of the ramp generator block in Figure 1. Please note that in many modern chips this ramp is added internally so you don't have to add it yourself.

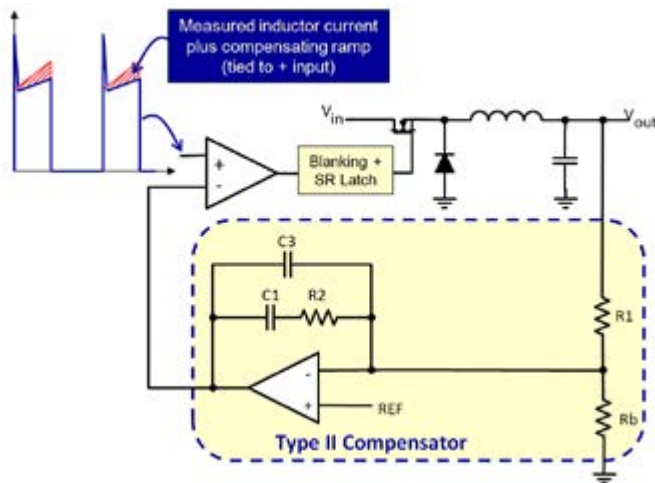


Figure 2 – Type II compensator

Peak Current Mode Compensator Design

For peak current mode control the error amplifier that we use is typically a Type II compensator. The circuit for the Type II compensator is given in Figure 2. The poles and zeros are set by the capacitors and resistors in the feedback network around the compensator. This compensator type along with the concept of poles and zeros has been covered in our previous articles.

From the previous articles we know the transfer function Hc(s) and equations relating the poles and zeros to component values are as follows:

$$H_c(s) = \frac{\omega_{CP0}}{s} \frac{\left(\frac{s}{\omega_{CZ1}} + 1\right)}{\left(\frac{s}{\omega_{CP1}} + 1\right)} \tag{Equation 1}$$

Here wcp0 and wcp1 are the compensator's poles and wcz1 is the compensator zero and our job is to calculate them so that we can calculate the component values from the equations below. Please note that these poles/zeros are in radians per second but we usually work in Hz so please don't forget to convert them if needed.

$$\omega_{CP0} = \frac{1}{R_1 (C_1 + C_3)}; \omega_{CP1} = \frac{(C_1 + C_3)}{R_2 C_1 C_3}$$

$$\omega_{CZ1} = \frac{1}{R_2 C_1}$$

Biricha Digital's automated power supply design software (Biricha WDS) automatically designs optimised compensators as discussed in the previous articles. However, if your transient response requirements are not very stringent, you can design a reasonable and stable compensator for the Forward topologies by following the steps outlined below.

Below are step-by-step guidelines on how to quickly design the compensator for this converter. All the values that we need are shown in Figure 1.

Step1: Determine the amount added ramp required

If your chip does not have internal ramp generation, many engineers work out the amount of ramp to add empirically i.e. set the converter to maximum duty and add enough ramp until oscillations do not occur. Alternatively you can calculate the required amount of slope compensation (the peak-to-peak height of the compensating ramp added to the sensed current) using the following equation which is valid for all Forward type converters and is based on [2].

$$V_{PP} = \frac{\left(\frac{1}{\pi} - 0.5 + D\right) R_i T_s V_{in} n^2}{L} \tag{Equation 2}$$

Where D is our steady state duty cycle, Ri is our current sense gain, Ts is the switching period, Vin is our input voltage, n is our transformer turns ratio (set to 1 for Buck converters) and L is the output inductance.

This will have the effect of damping the pair of complex conjugate poles at half the switching frequency such that they have a Q of 1. As mentioned earlier, these poles are responsible for the undesirable subharmonic oscillations which are an inherent characteristic of PCMC.

Step2: Determine plant Bode plot

You don't actually need to plot this at all but it is nice to visualize what is going on. There are many models for peak current mode converters, here we have used the popular Ridley model. For detailed mathematical analysis and equations please see [2], [3].

Figure 3 shows the Bode plot of our PCMC Buck converter. As you can see we have some low frequency/DC gain, one low frequency real pole, an ESR zero and a pair of complex conjugate poles at half Fs. The plot will be the same overall shape for all hard switched Forward type converters. However, the plant's low frequency pole and ESR zero will be different but the complex conjugate pair of poles will always stay at half Fs. (Please see Article 1A for our discussion of transfer functions).

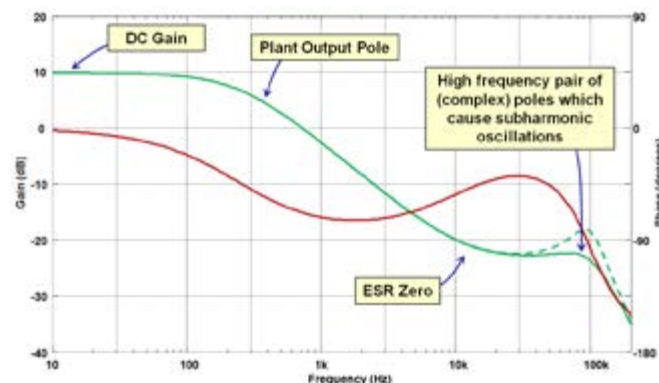


Figure 3 – Bode plot of plant stage for a PCMC Buck Converter. Green trace is the gain, red trace is the phase.

The dashed green line shows the complex conjugate poles at half the switching frequency without slope compensation. The peaking would be more pronounced with larger duty cycles. The solid trace shows what happens to these poles when we apply the slope compensation calculated in Step 1.

As you can see unlike voltage mode control discussed in the previous article, we only have a single low frequency plant pole, followed by a zero formed by the parasitic equivalent series resistance (ESR) of our electrolytic output capacitance.

Step 3: Calculate Type II Compensator Poles/Zeros

The method presented here is an approximate method to allow you to quickly calculate the poles and zeros for a compensator with relatively good performance for a reasonable crossover frequency (i.e. 1/10th of the switching frequency).

Our power supply design software (Biricha WDS) uses optimal algorithms, however, in this short article we will opt for this approximate method so that you can perform the calculations by hand (or perhaps with the help of your preferred math package).

You can see from the compensator's transfer function that we have 1 pole, 1 zero and 1 pole at origin. Please don't forget to change to Hz (we have changed w to f in the following equations to denote this change). To get reasonable performance:

1 – Place 1 compensator pole at the ESR zero frequency to cancel the plant's ESR zero:

$$f_{CP1} = \frac{1}{2\pi ESR C} = 11.6kHz. \quad \text{Equation 3}$$

2 – Place the compensator zero at 1/5th of your desired crossover frequency to give you a phase boost around crossover (remember zeros give you a phase boost – see Article 1A) F_x is the desired cross-over frequency. In our case let us design for $F_x = 10kHz$:

$$f_{CZ1} = \frac{F_x}{5} = 2kHz \quad \text{Equation 4}$$

3 – Finally we place the pole at origin at the frequency given in Equation 5.

$$f_{cp0} = \frac{A_1 A_2 A_3}{2\pi n L R_L} \quad \text{Equation 5}$$

Where A_1 , A_2 and A_3 are:

$$A_1 = 1.23 F_x R_L \left(L + \frac{R_L T_s}{\pi} \right)$$

$$A_2 = \sqrt{1 - 4F_x^2 T_s^2 + 16F_x^4 T_s^4}$$

$$A_3 = \sqrt{1 + \frac{4\pi^4 C^2 F_x^2 L^2 R_L^2}{(L\pi + R_L T_s)^2}}$$

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Please don't be intimidated by the large equations - there is nothing in there that we don't know. Evaluating this equation for a crossover frequency of 10kHz gives us:

$$f_{cp0} = 25.85\text{kHz}$$

Step 3: Calculate compensator component values

Now that we know the positions of our compensator poles and zeros, we can use the equations above to calculate component values for our compensator.

As we discussed in the previous voltage mode article, you can calculate R1 and Rb based on the current that you are willing to allow through them and the reference voltage needed on the controller IC. Please refer to Article 2B for more information. By allowing 1mA of current through this pot and using the standard potential divider equations and Ohm's law we can calculate:

$$R_1 = 750\Omega, \quad R_B = 2.55k\Omega$$

2 - Now that we know R1, by rearranging the equations for the poles and zeros above and solving for the component values we can calculate the values of C1, C3 and R2 using the equations below (please don't forget that these equations use the poles/zeros in rad/sec so we need to convert them from Hz).

$$C_1 = \frac{\omega_{CP1} - \omega_{CZ1}}{R_1 \omega_{CP0} \omega_{CP1}}$$

$$C_3 = \frac{\omega_{CZ1}}{R_1 \omega_{CP0} \omega_{CP1}}$$

$$R_2 = \frac{R_1 \omega_{CP0} \omega_{CP1}}{(\omega_{CP1} - \omega_{CZ1}) \omega_{CZ1}}$$

Evaluating these equations gives us:

$$C_1 = 6.8nF, \quad C_3 = 1.4nF, \quad R_2 = 11.7k\Omega$$

We can easily use WDS in "manual pole/zero placement" mode to verify our calculations. WDS provides us with all the important stability parameters as well the Bode plot. WDS Bode plot for our design is shown in Figure 4 and the stability information is shown in Figure 5.

From Figures 4 and 5, we can see that we have achieved a crossover frequency of 10kHz as desired and a phase margin of 74 degrees. Slope at crossover is -20db/decade and our gain margin is better than 20dB. Thus we have designed a very stable power supply with a respectable crossover frequency and large phase margin.

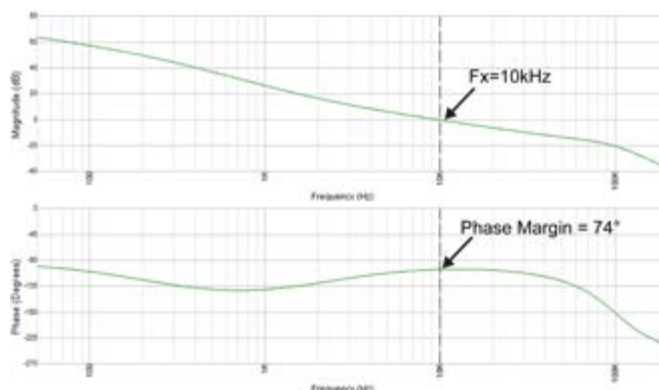


Figure 4: Simulated loop bode from Biricha WDS

Stability	Fx	P.m.	G.m.	Slope at Fx
Nominal	10000Hz	74°	20dB	-20.6dB/dec

Figure 5: Stability data from WDS

Concluding Remarks

In this article, we discussed how to design a compensator for all hard switched Forward type peak current mode converters (without optocoupler feedback). An approximate method has been presented that will give relatively good results in most cases. The advantage of the method presented here is that it is quick to calculate but we do not have any control over the phase margin. We also included a complete numerical example down to component value selection.

Things to Try

- 1 - Download a copy of Biricha WDS PSU Design software from www.biricha.com
- 2 - Attend one of our Analog Power Supply Design workshops

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- [1] Biricha's "Analog Power Supply Design Workshop" Manual
- [2] Ridley, R. B., A New Continuous-Time Model for Current-Mode Control
IEEE Transactions on Power Electronics, April, 1991, pp. 271-280.
- [3] Microcontroller Based Peak Current Mode Control, PhD Thesis, M. Hallworth

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Paralleling SiC Cascodes for High Performance, High Power Systems

Silicon carbide cascodes have no inherent limitations that impede their safe parallel operation. The paralleling of USCI's SiC cascodes in TO-247 packages enables efficient and reliable high power systems.

By Matt O'Grady, Ke Zhu, Xueqing Li, and John Bendel; USCI

The robustness and switching behavior of USCI's cascodes were discussed in articles in the May and June 2015 issues of Bodo's Power Systems [1], [2]. This article outlines the considerations for paralleling SiC cascodes for high performance, high power systems and provides tips for parallel cascode implementation.

The impetus for power switch paralleling is usually the need for greater current and power capability than can be achieved with a single power switch. Use of paralleled TO-247 cascodes also provides flexibility in system implementation that can be hard to achieve with prepackaged modules. This flexibility enables optimization of tradeoffs between switching and conduction losses, thermal design, cost, and system performance based on the requirements of a specific circuit topology and application. To realize these benefits, SiC cascodes can be paralleled with the same basic approach used to parallel silicon MOSFETs.

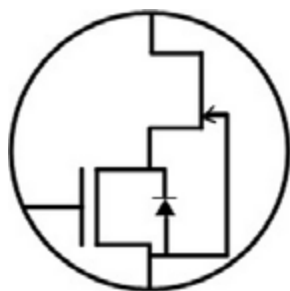


Figure 1: USCI cascode combines a Si MOSFET with SiC JFET in a single TO-247 package

A primary difference between operating a single power switch and multiple parallel switches is the need to account for any current and power dissipation imbalance when verifying that the device is used within its safe operating area. For SiC cascodes, the level of current and power dissipation imbalance is minimal and the devices may be used without significant derating provided some basic precautions are followed. In particular, adequate consideration should be given to gate drive design and power circuit layout to minimize sources of imbalance.

The following sections discuss the parallel gate drive scheme; current imbalance during conduction, turn-on, and turn-off; and practical tips for implementing paralleled SiC cascodes. Measurement results of current sharing of United Silicon Carbide's UJC1206K cascode are included. These measurements were made with a shunt resistor at the source node and include the gate current in addition to the drain current. For clarity, the case of two parallel cascodes is illustrated. The concepts are easily extended to paralleling of larger numbers of devices once they are understood for the two switch case.

Gate Drive for Parallel Cascodes

A notional schematic of a suitable gate driver circuit for parallel cascodes is shown in Figure 2. A separate R_{Gon} and R_{Goff} are used so that the turn-on and turn-off switching transitions can be independently controlled. For parallel operation, the most important gate drive consideration is that separate gate resistors be used for each of the paralleled devices. When paralleling only a few cascodes the optimum design uses a single gate driver for all of the paralleled devices. On the other hand, when driving a large number of parallel cascodes separate buffers for each switch will enable compact gate control loops which will reduce gate loop inductance. The layout of the cascodes themselves should allow for low and well matched stray parasitic inductance, particularly in the source connection. With low source inductance a good source Kelvin connection can be used at the cascode device leads.

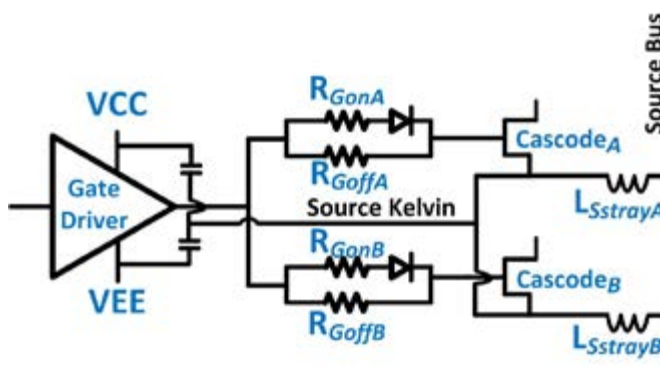


Figure 2: Notional Schematic of Parallel Gate Drive

Power Balance During Conduction

In steady state conduction, paralleled cascodes share a common V_{DS} and each cascode conducts current in proportion to its R_{DSon} . Like silicon MOSFETs, SiC cascodes have a positive R_{DSon} versus temperature characteristic (Figure 3). The positive temperature characteristic performs an important role as it provides negative feedback from a cascode's power dissipation to the amount of load current it conducts in parallel operation.

To understand this feedback effect, consider two cascodes, denoted Cascode A and Cascode B, biased at a fixed V_{DS} . At startup, if Cascode A has lower R_{DSon} than Cascode B, Cascode A will conduct a higher percentage of the load current than Cascode B. This will increase Cascode A's temperature relative to Cascode B. The higher temperature increase for Cascode A leads to higher R_{DSon} increase

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for Cascode A which lowers the percentage of load current through it. The end result is more balanced current sharing in steady state between Cascodes A and B. Notably, this behavior prevents thermal runaway which can occur with other switch technologies due to their positive on-resistance temperature characteristics.

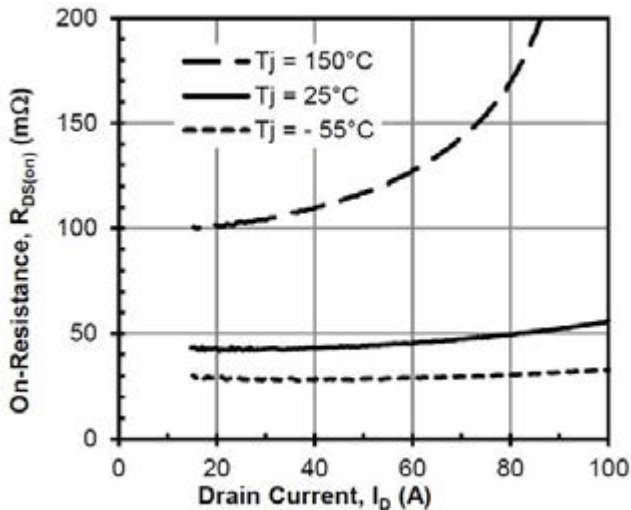
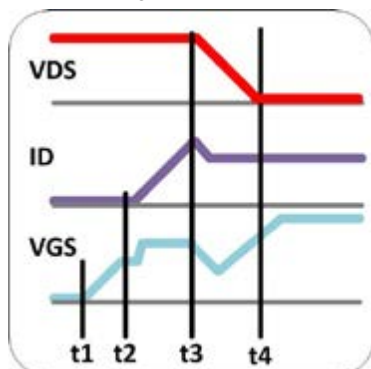


Figure 3: SiC Cascode $R_{DS(on)}$ versus Temperature Characteristic

To determine the startup and steady state conduction current sharing in detail the datasheet $R_{DS(on)}$ temperature characteristic, the device thermal impedance, and the parallel switch voltage and current conditions can be used to model the interdependence of $R_{DS(on)}$, temperature, and current sharing. This same analysis can be used to study sensitivity of the device conduction to any expected variations in thermal resistance. For this electrical and thermal analysis, the device datasheet thermal impedance information can be used as a starting point but final modeling should include the actual system thermal impedance as determined by simulation and measurement of the thermal characteristics of the actual system.

Power Balance During Switching

Turn-on: During cascode turn-on (illustrated in Figure 4), at $t_1 V_{GS}$ begins to rise at a rate determined by the time constant formed by the gate resistor and the cascode input capacitance ($R_{Gon}C_{iss}$) and the gate driver power supply voltage. When the V_{GS} value exceeds the cascode threshold voltage at t_2 , the device turns on and after a small delay the drain current increases at a rate influenced by the gate resistor and source inductance. The drain current di/dt causes a voltage rise across internal package inductance which is capacitively coupled from the source to the gate and reflected in the V_{GS} waveform as measured at the TO-247 leads. At t_3 , the drain current is fully commutated and V_{DS} falls. The turn-on switching loss is the integrated product of V_{DS} and I_D over the switching interval.



For paralleled devices with matched stray inductance, V_{DS} falls in parallel for all the cascades and does not affect the power balance between devices; any turn-on power imbalance results from differences in current sharing during the switching

Figure 4: Cascode turn-on behavior for a single device

time. Also, when paralleled cascades are turned on, matching of the di/dt rate can be assured by matching the parasitic source inductance and gate resistance. The source inductance matching can be controlled through identical layout from each cascode source lead to the associated bus. The gate resistors can be easily matched with available low cost, high tolerance resistors.

With common V_{DS} falling and matched di/dt , the potential for mismatch in the turn-on loss still exists if there is a skew in turn-on delay between the paralleled switches. Using a single gate driver helps minimize any turn-on delay skew by eliminating potential gate driver propagation delay variations. As discussed above, turn-on begins

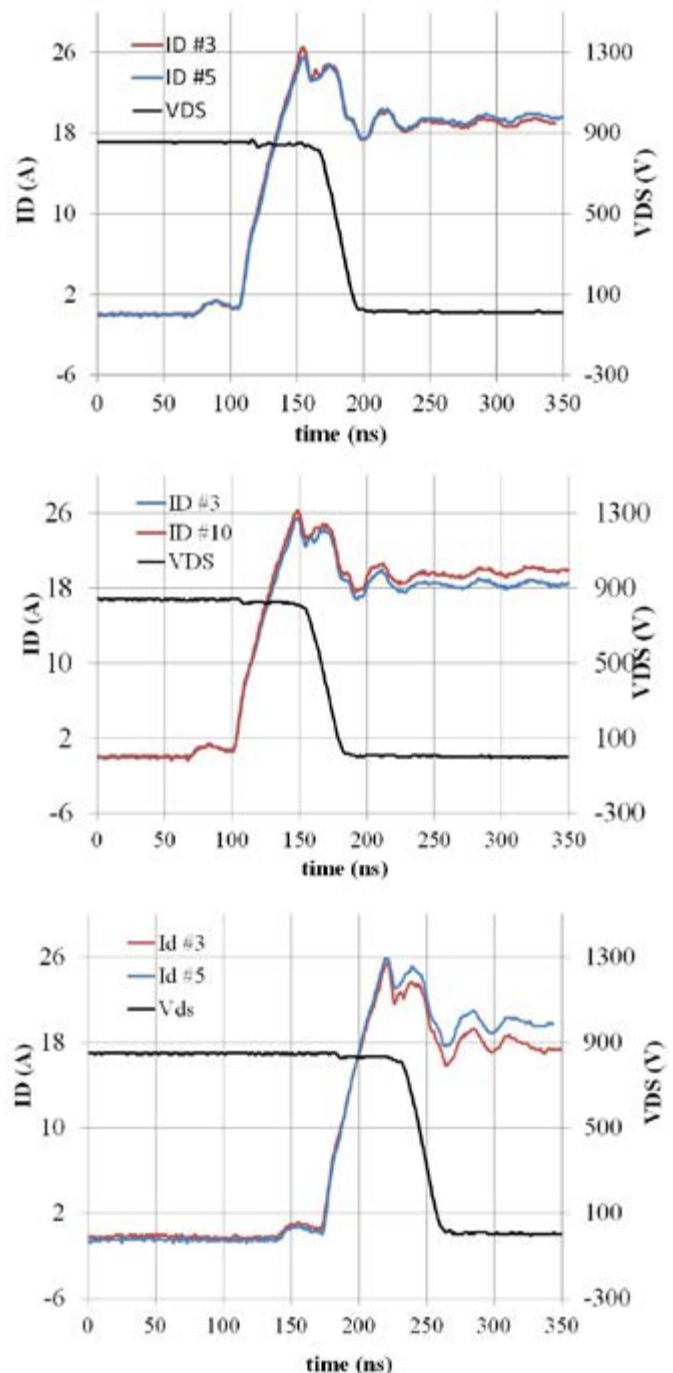


Figure 5. Turn-on current sharing at 850 V, 18A: top) matched cascodes, middle) mismatched threshold voltages, and bottom) 40 °C temperature offset between devices.

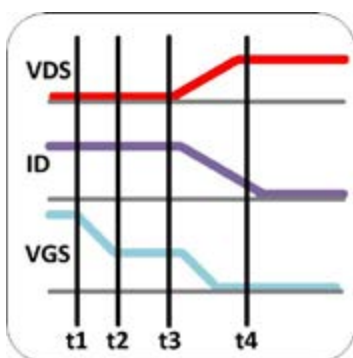
when V_{GS} exceeds the cascode threshold voltage and the rate of V_{GS} rise prior to cascode turn-on is controlled by the time constant $R_{Gon}C_{iss}$ and the gate driver power supply voltage. Since the cascode C_{iss} is well matched between devices, the gate resistors can have tight tolerance, and the gate driver power supply voltage is common across paralleled devices the V_{GS} rises uniformly for paralleled devices prior to turn-on. Therefore the primary contributor to turn-on delay skew is the variation in cascode threshold voltage.

Figure 5 shows the turn-on current sharing for two well matched cascodes and two cascodes which were selected as they had the highest threshold variation (150 mV) in the samples tested. The third plot in Figure 5 shows the turn-on when there is large temperature imbalance of 25 °C and 65 °C between the devices under test. As shown, even with variation in threshold voltages and temperature, the turn-on current sharing, and therefore switching loss, is very well matched between devices. At the beginning of the conduction period a significant difference exists in the current load as the results are from a double pulse test which does not allow sufficient time for the RDSon temperature dependence balancing to take effect.

The small impact of threshold voltage variation results from the low variation in cascode threshold voltage (+/- 200 mV typical) and the gate loop behavior which dampens the effect of variations in device characteristics.

For example, consider the case where Cascode A and Cascode B have threshold voltages of 4.3 and 4.7 V respectively. During parallel turn-on, the V_{GS} of Cascode A will reach threshold first and it will begin to turn-on. As soon as it turns on the di/dt across the inductance internal to the Cascode A package causes an increase in the V_{GS} as measured at the pins of the TO-247 terminals. This causes a drop in the gate current due to the lower voltage across the gate resistor. Meanwhile, Cascode B still has a relatively low gate voltage and its V_{GS} continues to slew with higher current. Based on the slew rate of the gate driver near threshold, the delay between the turn-on of Cascode A and Cascode B for the large threshold voltage variation of 400 mV is only 0.6 ns. With a di/dt of 1 A/ns this leads to less than 600 mA of current mismatch during turn-on due to threshold mismatch. For a 20 A load current this results in a 6% mismatch in current sharing. For lower load currents, the mismatch percentage is higher but is not usually of concern as it does not affect the safe operating area analysis due to operation well within the specified device limits.

Turn-off: During turn-off (illustrated in Figure 6) at t_1 the gate driver switches low and V_{GS} begins to fall towards the cascode threshold voltage. At t_2 , V_{GS} plateaus as the MOSFET inside the cascode reaches its miller plateau. At t_3 , the delay time ends and the V_{DS} transition begins. The overall effect of the turn-off delay interval on the turn-off loss imbalance is analogous to the turn-on case: close




matching of C_{iss} , gate resistor, and gate driver supply voltage results in the threshold voltage mismatch dominating the turn-off delay mismatch and the end result is only a marginal effect on the switching loss imbalance. However, in the case of turn-off there are some additional considerations.

Figure 6: Turn-off switching behavior


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First, at the start of turn-off there may already be a current imbalance due to differences in R_{DSon} between paralleled devices. This difference in the conduction current will lead to a different current level in the parallel devices at the start of the turn-off process. As shown in Figure 6, V_{DS} rises during the turn-off current transition so this current imbalance creates a switching loss imbalance between the paralleled devices.

Secondly, at high current levels and high dv/dt the cascode's internal response is underdamped which can lead to turn-off current ringing. The ringing does not necessarily lead to high cascode loss but it is coupled to the V_{GS} signal at the TO-247 leads through the common source inductance and it may be unacceptable at the system level. Any current ringing may also lead to imbalanced operation between paralleled cascodes as the di/dt it generates interacts with stray inductances which may not be perfectly matched. If the combination of high current and stray inductance lead to this problem it can be controlled through increase in the value of R_{Goff} or the addition of a small capacitor between the gate and drain terminals of the cascode. In general, the additional C_{GD} is the preferred method as it will provide good dv/dt control without adding to the total turn-off delay or impacting turn-off delay skew as would happen with large values of R_{Goff} .

The measured turn-off behavior is shown in Figure 7 for pairs of devices with matched (top) and mismatched (middle) thresholds. A plot (bottom) is also included where one device is heated to 65 °C to generate a current imbalance to illustrate the potential current ringing behavior.

When considering the impact of turn-off loss imbalance it is important to consider that the turn-off switching loss magnitude is much less than the turn-on and conduction losses in hard switched applica-

tions. This means that even a high turn-off loss imbalance may not significantly affect the overall power imbalance. Also, any imbalance in current sharing during the turn-off interval is short lived and unlikely to exceed the devices safe operating conditions.

Implementation Tips

The cascode's positive R_{DSon} temperature dependence helps ensure good current and power sharing during conduction. A common heat spreader or heatsink for paralleled switches will help leverage this effect. As with silicon MOSFETs, there can be a residual conduction

current imbalance which should be accounted for when verifying device operation is within the specified safe operating area.

Turn-on current and power imbalance is minimal and depends primarily on the MOSFET threshold voltage variation. The current imbalance will be limited to the di/dt multiplied by the turn-on delay mismatch value. With matched switch leg layouts, a typical threshold voltage mismatch of ± 200 mV, $R_{Gon} = 5 \Omega$, and a 12 V gate driver supply will lead to a turn-on delay mismatch of less than 0.6 ns. With a turn-on di/dt of 1 A/ns the resulting current mismatch is less than 600 mA.

Cascode turn-off loss is more susceptible to mismatches in percentage terms than turn-on losses due to the added effect of differences in conduction current and coincident voltage rise and current fall times. In extreme cases the turn-off may exhibit current ringing which is also seen in the V_{GS} signal as measured at the TO-247 leads. To control the current ringing, large gate turn-off resistors values may be used.

While the turn-off loss sharing may have a significant percentage mismatch between devices the turn-off loss magnitude is low compared to turn-on and conduction losses so the overall impact of turn-off balance on device power dissipation imbalance may not be significant.

For a small number of parallel devices a single gate driver with separate gate resistors for each switch will provide the best current and power balance. For large numbers of devices in parallel, gate drive buffers for each switch may lower the gate loop area and inductance. If separate gate drive buffers are used a simple single stage common emitter buffer should be considered over a complete gate driver IC due to the potential contribution of gate drive propagation delay skew.

In the power loop layout the TO-247 packages can be closely spaced with DC decoupling capacitors to lower the overall power loop inductance. For best matching, variations in the layout that can lead to difference in stray inductance should be avoided, especially at the source lead.

Conclusion

Theory and lab testing demonstrate the inherent capability of SiC cascodes to be safely paralleled. Due to the characteristic behavior and low production parametric variations of USCI's cascodes part screening is not required for paralleled operation. The worst case current and loss imbalance can be determined for a given system and operation within the cascode safe operating area can be verified in order to avoid over margining of designs.

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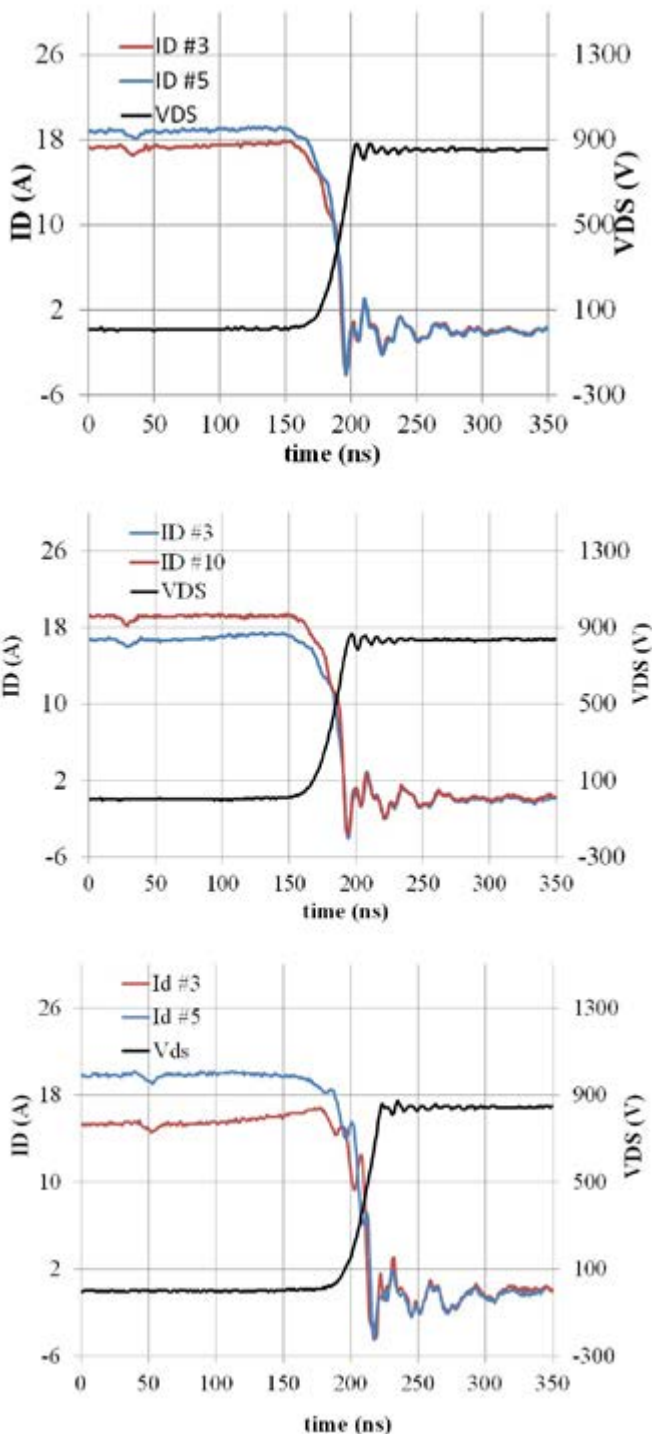
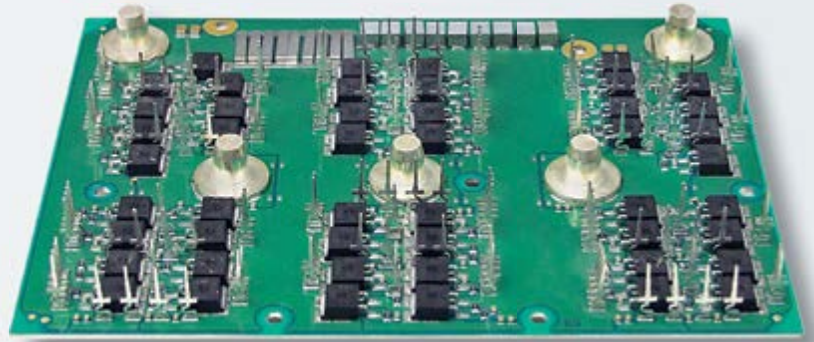


Figure 7: Turn-off current sharing at 850 V, 18A: top) matched devices, middle) mismatched devices, bottom) 40 °C temperature offset between devices



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Advances in SiC MOSFET Technology Drive Down Cost of High-Bay and Outdoor Lighting Fixtures

Single stage topologies are the designer's choice for lower power LED drivers. A new study of Cree C3M technology suggests the same single-stage topology could be extended well beyond what was previously possible.

By Marcelo Schupbach, PhD., Technical Marketing Manager and Edgar Ayerbe, Product Marketing Engineer, Cree, Inc.

For high-bay and outdoor lighting fixtures, the cost of the LED driver electronics is reported to be 17% of the total fixture cost. An additional 40% of the fixture cost is contributed by the mechanical, thermal, and electrical portions of the fixture [1], which help support the weight and volume of the LED driver, as well as protect the driver against surge events. New innovations in MOSFET technology enable rugged LED drivers that are also smaller, lighter, and cheaper than existing devices, bringing significant cost reductions to high-bay and outdoor lighting fixtures.

900V C3M™ Technology Outshines the Competition

This May, Cree introduced a new 900V class of SiC power MOSFETs that are well suited for high efficiency switch-mode power supply applications, such as LED lighting. The new SiC MOSFET family is based on Cree's third generation planar SiC technology. Design improvements in this generation of SiC MOSFETs include: a smaller cell pitch, an optimized cell structure, and increased blocking-layer doping levels that minimize resistances. The median specific on-resistance of the 900V SiC MOSFET is 2.3 mΩ·cm², which is a 42% reduction over the previous generation, and the lead product (C3M0065090D) features the lowest on-resistance rating (65mΩ) of any 900V MOSFET device currently available on the market. The 900V SiC MOSFET only shows a 46% increase in resistance when the junction temperature is increased from 25°C to 150°C, and the on-resistance of the SiC MOSFET is 3x lower than 900V CoolMOS® technology at a junction temperature of 150°C (Figure 1). This results in lower conduction losses and a higher current rating for the SiC MOSFET when operating at elevated temperatures. The transconductance of the 900V SiC MOSFET is improved by engineering the MOS channel structure so the device is fully turned on at VGS = +15V at 25°C and +12V at 150°C (Figure 1). In power supply applications, this eases the gate drive requirements for 900V SiC MOSFETs when compared to previous generations of SiC MOSFETs, which required +18 to +20V gate bias for full enhancement. Additional improvements were made to the high-voltage reliability of the SiC MOSFET by minimizing the internal electric fields under reverse bias.

Shedding New Light on LED Driver Designs

Single-stage topologies (such as the quasi-resonant flyback shown in Figure 2a) are widely used in low power (<100W) LED lighting applications, primarily due to their low cost, simplicity (i.e., low part count), and acceptable performance. At higher power levels, however, these single-stage topologies become impractical, forcing designers to increase the complexity of their designs (e.g., increasing switch count). This increases the overall driver cost and erodes the price/performance point that single-stage topologies are able to achieve. At power levels above 100W, two-stage topologies begin to deliver a better price/performance solution than single-stage topologies despite their increased complexity and part count. Consequently, higher power LED drivers are typically implemented using two-stage topologies, such as the power factor correction (PFC) boost converter plus LLC resonant half-bridge shown in Figure 2b.

The power semiconductor switch performance within the driver has a significant impact on where the price/performance boundary between single- and two-stage topology is established. For current silicon (Si)

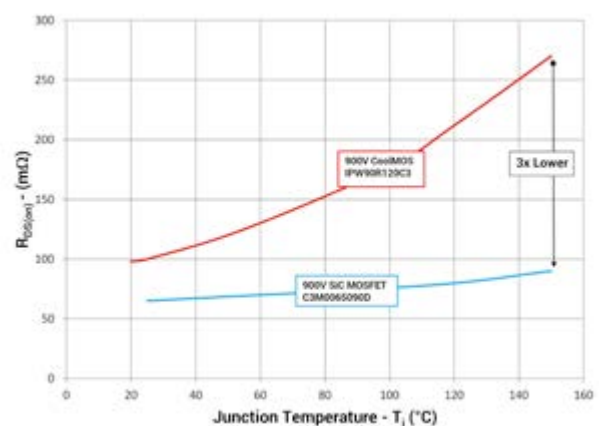
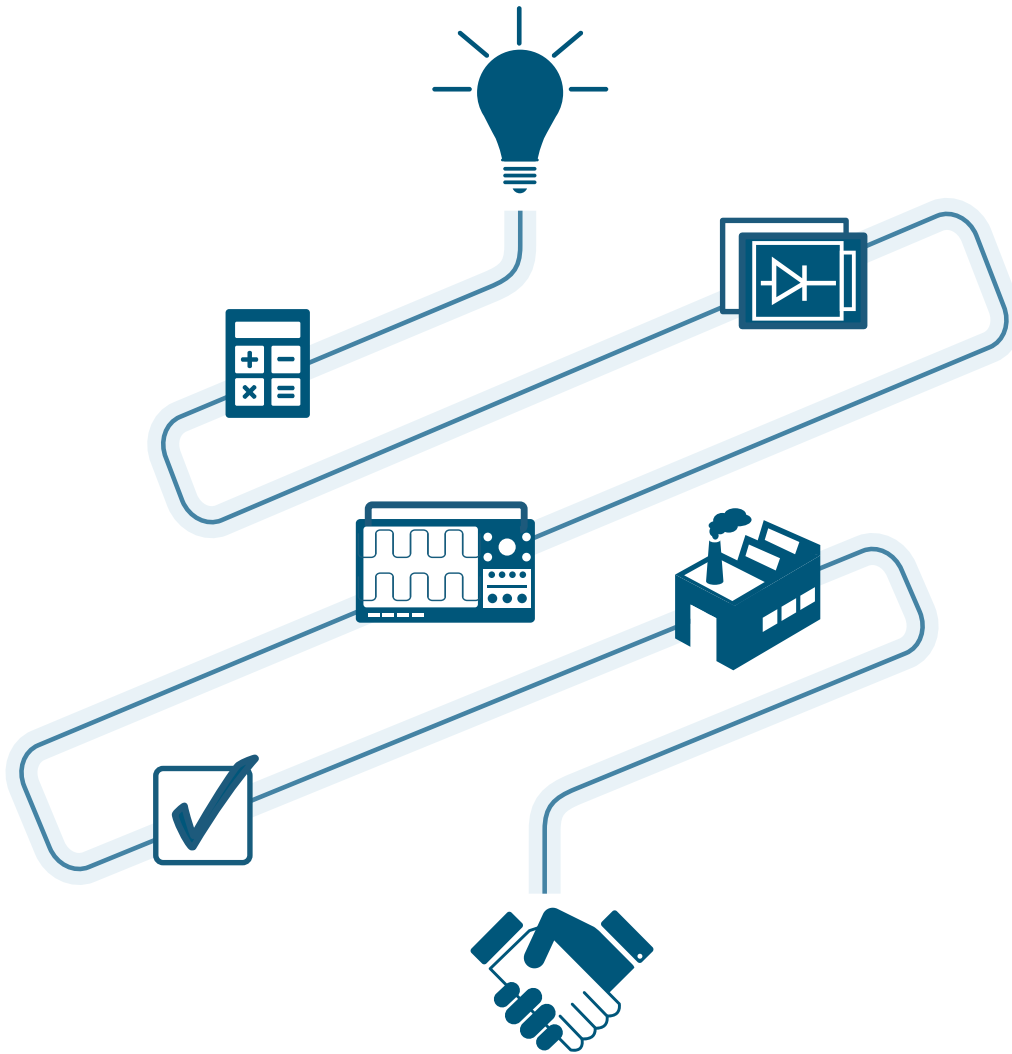


Figure 1: Temperature dependence of RDS(on) of Cree® 900V SiC MOSFET vs. 900V Si superjunction MOSFET



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superjunction MOSFET technology, this boundary appears in the 75–100W range. For third generation silicon carbide (SiC) MOSFET technology, which significantly outperforms Si devices (see Table 1), the price/performance boundary between single- and two-stage topologies is about 3x higher: 250–300W. As such, a new generation of high-power single-stage LED drivers based on SiC MOSFETs and capable of providing unprecedented price and performance characteristics is now possible. This new generation of high-power single-stage LED drivers delivers the performance of a two-stage topology while maintaining the cost structure of a single-stage topology. These new SiC MOSFET-based single-stage LED drivers are also capable of achieving unparalleled power density — delivering 40% volume reduction and 60% weight reduction compared to present driver technology (see Figure 3). These significant reductions in both weight and volume further increase the overall value of the new drivers by subsequently reducing the requirement for, and thus the cost of, the lighting fixtures' supporting mechanical structural components.

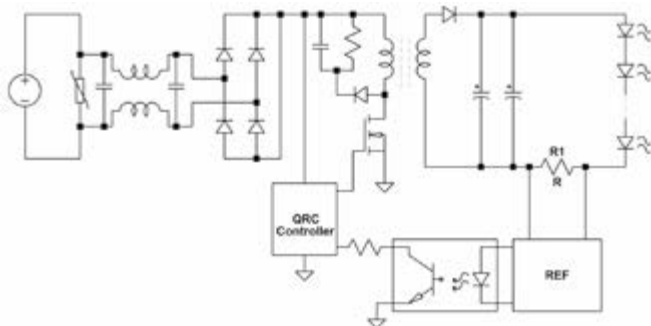


Figure 2a: Single-stage flyback-based LED driver topology

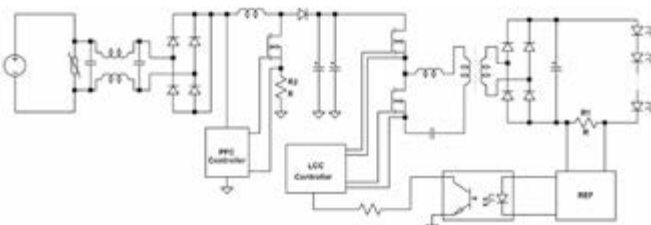


Figure 2b: Two-stage driver topology implemented using a boost PFC and LLC half bridge.

Additionally, the benefits of SiC MOSFET technology in LED drivers extend far beyond the 150–250W single-stage drivers discussed herein. For example, SiC MOSFETs used in two-stage topologies can also address especially challenging requirements, including: high



Figure 3: Side-by-side comparison of two 200W LED drivers: one using Si superjunction MOSFETs and two-stage topology, and the other using a Cree® C3M™ SiC MOSFET and single-stage topology.

input voltage (528VAC), ultra-wide input voltage ranges (90–528VAC), high power (>300W), and/or high efficiency (>95%). Further, as SiC MOSFET technology continues to move into lower voltage and lower power applications, they will also become the device of choice in LED power supply applications <100W.

Design Challenges: Implementing Single-Stage LED Drivers

Five key limitations and challenges must be overcome in order to implement a single-stage topology in high power LED lighting: 1) low efficiency, 2) narrow operating voltages, 3) the high cost of EMI filter components, 4) the high cost of surge protection components, and 5) high output current ripple (flicker) characteristics.

Low Efficiency and Narrow Operating Voltages

The current and voltage stresses imposed upon power MOSFETs are typically higher in single-stage topologies than two-stage topologies. These stresses are increased even further for wider input and output voltages. Ultimately, these stresses have a significant impact on the converter efficiency, as well as the rating (and hence the cost) of the power MOSFET used in the design. This is the primary reason why single-stage topologies are limited to low power designs with relatively narrow operating voltages.

SiC MOSFETs deliver figures of merit (FOM) that are 15 – 30x better than best-in-class 900V Si superjunction MOSFETs (see Table 1). As such, SiC MOSFETs increase the power level of single-stage topologies by approximately 3x while delivering efficiencies and operating voltages that are equivalent to those obtained with two-stage Si-based topologies. Figure 4 depicts an efficiency vs. input voltage comparison for two MOSFETs (a 900V silicon SJ MOSFET and a Cree C3M™ 900V MOSFET) in the same LED driver (a 220W LED driver implemented in a single-stage topology). The single-stage driver using the new 900V SiC MOSFETs exhibits superior efficiency, effectively demonstrating that SiC MOSFETs can address the typical limitations of high power single-stage LED drivers by providing high efficiency over a wide operating voltage range.

	Technology	V _{DS} (V)	R _{DS(on)} (mΩ) 25°C	R _{DS(on)} (mΩ) 150°C	Q _c (nC)	C _{oss} (pF)	FOM1 R _{DS(on)} ×C _{oss}	FOM2 R _{DS(on)} ×Q _c
C2M0280120D	SiC C2M	1200	280	350	20	23	8	7
C2M0160120D	SiC C2M	1200	160	290	34	47	14	10
C3M0065090D	SiC C3M	900	65	90	30	60	5.4	2.7
IPW90R120C3	CoolMOS	900	100	270	270	330	89	73

Table 1: Key parameters and figures of merit (FOM) for various MOSFET technologies

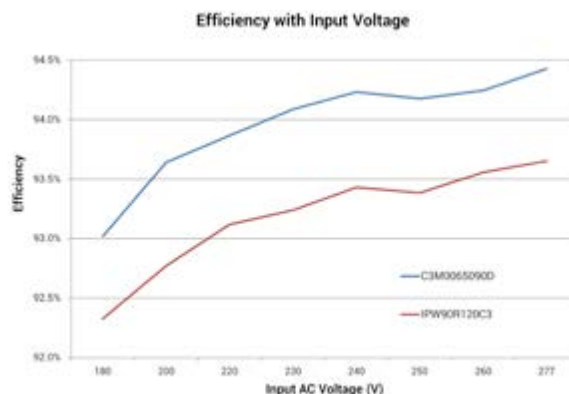
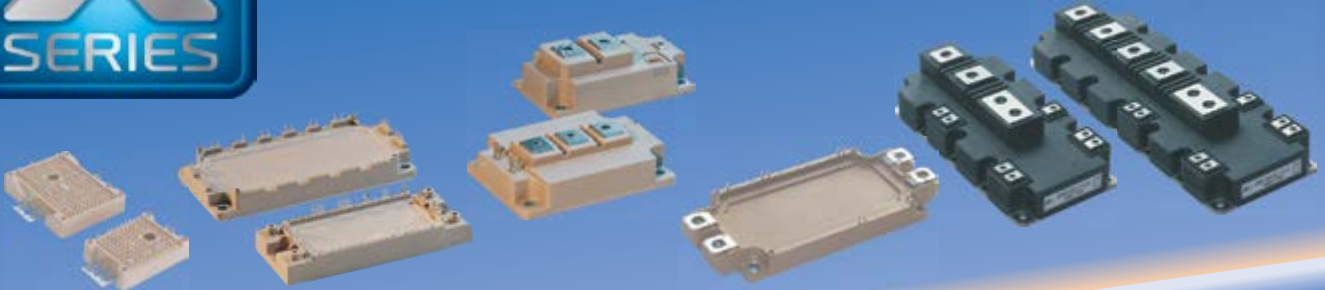


Figure 4: Efficiency vs. input voltage of a single-stage flyback driver using a Cree® 900V C3M™ SiC MOSFET vs. 900V Si MOSFET

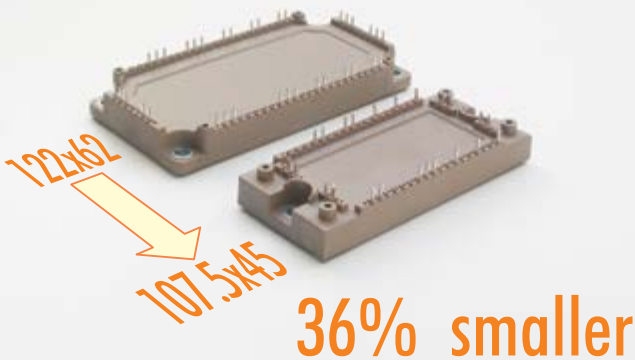


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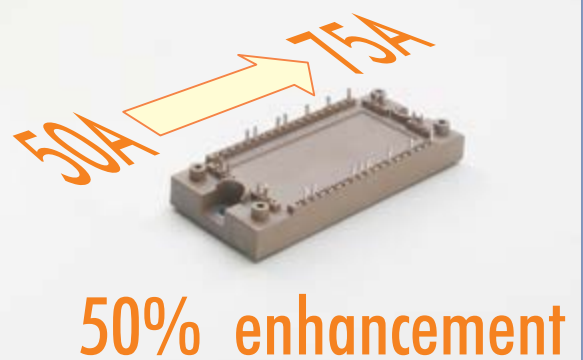


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Downsizing package
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Example 50A PIM-IGBT



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The High Cost of EMI Filter Components

One common perceived challenge of single-stage, high power LED drivers is the need for more expensive EMI filters. The EMI signature of a flyback configuration is higher than that of a continuous conduction mode (CCM) boost PFC. However, it is important to note that the EMI signature of a QRC flyback is similar to the EMI signature of the discontinuous conduction mode (DCM) boost PFCs typically used in two-stage LED drivers. Additionally, it is common knowledge that QRC flyback drivers operate using a variable switching frequency and have a reduced EMI spectrum compared to fixed-frequency flyback drivers. This spectrum reduction results from the spreading of RF emission over a wider frequency range as the switching frequency (and its harmonics) shift throughout the AC line cycle.

EMI signature is a function of topology and operating point. Therefore, one could conclude that changing from Si superjunction MOSFETs to SiC MOSFETs will not help in this regard. However, Class B conducted EMI compliance limits only drop with a 20dB/dec slope from 150–500kHz. Common EMI filters for single-stage topologies are implemented using a two-stage LC EMI filter, which provides a maximum attenuation slope of up to 80dB/dec. Thus, given a particular EMI filter size (and cost), the harmonic spectrum of a power converter operating at a higher switching frequency will be more attenuated than the harmonic spectrum of a power converter operating at a lower switching frequency.

Figure 5a shows the theoretical EMI signature of a two-stage topology with a DCM boost PFC first stage. Typically, the switching frequency of the first stage is 60–150kHz in order to keep the fundamental switching frequency component from approaching the lower EMI frequency limit (150kHz). However, two-stage LC EMI filters are generally required in order to reduce the spectrum of the second, third, and higher order harmonics for EMI compliance. As illustrated in Figure 5b, the higher operating frequency (>200kHz) enabled by SiC MOSFETs with the same EMI filter design used in the two-stage topology can deliver an extra 15dB attenuation for the first harmonic, 35dB attenuation for the second harmonic, and 40dB attenuation for the third harmonic, enabling the single-stage topology to reach EMI compliance without additional EMI filter cost. Additionally, a careful look at the two power supplies in Figure 3 also shows that the two-stage solution and the single-stage solution with SiC MOSFETs have similar EMI filter sizes (and hence costs).

High Output Current Ripple (i.e., Flicker)

Another challenge of single-stage topologies vs. two-stage topologies is output current ripple. Line frequency output current ripple translates into light output variation (i.e., flicker) for the LED array, so the Alliance for Solid-State Illumination Systems and Technologies (ASSIST) has established maximum light flicker acceptability criteria. Current ASSIST guidelines state that light flicker greater than $\pm 10\%$ percent at 100Hz and greater than $\pm 15\%$ percent at 120Hz is unacceptable [2]. To meet these criteria and minimize light flickering, LED drivers must minimize current ripple.

Figure 6 illustrates the relationship between LED current variations and light output variations. This figure shows that a $\pm 15\%$ variation on current translates to only $\pm 10\%$ variation on light output. While this relationship is unique for each LED type, it is generally accepted that an LED driver with $\pm 10\%$ variation in output current will meet the flicker demands of most LED arrays.

Two-stage topologies have a large, high-voltage DC link capacitor that is used as a line frequency energy buffer. The second stage is

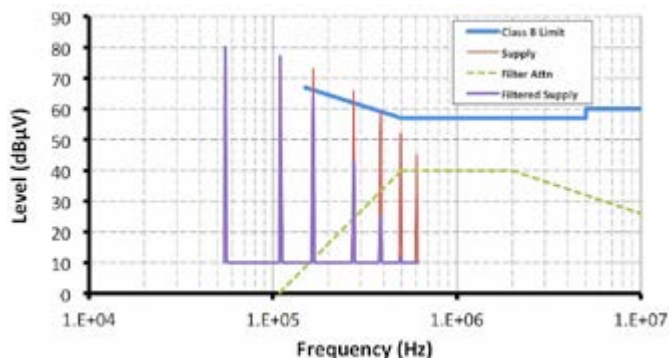


Figure 5a: An EMI filter design exercise for a conventional two-stage design showing the Class B conducted EMI limit, theoretical EMI signature of the unfiltered supply (Supply), EMI filter attenuation (Filter Attn), and EMI signature of the filtered supply (Filtered Supply).

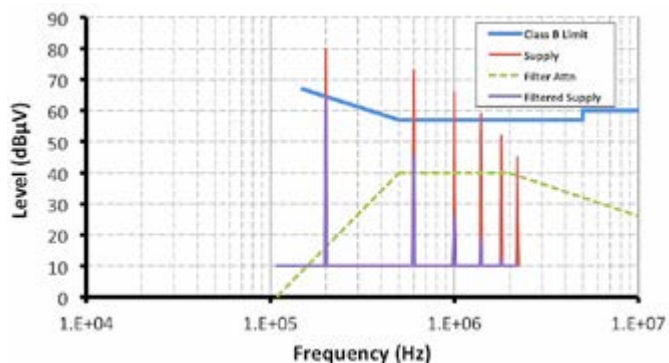


Figure 5b: An EMI filter design exercise for a single-stage high-frequency design showing the Class B conducted EMI limit, theoretical EMI signature of the unfiltered supply (Supply), EMI filter attenuation (Filter Attn), and EMI signature of the filtered supply (Filtered Supply).

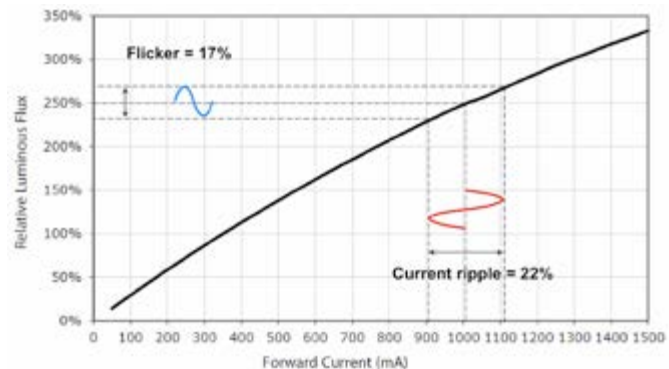


Figure 6: LED current variation vs. luminous flux variation for a Cree® XLamp® XP-G2 high-brightness LED

used to compensate for voltage variations in the DC link capacitor and to reduce output current ripple to $\pm 5\%$ via a high-bandwidth current control loop. Single-stage topologies do not employ high voltage DC link capacitors, but instead use their output capacitors as energy storage elements. The control of the output current is implemented as a low-bandwidth average current control loop, which is typically not capable of compensating for line frequency current ripple. This topological limitation cannot be addressed by simply changing power MOSFET technologies. However, the output current ripple can still be minimized in a cost-effective manner by minimizing output voltage ripple via output capacitor sizing and the proper tuning of the current control loop.



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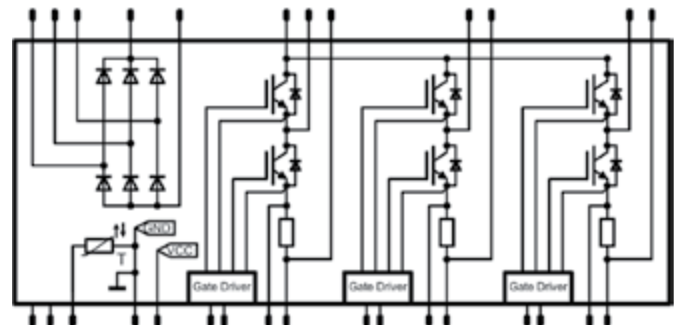
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A given LED array's dynamic resistance determines the current ripple for a given voltage ripple. High performance LED arrays tend to have lower dynamic resistance; hence, a small voltage ripple typically translates into higher current ripple. Figure 7 depicts measured current ripple when a single-stage flyback driver with a SiC MOSFET is used to drive a high performance LED array containing Cree® XLamp® XP-G2 high brightness LEDs. The measured output current ripple is ±11% at 120Hz, which translates into ±9% light flicker, and is well within the ±15% percent mandated by ASSIST.

The output capacitors in this SiC single-stage flyback driver are the same as the capacitors used in the DC link and output sections of the Si two-stage driver (See Figure 2). As such, both driver approaches have the same capacitor cost. Adding output capacitance could improve current ripple without significantly impacting cost, though, as capacitors represent only 8% of the total BOM cost, and reducing input current total harmonic distortion (THD) could reduce current ripple an additional 8–10% with no additional BOM cost while still meeting EN61000-3-2 standards.

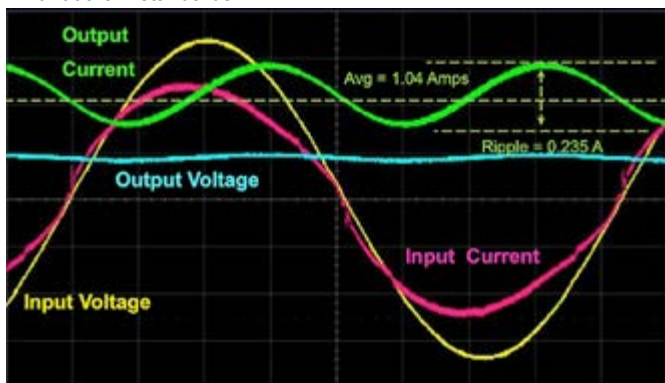


Figure 7: Measured output current ripple of a single-stage SiC MOSFET based flyback driver delivering 220W into a high performance LED array (worst case) containing Cree® XLamp® XP-G2 high brightness LEDs

	Two-stage Topology With Si FETs (1)	Single -Stage Topology Cree C3M SiC FETs (2)
Input Voltage Range	120-277Vac	180-277Vac
Output Voltage Range	150-210Vdc	150-240Vdc
Max Output Current	1.45A	1.05A
Peak Efficiency	93.50%	94.44%
Input THD	< 20%	< 10%
Input PF	> 0.95	> 0.95
Output Current Ripple	±5%	±10%
Size (~40% smaller)	220x52x30mm	140x50x30mm
Weight (~60% lighter)	2.7lbs/1.3kg	1.1lbs/0.5kg
Relative Cost	1	0.85

Table 2: Main characteristics of a 220W LED driver implemented using Si super junction MOSFETs and two-stage topology vs. a Cree® C3M™ SiC MOSFET and single-stage topology

Example: 220W LED Driver with Universal Input Voltage

Table 2 depicts the key metrics of a typical high performance 220W LED driver using Si super junction MOSFETs in a two-stage topology and SiC MOSFETs in a single-stage flyback topology. Both drivers have similar characteristics in terms of power, input voltage range, efficiency, THD, and power factor. The single-stage topology has higher output current ripple than the two-stage topology, but is still

squarely compliant with ASSIST mandates. More importantly, though, the single-stage topology using a SiC MOSFET provides significant cost reduction (>15%), volume reduction (~40%), and weight reduction (~60%) (see Figure 2), and is also capable of meeting EMI Class B requirements and surge requirements to 4kV, L-L while delivering acceptable output current ripple.

Table 3 contains the approximate cost reduction of the two-stage topology with Si super junction MOSFETs vs. the single-stage topology with a SiC MOSFET. Although the actual price of components will vary with volume, the relative price difference of the two solutions is quite relevant.

Component	Potential Cost Reduction	Comments
Magnetics	45%	Only 1 magnetic component instead of 2.
FETs	-51%	3 high speed SJ Si FET vs. only one Cree C3M SiC FET
Diodes	85%	5 high speed diodes (one in PFC and 4 in LLC) vs. one for flyback
Control	22%	2 controller (PFC + LLC) vs. only one very low cost flyback controller with low part count
PCB	40%	40% cost reduction based on size difference
Case	29%	29% cost reduction based on size difference
Caps	0%	Same caps needed in both designs
Potting	40%	40% cost reduction based on size difference
Others	5%	Small reduction based on less hardware needed (e.g., fewer heatsinks, screws, etc.)
Total	17%	

Table 3: Cost comparison for a 220W LED driver with universal voltage input implemented using two-stage topology with Si SJ MOSFET vs. a single-stage topology with SiC MOSFET.

Summary

Single-stage topologies deliver LED driver solutions with acceptable performance at a lower cost than two-stage topologies. As such, single-stage topologies are the approach of choice for lower power (<100W) LED drivers. At higher power levels, single-stage topologies face challenges that limit their usability and value, including: a limited operating voltage window, lower efficiency, and the need for additional surge protection. Consequently, two-stage topologies have dominated the market for high power LED drivers (>100W).

New advances in SiC planar technology significantly reduce the die size and cost, while at the same time reducing the on-resistance. Many of the limitations faced by single-stage topologies in high power applications can be traced back to a single root cause: the performance and FOM of the power MOSFETs employed therein. When using state-of-the-art 900V Si super junction MOSFETs, the value proposition of single-stage topologies — lower cost, smaller size, and reduced weight — is not possible. New 900V SiC MOSFET technology not only allows lighting designers to reap the benefits of single-stage topologies in high power applications, but also, by outperforming Si superjunction MOSFET technology (see Table 1), moves the price/performance boundary of single-stage topologies from the 75–100W range enabled by Si MOSFETs up to 250–300W. As such, single-stage topologies employing SiC MOSFETs can now deliver lower cost solutions than two-stage approaches without comprising performance. Also, although a flyback topology was used here as an example for 220W LED driver, other isolated and non-isolated single-stage topologies (e.g., forward, SEPIC, etc.) are also possible using SiC MOSFETs.

Further, the use of SiC MOSFET technology is not limited to LED

drivers in the 150–300W range. SiC technology can be combined with two-stage topologies in order to address an array of unique design challenges, including: high power LED drivers (up to 1,000W), ultra-wide input voltage ranges (up to 528VAC), high efficiency (>95%), and high power density. Additionally, as SiC MOSFET technology continues to move into lower power and lower voltage applications, typical single-stage LED drivers (<75W) will also benefit from the lower total BOM, improved performance, and higher power density it enables. Consequently, SiC MOSFET technology is poised to become the device of choice for LED drivers in all power ranges.

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[1] "Solid-State Lighting Research and Development, Manufacturing Roadmap," U.S. Department of Energy, Office of Energy Efficiency and Renewable Energy, (September 2013), http://apps1.eere.energy.gov/buildings/publications/pdfs/ssl/ssl_manuf-roadmap_sept2013.pdf.

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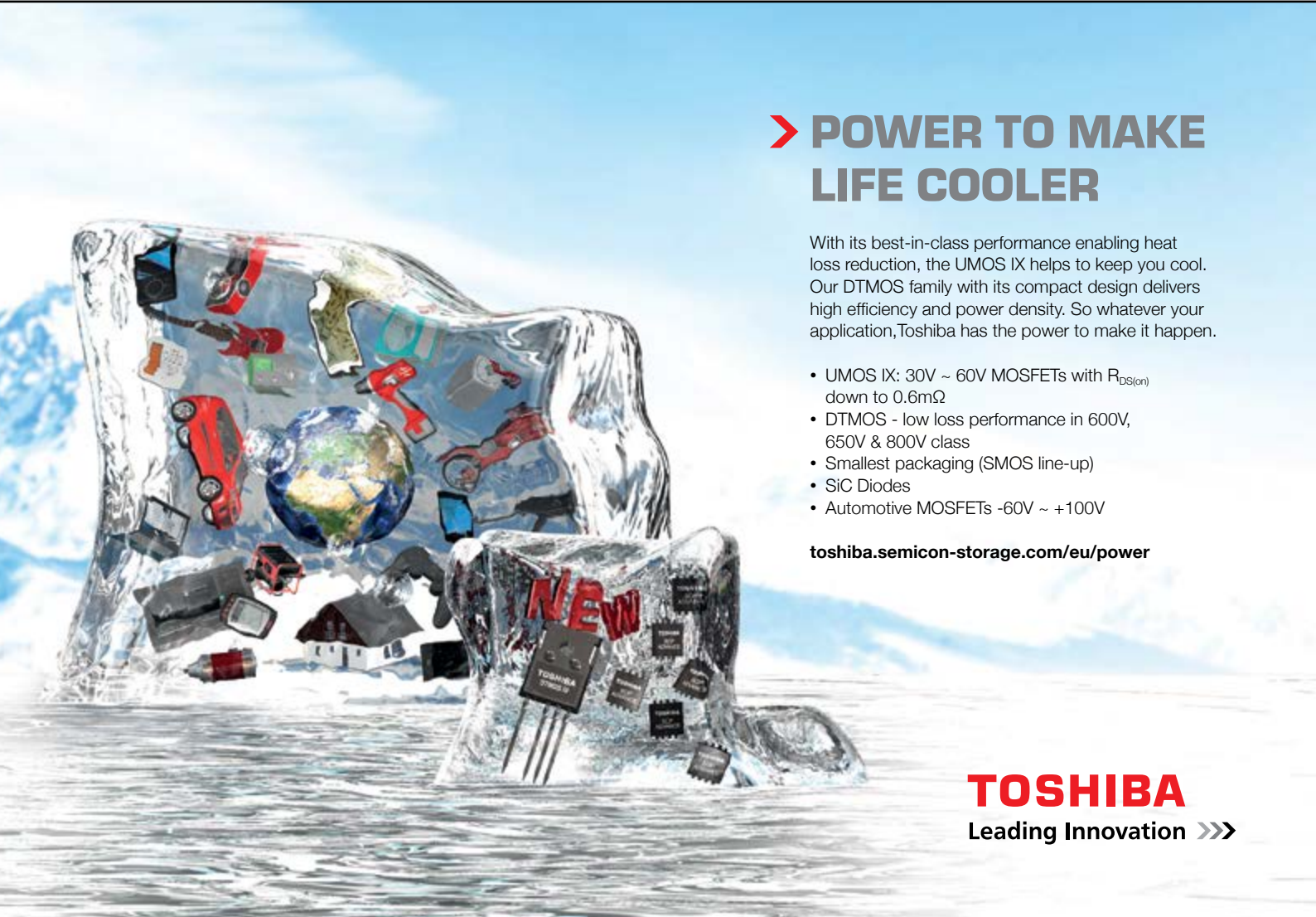
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Lighting up the Theatre, Safely

The recommended electrical and electronic requirements for the DMX512A lighting communications protocol

By Michael Pearce, Application Engineer, Microchip Technology

The most common lighting communications protocol used in theatrical lighting is DMX512, and it is also often found in architectural and other lighting systems. Uses of the standard include dimming theatrical lights, running colour mixing lighting fixtures, robot scanner lighting fixtures, strobe lights and fog machines. Some vendors use it to control commercial or domestic lighting fixtures and even giant high definition television displays have been built using multiple DMX512 universes.

The standard was created in 1986 by the United States Institute for Theatrical Technology (USITT) to be a more reliable replacement for the 0 to 10V standard commonly used at the time. In 1998, it was taken over by the Entertainment Services & Technology Association (ESTA). It became DMX512A in 1998, and was revised in 2008. It has been an Ansi standard since 2004 (Ansi E1.11-2008). Since 2011, the standard has also been maintained by PLASA in Europe.

Due to there being no error checking, there are some restrictions of use. Basically, any use that could potentially harm or kill a human or animal is not allowed. This includes, but is not limited to, moving stages, moving trusses and pyrotechnic control.

This simple, single master serial protocol uses the RS485 electrical layer at a data rate of 250kbaud, no error checking and up to 512byte of data. A DMX512 universe is made up of 512 channels of information sent from a single controller. Multiple universes can be created by using additional controllers. The electrical requirements are very well defined in the specification, including what circuit designs to use and the exact type of cable and connectors that are allowed. Despite this, there are many manufacturers that do not follow the specification and use invalid circuit layout and incorrect connectors, which can cause issues with compatibility and reliability.

The data packet is retransmitted continuously, which helps correct any data glitches. If no packet has been transmitted within one second, then most receivers will switch

to a default setting or to an off mode. The maximum refresh rate for 512 channels is 44 updates per second, which allows for nice dimming with little or no visible flicker on incandescent bulbs. LEDs may require smart control to smooth out fading.

Electrical requirements

The electrical requirements are based on the RS485 standard, with slight variation. It uses RS485 differential transceivers, maximum transmission line length of 1200m, and up to 32 receivers per RS485 transmitter. The driver output range is ± 1.5 to $\pm 6V$ and receiver sensitivity is $\pm 200mV$.

DMX512A requires the receivers to be isolated, which helps avoid earth loop and potentially lethal voltage differences. Many low-cost receivers, often used by DJs and for party lighting, are still non-isolated and can

strictly for use in permanent installations, where the cable is not being moved, and the connectors are only used on occasion. This is more cost effective, but would not last in a non-permanent setting.

The standard only specifies the use of five-pin XLR type connectors for DMX512 communications, and DMX512A added the use of RJ45 connectors for permanent installation. For the XLR connectors, the plug is used for the DMX in and the socket for DMX out. The pinouts for the five-pin XLR and RJ45 are shown in Figure 1.

Despite the standard specifying the connectors, many low-cost manufacturers use three-pin XLR connectors commonly found in professional microphones. This introduces a number of issues from different pinouts, and the common mistake of using microphone

Pin #	5-Pin XLR	RJ45
1	Signal Common	Data 1+
2	Data 1- (Primary Data Link)	Data 1-
3	Data 1+ (Primary Data Link)	Data 2+
4	Data 2- (Optional secondary link)	Not Assigned
5	Data 2+ (Optional secondary Link)	Not Assigned
6		Data 2-
7		Signal Common for Data 1
8		Signal Common for Data 2

Figure 1: Connector pinouts

cause communications issues or be a safety hazard, especially if part of a larger network of lights.

Cable requirements are specified as a cable with nominal characteristic impedance of 120Ω with a shield and two twisted pairs. Only one of the pairs is generally used, as the second pair is set aside for a secondary channel that is not commonly used. Because of this, many DMX512 cables use a single pair. Due to these requirements and the hard wearing environment of stage lighting, there are some cable manufacturers that make DMX512 specific data cable that is flexible and very heavy duty with DMX, DMX512 or DMX512A printed on the cable itself.

The DMX512A specification introduced the use of Cat 5E cable and RJ45 connectors

cable instead of DMX data cable, to plugging of DMX and audio equipment together accidentally. It is highly recommended that the user comply with the DMX512A specified cables and connectors to avoid these issues, and to ensure DMX512A compliance.

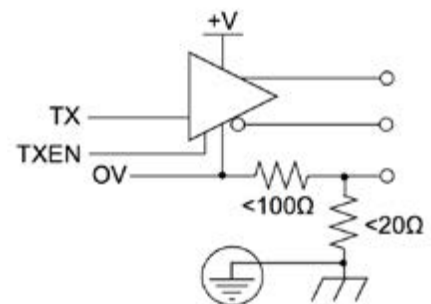


Figure 2: Controller transmitter circuit

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Circuitry

For the controller, the transceiver is usually a ground-referenced transmitter, although it is possible to have it isolated. The recommended circuit from the DMX512A specification is in Figure 2 and shows how to connect the signal and chassis (earth) grounds using resistors. Even though the resistors are optional, they can possibly reduce earth loop issues if they are included in the design. More details are found in Ansi E1.11-2008.

The receiver is isolated, as shown in Figure 3. The resistance from any pin on the DMX connector to chassis ground must be greater than $22M\Omega$ at 42V. An optional capacitor may be fitted between the data link common and the chassis ground for radio frequency bypass.

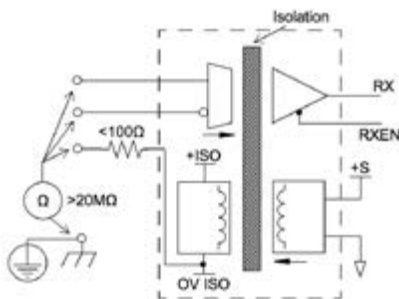


Figure 3: Receiver circuit

DMX512 uses a daisy chain connection topology, as shown in Figure 4. Up to 32 receivers can be daisy-chained from a single driver with a 120Ohm termination resistor at the far end of the chain. To achieve this, there are two connectors on each receiver, often labelled "DMX in" and "DMX out".

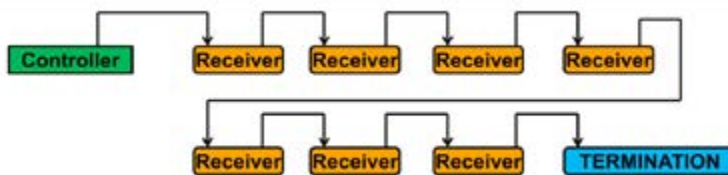


Figure 4: DMX512 daisy chain

These two connectors have the data and ground lines connected between them, so it electrically passes the data along the chain. To connect more than 32 receivers to a single controller, DMX splitters are required. These can be as simple as an isolated RS485 receiver that feeds to multiple RS485 transmitters or a more elaborate system that uses microcontrollers to capture and retransmit data with the possibility of limited back channel capability. Because of this, receivers with back channel capability should be connected directly to the controller's bus to avoid potential problems.

The standard does allow for bidirectional communications, and these are covered in Ansi E1.11-2008 Annex B – Enhanced DMX512. Communications can operate in full or half-duplex modes using just the primary data link, or using both primary and secondary data links. The data protocols and any timing requirements are not specified in the standard. To achieve bidirectional communications, all the transceivers must be bidirectional and controlled using an additional IO pin. In normal operation, the controller should be configured for transmit mode and the receiver for receive mode.

DMX512 library

The DMX512 library is completely interrupt driven and requires the use of a EUSART and one timer. The timer generates the break and the MAB (mark after break) timing for the controller and the data time out for the receiver. The timer also generates millisecond, minute and hour ticks and counts that can be accessed for general use.

Using the EUSART found on many Microchip PIC microcontrollers, the break can easily be detected using the framing error interrupt. The data rate of 250kbaud is a clean divide down from common oscillator frequencies, such as 4, 8 or 32MHz, which results in a theoretical 0% data rate error. These features make implementing DMX512 relatively simple.

The library currently implements a DMX controller, receiver or both, depending on how it is configured. A future version may add half-duplex communications capability and possibly a basic implementation of remote device management (RDM). Currently, the library is targeted at the Microchip Technolo-

gy 8bit microcontroller family with a EUSART, but can be easily ported to the 16 and 32bit families and some non-EUSART parts.

Conclusion

This article gives an overview of DMX512A, showing and explaining recommended electrical and electronic requirements, and how the protocol was implemented in the Microchip Technology DMX512 library.

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A Substrate to Rely On; New IPC Standards for Metal-Clad PCBs Give the Power to Choose

A new industry standard is about to emerge, which for the first time will enable product designers to make accurate and confident comparisons between insulated metal substrates for design projects where superior thermal performance is an imperative.

*By Dave Sommervold, Engineering Manager,
Thermal Substrates, Henkel Electronics Materials, LLC*

Extreme Hits the Mainstream

Thermally enhanced printed wiring board, or Insulated Metal Substrate (IMS), has become popular in industry sectors such as advanced lighting and high-power motor control. In applications such as these the form factors of electronic controllers are often restricted, for example by standard sizes for replacement bulbs or layout constraints in industrial machinery or vehicles such as forklifts.

Compared to ordinary laminate, the high thermal performance of IMS allows engineers to size heatsinks appropriately while designing for a low die temperature to ensure satisfactory reliability. In some applications, the heatsink and its associated fittings can be designed out entirely, allowing greater miniaturization and simplified assembly.

In the past, IMS has arguably been a niche technology, chosen by engineers facing extreme design pressures. The current dramatic growth of markets for LED lighting and the increasing numbers of hybrid/electric vehicle models on sale are two important trends now bringing those pressures into the mainstream.

Demand for IMS is expected to increase, and this will inevitably bring greater cost pressure into new design projects. This will have a number of effects. Firstly, vendors are likely to diversify their IMS product ranges to help customers achieve a favorable cost/performance balance when targeting a variety of markets and applications. In addition, new IMS brands will enter the market at attractively low prices but of uncertain quality and performance.

A Technology in Need of a Standard

Engineers designing with IMS need to be able to rely on the quality and performance of their chosen IMS. In particular, aspects such as the thickness and electrical strength of the dielectric have safety implications for appliances that are operated at high voltages. In an LED-lighting application with a large number of emitters in series, the potential applied across the string can be several hundred volts. At these operating voltages, a surge can cause permanent breakdown of a weak dielectric, bringing increased risk of circuit failure or exposing the user to the risk of electric shock. In addition the dielectric characteristics, as well as other factors such as the thickness of the metal base, dictate thermal performance and hence the overall reliability of the circuit.

Historically, there have been no standardized tests for IMS products that enable engineers to compare products from different manufacturers and be sure their chosen IMS will perform as expected. During 2013, a team from Bergquist approached industry association IPC to suggest that such a framework was needed urgently. IPC readily agreed, and gave the go-ahead to set up a committee to develop standardized specifications and tests for IMS.

The forthcoming document (proposed as a joint standard, IPC/CPCA-4105A), Specification for Metal Base / Copper Clad Laminates for Rigid Printed Boards is nearing completion, having initially begun in China by the China Printed Circuitry Association but now, as a joint industry standard, subject to global industry consensus review. The standard will for the first time provide an independent framework for comparing thermally-enhanced substrates from different vendors from around the world. This move will help designers select materials that will best meet the needs of their applications, and allow an assurance of quality.

IMS in Brief

IMS is available from a number of known and trusted suppliers. Generically, the IMS stack-up comprises a metal base layer, a dielectric layer or high thermal conductivity, and a top copper layer that is etched to create the circuit. The metal base is typically aluminum or copper. Figure 1 illustrates these aspects of the structure.

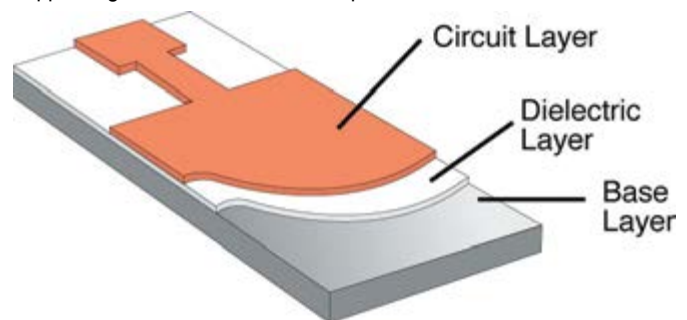


Figure 1: Generic IMS stack-up.

The dielectric layer is responsible for electrically isolating the circuit layer from the metal base. It must also have high thermal conductivity, to ensure efficient heat transfer from the surface-mount power components soldered to the copper pads of the circuit layer. Hence the dielectric material characteristics, nominal thickness, and uniformity



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of thickness, are critical factors that determine the performance of the IMS, and in particular its ability to withstand hazards such as high-voltage transients. As described earlier, breakdown of the dielectric can compromise the safety and reliability of the circuit.

On the other hand, the material properties of the metal base layer, and its thickness, govern the thermal capacity of the assembly, and hence have a critical role in determining the steady-state junction temperature of attached power components.

Introducing IPC/CPCA-4105A

IPC/CPCA-4105A is now progressing through consensus review and is expected to be finalized before the end of 2015. The specification encompasses classification, qualification and quality conformance requirements. It is the first to address, explicitly, thermally conductive metal base dielectric materials, including metal base laminate and prepreg. Note that the existing IPC-4101 specification, which refers to Base Materials for Rigid and Multilayer Printed Boards, does not address boards with a metal base layer.

The IPC/CPCA-4105A classification system, developed by IPC for its portion of the joint standard includes specific designations that can be used by PCB fabricators when ordering materials from suppliers. In addition, non-specific designations are defined, which are suitable for use by board designers. These non-specific designators are designed to be easy to use without requiring fabricator-level knowledge, and can be augmented with cross-sectional views or notes on the master drawing.

The classification system standardizes a means of describing all aspects of the board, including the type of metal base and its nominal thickness, as well as laminate and metal cladding. To classify the metal base, four characters are used to define the material, and there are also designators to define thickness and tolerance, as shown in tables 1 and 2.

Acceptable methods for measuring the thickness of applicable classes of dielectric materials are also specified. These include measurement by microsection for class D materials, or using a micrometer for other material classes, as illustrated in figure 2.

MBA1	Aluminum Alloy 1100
MBA2	Aluminum Alloy 1050
MBA3	Aluminum Alloy 1060
MBA4	Aluminum Alloy 5052
MBA5	Aluminum Alloy 6061
MBC1	Copper Alloy C11000
MBS1	Steel Alloy 1050
MBS2	Stainless Steel Alloy 304

Table 1: Designators for metal base types

A	Aluminum 0.5 mm ± 0.05mm [0.020in ± 0.0020in]
B	Aluminum 1.0 to 1.6 mm ± 0.09mm) [0.039 to 0.0630in ± 0.0035in]
C	Aluminum 2.0 to 2.2 mm ± 0.11mm [0.0787 to 0.0866in ± 0.0043in]
G	Aluminum 3.0 to 3.2 mm ± 0.15mm [0.118 to 0.126in ± 0.00591in]
H	Aluminum ≥4.0 mm ± 0.23mm [≥0.157in ± 0.00906in]
L	Copper ≥0.5 mm ± 5% [≥0.020 ± 5%]

Table 2: Metal base nominal thickness and tolerance

The new standard also covers metal cladding type as well as nominal weight and thickness, metal cladding grade, and nominal weight and thickness of metal foil, in a similar way to IPC-4101.

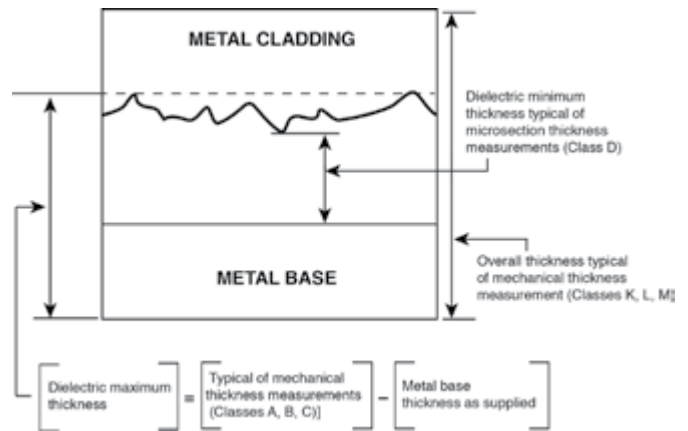


Figure 2: Measurement of dielectric layer thickness

A new method to measure thermal performance is in "Round-Robin" test prior to an IPC-TM-650 test method submission. It will allow the measure on an IMS substrate coupon rather than the dielectric only measurements that are being performed currently, where method and values are varied.

Test Method for Dielectric Strength

In addition to the specification documents, the test method "Electrical Strength of Metal Base Printing Wiring Material" standardizes a technique for evaluating the ability of an insulating metal base material, including conductor copper to resist electrical breakdown perpendicular to the plane of the material when subjected to short term, high voltages at standard AC power frequencies of 50-60 Hz and DC power.

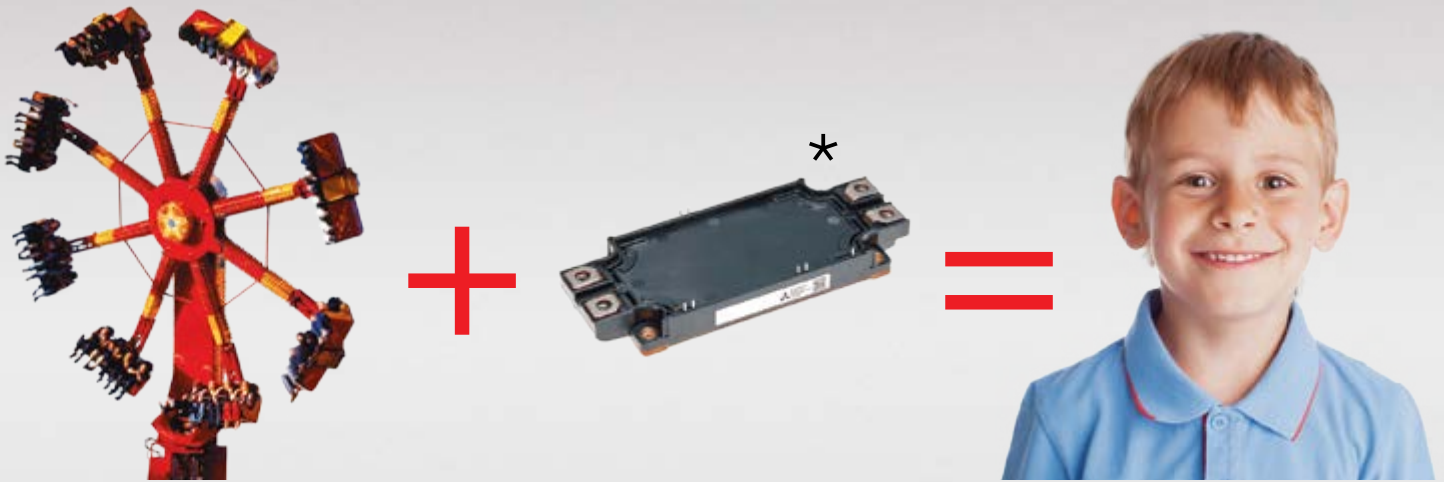
The method for testing electrical strength is based on the internationally recognized standard ASTM D149. In fact, IPC/CPCA-4105A as a whole, has been developed with reference to established applicable standards by a wide variety of world-class bodies. These include IPC base material performance standards, IPC-TM-650 Test Methods, JEDEC solderability standards and EU RoHS, as well as ANSI and ISO standards for measurement and test equipment.

As development of the standard has progressed, experts from a number of industry bodies and commercial organizations have engaged with the project. The working group within the IPC is representative of a broad cross section of the industry, encompassing material supply, IMS fabrication, and circuit-board and system design. The standard, when approved, is expected to gain universal acceptance among the industry's leading suppliers and users of IMS.

Conclusion

The new IPC/CPCA-4105A joint standard covering IMS will serve product designers seeking reliable solutions to their thermal management challenges, by empowering them to identify products that will meet their requirements, and make accurate comparisons in order to ensure the most satisfactory and cost-effective solution.

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Designing for Zero Standby Power (< 5 mW)

The electronic devices created in Edison's day were not as power-efficient as they are now. However, when they were not in use, they did not use or waste any power. That's because a mechanical switch was used to turn them off, thus dissipating zero power when not in use.

By Michael O'Loughlin, Senior Applications Engineer, Texas Instruments

Today, most appliances, phone chargers and other electronic devices do not have a mechanical switch. Therefore, they dissipate power unnecessarily when idle.

Energy agencies in many countries have mandated legislation to limit the amount of standby power that electronic devices can dissipate when idle to help conserve energy. Depending on the rated output power, country standards and end application, electronic devices being manufactured need to have less than 500 mW down to 75 mW of standby power. However, wouldn't it be better if these devices dissipated zero standby power when not in use?

While zero standby power is impossible to achieve without using a mechanical switch or unplugging the device, offline power converters with less than 5 mW of standby power are being designed and built today. These new power converters are being marketed as having zero standby power. Achieving less than 5 mW of standby power is possible when using primary-side regulated (PSR) flyback converters in low-power offline applications (Figure 1).

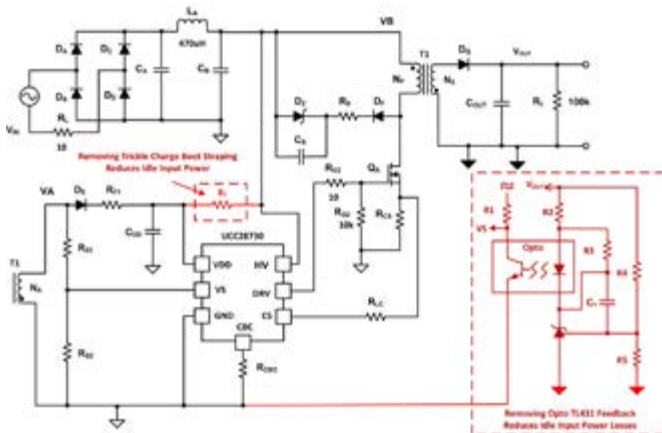


Figure 1: Schematic of an offline PSR flyback converter

One reason that the PSR flyback is a good choice for zero standby power is because the PSR control scheme senses (VS) the output voltage (VOUT) through the transformer's auxiliary turns ratio (NA/NS). This technique eliminates the need for TL431 optoisolator feedback circuitry. Removing the optoisolator feedback circuitry reduces your design's standby power by 2.5 to 5 mW. This reduces the system's standby power, making it easier to achieve zero power requirements (<5 mW). Equation 1 describes the mathematical relationship between VS and VOUT.

$$VS = \frac{\frac{NA}{NS} \times (V_{OUT} + V_{DG}) \times R_{S2}}{R_{S1} + R_{S2}} \quad (1)$$

Some offline PSR flyback converters/controllers use a trickle-charge resistor (RT) for to initially charge the power-supply controller's bias capacitor (CVDD) at power up. The only problem with this technique is that the trickle-charge resistor dissipates power when the power supply is idle. Power supply designers generally select RT and CVDD to meet startup and system holdup requirements. RT is generally 5 MΩ and can easily dissipate more than 5 mW, with 115-V root-mean-square (RMS) input when the power supply is idle.

To achieve zero standby power, I recommend developing smart startup circuitry or using a controller, such as the UCC28730, which has this circuitry internally. This green environmentally friendly startup circuitry only dissipates power while charging the CVDD capacitor. It turns off once the power-supply switching has begun and when there is enough energy in the auxiliary winding (NA) of the transformer (T1) to power the power supply's controller).

PSR controllers use a combination of valley switching; frequency modulation (FM) and primary peak current (IPP) amplitude modulation (AM) to control the duty cycle of the quasi-resonant/discontinuous flyback converter. This improves overall system efficiency and reduces standby input power. See Figure 2 for a functional schematic for this type of flyback controller.

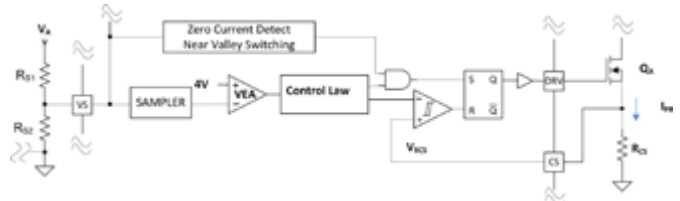


Figure 2: Functional schematic of constant voltage/current flyback controller

Figure 3 describes the frequency (fSW) and primary peak current amplitude (IPP) modulation by the flyback controller's constant voltage/constant current flyback controller, based on changes at the controller's voltage error amplifier (VEA) output. The transformer's primary inductance is selected so that the converter operates at a maximum switching frequency (70 to 80 kHz, 83.3 kHz maximum). As the load decreases and less duty cycle is required, the VEA output decreases; this causes the device's voltage-controlled oscillator to decrease the converter switching frequency, running the converter deeper into discontinuous mode. This reduces the FET's (QA) switching losses



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The PA99 is an industry first 2500V power operational amplifier that targets the increased voltage demands of ATE and programmable power supply applications. This general purpose op amp operates with symmetric or asymmetric supplies as long as the voltage between the positive and the negative supply rail does not exceed the maximum supply voltage specification.

Designed to provide up to 50mA of output current, the PA99 is fully capable of sourcing and sinking current for use in a wide variety of applications that drive any combination of resistive, inductive and capacitive loads. This small footprint, single package hybrid also has an output current limit function that can be set through external resistors to prevent runaway currents. Temperature monitoring is provided through a temperature sensing diode, and under typical operating conditions, the PA99 can achieve slew rates of 28V/ μ s.



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(PSW) with decreased loading, which improves the system's overall efficiency and reduces input standby power.

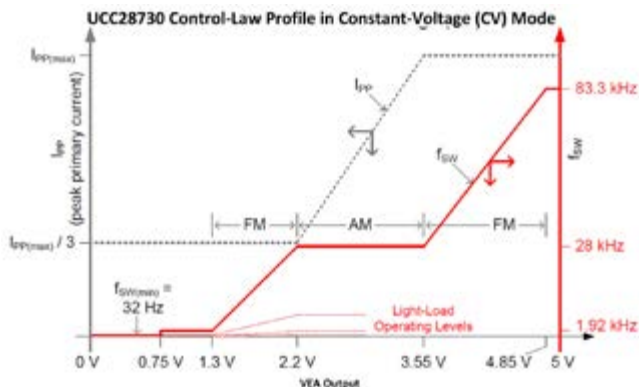


Figure 3: Control law of a controller with variations in VEA

To avoid audible noise when the VEA operates between 3.55V and 2.2V, the controller will operate at a fixed frequency of 28 kHz and adjust the converter's duty cycle by linearly modulating the amplitude IPP. The amplitude of IPP in this fixed-frequency operation linearly adjusts down from its peak value to one-third of its peak value. This adjustment decreases the energy stored in the transformer, thus decreasing the amount of energy available to produce audible noise at switching frequencies below 20 kHz. As the converter demands lower and lower duty cycles, when VEA output drops below 2.2V, the controller once again decreases the switching frequency all the way down to 32 Hz, reducing idle power-switching losses.

Equation 2 describes the switching losses of the FET's QA (PSW(FSW)) in a PSR flyback converter. IDS is the FET's peak drain-to-source current, where VDS is the voltage across the FET just before it is turned on. COSS is the FET's average drain-to-source capacitance, VG is the voltage level that drives the FET and QG is the gate charge at VG. Equation 2 shows that decreasing the frequency reduces FET switching losses. When the converter is idle, operating

around 32 Hz, the switching-power losses of the FET will be more than 2600 times smaller than they would have been operating at the maximum switching frequency of 83.3 kHz.

$$P_{SW}(f_{SW}) = \frac{C_{oss}(V_{DS})^2 f_{SW}}{2} + \frac{1}{2} V_G Q_G f_{SW} \quad (2)$$

Meeting low standby power also requires paying special attention to the selection of bulk, filtering and electromagnetic interference (EMI) capacitors. Select capacitors with the lowest leakage possible to ensure that you hit your standby power goals. In higher-power applications, you may want to consider some intelligent power management within your design, such as turning off a power factor corrected (PFC) pre-regulator or bypassing your EMI filter network when the converter is idle to reduce the converter's standby power.

Conclusion

You can use PSR flyback controllers to meet zero standby power (< 5 mW) by using PSR control techniques that remove the need for optoisolator feedback circuitry and reduce switching losses when the converter is idle. In higher-power applications, smart power management may be necessary to reduce loading when the electronic device is idle.

As a power supply designer, you will want to carefully review the data-sheet of the PSR controller to ensure that the switching frequencies can go low enough to reduce switching losses to meet this zero power standby requirement (< 35 Hz recommended). I also recommend selecting a PSR controller with low standby current and smart/green startup circuitry that does not require a trickle-charge resistor and only dissipates power at initial power up.

References

Download these datasheets:
<http://www.ti.com/product/ucc28730>
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Important Author Dates

January 15th, 2015: Digest submitted via the website
May 1st, 2015: Notification of acceptance or rejection
July 1st, 2015: Final papers with IEEE copyright forms

Other Important Dates

February 16th, 2015: Submission of Tutorial proposals
March 31, 2015: Submission of Special Session proposals



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The Seventh Annual IEEE Energy Conversion Congress and Exposition (ECCE 2015) will be held in Montreal, Canada, on September 20 - 24, 2015. ECCE 2015 is the pivotal international conference and exposition event on electrical and electromechanical energy conversion. To be held for the first time outside USA, ECCE 2015, in Montreal, Canada, will feature both industry-driven and application-oriented technical sessions, as well as industry expositions and seminars. ECCE 2015 will bring together practicing engineers, researchers and other professionals for interactive and multidisciplinary discussions on the latest advances in various areas related to energy conversion. Please visit <http://2015.ececonferences.org> for more information or contact the ECCE 2015 Technical Program Chairs at ecce2015tpc@gmail.com.

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Researching Film Capacitors for Converters in Wind Power Plants

The primary goal is to manufacture components with a longer life

The Husum-based capacitor specialist FTCAP participates in the innovation cluster “Power Electronics for Regenerative Energy Supply”. The project, which is coordinated by the Fraunhofer Institute for Silicon Technology in Itzehoe, researches new converter technology for wind power plants. FTCAP contributes its competences in the field of high-performance capacitors for converters to the project.

By Dr. Thomas Ebel, Managing Director, FTCAP

The increasing importance of regenerative electric power generation by wind power plants also results in higher requirements: while the electricity that is supplied must be of high quality, the power plants must also be designed for high performance and long service – even under extreme environmental conditions such as in offshore operation. Consequently, the demand for compact power electronics systems with high efficiency and a long life is high. Among the systems currently available on the market, however, there is ample potential for improvement in these respects.

The innovation cluster “Power Electronics for Regenerative Energy Supply” has therefore set the goal of improving power electronic components for wind power plants in the MW range. New components for wind power converters are being developed and tested throughout the entire industrial value creation chain: application-specific power semiconductor devices (IGBTs) for innovative connection technologies, highly reliable power modules based on sintered and copper wire bonding technology, efficient switching topologies and drive circuits as well as new mechatronic approaches form the basis for a new powerstack generation. The goal is to develop a 3-phase powerstack demonstrator with three power modules (one module for each phase) that is suitable for use in a back-to-back full-power converter. The target power rating is 1 MW.



Figure 1: FTCAP_Filmkondensatoren_Windkraft.jpg: As part of a research project the Husum-based capacitor specialist FTCAP is researching new, long-lasting film capacitors for converters in wind power plants

Innovative capacitors for wind power plants

Both the power modules and the capacitors will play a decisive role in the development of this system: the power converter in a wind power plant consists of two converter units. These, in turn, contain two power modules, which are connected to each other by a DC link equipped with capacitors and supply the entire power converter with electricity. The capacitors store energy that can be used in the case of a mains failure to ensure uninterrupted operation. Consequently, the system components that are subjected to the greatest load are the power modules and the capacitors, which must be as robust as possible. The main challenge with respect to capacitors for converters in wind power plants is the service life. A wind turbine should be able to operate for many years without the need for maintenance. This requires innovation with respect to the capacitors, as well.



Figure 2: Windkraftanlagen_Kondensatoren_FTCAP.jpg: The main challenge with respect to capacitors for converters in wind power plants is the service life – a wind turbine should be able to operate for many years without the need for maintenance. Picture © pedrosala – Fotolia

Innovation, however, also involves stumbling blocks – and there are many of these in the case of wind power plants. In this application, the capacitors are subjected to diverse stress factors: humidity, extreme temperatures and high ripple currents can impair the functionality. Depending on the type of capacitor, this results in different potentials for error: excessive ripple currents, for example, can damage electrolytic capacitors beyond repair. That is the worst case scenario, which of course has to be prevented. But also the normal deterioration process of the capacitors can become a problem in wind power plants. The

fact is that in normal operation a capacitor does not fail all at once – instead, this component is subject to a gradual deterioration process, which results in a continuous decrease in performance. It is therefore necessary to examine not only the mechanisms and causes of such a decrease in performance, but also the effects of the deterioration process on the performance of the overall system.

Exploring the promising potentials of PEN-HV

In the search for a high-performance capacitor for wind power plants, FTCAP is exploring the promising potentials of the high-temperature dielectric PEN-HV within the framework of the research initiative. PEN-HV combines the self-healing properties and the dielectric strength of oriented polypropylene (OPP) with the mechanical and thermal advantages of polyethylene naphthalate (PEN). This innovative material allows even better isolation of the capacitors for use at temperatures of up to 125 °C. FTCAP will test film capacitors equipped with PEN-HV and compare them with two standard products. Our hope is that the new technology will result in even more reliability and a significantly longer service life. At the same time we want to achieve an even more compact design of the capacitors – after all, the space in the nacelles of wind turbines is very limited. The reduction of the size of the capacitors will be possible especially due to the high temperature resistance of the new material, according to the experts: if the capacitor can also withstand high temperatures, the size of the cooling systems can be reduced or they can even be eliminated altogether.

Whether PEN-HV will indeed pave the way for innovative wind power capacitors will become apparent within the framework of the research project. The experts at FTCAP will examine these and other capacitors in extensive tests. They will test criteria such as the winding

parameters, the dielectric strength and, of course, the temperature resistance. But the storage life in combination with different encapsulations and housings, as well as the self-extinguishing properties of the different materials are also relevant. It will still take some time to determine the optimal solution: if everything goes according to schedule, the demonstrator should be completed and tested by the end of 2015.

Innovation cluster “Power Electronics” – the project partners

The consortium consists of the companies, Danfoss Silicon Power GmbH, FTCAP, Reese & Thies, Senvion SE and Vishay Siliconix Itzehoe GmbH in Schleswig-Holstein as well as the academic facilities of the Christian-Albrechts University in Kiel, the Kiel University of Applied Sciences, the Flensburg University of Applied Sciences and the West Coast University of Applied Sciences in Heide, Germany. The Fraunhofer Institute for Silicon Technology in Itzehoe is the coordinator of the innovation cluster in Schleswig-Holstein. The interests of the Federal State of Schleswig-Holstein are represented by the WTSH Corporation for Business Development and Technology Transfer. Subsidisation at the regional level is provided by the “Programme for the Future of the Economy” and the Ministry of Economic Affairs, Labour, Transportation and Technology of Schleswig-Holstein.

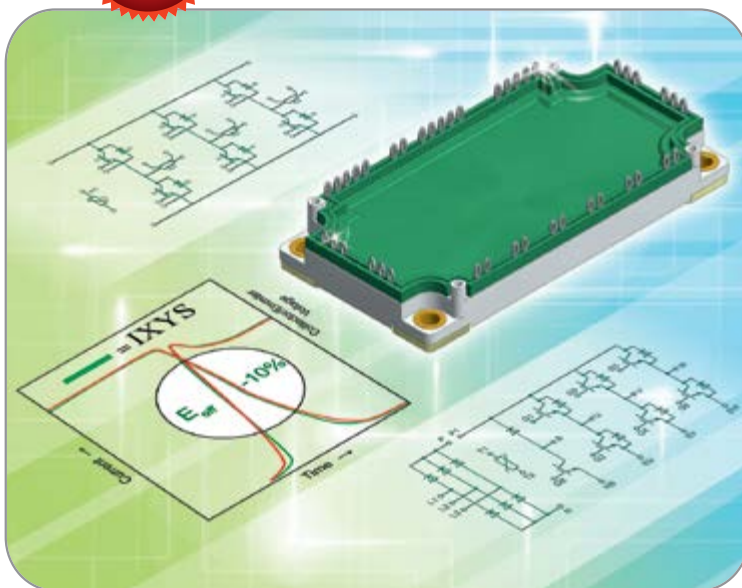
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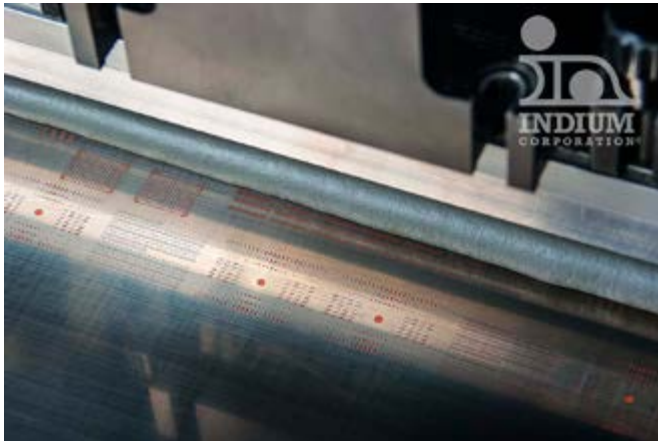
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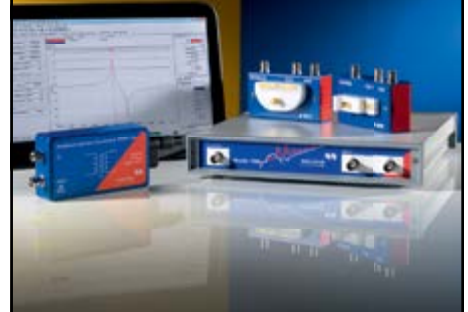
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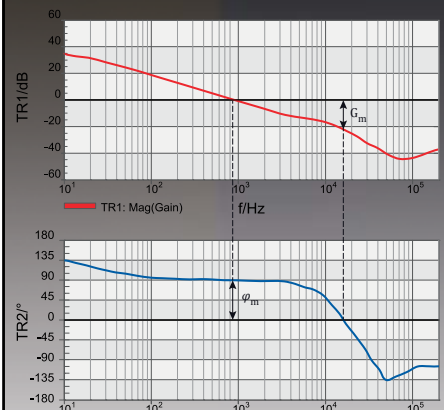
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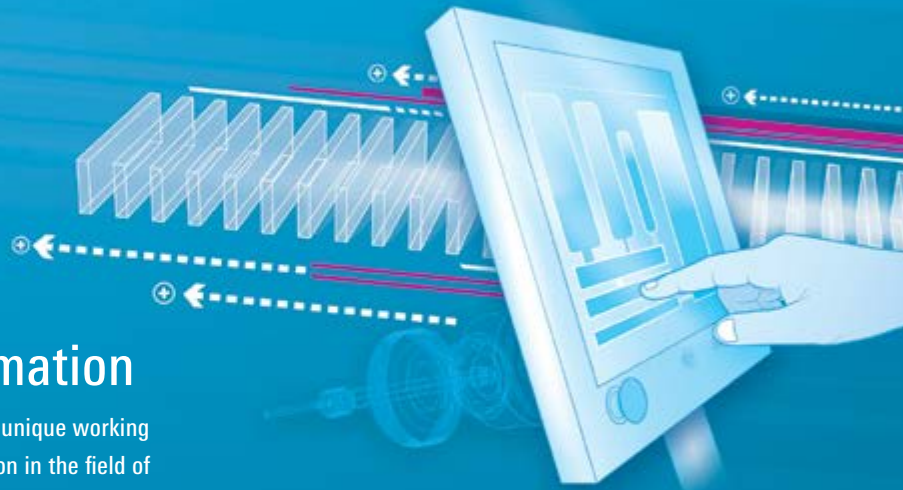
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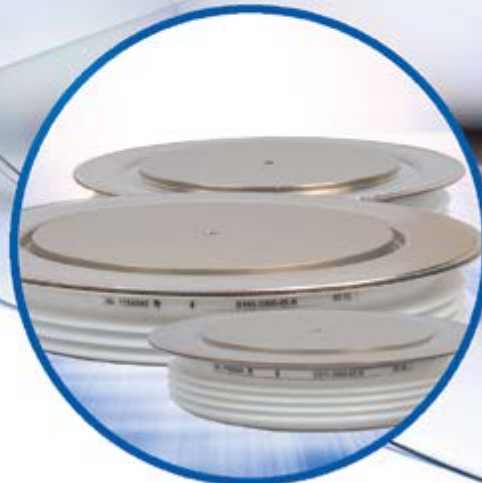
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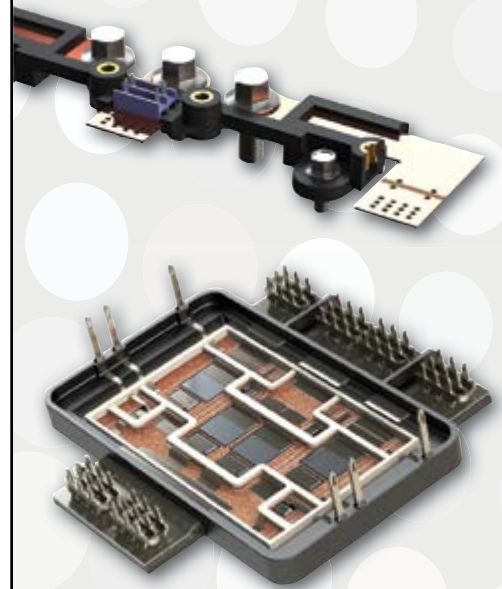
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escalators, cranes and winches, where the mechanical energy of the motor and connected load will be converted into electrical energy for returning (or regenerating) back to the AC supply grid.

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Consultant and owner of an electronics design lab since 23 yrs.
140 publications resp. patent applications, inventor of
the current-mode control in SMPS (US Patent 3,742,371).
Names and business affairs of clients are kept strictly confidential.

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Dual Isolation plus DC-DC Converter Si88x2x Now at Mouser Electronics

Mouser Electronics, Inc. is now stocking Si88x2x Dual Digital Isolators from Silicon Labs. The Si88x2x modules integrates proven digital isolator technology with an on-chip isolated DC-DC converter to provide



regulated output voltages of 3.3V or 5.0V at peak output power of up to 5W with external power switch.

The Silicon Labs Si88x2x Dual Digital Isolators, available from Mouser Electronics, include a DC/DC controller with user-adjustable frequency for minimizing emissions, a soft-start function for safety, a shutdown option, and loop compensation. The Si88x2x modules' topology allows them to sense the output voltage on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the DC-DC converter to operate with excellent line and load regulation while reducing external components and increasing lifetime reliability.

The DC-DC converter works in conjunction with an external transformer to provide up to 5W of isolated power with a 24V input supply and an external switch to supply the secondary side of the Si88x2x, as well as other circuits on the isolated side with a 5V supply. The ultra-low-power digital isolation channels offer substantial data rate, propagation delay, size, and reliability advantages over legacy isolation technologies. Data rates up to 100Mbps are supported, and all devices achieve propagation delays of only 23ns (max).

www.mouser.com/new/Silicon-Laboratories/silabs-si88x2x-isolators

www.mouser.com

Film Capacitors for High-Voltage Applications

The German capacitor manufacturer FTCAP has expanded its portfolio in the area of high-voltage capacitors. The company now offers film capacitors that enable a voltage of up to 120 KV DC, which makes them ideal for use in X-ray machines and high-voltage power supply modules, for example.

The new film capacitors for high-voltage applications are designed for flexible adaptation to the respective requirements: the edge steepness (dU/dt) can be changed individually as needed and the capacitors can also be implemented in diverse types. "We produce the housing ourselves, at the factory in Husum; custom designs are no problem. For example, the new film capacitors can easily be integrated in existing installation spaces," explains Dr. Thomas Ebel,

Managing Director of FTCAP. The innovative film capacitors are available with a voltage of up to 120 KV DC in a housing.

The newly developed vacuum casting technology achieves especially high-quality and homogeneous insulation, which reduces partial discharges to a minimum. The potting and encapsulation are resistant to high-voltage oil to guarantee a long service life. Because FTCAP always strives to convince its customers all along the line, each single film capacitor is subjected to extensive tests and measurements for quality assurance prior to delivery.

www.ftcap.de

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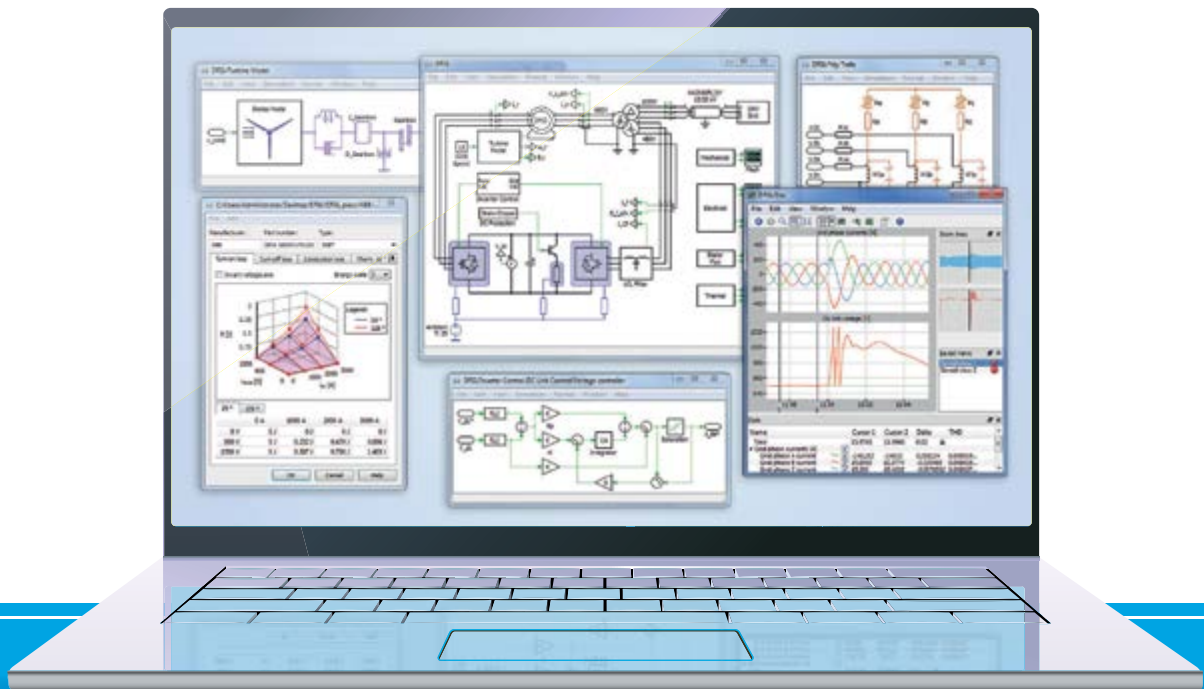
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PMBus Converters with Frequency Synchronization Reduce EMI

Texas Instruments introduced the industry's first 20-A and 30-A synchronous DC/DC buck converters with frequency synchronization for low-noise and reduced EMI/EMC and a PMBus interface for adaptive voltage scaling (AVS). TI's SWIFT™ 20-A TPS544B25 and

30-A TPS544C25 converters integrate MOSFETs and feature small PowerStack™ QFN packages to drive ASICs in space-constrained and power-dense applications in various markets, including wired and wireless communications, enterprise and cloud computing, and data storage systems. Used in conjunction with TI's award-winning WEBENCH® online design tools, the converters simplify power conversion and speed the power supply design process. For more information, samples and an evaluation module, visit <http://www.ti.com/pmbusswift-pr-eu>.

The highly integrated converters feature 0.5 percent reference-voltage accuracy and full differential remote-voltage sensing to meet the voltage requirements of deep sub-micron processors. Frequency synchronization to an external clock eliminates beat noise and reduces EMI. Additionally, the TPS544B25 and TPS544C25 offer pin-strapping that enables the devices to start up without PMBus commands to an output voltage set by a single resistor. Programmability, real-time monitoring of the output voltage, current and external temperature, and fault reporting via PMBus simplify power-supply design, increase reliability, and reduce component count and system cost. Read a blog post on "Selecting the correct PMBus POL solution for your applica-



www.ti.com

2kV and 8kV Safety-Rated High Voltage Differential Probes

Teledyne LeCroy introduces two additions to the HVD3000 series of high voltage differential probes — the 2 kV safety-rated HVD3206 and the 8.4 kV safety-rated HVD3605. These probes demonstrate Teledyne LeCroy's leadership in the fast growing power electron-

ics market by providing superior performance and uniquely meeting specific industry test needs per the latest industry standards. Like the existing 1 kV safety-rated HVD310x probes, these new probes provide excellent performance by offering the best gain accuracy, widest differential voltage range, high offset range and exceptional common-mode rejection ratio (CMRR).

The HVD3605 is safety-rated for 8485 V (DC + pk AC) and 6000 Vrms for the best test coverage of 5kV class electrical apparatus and power electronics. This probe has exceptional 1% gain accuracy, excellent CMRR, standard 6 meter cable, the industry's widest differential voltage range of 7000 V (DC + pk AC) with a 7600 V maximum measurable differential voltage before amplifier saturation, and an industry-best offset range (up to 6000 V) along with 100 MHz of bandwidth. The HVD3605 is the only probe that permits AC Line, DC bus, and drive/inverter output voltage probing through 4160 V apparatus ratings.



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Medium power modules. Industry icons go quality.



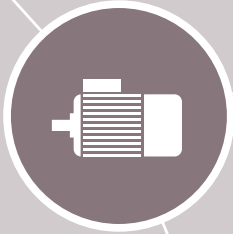
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