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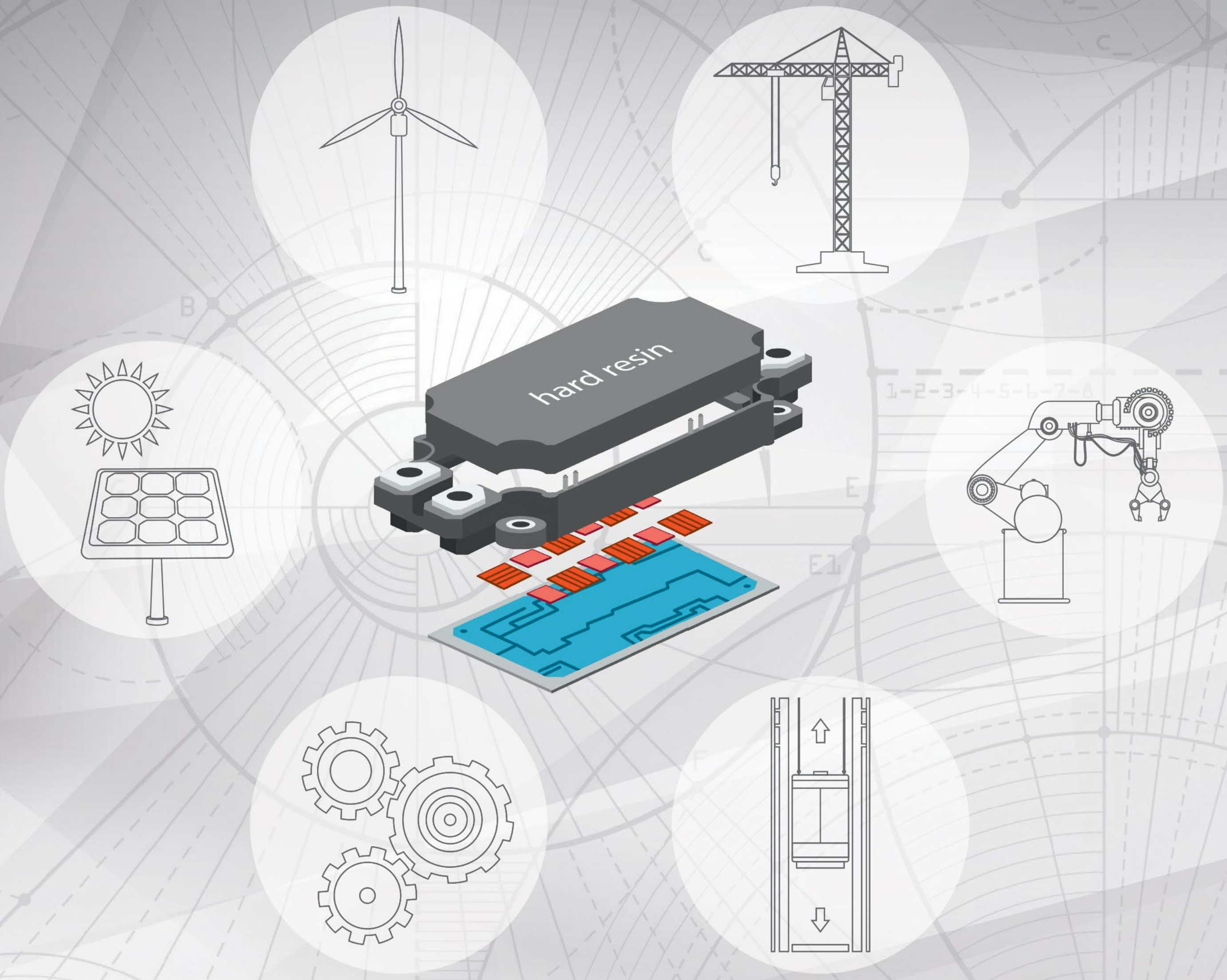
Bodo´s Power Systems®

Electronics in Motion and Conversion

June 2016



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Events

ISPSD'16 Conference,
Prague, Czech Rep. June 12-16
http://www.ispsd2016.com

Intersolar 2016,
Munich, Germany, June 22-24
http://www.intersolar.de/de/intersolar-europe.html

PCIM Asia 2016,
Shanghai, China, June 28-30
http://www.mesago.de/en/PCC/home.htm

SEMICON West 2016,
San Francisco, July 14-16

EPE ECCE 2016,
Karlsruhe, Germany, September 5-9
http://www.epe2016.com/

WindEnergy Hamburg, September 27-30
www.windenergyhamburg.com/

ECCE 2016,
Milwaukee, WI USA, September 18-22
http://2016.ecceconferences.org/

Ten Years Young

This month we celebrate ten years of success for the magazine - and we are still young and moving fast. It has been a decade of success in reporting. We distributed a total of 600 print issues with over 45,000 pages of technical content to our 24,000 subscribers around the world.

On our 10th anniversary, we are still moving quickly, and continually adapting to the pace of developments in power electronics. In addition to the print version, the magazine is available on my web site and is archived, so every issue can be downloaded there for free. New readership has increased steadily year over year, and it is always interesting to follow preferences between print and web usage.

What are ten years in life? It has been a lot for me. After twenty-five years spent in design, application and marketing, editing and publishing was not really new to me. I had always been writing to promote the products I was charged with bringing to market. Traveling to meet with clients or to attend conferences was always the norm. So, although my hair has become grey or disappeared entirely, I still greatly enjoy the traveling and writing for my magazine.

I am just home from a successful PCIM in Nuremberg. Wide Band Gap devices are now on the fast track, and are outperforming established silicon based designs in all kinds of applications. Technology in semiconductors is a fascinating subject, especially considering how much progress we've seen over the ten years. I hope that young people see more than just the surface of a smart phone or tablet. The magic is below the surface. Highly efficient power technology makes it happen.

Our young grandchildren are becoming interested in what I do in my office, along with my train toys that is. Soon it will be time to take them to PCIM to give them a smell of what power electronics is all about. We must encourage our children to understand the relevance of a good education, and a career in engineering. I still have the electric trains of my childhood, and now they fascinate my grandchildren and grand nephews. It's a hobby that can forge long lasting bonds. I learned to love trains from my father and am passing on his enthusiasm to the next generation.

Bodo's Power Systems reaches readers across the globe. If you are using any kind of tablet or smart phone, you will now find all content available on the new web-site www.eepower.com. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodoschina.com

My Green Power Tip for June:
Enjoy the summer and take a rest from work to recharge your batteries. It is time for a swim. If you have a beach nearby use your bike to get there.

Best Regards

Tracking/Security Numbers, Lot Numbers, and Production Dates

Rogers can add data matrix codes (DMCs) to a wide range of metalized substrates, including direct-bonded-copper and active-metal-brazed substrates. Codes, which can be text or numeric in form and encoded by code-reading camera systems, are written on metalized surfaces by means of a thin oxide layer formed by an optical laser system; no additional material is required on the substrate. In addition to bare copper surfaces, data matrix codes can be written on nickel (Ni), nickel/gold (Ni/Au), and silver (Ag) plated surfaces.

Standard data matrix code sizes are 2.3 × 2.3 mm and 3.0 × 3.0 mm, with other sizes available upon request. The single dot resolution is 0.164 × 0.164 mm. Positioning tolerance on a copper pad is ±0.3 mm. Using a data matrix code with 14 × 14 dots, for example, provides as many as 16 digits in a numeric code and 10 digits in an alphanumeric code.

Rogers PES brings its 40+ years of experience together in a handy online resource that is available 24/7. The PES Design Support Hub features complete technical information on ROLINX busbars and curamik ceramic substrates, a library of technical papers on product design and problem solving, helpful videos on products and power distribution topics, and PES University training programs. Registration for access is quick and free. The Design Support Hub helps design engineers increase power, manage heat, and ensure the quality and reliability of their devices for optimal new product design.

www.rogerscorp.com/designhub

Strengthening Custom Power Solutions for Demanding Applications

Powerbox, one of Europe’s largest power supply companies and a leading force in optimizing power solutions for demanding applications, announced today that it has acquired the privately-held German power supply manufacturer Eplax. The acquisition strengthens Powerbox custom-power capabilities, addressing its four major markets - industrial, medical, railway/transportation, and defence - for which the company designs and distributes premium power conversion solutions for systems requiring high reliability.

With more than 80 years of combined expertise, Powerbox and Eplax have delivered more than 3,500 custom-power solutions for a variety of demanding applications worldwide. Formed in 1964 (VERO) the company Eplax has a track record of more than 1,000 successful custom-power projects. With their in-depth competence, they are known for exceeding customers’ expectations in quality, robustness and energy efficient optimization, contributing to longer lifetime and reliability of products. The company portfolio also includes a large range of standard products for rack type applications.

“Powerbox and Eplax have a long history in serving some of the world’s most demanding industries with high quality customized power solutions, bringing simplicity into complex power applications” said Martin Sjöstrand, Powerbox C.E.O. “We are thrilled by this acquisition, which by adding Eplax expertise and skilled employees to the Powerbox Group will benefit all of our customers and support the company’s strategy of bringing simplicity and quality into complex power systems.”

“The previous long lasting working partnership between Powerbox and Eplax has already shown that the combined competences and assets have been valued by our common customers. Together we offer the marketplace leading technical and cost-optimized solutions” said Andreas Mielke, Eplax co-owner. “I’m convinced that with our enhanced worldwide sales presence, in combination with a strong R&D capability and standard portfolio range, we can jointly exploit the full potential of our capabilities to achieve further success in the market place.”

www.prbx.com

US President Obama and Chancellor Merkel at HARTING

Great joy at the HARTING Technology Group: The opening of the world’s largest industrial trade show saw US President Barack Obama visit the company’s stand together with German Chancellor Angela Merkel, with the Harting family greeting the two heads of state. The United States is this year’s partner country of the Hannover Messe.

President Obama was accompanied by a large delegation. Together with Chancellor Merkel, the 44th US president learned about HARTING products and solutions, which are accompanying companies around the globe into Industrie 4.0. The HARTING MICA (Modular Industry Computing Architecture) has been developed for this digital transformation. The MICA is a mini industrial computer that is positioned as a neural interface between machine and Cloud, and enables systems and machines to function as part of the Internet of Things (IoT). President Obama and Chancellor Merkel showed great interest in the presentation of the Rinspeed “Etos” car, in which the MICA captures drive and emissions data and transmits it to testing institutes for independent monitoring.

The HARTING Technology Group is a leading driver and partner on the way to Integrated Industry, and its Industrie 4.0 solutions have been met with great interest in the United States. The re-industrialisation of the nation is acting as a growth engine. This development has also benefited HARTING, which has operated its own production plant in Elgin (Illinois) for a number of years. Sales in the Americas have seen growth of a strong one-third over recent years. The 2014/2015 financial year alone witnessed an increase of more than 17 percent, to 61 million euros.

The visit of Barack Obama is a notable highlight in the history of the HARTING Technology Group. The company is always represented with one of the most attractive stands at the Hannover Messe and ranks among the top 5 largest exhibitors. In addition, HARTING is one of the few companies which have been present every year since the trade show began in 1947.

Caption: The Harting family greeting the two heads of state: Margrit Harting, Maresa Harting-Hertz, Dietmar Harting, Angela Merkel, Barack Obama, Philip Harting (from left to right).The HARTING Group develops, manufactures and distributes electrical and electronic connectors, network components, pre-assembled system cables, and backplane assemblies. These products are capable of withstanding the harshest demands in industrial environments and provide high data rates for electronic applications.

www.HARTING.co.uk

Mersen Laminated Busbar, a Key Enabling Technology

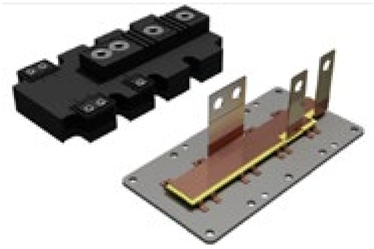
Mersen, a global expert in electrical specialties and graphite-based materials, has presented its unique solution to get the best of the 2 worlds: high T° (up to 200°C) and low inductance laminated busbar for power module packaging, at PCIM Europe 2016 in May.

Mersen Laminated Busbar, a key enabling technology for high frequency, high voltage and high temperature electronics

SiC and GaN power electronics is now gaining momentum offering a complete range of transistors and diodes with enhanced characteristics compared to incumbent silicon devices:

- Higher electron mobility
- Higher junction T° (up to 250°C)
- Higher switching frequency (several 10's of kHz)
- Higher power density

At Mersen, we have increased again our busbar know-how toward carefully selected materials (dielectric and glue), simulation, design rules and related manufacturing process. This enables internal copper busbar compliant with high T° (up to 200°C) and high switching frequency (Stray inductance as low as 35nH in this example).



Picture:An example of newly designed high T° internal laminated busbar for Prime-Pack™ power modules

A complete simulation toolset tailored to your power module

Whatever the power module package type, our multiphysics simulation tools will predict mechanical, thermal and electrical behavior of the whole system. In the PrimePack™ example, the newly designed laminated busbar simulation has been performed using:

- Distance between the plates : 0.23 mm
- Impedance calculating for the complete loop, without influence of the electronic components
- Material used : copper 1 mm.
- The impedance $Z = R + jX$ has been solved from 10 Hz to 10 MHz.
- The loop inductance L is deduced from the imaginary part of the impedance X using $L = X / (2\pi f)$

www.mersen.com

First Section of Europe's Biggest Lithium-Ion Battery Manufacture

Following a construction time of only a little more than one year the Karlstein BMZ GmbH, Europe's leading developer and producer of intelligent lithium-ion batteries, has now opened up the first two production, logistics and office buildings in Karlstein-Großwelzheim in addition to the already existing production areas of 7,000 m² at the present company headquarters. In the manufacturing units disposing of 4,800 m² each, up to 200 million lithium-ion batteries of the most different kind and size with an overall storage capacity of about 15 GWh can be developed, produced and tested every year. Until 2020 four further production, laboratory and office buildings covering an entire space of 15,000 m² are planned on the new company site comprising 55,000 m². After the completion of the construction works up to 1,500 BMZ staff members will produce an annual 800 million lithium-ion batteries of the most different sizes with an overall storage capacity of 30 GWh at the industrial site in Karlstein-Großwelzheim alone.

For years BMZ has been investing enormous double-digit sums amounting to millions of euro in the rapid development and enlargement of its international production capacities. At the moment the company disposes of around 120,000 m² production sites in its own companies in Germany, China, the USA and Poland. As company founder and owner Sven Bauer explained during the official opening celebration for the two new buildings to numerous guests from the world of politics and business, as well as administration, the large-scale project in Karlstein-Großwelzheim now marks one further important milestone in the company's 20-year-long history considering the total investment volume of about 80 million euros. "The current discussions on subsidies for electric cars often forget that lithium-ion batteries are also used in e-bikes, electrical appliances, gardening tools, energy storage systems, transport vehicles, excavators and so on. Unlike electric cars we are presently undergoing a real demand boom in many of these sectors, and we assume that the demand in these segments will further increase by 15 to 30 per cent annually in the coming years depending on application range.

The modular concept of our new ultra-modern factory units enables BMZ to respond even faster and more flexible to this growth scenario as well as specified customer requests in the future," Bauer is pleased.

www.bmz-gmbh.de

The ECPE Calendar of Events 2016

ECPE Workshop '**Power Electronics for e-Mobility'**
22 - 23 June 2016, Stuttgart, Germany
Chairmen: Dr. B. Eckardt (Fraunhofer IISB), H.-P. Feustel (Conti Temic), Dr. T. Leifert (Volkswagen), Dr. L. Schindele (Robert Bosch)

ECPE Tutorial **'EMC in Power Electronics'**
6 - 7 June 2016, Nuremberg, Germany
Chairmen: Prof. E. Hoene (Fraunhofer IZM),
Prof. J.-L. Schanen (G2ELab)

ECPE Tutorial ***'Power Electronics Packaging'***
20 - 21 June 2016, Barcelona, Spain
Chairmen: Prof. U. Scheuermann (Semikron),
Dr. J. Popvic-Gerber (TU Delft)

ECPE Tutorial '**Thermal Engineering of Power Electronic Systems - Part I (Thermal Design and Verification)'**
19 - 20 July 2016, Erlangen, Germany; Chairmen:
Prof. U. Scheuermann (Semikron), D. Malipaard (Fraunhofer IISB)

ECPE Tutorial '**Thermal Engineering of Power Electronic Systems - Part II (Thermal Management and Reliability)'**
18 - 19 October 2016, Nuremberg, Germany;Chairmen:
Prof. E. Wolfgang (ECPE), Prof. U. Scheuermann (Semikron)

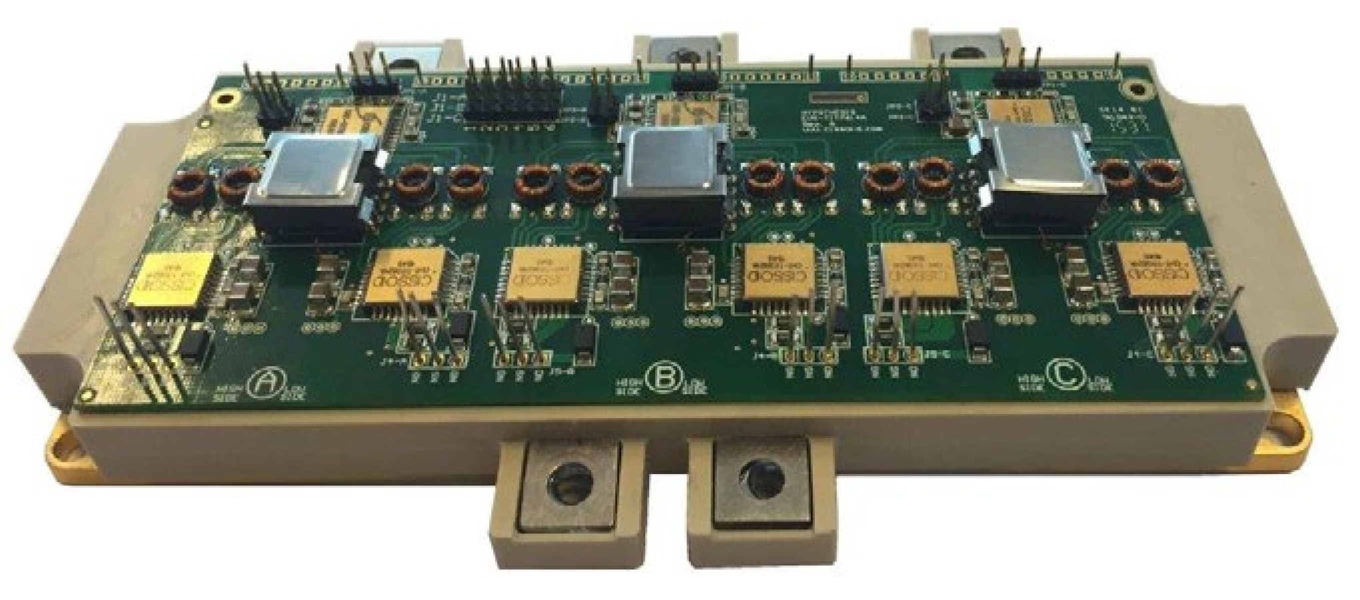
For the ECPE Calendar of Events 2016 with all ECPE Workshops and Tutorials please visit the ECPE website

www.ecpe.org

Delivering first SiC Intelligent Power Modules to Thales

CISSOID, the leader in high-temperature and extended lifetime semiconductor solutions, announces the delivery of the first prototypes of a 3-phase 1200V/100A SiC MOSFET Intelligent Power Modules (IPM) to Thales Avionics Electrical Systems. This module, developed with the support of Clean Sky Joint Undertaking, will help increasing power converters density, by decreasing weight and size, for power generation and electromechanical actuators in More-Electrical Aircrafts.

This IPM offers an optimal integration of the gate driver with power transistors together in order to take advantage of the full benefits of Silicon Carbide (SiC), i.e. low switching losses and high operating temperature. Leveraging on HADES2® Isolated Gate Driver that incorporates years of development in driving SiC transistors, it combines advanced packaging technologies enabling a reliable operation of power modules in extreme conditions.



For this Aerospace module, a 3-phase power inverter topology was selected while other topologies are being investigated for HEV and Railways projects. In this 3-phase topology, each of the 6 switch positions includes a 100A SiC MOSFET transistor and a 100A SiC Schottky free-wheeling diode. These devices can block voltages up to 1200V, which provide enough headroom against overvoltages in a 540V Aerospace DC bus, and the module is designed to be easily upgraded with 1700V/150A SiC devices. The transistors have a typical On resistance of 12.5mOhms or 8.5mOhms depending on their current rating, either 100A or 150A.

Special care was put on thermal aspects during the design of the module. First, all the materials have been selected to allow reliable operation at high junction temperatures, up to 200°C with peaks at 225°C, in order to decrease cooling requirements. This materials selection also enables high case and storage temperatures, up to 150°C. Finally, the module is based on high-performance materials such as AlSiC baseplate, AlN substrates and Silver Sintering in order to offer near perfect CTE matching with SiC devices and high robustness against thermal and power cycling.

Co-designing the gate driver with the power module in a single IPM allowed CISSOID to optimize the gate driver circuit taking into account parasitic inductances of the power module while minimizing them when possible. Minimizing parasitic inductances allows to switch SiC transistors faster and to lower switching losses. An IPM also offers a plug-and-play solution to power electronic designers who save a lot of time in the design of the gate driver board, which is particularly challenging with SiC transistors. They can then focus on the design of high density power converters taking advantage of SiC.

“It was a pleasure to work with CISSOID team in the frame of this Clean Sky program. They showed a great flexibility in proposing us solutions addressing the requirements of the next generation of high density power converters for the More-Electrical-Aircraft” said Taoufik Bensalah, Power Converter Design Team Manager at Thales Avionics. Etienne Vanzieleghem, VP Engineering at CISSOID added: “We are very glad with this fruitful cooperation with Thales and with the open discussions we had in specifying this IPM. We also thank Clean Sky for making this cooperation possible which is a good example of CISSOID combined expertise in packaging and circuit design. This project was also an opportunity to strengthen our cooperation with PRIMES platform in Tarbes which is hosting CISSOID packaging team.”

For more information, visit www.cissoid.com or contact the company’s representatives at

www.cissoid.com/company/about-us/contacts.html.

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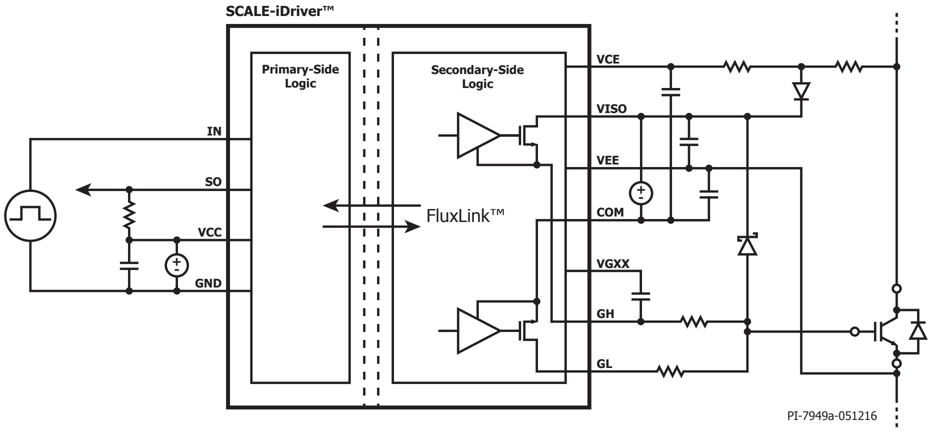
Single-Channel Gate Driver ICs with Reinforced Isolation



- 2.5 A, 5 A, 8 A output current devices
- Drives 1200 V IGBTs and MOSFETs up to 110 kW
- Revolutionary FluxLink™ communication technology
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Win a mTouch Capacitive Touch Evaluation Kit!

Bodo's Power is offering its readers the chance to win the new mTouch Capacitive Touch Evaluation Kit from Microchip. The mTouch Capacitive Touch Evaluation Kit enables designers to quickly and easily develop capacitive touch user-interface applications using Microchip's 8- and 16-bit PIC® microcontrollers (MCUs). The flexible, comprehensive kit includes two main boards - one populated with a PIC16F72X 8-bit MCU and the other with a PIC24F256GB110 16-bit MCU; four daughter boards for developing capacitive-touch keys, sliders and a matrix; a PICkit™ Serial Analyzer; an easy-to-use Graphical User Interface (GUI); and several code and schematic examples. The modular kit makes it easy for designers to try different keypad configurations, and experiment with touch-pad sizes and shapes using the mother boards.

Touch-sensing technology is increasingly being adopted to improve the look and durability of user interfaces in appliances, consumer-electronic devices, medical electronics, automobiles and many other markets and applications. Microchip's new MCU-based kit provides a one-chip, highly integrated solution based upon either the PIC16F72X 8-bit or the PIC24FGB 16-bit general purpose MCUs, providing a flexible evaluation platform that lowers costs and shortens time to market.

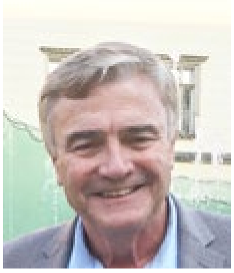
For your chance to win a Microchip mTouch Capacitive Touch Evaluation Kit, visit and enter your details in the online entry form:

http://www.microchip-comps.com/bodo-mtouch0610


REMOTE HOME CONTROL
22°C
ECO MODE
NORMAL
OFF

Podium Session at PCIM Europe Marks New Chapter in GaN Power Device Adoption

By Greg Evans, WelComm, Inc, Special Correspondent



Over the years, GaN power has been sarcastically described as “the technology of the future…and always will be.” While silicon carbide devices have been gaining a stronger beachhead in displacing IGBTs in higher voltage applications, the evolution of GaN as a cost-effective alternative to Si MOSFETs in applications from 200V up through 600V was, in many instances, moving at a glacial pace. This year’s podium session, hosted by Bodo’s Power Systems, entitled “GaN – Volume, Production and Cost” made it clear that this is no longer true.

Senior representatives GaN power manufacturers (EPC, Transphorm, GaN Systems, Infineon and Navitas) presented details of their significant developments in moving the technology into mainstream, volume applications. Based on the information presented in the five talks, there are three significant reasons to expect dramatic growth in adoption of GaN power devices.

The first of these is qualification testing. Long term reliability data, by definition, takes time. Process enhancements by the early participants in this sector - EPC, Transphorm and GaN Systems - have all demonstrated that, once the GaN on Silicon process challenges have been met, the intrinsic reliability of the devices is without question. Industry committees are now working on solidifying the JEDEC-style quality and reliability standards for GaN devices.

The second key ingredient is production volume. There are now five GaN wafer fabs in operation. All of the major players, including the three previously mentioned plus Infineon have active lines in place. GaN Systems is working with tsmc, EPC with EPISIL. Transphorm now has dedicated use of Fujitsu’s GaN facilities, plus a R&D fab in the US. GaN systems projects a 10X expansion of capacity in 2016. EPC projects its current capacity to fully exceed market forecasts through 2020. And Transphorm announced that is has actually produced over one million production devices in the past 12 months.

The third, and clearly the most significant reason, is adoption of the technology by volume manufacturers. Applications described that are either in early production stages or will soon be announced include plug-in and wireless charging, on-board EV chargers, solar inverters, data center power supplies and industrial motor drives.

The areas where there are still vast differences in approach to this nascent market are topology and packaging.

In terms of topology, both GaN Systems and EPC and Infineon (IR) have adopted an eMode topology. Transphorm have developed their devices using a cascode topology. All four of these utilize a separate gate driver. Navitas, the latest entrant to the GaN discussion, is developing an eMode GaN power IC with integrated driver. At this point, it would appear that an important trade-off between the two topologies, eMode vs. cascode, is switching speed vs. driver compatibility. eMode devices can operate at higher frequencies but have very tight limits on driver input voltage; cascode mode devices are limited in operating frequency but can use any power MOSFET driver.

Packaging is the other differentiator. One one end of the spectrum, EPC has taken the position that no packaging is the best answer. In its target markets, it is delivering chip-scale devices. On the other end of the spectrum, Transphorm is packaging some of its devices in traditional TO-220 and TO-247 packages to satisfy their customers’ requirements.

Finally, the idea of costs, when compared with Si solutions was discussed by several of the presenters. EPC made a chip-by chip comparison that claimed eGaN FET costs to be lower than MOSFETs (at the chip level).

GaN Systems, Transphorm and Navitas viewed this question from the perspective of final system cost. According to GaN Systems, “its’ not the cost of the part. It’s what you get for your money.” Transphorm reinforced this by presenting an example of a server power supply PFC with a 10% lower parts cost using GaN compared to Si. In addition, the overall 1.35% loss of the totem pole design is nearly a 40% improvement over the silicon solution power loss of 2.2% . Finally, Navitas is projecting its GaN IC to have a lower system cost per Watt than all other solutions.

In summary, the conversation about GaN has clearly changed. It is no longer a question of if or even when GaN power devices will start to impact the power conversion industry. GaN is the technology of the future…and the future is now.

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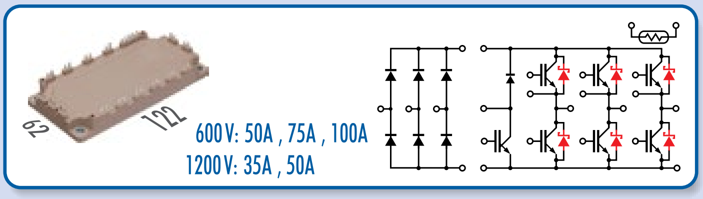
Hybrid IGBT Modules

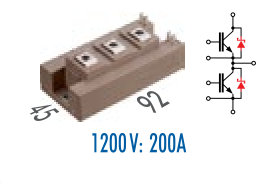
Si-IGBT with SiC-Schottky diode

- Higher efficiency
- Higher output current
- Suitable for high switching frequencies
- Significant lower reverse recovery and turn-on losses

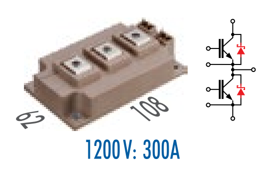
1200 V: 100A



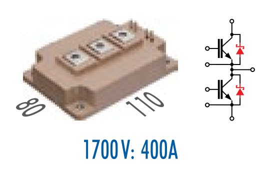
600 V: 50A , 75A , 100A
1200 V: 35A , 50A



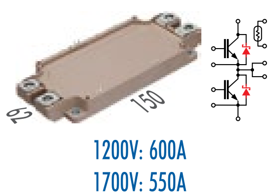
1200 V: 200A



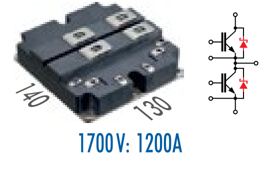
1200 V: 300A



1700 V: 400A



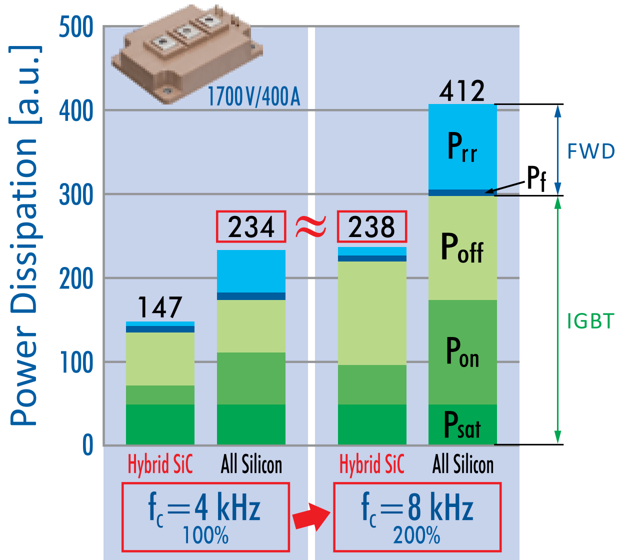
1200V: 600A
1700V: 550A



1700 V: 1200A

Comparison between All Silicon and Hybrid-SiC Module

Power dissipation at f_c = 4 & 8 kHz

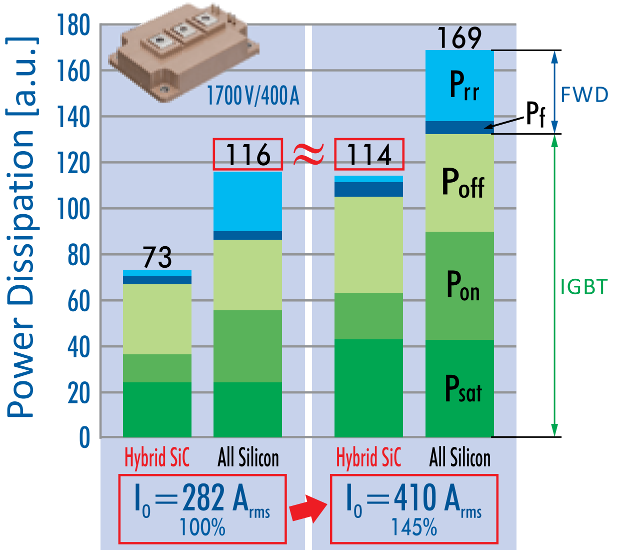


100% higher carrier frequency at same power dissipation

Conditions

V_{CC} = 900 V • f_0 = 50 Hz • cosφ = 0.9 • λ = 1.0
I_0 = 282 A_{rms}
f_c = 4 ~ 8 kHz

Power dissipation at I_o = 282 & 410 A_{rms}



45% higher output current at same power dissipation

Conditions

V_{CC} = 900 V • f_0 = 50 Hz • cosφ = 0.9 • λ = 1.0
I_0 = 282 ~ 410 A_{rms}
f_c = 4 kHz

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Enhanced Power Density and Expanded Line-up of the 7th Gen Industrial IGBT Modules Utilizing the Improved Thermal Conductivity of the Highly Reliable SLC-Technology

The 7th gen. Industrial IGBT modules have been successfully developed for the 650V and the 1200V classes to cover important power electronics system requirements such as high efficiency, high power density and high reliability. The outstanding results pertaining to the thermal cycling capability, the "pumping out failure" free package and the low thermal resistance of the SLC-Technology in combination with the low loss 7th generation chipsets are the key reasons for the success of the 7th gen NX-type IGBT modules. To expand this technology to the 1700V class IGBT modules, the insulation capability and the thermal conductivity of the SLC-Technology's IMB has been improved.

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Power Device Works

Introduction

The 7th gen. 650V and 1200V class Industrial IGBT modules have been introduced recently to the market. In this new IGBT module generation, the latest chip technology has been utilized [1] to cover the requirements of industrial power electronics applications. All those applications utilize the superior characteristics of the 7th gen NX-Type IGBT modules which are - compactness, high power density, high reliability, high efficiency and reasonable cost [2]. To expand the area of applicability to the 1700V class modules, the IMB (Insulated Metal Baseplate) which is a key element of the SLC-Technology has been improved.

SLC-Technology with high thermal conductivity and insulation properties

Generally, Al_2O_3 substrates are often used as the insulating layer in power modules. However, Mitsubishi Electric has employed the Aluminum Nitride (AlN) substrate in the previous generations e.g. 5th and 6th gen. IGBT modules. Due to the superior thermal conductivity achieved by using AlN instead of Al_2O_3 the total thermal resistance Rth(j-c) between the chip and the baseplate was reduced by about 35%, see Figure 1

However, it is difficult to improve the thermal conductivity of ceramic any further. In addition, there is a stress experienced at the interconnection between the ceramic layer and the metal layer during thermal cycling due to the mismatch of CTE (Coefficient of Thermal Expansion) between these materials as shown in Table. 1. However, employing thinner ceramic substrates with the aim of improving the thermal resistance is not always the best approach. The thinner the substrate, the more sensitive it becomes against damages as a result of mechanical stresses. To address this problem, the SLC-Technology with the IMB structure has been developed [3]. A cross section of this new structure is shown in Figure 2,

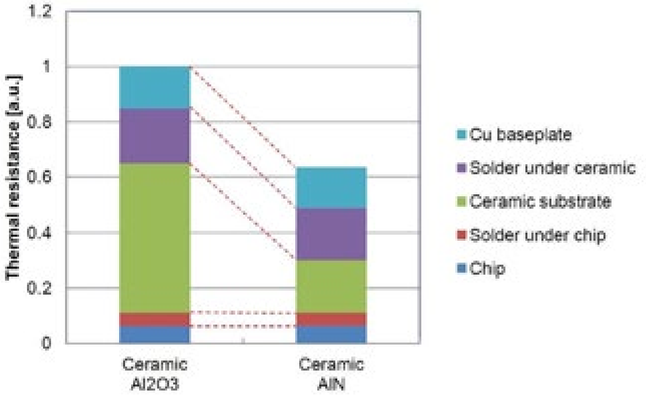

Figure 1: Simulation result of thermal resistance Rth(j-c)

By selecting the CTE-value of the IMB's insulating resin layer to be close to the CTE-values of the top and bottom metal layers, the mechanical stress caused by the mismatch of the CTE-values is re-

Material	CTE [ppm/K]
Ceramic	4.5 ~ 7.0
Cu	≈17
Insulating resin layer	≈17

Table 1: Coefficients of Thermal Expansion CTE

duced. Therefore, in comparison with the conventional structure using ceramic isolation substrates, the thickness of the insulating layer in the IMB can be reduced and the thickness of the metal layers can be increased respectively. By this approach, a thick metal layer can be chosen at the bottom side, thereby substituting the metal baseplate and eliminating the large solder layer area between baseplate and the ceramic substrate which is typical for conventional modules. As a result, the thermal resistance and the thermal cycling capability can be improved.

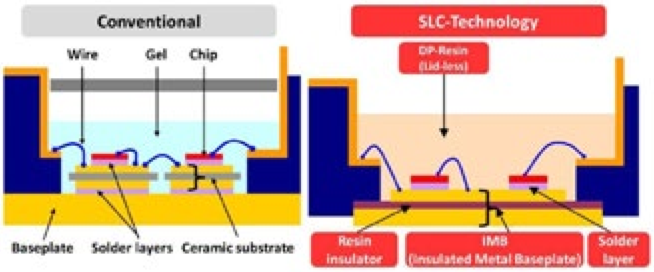

Figure 2: Package structure of conventional and new 7th gen NX-type IGBT module with SLC-technology

Furthermore, compared to the surface area available for chip mounting at ceramic substrates, the surface area of the newly developed IMB can be enlarged because the size limitation known for ceramic substrates does not exist for IMB. Eliminating this size limitation provides flexibility in designing the size and the shape of the IMB. As result a higher chip mounting density in the module can be achieved by eliminating the interconnecting wires between the multiple isolation substrates. In addition, the thickness of the topside metal layer can be increased resulting in a reduction of the electrical lead resistance. This allows for designing the top side metallization pattern with narrower current traces, which helps in further increasing the area available for chip mounting and thereby increasing the power density in the module.

A second positive result obtained by employing an increased thickness of the topside metal layer is associated with the heat spreading effect which in-turn facilitates a further reduction in the thermal resistance "Rth(j-c)" and a reduction in the transient thermal impedance "Zth(j-c)" by virtue of the enhanced thermal capacity.

Optimization of the properties of the IMB for higher isolation voltage

The complete line-up of 7th gen NX-type IGBT modules is given in Table 2. The isolation voltage of 650V and 1200V class modules is specified as Viso=2,5kV AC 1min; for the 1700V class modules the isolation voltage is Viso=4kV AC 1min.

Circuit	Package Size [mm²]	I_C [A]		
		650V	1200V	1700V
2in1	62x152		225	225
		300	300	300
		450	450	450
		600	600	600
	114x110		1000	
6in1	62x122	100	100	100
		150	150	150
		200	200	
7in1	77x137	150	100	
		200	150	

Table 2: Line-up of 7th gen NX-type IGBT modules

An example of module package is shown in Figure 3. The same package size (62mm x 152mm footprint) is used for the 600A 2in1 modules for all three voltage classes 650V, 1200V and 1700V.

For reaching the same 600A rated module current at Vces=1700V and Viso=4kV in the same package size with 62mm x 152mm footprint, the IMB had to be improved. It was necessary to increase the specific thermal conductivity of the insulating resin layer in order to compensate the additional thickness of the insulating layer needed for Viso=4kV.

Figure 3: Package outline of 600A 2in1 NX-type IGBT module for 650V, 1200V and 1700V

The insulation layer of the IMB consists of resin and ceramic particles. To achieve an improvement in thermal conductivity, it is necessary to increase the area of the heat conducting path within the isolation layer (represented here by the ratio of the ceramic particles to the resin quantity, the higher the ceramic particles ratio, the better the thermal conductivity and vice versa). However, for a given fixed volume, if the ratio of ceramic particles to the resin quantity is increased, the quantity of resin shrinks. This reduced resin quantity results in lower viscosity and consequently hinders the productivity of the IMB manufacturing process. Further, if the ceramic particles volume concentration exceeds a critical value, the dielectric breakdown voltage capability decreases drastically. Thus, the quantity of ceramic particles, the resin quantity and the distribution of the ceramic particle size need to be carefully adjusted in order to achieve well-tuned trade-off characteristics of the isolation layer. By virtue of tailored resin material composition design and IMB manufacturing process optimization, it was possible to enhance both the thermal conductivity and the withstand voltage capability as reflected in the successful realization of the NX-Type 1700V class modules [3].

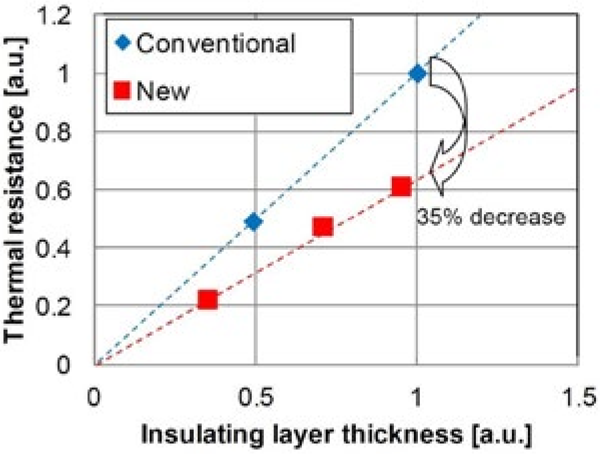

Figure 4: Measurements result of IMB thermal resistance with different thickness

Figure 4 shows the measurement result of the thermal resistance of the IMB versus the resin insulating layer thickness. The total thermal resistance of the IMB is approximately 35% better compared to

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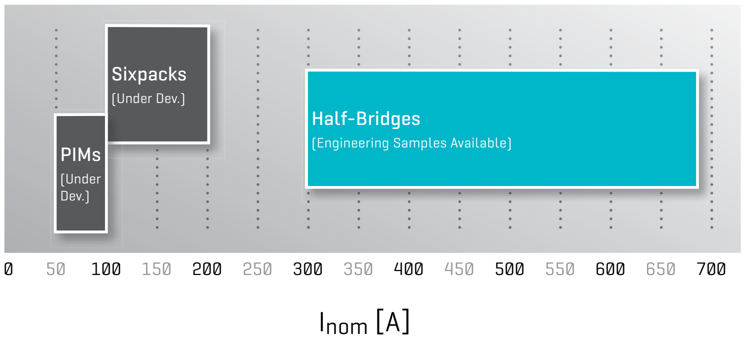

the conventional IMB because the thermal conductivity of the resin insulation layer is enhanced by 50%. The new IMB’s partial discharge inception voltage (PDIV) shows almost the same dependency on layer thickness as the conventional IMB. Thus, the proposed IMB has been confirmed to have equivalent PDIV and insulation characteristics while possessing an improved thermal conductivity.

Figure 5:
Example of the improved 1700V IGBT module by the new IMB

An example for the achievable package size reduction by improved IMB is shown in Figure 5. For the previous 6th generation 600A/1700V 2in1 module the package footprint was 122mm x 152mm; the 7th gen NX-type has a footprint of 62mm x 152mm, which corresponds to a 49% reduction.

Figure 6 shows a summary of the characteristics of the new and the conventional IMB. It is confirmed by evaluation that the thermal resistance of the new IMB for the 1700V module is approximately 5% better than the conventional IMB for the 1200V module.

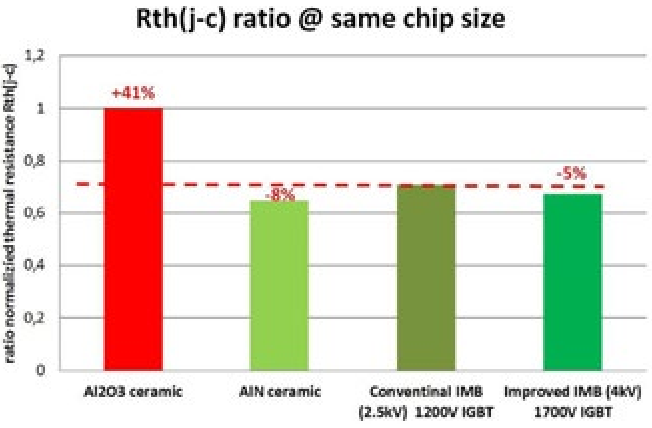

Figure 6: Comparison of thermal resistance Rth(j-c) ratio

On the other hand, the new IMB could also potentially reduce the thermal resistance for 650V and the 1200V class IGBT modules. Such combination of low loss 7th generation chips and the proposed improved SLC-Technology would enable us to increase the current density of the modules further. This option is currently under investigation.

High thermal cycling capability

The SLC-Technology utilizes layers with matched CTE-values as described above. Additionally the epoxy resin encapsulation can reduce the strain on the solder layer under the chip. [4] This ensures higher reliability during heat cycling and thermal cycling. Figure 7 shows the Scanning Acoustic Tomography (SAT) images by heat cycling test (-40~+125deg.C) at initial, 300 cycles and 600 cycles. Conventional structure had degradation of the solder layer under the ceramic substrate after 300 cycles. On the other hand, the new structure with the DP encapsulation has the solder layer only under the chip and no degradation after 600 cycles was observed. This result is the consequence of the elimination of the substrate solder layer and the utilization of the epoxy resin layer.

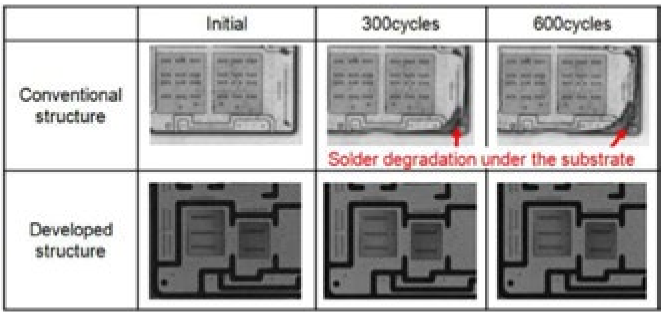

Figure 7: SAT images at different number of cycles

Figure 8 shows the result of the thermal cycling test (ΔTc=80K (+45~+125°C)). The newly developed structure was tested until 40k cycles and has not failed yet. On the other hand, the conventional structure had degradation of the solder layer under the substrate (similar to the result of heat cycling). From this result, the new package with DP resin and IMB increases the thermal cycling life dramatically comparing with the conventional structure. This aspect is contributed by eliminating a solder layer under the insulator and thereby reducing the strain of solder layer under the chips.

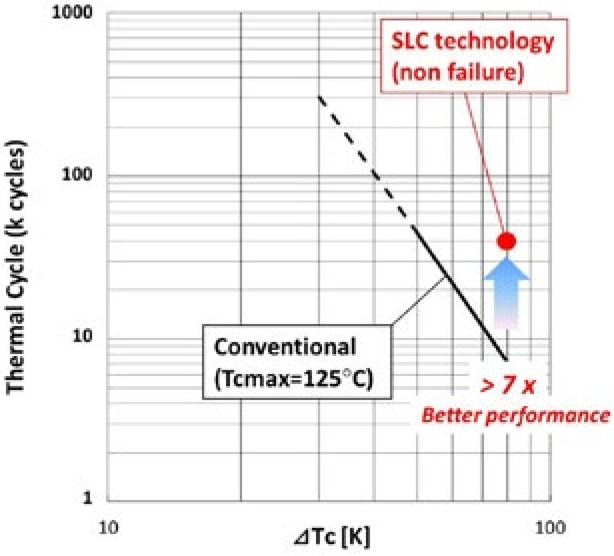

Figure 8: Thermal cycle test result of the SLC-Technology

SLC-Technology offers a ‘pumping-out-failure’ free package

The thermal resistance between the junction and the case has been successfully reduced by the improved IMB (as explained above). To achieve a higher power density and a high reliability, the thermal resistance Rth(c-s) between base plate and the heatsink must be optimized.

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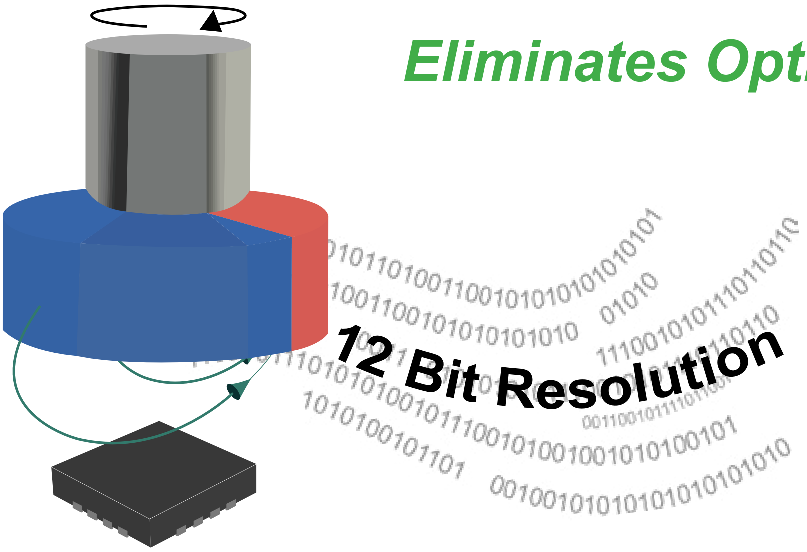

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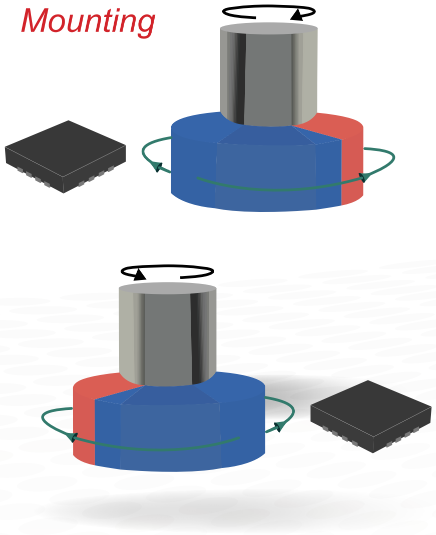

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In general, thermal interface materials are applied between the base plate of the module and the cooling fin to get an enhanced thermal contact, and its parameters (such as thickness, performance, material property) have an impact on the heat dissipation capability and reliability [5]. On the other hand, it is well known that the shape of the base plate of the power module is deformed by temperature changes generated by power losses in the IGBT- and Diodes-chips. This small but repetitive deformation of the base plate pushes out the thermal interface material, and is referred-to as the “pumping out phenomenon”. For assuring a long-term stability in the thermal interface material, it is required to develop an advanced package structure which is capable of preventing the warpage of the base plate under continuous temperature cycles.

The conventional structure of the power module is shown in Figure 2 and their components along with their coefficients of thermal expansion (CTE) are described in Table. 1. In this structure, ceramic, solder and copper base plate, which are the constituents of module base, have different CTE-values. When the case temperature changes with the heat generated by the various IGBTs / FWDs operation, each component expands and contracts to different extents due to the different CTE-values. Finally, among the various layers, the differential strain results in differential deformation, such as with typical bimetal structures. This phenomenon is the cause of the base plate warpage.

The repetitive temperature change in a power module creates a repetitive warpage of the base plate as shown in Figure 9 (a) and (b). This warpage pushes out the thermal interface material. This pumping out phenomenon results in an ineffective thermal contact between the base plate and heatsink. This causes the degradation of Rth(c-s) and the heat dissipation capability of the power module. The consequence is an accelerated aging of the power module which in the worst case - results in the thermal destruction of the module when the junction temperature exceeds the absolute maximum rating.

a) Plus bend (convex) by high temperature

b) Minus bend (concave) by low temperature

Figure 9: Phenomenon of baseplate warpage

The new package structure can dramatically reduce the differential strain between component materials of the module by matching their CTE-values. The internal structure of the package and their CTE-values are described in Table 1 and Figure 2. This well-balanced (with respect to the CTE-values) structure results in much less deformation of the base plate caused by temperature change in comparison with a conventional structure. Figure 10 shows the result of the stress analysis (finite element method) for the base plate components (conventional and new structure respectively). The magnitude of the displacements shown in the Figure 10 have been enlarged by the same factor in order to make the differences more visible.

The simulation results depict that the new structure with the resin material has an improved response with respect to the base plate deformation during temperature changes.

For experimental verification, the vertical displacement of the baseplate center point was measured at three different ambient temperatures controlled by an environmental chamber. The reference length was 91mm in the longitudinal direction. The displacement measured during the temperature change from 25°C to 125°C resulted in only 13.4μm, which means that there was no significant warpage of the base plate. In the actual evaluation with a typical thermal interface material, no pumping out was found after 300 heat cycles (-40°C ~ +125 °C).

It is confirmed that the new power module structure, which has a matched coefficient of thermal expansion between adjacent layers, is able to minimize the warpage of base plate during temperature cycling and thereby provide a substantial reduction of the possibility of a pumping out failure event.

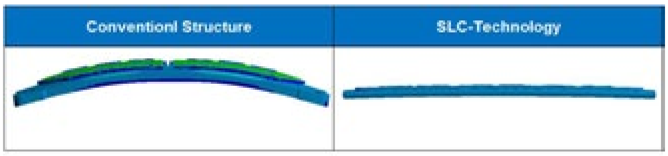

Figure 10: Finite element simulation results of baseplate warpage

Summary

The improved SLC-technology enables an expansion in the line-up of the 7th gen. NX-series IGBT modules to the 1700V class by utilizing the higher insulation voltage and the superior thermal conductivity of the improved IMB. This technology enables the development of a 600A/1700V module with a 122x62mm² footprint.

This SLC-Technology also offers a drastically improved thermal cycling capability in combination with the elimination of the pumping-out failures. The 7th gen chips provide excellent efficiency by the reduction of power losses. By combining this chip set with the SLC-technology, the newly developed 7th gen NX-series IGBT provides an excellent answer to the requirements of power electronics systems such as high efficiency, high power density and high reliability.

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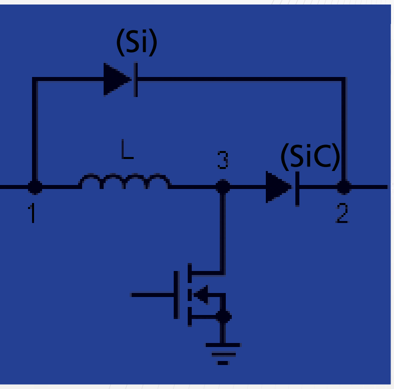

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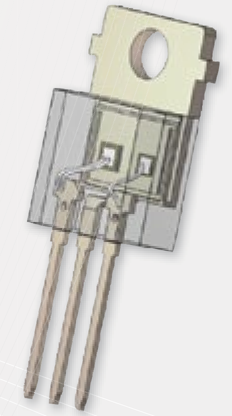

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Modern Shunt Reactors and Static Var Compensators for Electrical Grids Can Be More Economical

With the circuit topology presented in this article, it is possible to construct reactive power compensation devices, which are significantly more economical than comparable SVC (Static Var Compensators), though they exhibit nearly the same functional properties. The proposed circuit topology is especially advantageous in the high-voltage grids (110 kV and above) and for applications as a pure controllable shunt reactor.

By Andrey Gavrilov, Maschinenfabrik Reinhausen GmbH, Regensburg, Germany

Modern electrical power grids are facing many challenges due to their increasing complexity in operation and structure. Primarily their stability is often nearly exhausted [1-4]. One of the main causes of grid instability is the grid's inability to meet the demand of reactive power [3].

The most popular means of improving the ability of a power system to ensure the required reactive power flow at the correct time is shunt compensation with controlled or uncontrolled devices [5]. Under specific conditions and for specific purposes, such as flicker reduction or damping of voltage oscillations, it is very reasonable to employ controllable reactive power compensation devices with response times of less than 20 ms, which can only be achieved by using semiconductor switches.

The first power electronic devices for reactive power compensation were static var compensators (SVC) combining thyristor-controlled reactors (TCR) and thyristor-switched capacitors (TSC) that appeared in the 1970s [6]. As the power switches with forced turn-off capability, such as IGBT or GTO, became commercially available, STATCOM (Static Synchronous Compensator) began to gain substantial market share. Although the latter provides more functionalities and advantages regarding dimensions and weight, the choice between SVC and STATCOM is influenced by a number of specific conditions and requirements. Especially at the power range above 35 Mvar, STATCOM becomes unacceptably expensive and can rarely compete with SVC.

This article focuses on thyristor-controlled devices for reactive power compensation that have very similar performance to TCR and SVC but has significant advantages in economical terms at high power applications.

Functional Overview

The main feature of the proposed circuit topology is its inductive part, which basically consists of an inductor and a transformer with a main winding and galvanically isolated control windings that are controlled by a solid state switch. The basic scheme of the inductive part is shown in Figure 1.

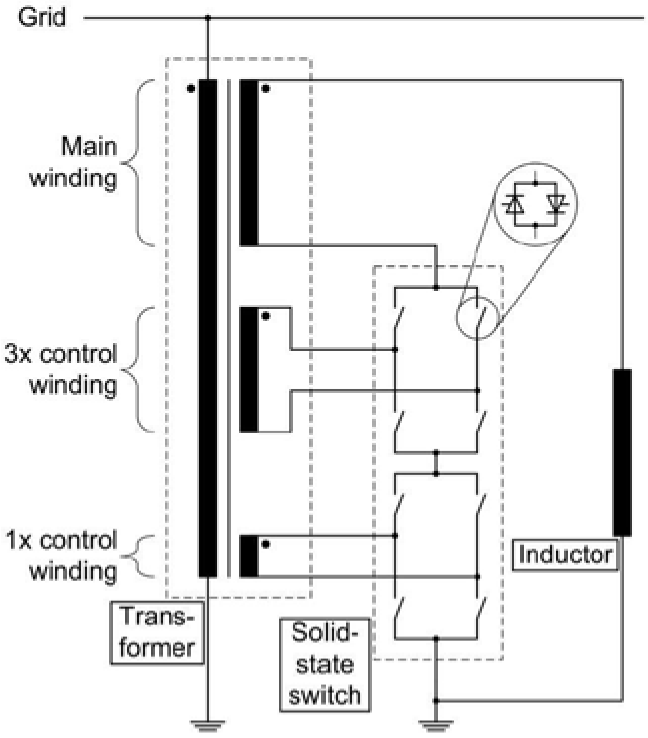

Figure 1: Circuit diagram of the inductive part

The semiconductor switch is built of one or several commutation cells. The purpose of each commutation cell is to establish a connection between the corresponding control winding and the main winding. There are three possible positions of the control winding: it can be connected in the same direction, in the reverse direction or in neutral position in relation to the main winding. For safe tap changing a safe commutation algorithm is required, which preserves the windings against short circuit [10]. In fact, different topologies may be realized with bidirectional switches, an overview of some of them can be found in [7]. A compromise between construction complexity and achievable number of steps can be realized by, for instance, three control windings proportioned as 1x-3x-9x, resulting in 27 steps.

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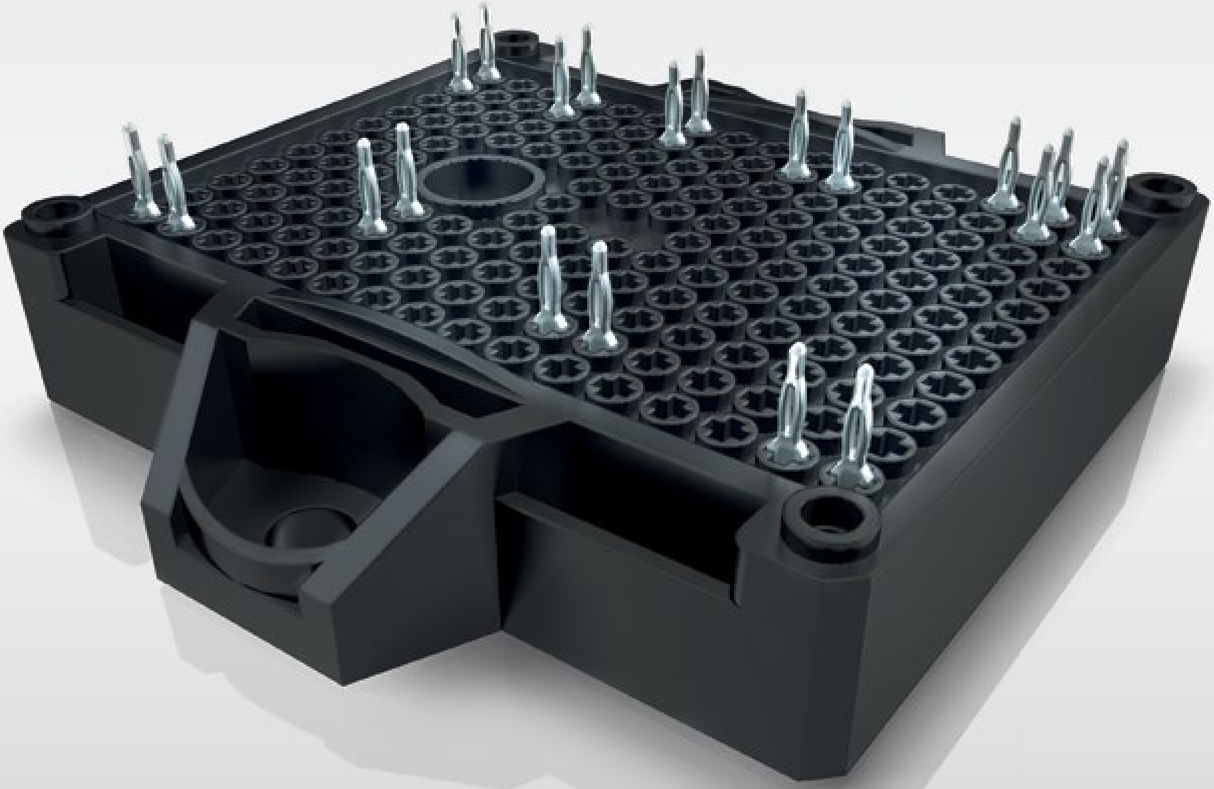

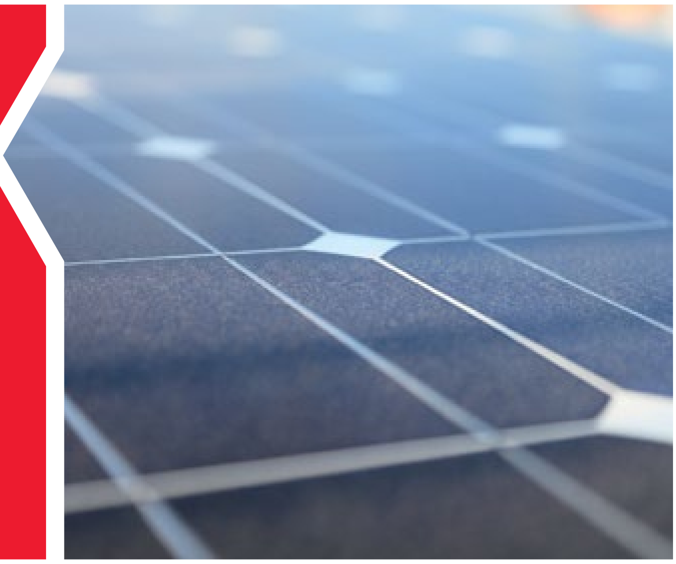

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In this way, the effective number of turns at the high voltage side of the transformer can be varied, which controls the voltage and the current of the inductor and therefore the overall reactive power supplied by the system. Therefore, the compensated reactive power is proportional to the square of the resulting transfer ratio of the controlled transformer. The following equation defines the reactive power in the inductive range:

$$Q_{Ind} = \frac{U_{Grid}^2}{2\pi fL} \cdot \left(\frac{N_{PW}}{N_{SW}}\right)^2, \qquad (1)$$

whereas UGrid is the grid voltage at the connection point;
L – inductance of the inductor;
N_{PW} – number of turns in the primary winding of the transformer;
N_{SW} – number of turns in the secondary winding of the transformer.

The described way of operation yields some considerable advantages: firstly, the overall rated power of the semiconductor switch amounts to only half of the rated inductive power capability of the system; secondly, no harmonic filters are required, because the currents are sinus-shaped in contrast to the classical SVC, where the currents are significantly distorted due to the thyristor phase control.

Utilization as a fast controllable shunt reactor

The quadratic relationship between the transformer's turn ratio and the compensated reactive power determines a further potential for savings in terms of investments if the control range does not approach zero.

This can be seen in Figure 2, where the control characteristic is shown. In this example, the required control range is defined from 20% to 100% of the maximum reactive power. This implies that the power rate of the semiconductor switch has to be as high as 28%, i.e. less than one third of the power rate of the system. As the semiconductor switch for the proposed circuit has two identical branches, and each of them must be rated to the whole switch power, the overall rating of the thyristors compared to a TSR (Thyristor-Switched Reactor) with only one branch will be about 56%, which is nevertheless a significant saving.

In general, the relation between the ratings of power electronic switch and maximum reactive power is defined by the following equation:

$$v = \frac{1 - \sqrt{Q_{min}}}{2}, \qquad (2)$$

where Qmin is the lowest limit of the control range or – in other words – the minimum reactive power absorbed by the device.

Fast controllable shunt reactors are becoming an important part of high-voltage power transmission lines, especially when electrical power has to be transferred to distant and abruptly changing loads. In this case, shunt reactors are used to eliminate overvoltages caused by the Ferranti effect and to increase grid stability as well as its transmission capacity [8].

Utilization of reactive power compensation in both inductive and capacitive range

The fast controllable shunt reactor described above may be combined with capacitor banks thus providing the possibility to compensate both inductive and capacitive reactive power in the electrical grid. An example of such an arrangement rated at ±100 Mvar is shown as a single-line diagram in Figure 3.

Depending on the demands of every specific application, the capacitor banks may be placed directly at the same transformer like the shunt reactor or they may be distributed over grid nodes like in the Norte de Angola energy system [9]. Two shunt reactors, each rated by 60 Mvar and 15 capacitor banks with an overall power capability amounting to 150 Mvar, were installed there in 2009. Just after several months of the installation, it has prevented a grid crash which would have happened without those devices.

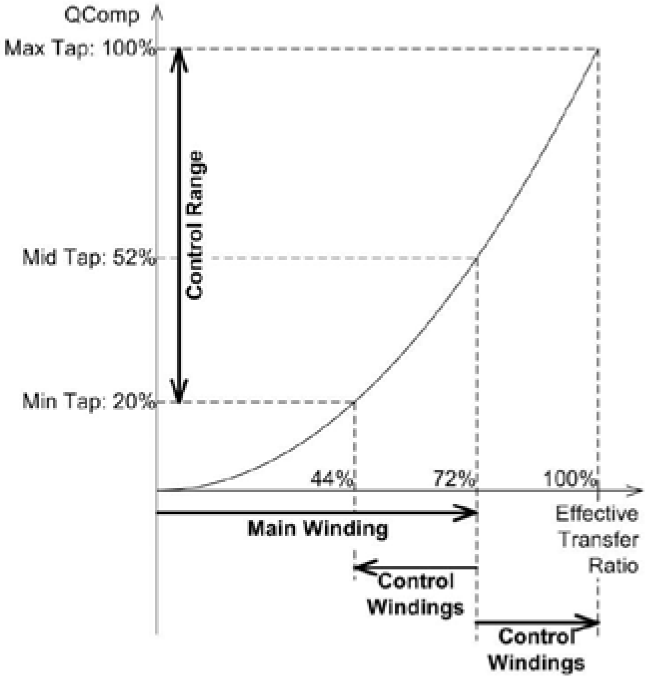

Figure 2: Control characteristics of windings

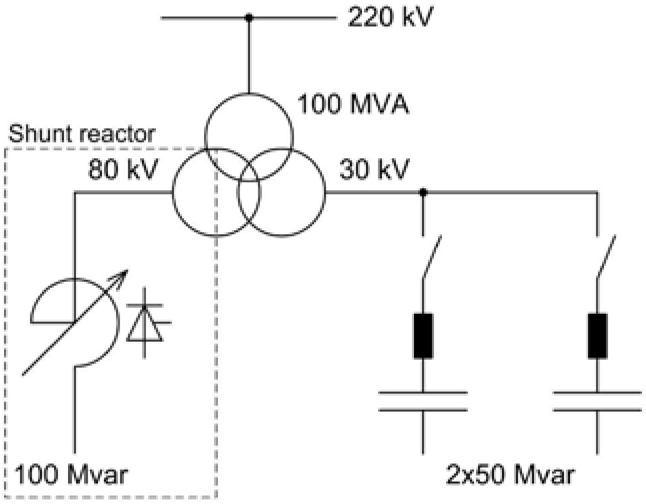

Figure 3: Single-line diagram of the full reactive power compensator

Implementation

At Maschinenfabrik Reinhausen GmbH, a laboratory model of the inductive part as well as a prototype of a solid state switch rated at 1 kA and 15 kV (1x-3x-9x winding segmentation) were designed and successfully tested.

Figures 4 and 5 show voltage and current diagrams while one of the control windings was switched from neutral to the same direction regarding to the main winding and then vice versa. In the first case,


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the voltage and current of the inductor were both increased thus increasing the reactive power consumed by the system. In the second case, the system was returned into the original state.

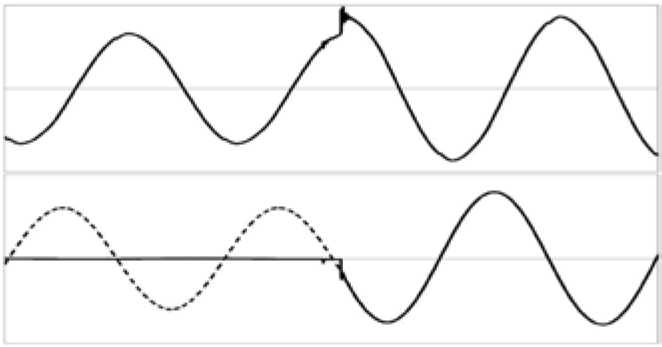

Figure 4: Switching a control winding from neutral to the same direction regarding to the main winding
Top: voltage across the inductor
Bottom: current in the inductor or in the main winding (dashed line) and in the control winding (solid line)

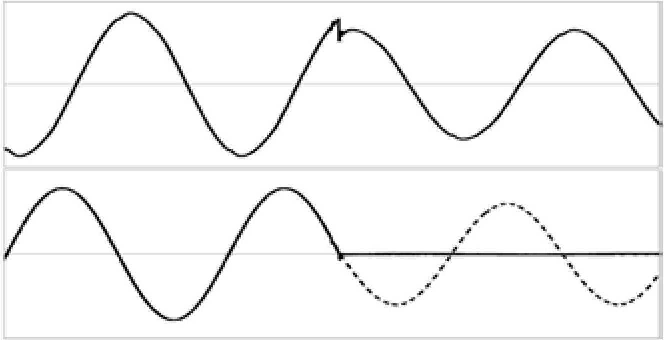

Figure 5: Switching a control winding from the same to neutral direction regarding to the main winding
Top: voltage across the inductor
Bottom: current in the inductor or in the main winding (dashed line) and in the control winding (solid line)

A prototype of the power electronic switch is shown in Figure 6.

Conclusions

Thyristor-based means of supporting electrical power grids are remaining advantageous for high-voltage lines and networks, especially if high reactive power capacity is required.

The new technical approach of reactive power compensation presented in this paper allows design of economical systems with nearly the same functional characteristics as broadly known SVC. Due to reduced costs, the range of reasonable applications of reactive power compensation devices may be enlarged. Cost-effective fast controllable shunt reactors allow operation of long power transmission lines with rapidly changing load conditions.

In this paper, functional characteristics of the new circuit topology for reactive power compensation were explained. Compared to SVC, it has many advantages that allow cost-effective compensation of reactive power in electrical power grids.

Figure 6: Power electronic switch for transformer control rated at 15MW, 1x-3x-9x winding segmentation topology

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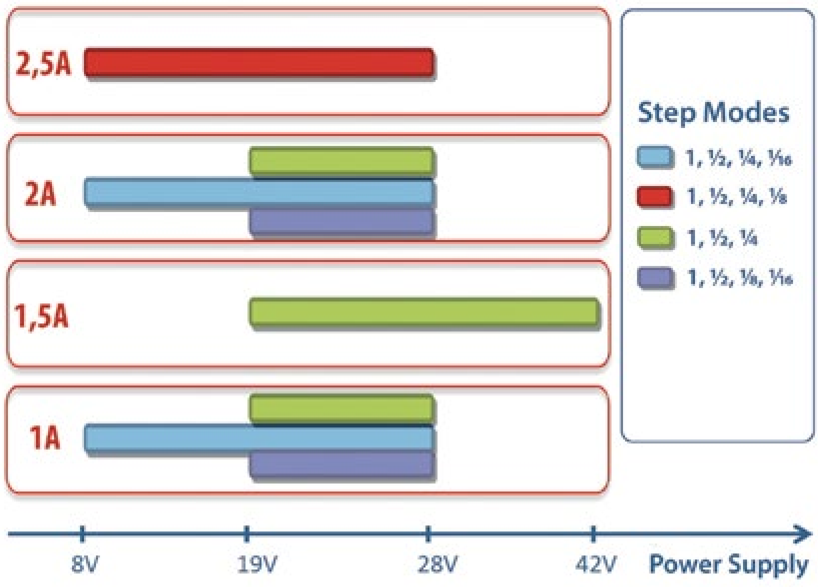

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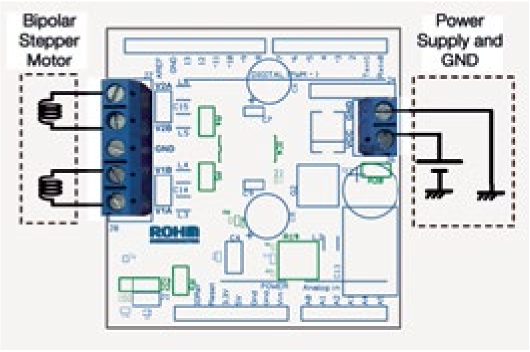

Soft-Short Protection, a Burning Issue in Mobile Travel Adapters

Most everyone, at one time or another, purchases a new smartphone or tablet charging cable from a discount store that was probably the cheapest cable available, with not even an afterthought about its quality. All cables are the same, right?
And, virtually guaranteed, not one person thought about the repercussions of using low-quality, low-cost cables, with their low cost connectors, for connecting the power adapter to their smartphone, tablet or Ultrabook™.

By Scott Brown Senior Director,
Marketing Power Conversion Business Group Dialog Semiconductor

The micro-USB connectors on our smartphones may become cluttered with dust or lint, potential hazards if not removed prior to connecting the power adapter. With the increasing amount of power running through these cables, connectors and sockets, these external factors can cause problems that previously were inconsequential. The advent of new charging protocols and connector types that call out high output power capability to rapidly charge a high capacity battery magnifies the need for new technology to be integrated into the power supply that can help better protect these electronic devices.

Just about every power supply designer has dealt with soft shorts at one time or another when bread-boarding a new design. This phenomenon now wreaks havoc in the mobile space. Soft shorts are shorts on the output of a power supply caused by a low resistance connection between the power lines and they occur in mobile applications more often than anyone would expect. A dirty charging port on a mobile device cluttered with dust or lint, low quality cables with low quality connectors, or simply forcing the wrong type of cable for the mobile device can cause soft-short conditions between the supply voltage pin and ground. These conditions leave small amounts of resistance, enough to draw current in excess of the normal operating output power range and enough that the output of the adapter will source a significant amount of power prior to entering over-current protection or over-temperature protection, whichever may come first. Figure 1 shows the end result of these faulty connections: burned or melted cables and damaged mobile devices, potential issues that are a major concern for the manufacturers of these devices.

Existing power supplies protect against over-current conditions primarily in one of two ways. The first over-current protection method entails current foldback and latching. Figure 2 shows the output characteristics of a foldback current limit circuit. The output of the adapter is in constant voltage mode up to point A on this graph. Once maximum output current is reached, the output enters constant current mode. The output voltage will reduce during constant current mode in order to match the current demand of the load, in this case the battery under charge. If the load attempts to draw an excessive amount of current, an over-current threshold will force the output into foldback mode. At point B, both the output voltage and current fold back, reducing the power loss in the converter and somewhat protecting the load. When the output voltage drops below a minimum voltage C, the output of the converter latches off to fully protect the output.

There are two main issues with this technique. The first and primary issue has to do with soft shorts. In a soft short, in constant current mode or where the foldback current limit threshold has been reached, but not enough to reduce the power dissipation to a reasonable level, a continuous amount of power can still cause damage since the cables and connectors are dissipating the majority of the power output of the adapter, generating dangerous levels of heat. The second issue occurs when there is a very low resistance short and the output latches off. In order to reset the charging, the adapter needs to be unplugged for a sufficient amount of time to allow the bulk capacitance to discharge and then plugged back in. If the user does not realize that the adapter needs to be reset this way, or does not wait long enough prior to plugging the adapter back in, it could be deemed faulty and the user might unnecessarily replace it.

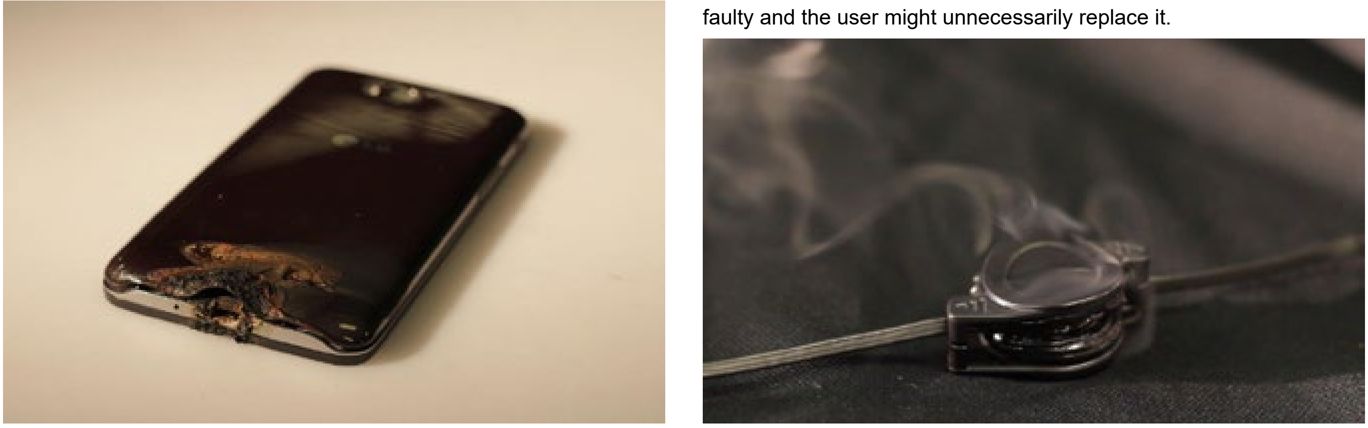

Figure 1: Examples of a damaged Smartphone (Left) and charging cable (Right)

The second method prevents the perception that the adapter is completely dead by cycling the power on and off when under a short condition. This cycling, typically called hiccup mode, has the benefit of allowing a temporary soft-short condition caused by a loose connection or from dirt in the connector to resolve itself and resume charging correctly. But, in the event that the short condition persists, repetitive bursts of high power into a short can stress the system to the point where melting or even burning of the plastic connector, cable or even the mobile device itself can occur.

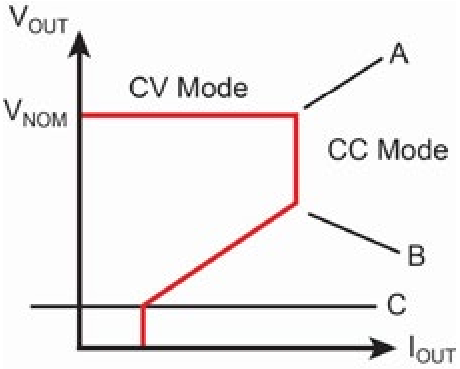

Figure 2: Foldback Current Limiting

The issue of damaged mobile devices is very real. To the point where the National Institute of Technology and Evaluation (NITE) in Japan, as well as other government consumer protection agencies, have issued warnings to consumers that recharging cables for smartphones can dangerously overheat.(1) These warnings resulted from high-profile incidents of damaged phones and cables due to exactly the soft-short issues mentioned above.

New technology to address this important safety issue must tackle the overheating problem, while keeping the adapter functional and avoiding the issue of perceived adapter failure. Ideally, a solution that allows for auto-retry of the adapter with significantly reduced power dissipation protects the system and at the same time, removes the possibility that the adapter goes to the trash because the consumer thinks it has failed.

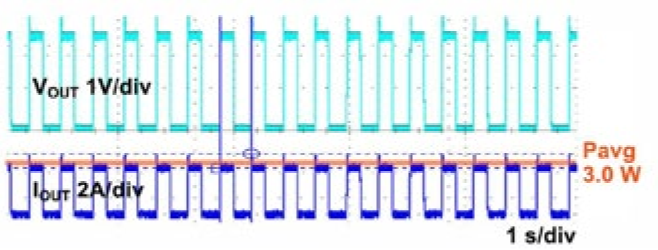

Figure 3: Standard Hiccup Mode Approach - High Average Power

SmartDefender™ advanced hiccup technology, developed by Dialog Semiconductor, builds on the conventional hiccup mode approach. In a conventional hiccup mode configuration, the amount of power provided to the load is set by the output voltage, current limit setting and the retry duty cycle. Most hiccup modes work at a standard 50% duty cycle with the off-time set internally within the controller (figure

3). During normal operation, a power supply dissipates very little power in the cables and connectors. Conventional hiccup modes using a 50% duty cycle dissipate the maximum output power of the adapter across the cable, connector and mobile device during the fault condition.

Using advanced digital control circuitry to modulate the power-on-reset (POR) duty cycle of the hiccup mode, SmartDefender technology significantly reduces the power dissipated in the system to the point where a soft short can safely exist without the risk of damage. Upon entering a soft-short condition, the output pulses the load for two POR cycles. If, after these initial pulses, the output current draw does not reset back down to normal operating conditions, the digital control algorithm changes the POR duty cycle to reduce the power dissipated in the system. Figure 4 shows the resulting waveforms of an example system using SmartDefender advanced hiccup technology. The smart hiccup retry duty cycle in this example is 25% (2/8), reducing the average power dissipation during the fault by up to 75%.

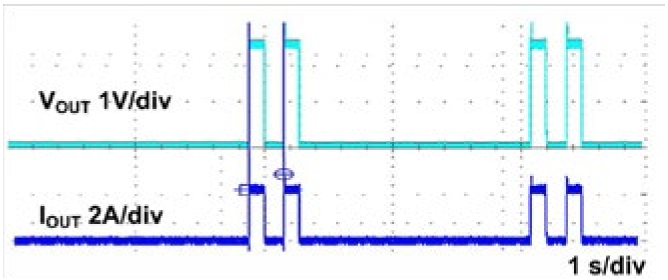

Figure 4: SmartDefender™ Advanced Hiccup Mode Technology Example Reduces Power Dissipation by up to 75%

The iW1782, a primary-side AC/DC controller IC, integrates SmartDefender technology to ensure safe and reliable operation under soft short fault conditions. The iW1782 works with the iW636 secondary-side controller to create a RapidCharge™ solution for both Qualcomm® Quick Charge™ 2.0 and 3.0 Technologies. SmartDefender technology in the iW1782 controller sends out the PWM switching pulses in two POR cycles then blocks them in the next six cycles. This increases the shutdown interval every two cycles and reduces the average power delivered to a short circuit by up to 75% without latching off.

When a soft short occurs in a cable, the most common failure mode is a short between the VBUS power line and ground. But, at times the short can pull either the D+ or D- data lines in the USB cable or connector up to VBUS. This could damage the USB controller D+/D- pins in the mobile device. The iW636 provides protection on the D+ and D- pins so that in the event of a soft-short condition the D+ and D- pins are protected from a possible overvoltage condition. The iW636 can detect this fault and send a signal back to the primary side controller, the iW1782, so that the charging circuit can be disabled, protecting the USB data lines. This double layer protection of SmartDefender and D+/D- protection provides a mobile charging solution safeguarding the entire charging system, both power and data.

Mobile devices such as smartphones, tablets and Ultrabooks are expensive and indispensable tools for our day-to-day lives. Protecting these devices now goes beyond dealing with basic faults. Integrating advanced technologies to detect and protect against less common, yet equally important faults has become a necessity. Advanced hiccup technology such as SmartDefender enables safer and more reliable power adapter solutions to power and protect our mobile devices.

http://www.pcworld.com/article/2603260/smartphone-chargers-and-cables-seen-as-fire-risk-in-japan.html

http://www.dialog-semiconductor.com/

Improving Thermal Performance with Chip-Scale Packaged Gallium Nitride Transistors

With power converters demanding higher power density, transistors must be accommodated in an ever decreasing board space. Beyond gallium nitride based power transistors' ability to improve electrical efficiency, they must also be more thermally efficient. In this article we will evaluate the thermal performance of chip-scale packaged enhancement-mode GaN field effect transistors (eGaN® FETs) and compare their in-circuit electrical and thermal performance with state-of-art silicon (Si) MOSFETs.

By David Reusch, Ph.D., Executive Director of Applications Engineering and Alex Lidow, Ph.D., CEO and Co-founder, Efficient Power Conversion Corporation

Improving Thermal Performance

The main source of heat in a power converter generally originates from the losses inside the power transistor. Therefore, improving thermal efficiency of the power device package is a natural starting point to improving system thermal performance. The thermal efficiency of a package can be determined by comparing two parameters, $R_{\Theta JC}$ and $R_{\Theta JB}$, normalized to the package area. $R_{\Theta JC}$ is the thermal resistance from junction-to-case; this is the thermal resistance from the active part of the eGaN FET to the top of the silicon substrate, including the sidewalls. $R_{\Theta JB}$ is the thermal resistance from junction-to-board; this is the thermal resistance from the active part of the eGaN FET to the printed circuit board (PCB).

The junction-to-board resistance ($R_{\Theta JB}$) of eGaN FET chip-scale packaged transistors and Si MOSFET packages generally fall on a single trend line indicating that performance for this element of thermal resistance is determined primarily by package size, and not technology [1], [2]. In contrast, figure 1 shows a plot of the thermal resistance from junction to case ($R_{\Theta JC}$) for chip-scale packaged eGaN FETs [3], [4], represented by blue square dots, and state-of-the-art double sided cooling Si MOSFET packages [5]-[7], represented by red circular dots. Even the most advanced double-sided cooling Si MOSFET packages are far less efficient at extracting the heat out of the top of the package than the chip-scale packaged eGaN FETs. This makes chip-scale packaging the most efficient thermal package for double sided cooling and most suitable for high density power designs.

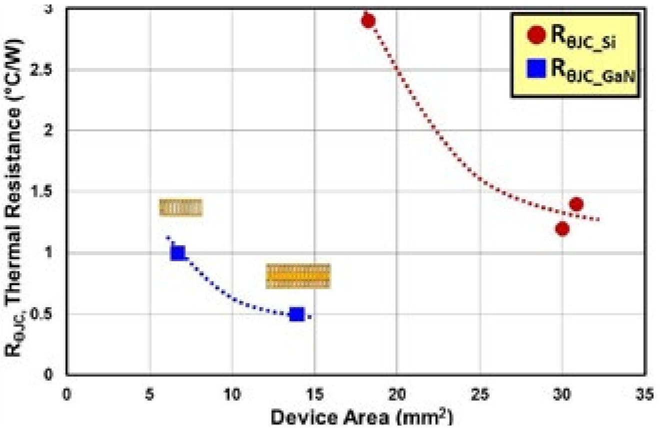

Figure 1: $R_{\Theta JC}$ (Junction-to-Case Thermal Resistance) for several package styles [3]-[7], eGaN FETs represented by blue square dots and Si MOSFETs represented by red circular dots

Improving Electrical Performance

The most straightforward way to improve thermal performance is to improve electrical performance, reducing power loss and therefore reducing the amount of generated heat that must be extracted. As discussed in [8], eGaN FETs have universally lower figures of merit and superior electrical packaging, resulting in improved electrical performance.

To compare the overall performance of eGaN FETs and state-of-the-art Si MOSFETs, three identical 48 V_{IN} buck converter evaluation boards were designed, shown in figure 2. All of the boards were 2x2 inches and had active copper areas of one (1) in^2 (645 mm^2), outlined by the white border in the figure. The boards, designed on the same PCB panel to be consistent, had four layers of two-ounce (2.8 mils/71 µm) copper and used an optimized layout as discussed in [8].

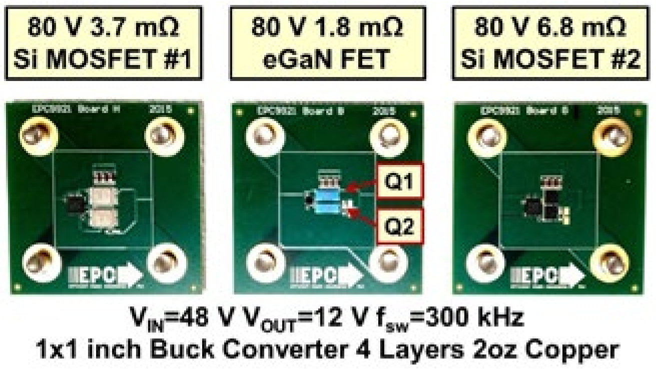

Figure 2: eGaN FET and Si MOSFET thermal evaluation boards

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The 80 V Si MOSFETs used for comparison have advanced double-sided cooling packaging (Infineon BSB044N08NN3), shown on the left in figure 2, and the more traditional S3O8 packaging (Alpha and Omega Semiconductor AON7280), shown on the right in figure 2. For both Si MOSFETs, the lowest commercially available FOM devices for their respective package technologies were selected. A state-of-the-art MOSFET driver (Intersil ISL2111) was used for the MOSFET-based designs and the gate voltage for the Si MOSFETs was 10 V.

For the eGaN FET based design, shown in the center of figure 2, two 80 V Land Grid Array (LGA) chip-scale packaged EPC2021 were used with the Texas Instruments LM5113 driver and the gate voltage for the eGaN FETs was 5 V. The eGaN FET based design takes up less than half the active board area of the Si MOSFET based designs. The first reason for the improved power density of the eGaN FET-based design is that the power device is much smaller in size, when compared to the MOSFET in terms of $R_{DS(ON)}$ times the area. The second improvement in density is driven by the gate driver, which is also much smaller than its counterpart, in part from better packaging and in part from the reduced drive requirements of low charge, low drive voltage for eGaN FETs.

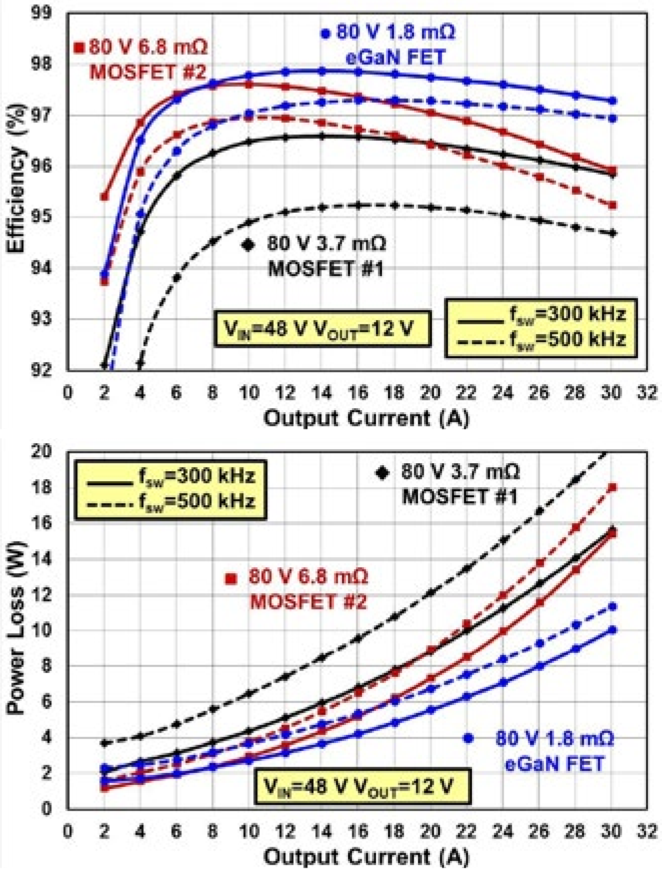


Figure 3: Experimental electrical comparison between GaN and Si based buck converters (a) efficiency (b) power loss, V_{IN}=48 V to V_{OUT}=12 V, f_{sw}=300 kHz and f_{sw}=500 kHz (L=4.7 µH Coilcraft SER2915L)

The total system efficiency and power loss comparisons of the eGaN FET and silicon MOSFET based 48 V_{IN} to 12 V_{OUT} buck converters operated at switching frequencies of 300 kHz and 500 kHz are shown in figure 3. These plots take into account losses for the entire system, including the inductor, capacitors, and PCB losses.

The eGaN FET based design offers similar light load efficiency with the Si MOSFET #2 based design, which has an almost 4x higher on-resistance, demonstrating the effect of the low charge of eGaN FETs. At full load, the low eGaN FET on-resistance enables higher efficiency. Combining low conduction losses and low switching losses, the eGaN FET based design has higher efficiency at almost every design point.

When comparing the eGaN FET and larger Si MOSFET #1 based design, the performance is improved under all conditions.
For the larger, slower switching Si MOSFET the higher switching losses become the major loss mechanism. At a switching frequency of 300 kHz and a load current of 30 A, the eGaN FET based design reduced the total system loss by 35% over both Si MOSFET based designs. At 500 kHz, the eGaN FET based design, with low switching charges, low on-resistance, and improved packaging, had a minimal drop in efficiency when compared to the Si MOSFET based designs. Furthermore, at 30 A, the total system loss is reduced by almost 40% when compared to the best Si MOSFET based solution.

Improving System Performance
In figure 4, the thermal performance of chip-scale packaged eGaN FET and Si MOSFET based designs are compared. For this work, the selected maximum temperature point for this evaluation was well below the 150°C maximum junction temperature of power devices. A 100°C maximum temperature was selected to provide margin for higher ambient temperatures and provide device de-rating, which is a common design practice.

At 14 A of output current, the Si MOSFET #1 based design, shown on the left of figure 4, reaches 100°C with an airflow of 200 LFM. The Si MOSFET generates higher power loss from lower electrical efficiency and the package is also less thermally efficient than the chip-scale packaged eGaN FET, shown in the center of figure 4. For the same maximum temperature, the eGaN FET based design is operated to 22 A, where the maximum device temperature matches that of the advanced double-sided cooling packaged Si MOSFET #1 on the top device (Q1). The eGaN FET based solution can achieve almost 60% more output power while maintaining the same maximum junction temperature and occupying significantly less board space.

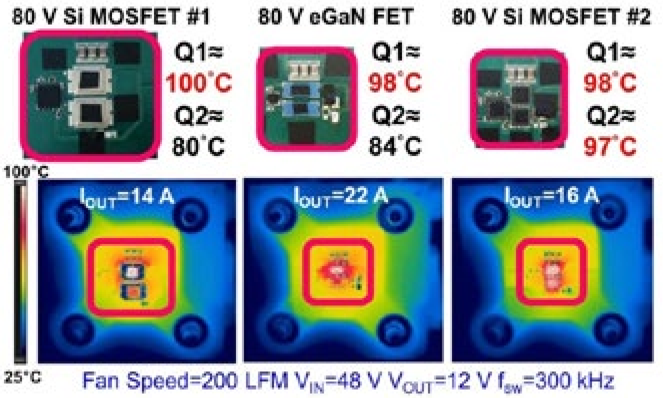


Figure 4: Experimental thermal comparison between chip-scale packaged eGaN FET (center), double-sided cooling packaged Si MOSFET #1(left), and S3O8 packaged Si MOSFET #2 (right) based buck converters without heat sinking, V_{IN}=48 V to V_{OUT}=12 V, f_{sw}=300 kHz, air-flow=200 LFM, ambient temperature=25°C with same approximate maximum device temperature

At 16 A of output current, the S308 packaged MOSFET #2 design, shown on the right of figure 4, approaches 100°C with an airflow of 200 LFM. For the same maximum temperature, the eGaN FET based design is operated to 22 A, where the maximum device temperature matches that of the S308 packaged Si MOSFET #2 on the top device (Q1), while the low side (Q2) eGaN FET runs 13°C cooler. The eGaN FET based solution can push almost 40% more output power while maintaining the same maximum case temperature.

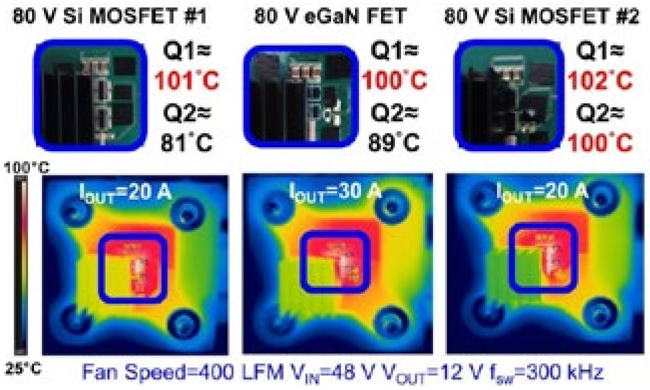
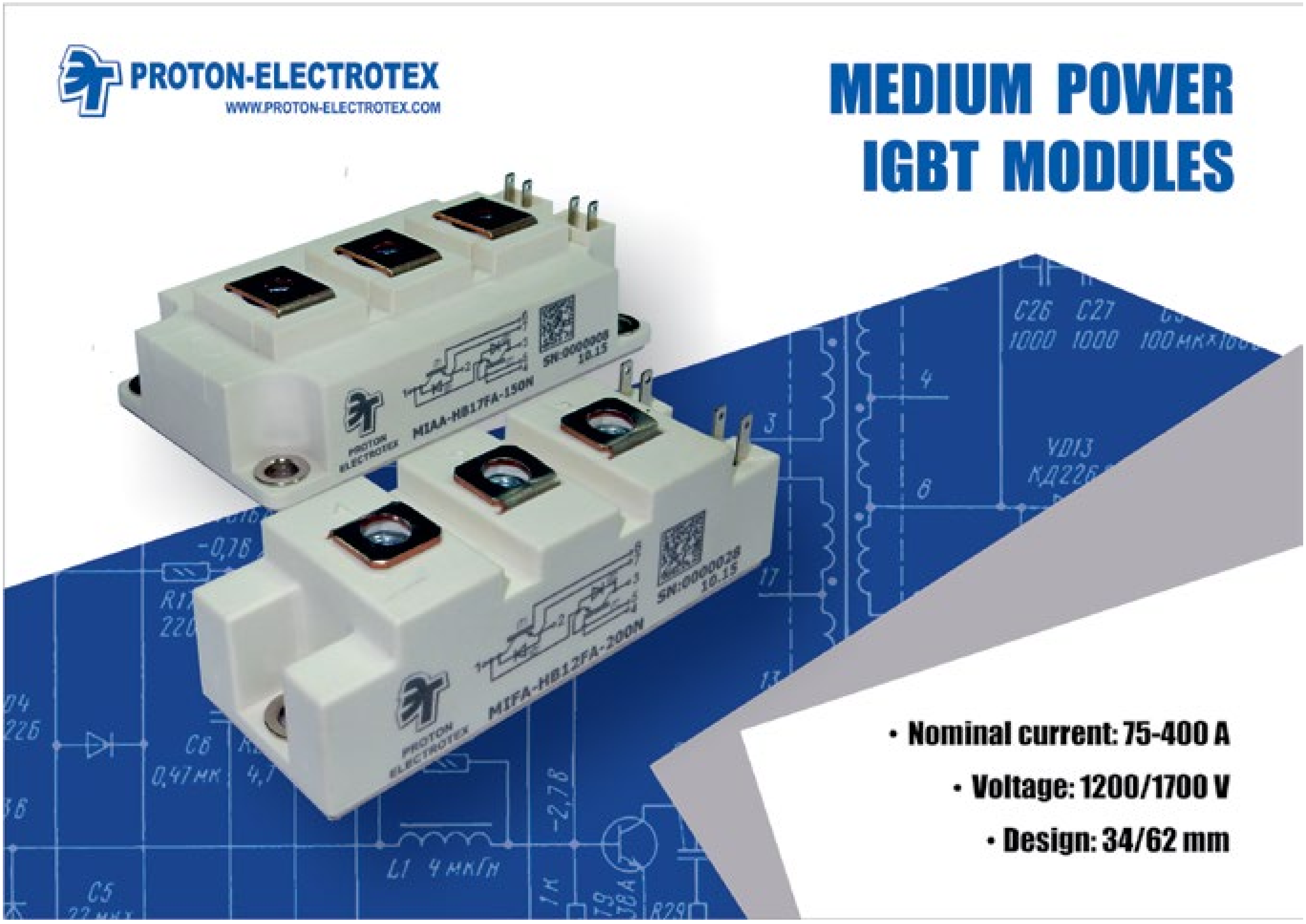


Figure 5: Experimental thermal comparison between chip-scale packaged eGaN FET (center), double-sided cooling packaged Si MOSFET #1(left), and S3O8 packaged Si MOSFET #2 (right) based buck converters with heat sinking, V_{IN}=48 V to V_{OUT}=12 V, f_{sw}=300 kHz, air-flow=400 LFM, ambient temperature=25°C with same approximate maximum device temperature

To compare the thermal performance of eGaN FETs and Si MOSFETs capable of utilizing double-sided cooling by adding heat sinking, test cases with heat sinks were also evaluated. The heat sink and attachment methods were kept consistent between designs and followed the attachment process outlined in [1] and [2].

For the thermal evaluation with heat sinking, the chip-scale packaged eGaN FET based design, shown in the center in figure 5, reaches 100°C at an output current of 30 A with an airflow of 400 LFM. Both Si MOSFET based designs, with the double-sided cooling and conventionally packaged Si MOSFET based designs shown on the left and right of figure 5, respectively, reach 100°C at 20 A output current and 400 LFM airflow. The eGaN FET based solution achieves 50% higher overall output power, despite occupying a much smaller board space, while maintaining the same maximum case temperature. The eGaN FET shows much better junction-to-case cooling than the conventionally packaged Si MOSFET. The double-sided cooling packaged Si MOSFET occupies around three times the board area of the much smaller eGaN FET and the junction-to-case cooling improvements are similar for both designs. The eGaN FET, which is a much smaller device, has larger thermal impedance introduced by the thermal interface used to attach the heat sink. This is due to the much higher transistor density and smaller surface area to connect the heat sink.

The equivalent junction-to-ambient system thermal impedances, shown in figure 6, were calculated for the eGaN FET and Si MOSFET based designs at various airflows for the design cases with and without heat sinking. The eGaN FET based design, occupying the small-



est active area, provides the best overall thermal performance. This demonstrates the chip-scale packaged eGaN FETs superior thermal efficiency when compared to even the most advanced Si MOSFET packaging methods.

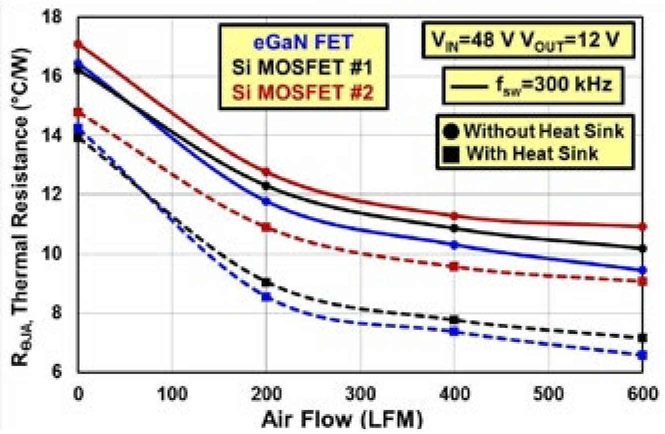


Figure 6: Comparison of junction-to-ambient system thermal impedance vs. airflow for eGaN FET and Si MOSFET based buck converters with an input voltage of 48 V, output voltage of 12 V, and switching frequency of 300 kHz

When the superior thermal performance is combined with the improved electrical performance, eGaN FETs can enable improved overall system performance, in a fraction of the occupied board space. This is a combination for game changing performance improvements.

Summary

In this work, the thermal performance of chip-scale packaged GaN transistors was evaluated. For high voltage lateral GaN transistors, all of the electrical connections are located on the same side of the die, allowing for the elimination of complex, performance limiting two sided packaging common in vertical Si power MOSFETs. Chip-scale packaging is a more efficient form of packaging that reduces the resistance, inductance, size, thermal impedance, and cost of power transistors, enabling unmatched in-circuit performance.

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104M
1KV
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50V
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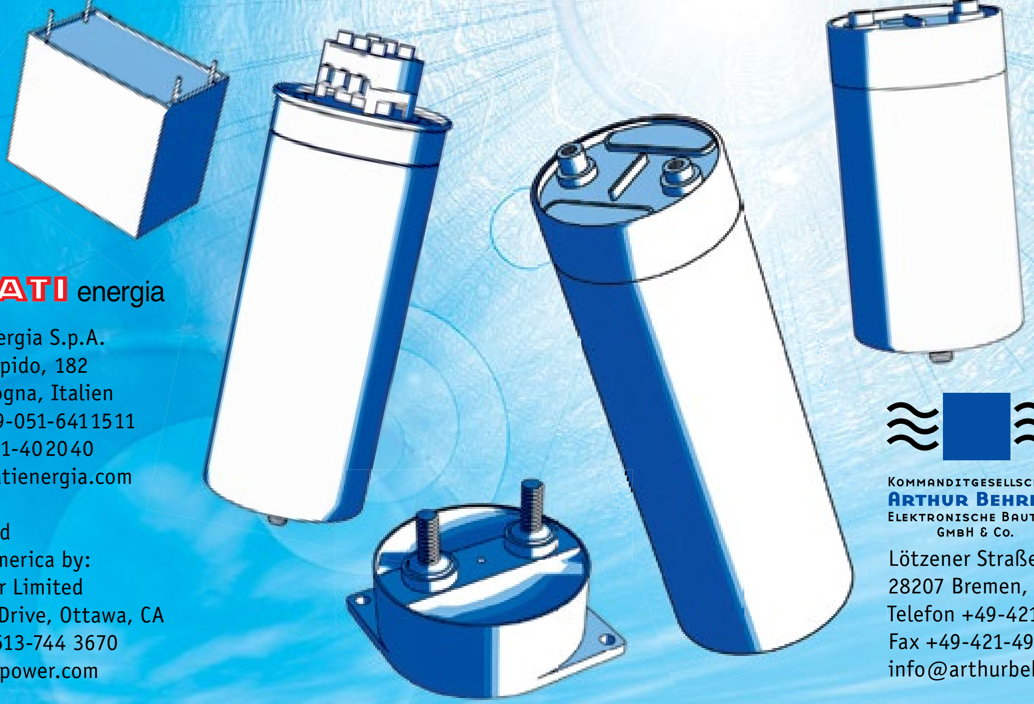

Design Methodology for First Pass Success

A rationale for hardware simulation

Market dynamics and competition demand timely new products. This increases the pressure to speed-up product development. In this article, I recount my experience and the role of simulation to reduce and even eliminate design iterations to minimize development time.

By Mike Walters, Walters Power Electronics, LLC

Technological change is occurring at ever-faster rates. Just think about how much things have changed in the past 10 years - computing speed, electronic navigation, the internet of things, and self-driving cars. Technology has replaced old business with new business – digital cameras displaced film cameras and now your cell phone includes an integrated camera.

Also, consider the increasing rate of change of technology as illustrated by the adoption of the cell phone, which was 7 times faster than the landline phone. Engineers made all of this change possible by being at the forefront of the technological revolution. This rate of technological change is challenging engineers to speed up their new product development cycle.

The design methodology presented here promotes the virtues of power system modeling and simulation. Specifically, this design methodology reduces the number of design iterations for integrated circuit (IC) design and development, and is broadly applicable to all power electronic design. I detail my experience with fast time-to-market IC development and contrast the approach with other techniques intended to reduce the product development time.

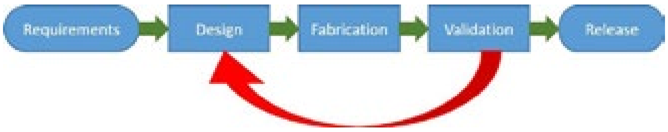

Figure 1: Product development process

Figure 1 illustrates the steps of the product development process. The development starts with the new product requirements as an input to the design phase. Fabrication builds the product from the design, followed by validation that the product meets the requirements. If during the validation step the product does not meet the requirements, the design must be revisited (red arrow). The steps of design, fabrication, and validation, commonly known as the development cycle, repeat until the product successfully meets the requirements for release to production.

There is an ever-increasing need to speed up new product development. The market and competition pressure companies to reduce the time-to-market for their products. Development organizations scrutinize each of the development steps (design, fabrication, and validation) in an effort to hasten product release and this may lead to adopting short cuts. Many of us have witnessed cases where such short cuts lead to the product failing one or more of the validation tests. Of course, the development time increases because of the effort needed to correct the issue, refabricate the product, and repeat validation.

One way to speed up a new product development is to reduce the number of development cycle iterations. Rather than focusing on each development step (design, fabrication, and validation), let us consider how to validate the product with the first design effort. I assert that better understanding of the design reduces the number of iterations. Simulating the design adds to an engineer’s knowledge and leads to a better understanding of the product.

I have witnessed companies actively discourage any activity that increases the design time. Under the mantra of failing fast, they would rather quickly get the product fabricated, find issues through testing physical hardware, correct the design and refabricate the product. With this approach, the responsible engineer finds and resolves issues and learns more about the design. However, by the time the development has advanced to hardware, there are a number of constraints on solving any issues. It is more expensive to change the form factor or add components at this phase of development compared with exposing and mitigating issues during the design phase. Simulating the design to expose issues allows less costly resolution during the design phase and minimizes development cycle iterations.

Some believe it is counter intuitive to increase the design time with a simulation task. After all simulation can be intimidating. Some simulation tools have a steep learning curve requiring the engineer to expend effort understanding the tool’s operations and procedures. Unsuccessful simulations may report cryptic error messages or just simply fail to complete. Engineers would rightfully prefer to expend their effort on their assigned project and not on the simulation tool. In addition to learning a simulation package, a successful simulation also requires engineers to expend effort on a model. Constructing the model may be intimidating. However, model building directly increases an engineer’s understanding of the design. I would argue that this is a worthwhile investment. Later in this article, I describe my process of model development.

Failing fast takes too long

Simulation during the design phase shortens the end-to-end development time even though it lengthens the design time. Figure 2 illustrates the design cycle as a time line for both methodologies. The fail fast approach quickly fabricates the product by minimizing the design time and identifies the issues during validation testing. Comparatively the design interval of the simulation approach is longer.

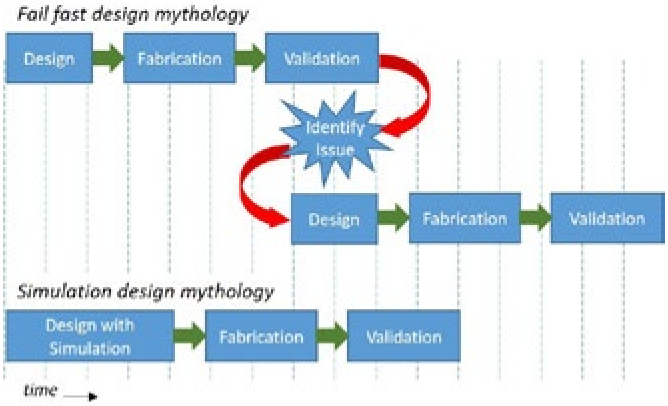

Figure 2: Product development time line

Consider the time required to fabricate and validate the product. If we gain confidence (with simulation) that the product will pass validation the first time, then we avoid the time repeating the fabrication and verification phases. The total end-to-end development time is shorter than the methodology with multiple design iterations. The justification for simulation in terms of development time is a simple inequality. A simulation effort that is less than the fabrication and validation efforts will be a faster development time. The premise is that better understanding of the product design reduces the number of development cycle iterations.

$$T_{Simulation} < T_{Fabrication} + T_{Validation}$$

Simulation reduces development cycle iterations

In my experience, a design methodology that includes a simulation task does indeed reduce the number of design iterations. The development of ICs and solutions to power Intel's CPU provides a good example. As background, Intel would issue a power requirements specification and a release schedule for their next generation CPU to multiple IC vendors. This was essentially a race for the IC vendors.

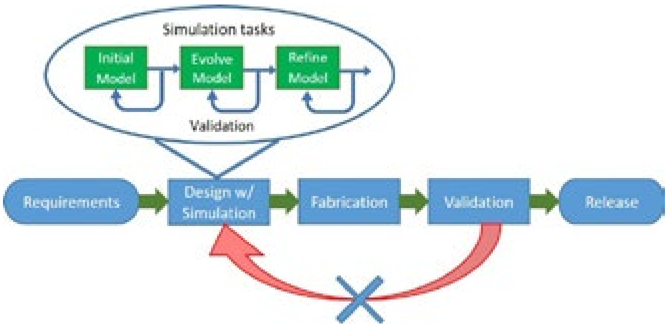

Figure 3: First pass development process

The first vendor to sample their IC and power solution to customers would be in the best position to win the business. I used simulation in my role for one of the IC vendors to design the power solution and define the control IC. I am proud that the market rewarded us with a majority share for multiple generations of Intel CPUs. Over the course of several generations, we were able to sample our IC and power solution on the first pass. There are multiple factors for this success, including a great team, but limiting the number of design iterations with simulation and being fast to sample our solution was key.

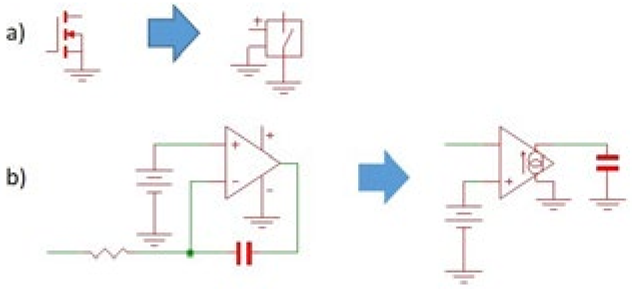

Figure 4: Initial simulation uses ideal models

Let me contrast this design mythology, which includes a simulation task with the fail fast approach. The fail fast approach by definition means the total development time needs at least two fabrication and two validation intervals. IC fabrication time takes several weeks and more typically, 8 to 10 weeks to process the initial wafer, cut into die and package the IC in a chip carrier. The fabrication of a power solution as reference design is concurrent with the IC fabrication and takes a few weeks (depending upon the complexity) to fabricate the printed circuit board (PCB) and populate all of the components.

Validation of the initial design also takes several weeks depending again on the complexity and the required compliance testing. Clearly expending a couple of extra weeks of effort to model and simulate the design with the goal to reduce the number of design iterations yields a faster development time. Failing validation extends the end-to-end development time by over 2 weeks: to correct the issue, refabricate the IC and repeat revalidation testing.

Another example of a first pass success also used the simulation methodology. The company's objective was to reduce the cost of a LED bulb and my approach was to develop a new control IC along with some minor power driver modifications. A short development time was necessary to improve the corporate margins. My role was to define the IC and work with an IC vendor on the design and development. The project challenges included a new IC architecture and a remotely located IC vendor. The simulation effort helped overcome these challenges and resulted in a functional IC on the first pass that enabled us to start validation. The design team found a minor ESD issue on one of the pins of the initial IC, but the issue quickly corrected and allowed us to meet the initial schedule. There were many factors to this first pass success, but the simulation model was one of the key factors.

A template for simulation

Figure 3 details the simulation tasks within the product development process. A successful simulation strategy builds a model of the relevant parameters. Clearly define your modeling objectives to avoid unnecessary complexity. Start with a simple initial model, and run a quick simulation. If the results meet your expectations, continue incrementally building the model. Simulation allows you can quickly expose and mitigate any issues without the constraints imposed by the hardware.

It is difficult for me to separate the design and simulation activities. The design parameter calculations are concurrent with the placement of components into the schematic of the simulation tool. Below I describe the modeling and simulation steps using the LED bulb development as an example. The steps include an initial model, a definition model, and a development model.

The initial simulation uses simple and idealized models. For example, a voltage controlled switch represents the main switching MOSFET (Figure 4a) and a voltage controlled current source with a capacitor represent the error amplifier (Figure 4b). Keeping the initial model simple speeds up the simulation and is easier to troubleshoot. I use this initial model to develop the control algorithm. For a new control algorithm, it is best to start with a simple analog behavioral model and add digital elements as the model evolves. After successful validation, additional parameters add to or replace the ideal functions of the initial model.

The definition model development identifies the functions for integration and adds bandwidth, offset, time delays, and common mode signal limits. I use parametric simulation to help establish the limits in the IC specification. Further parametric variations of the definition model document the impact of external component tolerances and variations on system requirements.

I share the simulation results, which include start-up, and transient disturbances with the IC design team. The simulation model and results supplement the IC specification. The simulation provides an excellent communication medium for the expected system performance over the operating range, compared with the static limits shown in the specification.

The model continues to evolve during the IC development. The simulation results help communicate some of the design nuances with the vendor's IC designers. The IC development model supports the trade-offs and design decisions that typically involve the reuse of IC functions. As the design evolved, the IC development model is revised with parameters and characteristics of the functions selected for the final design.

My simulation tool of choice is SIMPLIS and its features documented in the reference. I like SIMPLIS because it is easy to use, specifically designed for power electronics, and it does not have convergence issues. SIMPLIS helps me focus on the product design. It is intuitive with minimal learning to get started and yet supports advanced functionality for more complex modeling needs. During the LED bulb development, I evaluated phase dimming by adding a TRIAC dimmer model in series with the AC source of the definition model of the LED driver. I also evaluated conducted EMI by adding a LISN model in front of the definition model with good results. Both of these simulations required exercising the model for over 500 ms of run time while switching at frequencies just below 100 kHz and SIMPLIS completed each task in less than 3 minutes.

I have also found the simulation model helpful for issues that are difficult to solve with hardware alone. Some nodes are hard to monitor in hardware, which complicates troubleshooting. With simulation, you can easily probe these nodes while comparing with signals easily observed on the hardware. In addition, simulation can help you evaluate tolerances and parametric shifts of components, which can help improve the manufacturing yield of high volume designs (where you are likely to have components from the entire distribution curve).

Admittedly, developing valid models requires time and effort, but you can reuse the verified models in future designs. Always weigh the simulation effort against simply testing the hardware. For example, the model of the TRIAC dimmer referenced above was only valid for a single dimmer. Developing and verifying a model for each of dimmers offered on the market would be a huge task. Instead, we elected to validate the LED bulb hardware with a representative sample of dimmers. I used the single TRIAC dimmer model to validate the dimming algorithms incorporated in the IC.

I have been fortunate to be part of some great development teams that have achieved first pass design success. The design methodology used in all of the first pass successes benefited from the knowledge gained by simulation. I encourage all engineers to simulate their designs.

The time to develop products is bound to get faster in the years ahead. If we recognize that successful validation of the product is the result of engineer’s knowledge of the design, the product development team should invest in the design interval with the goal to validate the product the first time. My experience has shown that modeling and simulating the design is the best method to acquire the knowledge to achieve a first pass success.

http://www.simplistechnologies.com

Mike Walters has over 35 years of power electronic design experience in the fields of LED lighting, computer power, and military aerospace. He has filed over 60 US patents with Cree, Intersil, International Rectifier, IBM, & GE. Mike is currently the proprietor of Walters Power Electronics, LLC specializing in power supply system architecture, system & product simulation, competitive analysis, integrated circuit definition as well as analog/digital control & circuit design.

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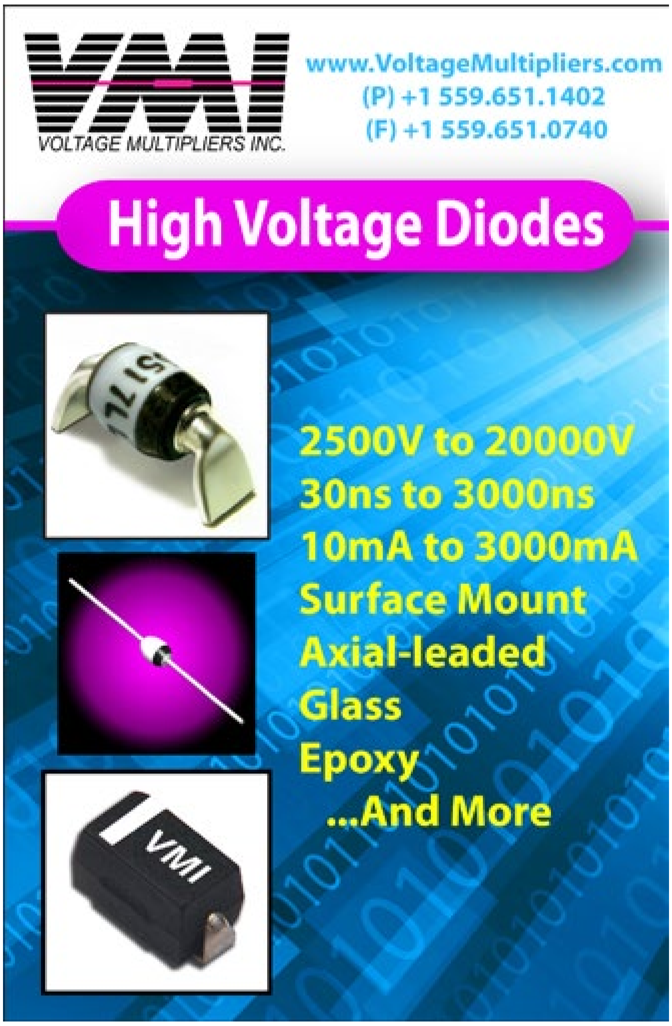

Towards Better Power Electronics Prototyping?

When it comes to power electronics prototyping, everyone has their own practices involving their preferred power and control hardware. However, does anyone really know what the hidden costs are behind such prototyping hardware? And what the alternatives are?

By Dr. Simon Delalay, Matthias Lambert, Dr. Nicolas Cherix – imperix Ltd. Switzerland

In a growing market of modern power electronics, targeting applications of increasing complexity (such as multilevel inverters), the engineering teams responsible for the control development and testing must cope with tasks of increasing complexity. This is however difficult to combine with an expected reduction of the overall development time and costs.

In particular, prototyping activities are not only often time-intensive, but also require dedicated hardware and software, which are linked to high internal maintenance costs. On the other hand, these activities are generally indispensable to completely assess the industrialization potential of a future product or idea. Indeed, general-purpose simulation tools are often unable to completely highlight all the typical real-world challenges related sampling, synchronization, limited measurement accuracy, noise, etc.

When building prototypes, three approaches are widely used: either relying on some self-made prototyping hardware, relying on commercial development kits or finally re-using hardware from existing product lines. Independently from the pros and cons of each approaches (see our observations in table 1), we noticed that all three imply much underestimated and constant development efforts and costs. One typical example of hidden costs are the efforts required to keep hardware, software, internal documentation and team knowledge up-to-date. This is especially true for the users of development kits, who are often deemed to focus on low-level programming rather than on their real work: the control of power electronics.

	Custom designs	**RCP systems**	**Boom-Box**
Necessary engineering skills	very high	low	low
Software maintenance costs	very high	medium	low
Recurrent development costs (e.g. interface circuits)	n.a.	fair to high	low
Costs of the development tools (hardware + software)	low	fair to high	fair
Modularity & versatility	poor	fair	excellent
Time to operation	very long	short	very short

Table 1: Comparison of the observed costs in a typical research and development environment

More generally, performing power electronics prototyping with untailored hardware leads to longer engineering times, for example to continuously adapt it to new converter setups: designing new analog interfaces, expanding I/O capabilities, designing software/hardware safeties, converting/optimizing the firmware, etc. If improving the traditionally low reusability of such prototyping hardware is a must, it is often incompatible with the time and cost constraints imposed to academic and industrial R&D teams.

A NEW PROTOTYPING APPROACH

Recently, imperix Ltd. released its BoomBox RCP platform in order to provide R&D engineers with a truly tailored tool for the development of power electronic converters and systems. The BoomBox controller provides a new experience of prototyping, by allowing the engineers to jump straight from the simulation to a real hardware implementation thanks to its software-independent protections. These react on overvalues within a few micro seconds and immediately block the entire application. With this safety layer enabled, R&D engineers can instantly try and implement new control schemes on hardware, without the risk of damaging it, thus shortening the total development time and efforts.

Figure 2: The BoomBox RCP platform

The BoomBox RCP is built around a powerful and versatile DSP+FPGA combination, providing the user with a powerful processor, as well as peripherals tailored for power electronics prototyping, developed and thoroughly tested at imperix during the previous years. Compared to traditional approaches, there is no longer a need to optimize software or to dig into tons of documentation to get a converter prototype running.

Several BoomBoxes can also be tied together to easily expand the number of I/Os for the most ambitious implementations. This makes it a modular and I/O intensive control platform, addressing all innovative modular setups such as MMC, CHB, … Even in such complex converters, all time delays between data sampling and modulation are continuously mastered, even in the case of particular modulation patterns or interleaved operations.

Unlike development kits, the BoomBox RCP embeds a custom operating system that provides a convenient access to power electronic function libraries, whilst guaranteeing at any time the critical real-time operation of the user code. Those functions (modulation, acquisition, controllers, etc.) are either accessible through efficient C/C++ programming, or through automated code generation from several well-known simulation software. A growing library of application examples and tutorials that rely on such libraries can be freely accessed online.

SPEEDING UP PROTOTYPING

Building a converter and turning it into a working prototype is one great step. The (potentially huge) remaining work is all about getting results out of this, which can be a burdensome task. For this particular need, BoomBox Control is shipped with the control platform. This user-friendly GUI facilitates debugging and helps with obtaining results during development. All variables can be monitored and altered while the code is running and can also be sent to the analog outputs to be viewed live on an oscilloscope. A data logging module provides a visual interface, where data can be exported directly to MATLAB or Excel. Additionally, validating the control loops and algorithms could not be easier with the provided transient generator.

Figure 3: Modular multilevel converter prototype

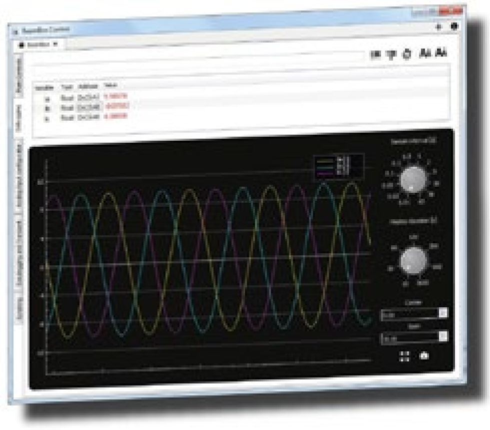

Figure 4: Retrieving experimental results through BoomBox Control GUI

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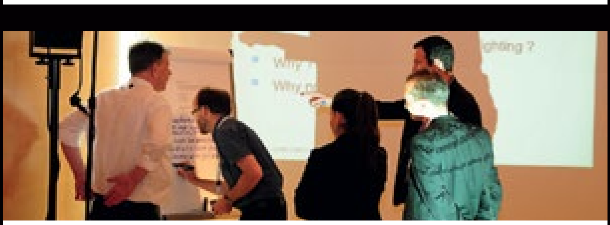

Interactive Workshops & Forums

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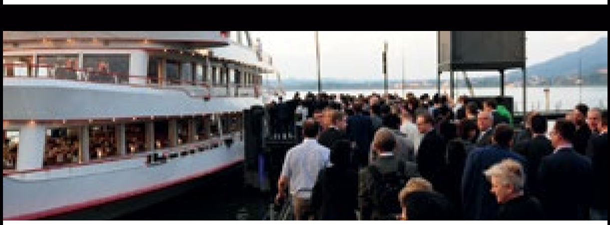
- Design-meets-Technology Forum by APIL
- Horticultural Lighting Workshop by EPIC
- Int'l lighting and photonics cluster forums

Innovation Platforms

- Technical innovations presented by start-up innovators
- Light-Art-Designs by lighting designers and students
- Product launches presented by industry leaders



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The hardware interfaces are tailored for power electronics whilst also remaining open and flexible: semiconductor switches are controlled using standard fiber optics, while inputs provide configurable and highly EMI-immune differential connections for analog measurements. Interfacing the BoomBox RCP to any custom or industrial power stage or sensor solution is completely supported. Nevertheless, for use in situations where a complete package is needed with a tight schedule, imperix provides some accessories which ideally complement the BoomBox philosophy and enable the user to get a power conversion setup running in no time.

Figure 5: Ready-to-use power modules and sensors

Figure 6: Industrial controller ‘BoomBox Embedded’

For example, some rack-mountable power modules are available. Those are embedding half-bridge or full-bridge IGBTs, gating circuits, sensors and capacitor banks for assembling and running a converter without needing to design PCBs. Some external DIN-rail mountable sensors can also be quickly and easily connected to the BoomBox RCP to measure external parameters, such as grid voltages and currents.

INDUSTRIAL INTEGRATION

Initially intended for power electronics development within R&D teams, the BoomBox RCP can also easily be integrated in a production converter thanks to its standalone mode, which makes the PC connection dispensable. Moreover, a high speed CAN interface can be used to easily exchange set points or measurements with other industrial equipment such as sensors, actuators or even SCADA units.

For a more cost-effective industrial approach, imperix provides a development service that aims to supply its industrial customers with a cost-optimized and tailored control hardware (example on Fig. 6) that is fully compatible with the code that has been developed on the BoomBox RCP. Indeed, the BoomBox operating system provides a full hardware independency over time and hardware. Imperix is thus capable of bridging R&D activities and industrial products within a simple and efficient control hardware ecosystem.

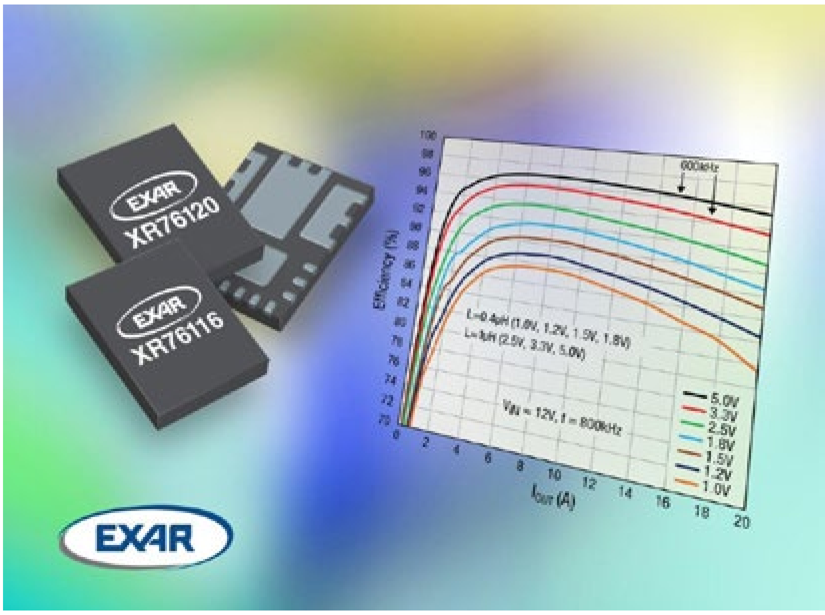
VERSIONS AND AVAILABILITY

Immediately available, the BoomBox RCP is packaged in two versions. The standard edition provides all the tools required to run standard converters, up to 16 measurements and 16 gating signals. To deal with more complex converters (e.g. multilevel) that require more I/Os, the expert edition is required, which enables the use of I/O expansion boxes. Both variants are provided with a lifetime license including the C/C++ programming environment, a visualization software, as well as 1-year of free software upgrades. For academic customers, imperix provides privileged conditions, including rental options.

http://www.imperix.ch

15A and 20A POL Regulators Power Next Generation Servers

Exar Corporation introduced the XR76116 and XR76120, 15A and 20A point-of-load (POL) step-down buck switching regulators using the latest generation of Exar's patented emulated current mode constant on-time (COT) control. This control loop provides the fast transient response required in demanding server applications while making implementation simple and easy. Improved gate driver technology has reduced dead times to 10ns, resulting in improved efficiency across the entire operating range.



The XR76116 and XR76120 extend the output current range of the PowerBlox™ line of Exar's high current POL regulators up to 20A. The patented COT control loop enables operation with ceramic output capacitors without degradation in transient performance and eliminates loop compensation components, making a simpler and more reliable design. Additional features targeted at server applications include a power good pin which maintains a low impedance when the chip is unpowered thereby avoiding false power good signals. Also, there is a second output voltage sense pin, ensuring any failure of the main feedback does not result on damaging voltages being applied to expensive low voltage digital circuitry. These POLs have exceptional full range 0.1% load regulation and 1% output accuracy over the full -40°C to 125°C temperature range. A host of supervisory and protection features for proper sequencing, safe operation under abnormal operating conditions and light load operation is built in.

www.exar.com

High-Speed High-Accuracy Line Expands Production Capacity

Mumbai-based EOS Power Pvt. Ltd. just opened a new high-speed, high precision production line. The new highly automated line enables the german-indian “low to mid volume/ high mix” global power solution experts to provide an additional production capacity of 3.500 pieces per day – fifty percent more than EOS’ current output.

EOS is known for its small, high efficiency AC/DC power supplies like the current (M)WLP series for medical and industrial applications. The new line is a perfect match for EOS’s “one stop-shop” philosophy. SMT, through hole assembly, lead free wave soldering, post wave out of box line testing, Burn-in, final test and conformal coating processes are served from a single shop-floor.

Core of the new line is one a FUJI XPF-L high speed multi-function precision placer - the world’s first placer which can change its placing heads automatically during manufacturing process. State-of-the-art digital and automated production control devices and software solutions from the U.S., Japan and Korea are supervising the production process. The brand new EMST wave soldering machine is accurately speeding up the production process.

In consequence 3654 more boards can be printed, 122625 more components can be placed, glue and solder levels and up to 16,000 pins can be checked automatically during one shift at EOS’ plant in Mumbai. “The highly automated and precise line was one of the results of our latest Kaizen process”, tells Ralph Bischoff, Director of EOS Power. “It will help us to guarantee even higher productive precision and quality to our customers – which will soon show in a revolutionary warrantee campaign we’re up to.”

Image: EOS Director Ralph Bischoff inaugurating the Wave Soldering machine of the new production line

www.eospower.com

288 Watt Narrow Profile DC-DC Regulated Power Supply Series

Acopian Power Supplies, a leader in the design, manufacturing and distribution of standard, modified-standard and custom power supplies, announced that their Narrow Profile DC-DC Regulated Power Supply Series is certified to UL 60950 (Information Technology Equipment) and UL 508 (Industrial Control Equipment) Safety Standards, conforms to the low voltage directive legal requirements to achieve CE marking, and is RoHS Compliant. The over 150-part series comprises 100 kHz single-output power supplies in DN8 and DN8A case sizes that support inputs from 110-350 VDC, outputs from 3.3 to 125 VDC, and up to 288 watts of power. Units provide excellent load regulation, overall stability and low output ripple and noise. These forced-air converters are supplied with either one or two fans, and are offered in dimensions as small as 1.7" x 3.5" x 8.78". Due to the series' narrow profile, small footprint and wide selection of input ranges, output voltages and current ratings, the power supplies are suitable for use in the broadest spectrum of industrial, consumer and industrial applications in which component size and weight are restricted. Parts are ideal for employment in nuclear, coal and gas power generation/storage/distribution, automotive, manufacturing, oil exploration and refinery, as well as information and communications technology equipment (ICT). They are also appropriate for instrumentation, test and measurement, R&D, industrial automation, mass transit and railway industry applications.

http://www.acopian.com/dcdc-narrow-m.html

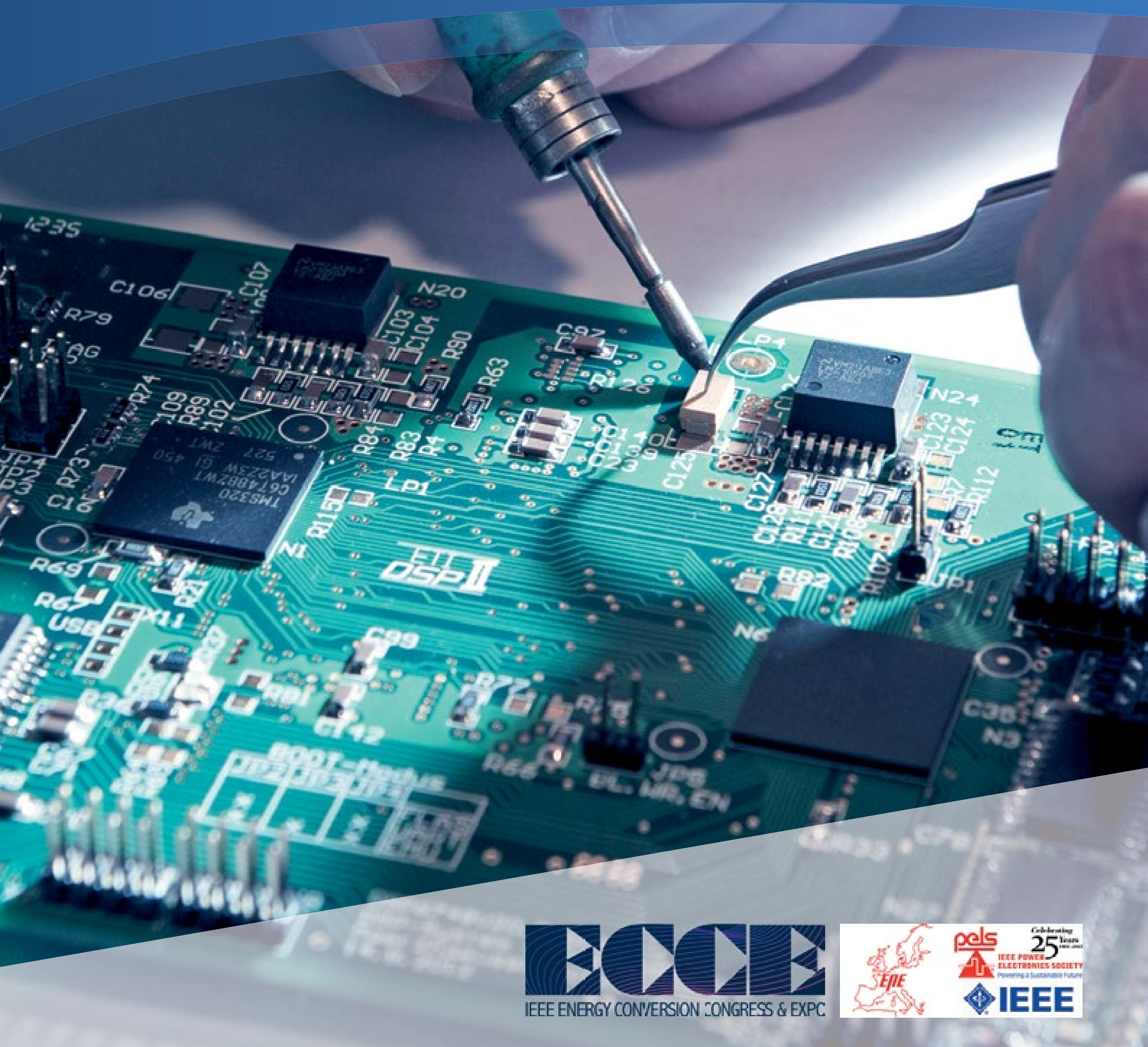
TO-220 FullPAK Wide Creepage Package

Infineon Technologies AG introduced the TO-220 FullPAK Wide Creepage package. The package is offered for the 600 V CoolMOS™ CE, targeting a broad range of low power consumer applications. This package features an improved creepage and has been developed to meet the demanding requirements of open frame power supplies where pollution might lead to arcing failures of applications. The TO-220 FullPAK Wide Creepage replaces frequently used workarounds to increase creepage distance such as silicon potting, the usage of sleeves, pre-bending of leads or others. Offering a better alternative to workarounds, customers profit from reduced system costs when implementing the new package.

Wide spread pins prevent failures

The TO-220 FullPAK Wide Creepage package targets open frame power supplies such as TV adapters where dust can enter the case through air vents. These dust particles can reduce the effective creepage between pins over time which may lead to high voltage arcing. The new TO-220 FullPAK Wide Creepage package comes with a pin distance of 4.25 mm instead of the prevailing 2.54 mm found in a standard TO-220 FullPAK package.

www.infineon.com/TO220-FP-widecreepage



High-Reliability SCALE-2 Driver Technology to 1200 V Applications

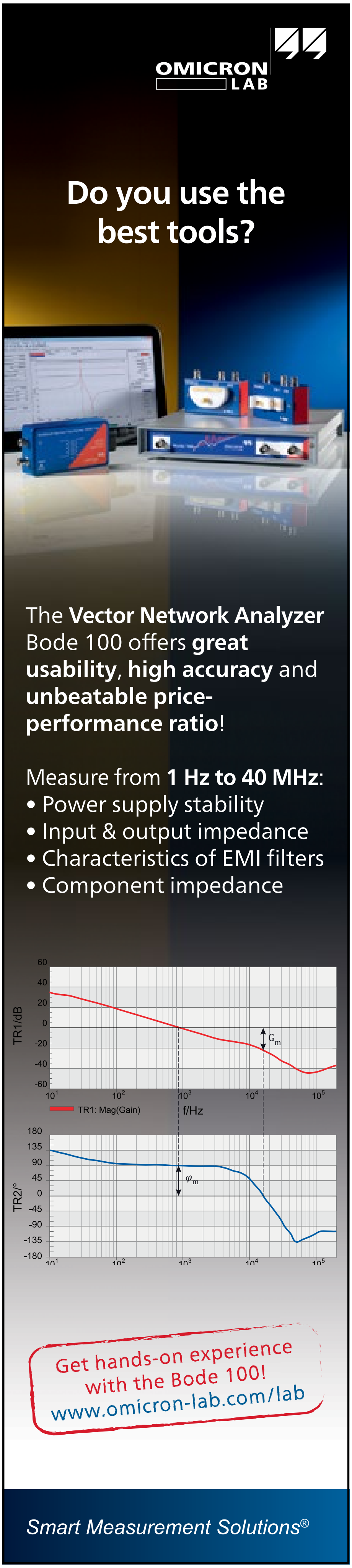
Power Integrations, the leader in IGBT and MOSFET driver technology for medium and high-voltage inverter applications, announced a family of galvanically isolated single-channel gate driver ICs ranging in output current from 2.5 A to 8 A – the industry's highest output current without an external booster. SCALE-iDriver™ ICs, optimized for driving both IGBTs and MOSFETs, are the first products to bring Power Integrations' pioneering FluxLink™ magneto-inductive bi-directional communications technology to 1200 V driver applications. FluxLink technology eliminates the need for unreliable opto-electronics and the associated compensation circuitry, thereby enhancing operational stability while reducing system complexity. In addition to combining industry-leading isolation technology, the new gate drivers incorporate advanced system safety and protection features commonly found in medium- and high-voltage applications, further enhancing product reliability. The innovative eSOP package features 9.5 mm of creepage and a CTI of 600, ensuring substantial operating voltage margin and high system reliability.

SCALE-iDriver single-channel gate driver ICs dramatically reduce component count for inverters up to 110 kW, saving space and BOM cost and increasing design flexibility. With the addition of a simple, low-cost booster stage, it is now far quicker to develop efficient, space-saving, reliable inverter designs rated up to 400 kW (15 A). The new devices meet the IEC 60664-1 and IEC 61800-5-1 standards, and operate from -40 °C to +125 °C and at frequencies of up to 250 kHz. They also feature Power Integrations' Advanced Soft Shut Down (ASSD) mechanism that protects the power semiconductor switch in the event of a short circuit. ASSD is automatically triggered by monitoring desaturation levels and requires no extra components.

Comments Michael Hornkamp, senior director of marketing for high-power products at Power Integrations: "SCALE-iDriver ICs will revolutionize gate driver design. By pairing Power Integrations' SCALE™ technology – which already incorporates all key gate-driver functions into an ASIC – with accurate, high-speed FluxLink communication, we have increased performance and reliability by an order of magnitude when compared to devices that use opto- or silicon-isolated capacitive or magnetic couplers. Bi-directional communication results in fast, efficient, accurate switching and minimizes signal jitter. The wide FluxLink isolation gap delivers exceptional robustness, and the use of low-profile packaging technology enables basic two-layer PCBs to be used, reducing size and system cost."

SCALE-iDriver ICs suit applications in industrial drives, power supplies and UPS, photo-voltaic inverters of all sizes, industrial HVAC, EV charging and traction equipment including commercial EVs. SID1132K (2.5 A), SID1152K (5 A), SID1182K (8 A) devices are available and priced at $2.57 in 10,000-piece quantities. Reference designs RDHP-1608 (2.5 A, 5 A and 8 A versions) and RDHP-1526 (15 A) and technical support for SCALE-iDriver ICs are available from the Power Integrations website at:

https://www.power.com/products/scale-idriver



High Temperature Ceramic MLCs are a 'HiT' with Demanding Applications

Knowles capacitor brands Novacap and Syfer Technology jointly announce the launch of a new range of high temperature MLC chip capacitors. The HiT range of MLCCs has an operating temperature range of -55 to +200ºC and are suitable for a variety of high temperature applications and offer tin over nickel terminations – not previously available.

Projects in oil exploration, geothermal, military, automotive underhood and avionics will find the wide capacitance range of 4.7pF to 3.3uF, over the rated voltage spread 16 to 630V dc, of interest. Stable and ultra stable dielectric options, C0G & X7R materials, are both RoSH compliant and lead free

This range is manufactured to exacting standards using Knowles unique screen printing process to provide a high quality component suitable for demanding applications.

HiTEC 2016 continues the tradition of providing the leading biennial conference dedicated to the advancement and dissemination of knowledge of the high temperature electronics industry. Under the organizational management of the International Microelectronics Assembly and Packaging Society (IMAPS), HiTEC 2016 is the forum for presenting leading high temperature electronics research results and application requirements. It creates an opportunity for networking with colleagues from around the world working to advance high temperature electronics.

www.knowlescapacitors.com

3500/5000 Watt 3-Phase AC-DC Power Supply

Murata announced the D2U5T-H3-5000-380-HU3C; a highly efficiency, 3500/5000 Watt, three-phase power converter for 230/480VAC systems from Murata Power Solutions.

The D2U5T-H3-5000-380-HU3C power supply operates from utility-grade, three-phase AC power to deliver 5000 Watts of reliable power to 380V distributed power systems, HVDC datacenters and other industrial applications. It is provided with droop sharing to provide N+1 redundancy of supply to the application. Up to three supplies may be operated in parallel for a total system power of 15,000 Watts.

The D2U5T power supply uses a Vienna rectifier topology to allow true three-wire input without the need for a neutral connection. Its use of digital controls allows a linear efficiency curve, with efficiency greater than 95% at 50% load. The unit accommodates input voltages in the range 180- 264 VAC for 3,500 Watt operation and 320 – 525 VAC for 5,000 Watt output.

Packaged in an industry standard 2U format and delivering a 23.1 Watt per cubic inch power density, the D2U5T is designed for use in broadcast, industrial and large data centre applications where high power conversion efficiency is vital. +++ends

http://www.murata.com

Introduction of CoolPerformance Plus Coolers

Rogers Corporation's Power Electronics Solutions (PES) group has introduced its latest high-performance cooling material, curamik® CoolPerformance Plus. curamik CoolPerformance Plus is an advanced liquid-cooled material designed to dissipate large amounts of heat and provide reliable thermal management of high-power laser diodes and other heat-generating optical devices.

curamik CoolPerformance Plus for Laser Diodes

CoolPerformance Plus coolers build upon the effective cooling approach employed in Rogers curamik CoolPerformance coolers. Both types of coolers feature several layers of pure copper, taking advantage of its excellent thermal conductivity. The copper foils are formed into hermetic, three-dimensional microchannel or macrochannel water-cooled structures capable dissipating large amounts of heat in small areas.

The new curamik CoolPerformance Plus coolers feature the addition of aluminum-nitride (AlN) isolation layers to proven curamik CoolPerformance copper cooling structures. The ceramic AlN layers separate the cooling water channels from the electrical contacts of laser diodes. They also provide a close match in coefficient of thermal expansion (CTE), in the range of 5 to 7 ppm/K, between the copper cooling structures and high-power ceramic laser diode packages for improved reliability even at high power levels.

The mounting surfaces of the new curamik CoolPerformance Plus coolers can be diamond-milled to meet the fine tolerances required for mounting of laser diode packages, for optimum flow of heat away from the diodes. Both curamik CoolPerformance and CoolPerformance Plus coolers provide more efficient cooling solutions than traditional liquid-cooled methods, and they can provide effective thermal-management solutions for laser diodes operating at power levels to 100 W or more.

www.rogerscorp.com

High efficiency AC-DC power modules have ratings up to 1000W

TDK Corporation announces the introduction of the PFE1000FA series of power modules, representing a significant upgrade to the PFE1000F launched eight years ago. The new series offers efficiencies as high as 90%, an improvement of up to 4%. Rated between 720W and 1000W, the products are designed for use with a cold-plate where cooling fans are not permitted, including industrial, MIL-COTS and communications applications.

The PFE1000FA is available with nominal output voltages of 12V, 28V and 48V that can be adjusted over a ±20% range for non-standard voltage requirements. The series accepts a wide range 85 to 265Vac input and can operate at full load with baseplate temperatures of between -40 and +100°C. Having the same pinout and package dimensions as the original series, 100 x 13.4 x 160mm, the new series can easily be used to upgrade existing designs, offering up to 30% lower losses and reduced operating temperatures. Input current wave-shapes have been improved to be more sinusoidal, allowing the PFE1000FA to meet the harmonics standard IEC 61000-3-2 with even greater margins.

All models feature remote on/off, an opto-isolated module good signal, single wire current sharing and a 12V 20mA standby voltage as standard. The PFE1000FA modules are safety certified to IEC/EN/US 60950-1, with CE marking for the Low Voltage and RoHS2 Directives. The series now carries an extended warranty of five years.

www.uk.tdk-lambda.com/pfe-fa

www.tdk-lambda.com/

Clamp AC Current Sensors Expanded for High Current Applications

TDK Corporation has expanded its CCT series of clamp AC current sensors with a new 600 A type. The lineup of TDK current sensors is now positioned to meet the high-current sensing needs of energy management systems (EMS) for buildings, factories, stores and communities. The new CCT406393-600-36 current sensor has a clamp inner diameter of 36 mm and external dimensions of 56 mm x 67 mm x 96 mm. With a current transformation ratio of 3000:1, the output current is 200 mA. Mass production will begin in July 2016.

The new clamp AC current sensor achieves its high current rating thanks to its optimized sensor shape and high-performance ferrite material developed especially for current sensors. Moreover, the CCT series is manufactured with automated winding and soldering processes to ensure high quality.

With the addition of this new component to a current sensor lineup that already includes a 300-A (24 mm inner diameter), 100-A (16 mm) and 30-A (6 mm) types, TDK offers a comprehensive portfolio of clamp AC current sensors for a wide range of currents.

http://www.global.tdk.com/

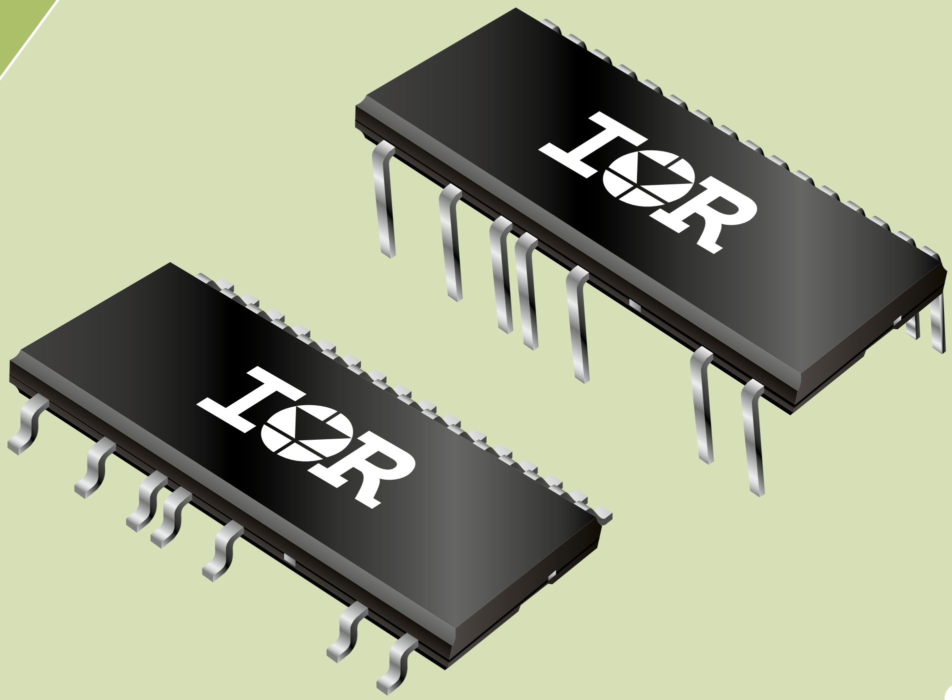
High-Performance Power Conversion with TI's 600-V GaN FET Power Stage

Building on decades of power-management innovation, Texas Instruments (TI) (NASDAQ: TXN) today announced the availability of 600-V gallium nitride (GaN) 70-mΩ field-effect transistor (FET) power-stage engineering samples, making TI the first and only semiconductor manufacturer to publicly offer a high-voltage driver-integrated GaN solution.

The new 12-A LMG3410 power stage coupled with TI's analog and digital power-conversion controllers enables designers to create smaller, more efficient and higher-performing designs compared to silicon FET-based solutions. These benefits are especially important in isolated high-voltage industrial, telecom, enterprise computing and renewable energy applications.

www.ti.com/lmg3410-pr-eu

Advertising Index



Best-in-class performance for low power motor drives

600 V Intelligent Power Module optimized for 70 – 250 W fan drives

The IRSM506-076 series extends the µIPM™-DIP driving capability to 90 W without and 250 W with a heat sink. The new part offers the best power output capability of any module in its form factor. Target applications include fan and pump drives.

Main Features

- Low loss Trench IGBT + Pt diode technology
- Integrated bootstrap functionality
- Under-voltage lockout for all channels
- Matched propagation delay for all channels
- UL certified NTC for temperature feedback available
- Optimized dV/dt for loss and EMI trade off
- Advanced input filter with shoot-through protection
- Separate low-side emitter pins for single or leg-shunt current sensing
- 3.3 V logic compatible
- 1900 V_{RMS}, 1 min isolation (UL Certified: File Number E252584)

Benefits

- Lower losses then similar modules in the market
- Advanced input filter & shoot through protection
- Accurate temperature feedback via UL certified NTC

www.infineon.com/uIPM