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Bodo´s Power Systems®

Electronics in Motion and Conversion

March 2017

Dry Film Capacitors for High-Frequency Electronics

The Gallery

Bodo´s Power Systems®

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Make the World Great,

We have only the one world to live in, and everyone's goal should be to make this one world great.

Peace and respect is therefore of utmost importance. "Alternative Facts" are words that should raise concerns. But a belief in an "Alternative Reality" should qualify one for medical assistance. Respected members of science have written a letter addressing the global warming issue and the need for corrective actions. To read this letter, signed by 706 US Physicists and Astronomers from Colleges and Universities across the United States, just go to: http://people.usm.maine.edu/pauln/climate/the-letter.html .
To deny the existence of global warming, or to take actions that accelerate it, are bad for our world. As engineers we can do our part by placing a focus on energy efficiency.
I hope the future will show us that a better world for our kids is achievable.

This year is a special one for me. As a young engineer 30 years ago, I worked with a customer to develop a design for a variable speed drive for a household appliance, using a switching device known in 1987 as a COM-FET. Today these are known as an IGBT. In the 30 years since a lot has happened, now all over the world the IGBT is the work horse for power switching applications. And still, new developments are still being made. Looking back is not what drives progress, so I look forward to the wide band gap devices and exciting new designs that reduce losses and continue improvement. The APEC Conference is a time to see engineers from around the world discussing progress in the technology of power electronics. I look forward to meeting my friends – all a big family, young and old. They're a well-established group, many of whom I have known for decades, always working for progress in semiconductors. Through respect and cooperation, we can provide a positive example to our children. I look forward to seeing you in a few weeks at the APEC conference in Tampa.

Bodo's Power Systems reaches readers across the globe. If you are using any kind of tablet or smart phone, you will now find all of our content on the new website www.eepower.com.
If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com

My Green Power Tip for March:
Driving an electric car in the winter requires a warm jacket, as heating the car may significantly reduce the driving range of the battery. So bundle up!
Best Regards

Events

Smartsystemsintegration
Corck Ireland, March 8-9
http://www.smartsystemsintegration.com

Battery Experts Forum 2107
Aschaffenburg, Germany, March 14-16
http://www.battery-experts-forum.com/

Embedded World 2017
Nuremberg, Germany, March 14-16
http://www.embedded-world.de

EMC 2017
Stuttgart, Germany, March 28-30
http://www.mesago.de/en/EMV/home.htm

APEC 2017
Tampa FL , March 26-30
http://www.apec-conf.org/

Internat. Power Workshop on Packaging
Delft, The Netherlands, April 5-7
http://iwipp.org/

ExpoElectronica 2017
Moscow Russia, April 25-27,
http://expoelectronica.primexpo.ru/en/

SMT Hybrid 2017
Nuremberg, Germany, May 16-18
http://www.mesago.de/en/SMT/home.htm

PCIM Europe 2017
Nuremberg, Germany, May 16-18
http://www.mesago.de/en/PCIM/home.htm

ISiCPEAW 2017,
Stockholm, Sweden, May 21-23
mietek.bakowski@acreo.se

Sensor + Test 2017
Nuremberg, Germany, May 30 June1
http://www.sensor-test.com/press

Intersolar 2017
Munich, Germany, May 31 June 2
www.intersolar.de/de/intersolar-europe.html

Workshops about PLECS

Real-Time Simulation using the PLECS RT Box

Plexim is planning hands-on workshops on real-time simulation with PLECS and the RTBox.

In the workshop, you will learn modeling techniques for real-time simulations using PLECS with the PLECS RT Box. You will work hands-on with hardware-in-the-loop (HIL) and rapid control prototyping (RCP) application examples. You will see that step size can be reduced to microseconds, even for large-scale models. A detailed agenda will be available soon. In addition to the technical aspects, the workshop offers an opportunity to connect with the developers of PLECS. The required software and PLECS RT Box hardware will be provided for the workshop.

RT Box LaunchPad Interfaces available

The PLECS RT Box LaunchPad Interface is an add-on for the PLECS RT Box. It is designed to get you up and running with our real-time testing unit even faster. The microcontroller comes already flashed with an embedded control project.The corresponding plant models in PLECS introduce a demonstration set of hardware-in-the-loop (HIL) applications.

Thursday, 4 May in Zurich (CH)
www.plexim.com/events/seminars/1062
Wednesday, 7 June in Zurich (CH)
www.plexim.com/events/seminars/1068

For an in-house workshop at your company, please contact us at info@plexim.com.
Pricing information is available on:

www.plexim.com

VP of Technology Elevated to IEEE Fellow

Indium Corporation's Dr. Ning-Cheng Lee, Vice President of Technology, has been bestowed the prestigious title of Fellow of the Institute of Electrical & Electronics Engineers (IEEE) for his leadership in surface mount technology and interconnect materials.

IEEE is the world's largest technical professional association with more than 400,000 members in 160 countries. To be chosen as an IEEE Fellow is a distinction reserved for select IEEE members whose extraordinary accomplishments are deemed fitting of this esteemed designation. Less than 0.1% of voting members are selected annually.

Dr. Lee is a world-renowned soldering expert, an SMTA Member of Distinction, and IEEE Fellow. He has extensive experience in the development of fluxes, alloys, and solder pastes for SMT industries, and extensive experience in the development of high-temperature polymers, encapsulants for microelectronics, underfills, and adhesives. In addition to SMT and semiconductor soldering materials, his research also extends to nanobonding technology and thermal conductive materials.

www.indium.com

Opening of Blacksburg, Virginia eGaN® FET and IC Applications Center

Efficient Power Conversion Corporation (EPC) is proud to announce the opening of an Applications Center in Blacksburg, Virginia. This center will increase the reach of EPC to support research and development for the applications of enhancement-mode gallium nitride transistors and ICs. In addition to traditional FET and IC power conversion applications, GaN technology has enabled emerging applications such as wireless power transfer, LiDAR for autonomous vehicles, and envelope tracking for high bandwidth 4G and 5G communications.

In support of the center's opening, Suvankar Biswas, Ph.D. has been appointed as senior applications engineer. Dr. Biswas' experience includes work involving converter topology for integration of photovoltaic modules, grid-tied inverters, and storage. Additionally, Suvankar has research experience in the integration of harvested power in mobile devices, power delivery architecture in mobile platform-level systems, and plug-in hybrid vehicles and their connectivity with the Smart Grid. He is an active member of IEEE with numerous peer-reviewed published articles. Dr. Biswas obtained his bachelor of electrical engineering degree from the Indian Institute of Technology Kharagpur and his doctorate degree from the University of Minnesota.

"The opening of the Blacksburg Applications Center is an important component of our continuous efforts to focus on customer partnerships when designing eGaN technology-based solutions and demonstrating eGaN transistors' superior performance over MOSFETs and LDMOS. We are very pleased to have Dr. Biswas joining us at this time of widespread, fast growing adoption of gallium nitride-based solutions," said Alex Lidow, CEO and co-founder of Efficient Power Conversion Corporation.

www.epc-co.com

Announcing New Stencils Partnership for the French Market

Alpha Assembly Solutions, the world leader in the production of electronic soldering and bonding materials, is pleased to announce a new stencils partnership with STP Electronics for the French market, commencing the 1st February 2017.

Alpha's Country Manager for France, Mathias Mary, commented, "Alpha has been one of the leading manufacturers of stencils for the solder paste printing process in France for more than 20 years. The new partnership with STP Electronics will enable us to increase our commercial and technical footprint and support network for French customers."

STP Electronics, led by manager Eric Vignard, has over 25 years' experience in the sector and was one of the first suppliers of solder paste printing stencils in France. Customers will be able to benefit from STP Electronics' technical expertise and commercial support in collaboration with the existing Alpha team. In this new partnership, Alpha France will continue to process and produce stencils orders at its Cholet facility.

www.stp-electronics.com

www.AlphaAssembly.com

Hub with TI LaunchPad™ Board - a new STEM solution

Texas Instruments (TI) has announced the European launch of TI-InnovatorTM Hub with TI LaunchPad™ Board, a classroom tool that introduces students to coding and engineering design to prepare them for the jobs of the future. Most educators and experts agree coding is a skill so important that every student needs to know the basics to excel in a rapidly changing world. Coding classroom activities enjoy a growing interest in several European countries such as France, UK and the Netherlands, which are working to implement them into their maths and science curriculum.

The TI-Innovator™ Hub, a palm-sized box with a built-in microcontroller, plugs into the graphing calculator many secondary school students already own, a TI-84 Plus CET or a TI-Nspire™ CX and TI-Nspire™ CX CAS, and allows them to analyze and explain the world around them. It was created using the TI LaunchPadTM Board, the same technology used by leading engineers around the world to design cutting-edge products from smart watches to 3-D printers. For example, students can start by learning to write a program to play a single note, and then put together sounds at different frequencies to play a song.

www.education.ti.com

www.ti.com

Battery Experts Forum in Aschaffenburg, 14 – 16, March 2017!

The 13th Battery Experts Forum is the highlight of the year and will take place from 14 -16 March 2017 in City Hall of Aschaffenburg. Experts from leading battery and charger manufacturers will inform you about the most recent product developments and solutions. Meet the experts of lithium ion battery industry. Keynote Speakers:
World market analysis– trends and future visions, Sven Bauer, CEO BMZ GmbH
Electrical Vehicle: Market, Trends, Quantity, Christophe Pillot, AVICENNE Développement
The future of a cell production in Germany, Dr. Michael Krausa, Kompetenzzentrum Lithium-Ionen-Batterien e.V. (KLIB)
Be part of it

www.battery-experts-forum.com

BATTERY EXPERTS FORUM

N°13 | March 14th - 16th 2017 | ASCHAFFENBURG

PSMA Announces APEC 2017 Industry Session on Energy Harvesting

At APEC 2017, the PSMA's (Power Sources Manufacturers Association's) Energy Harvesting Committee will host an Industry Session featuring five industry experts who will cover such topics as real-world applications, conditional monitoring, energy harvesting systems, PMICs (Power Management ICs) and low-power IoT (Internet of Things) devices. The Energy Harvesting Session (IS16) will be held on Thursday, March 30, from 8:30 a.m. to 11:30 a.m., at the Tampa Convention Center.
The key message of the session is that energy harvesting has moved out of the lab and into real life. Energy harvesting presents a major opportunity for the power electronics industry, from components (batteries, ICs, magnetics, semiconductors, etc.) to systems (e.g., wearable devices, building energy management, assisted living, environmental monitoring, security, transportation). But to fully exploit this opportunity, and to make energy harvesting more mainstream, stakeholders need to work more closely to get energy harvesting solutions working reliably in actual applications.
This industry session attempts to accelerate such engagement by providing an overview of the considerations, applications, constraints and trade-offs that need to be taken into account. The session will include a 30-minute slot for live and hands-on demonstrations, many of which will relate to the speaker presentations.

www.psma.com/

PCIM Europe 2017 Conference Program is Online

The PCIM Europe 2017 conference program is now available. Conference participants gain a complete overview of the market as well as access to specialized knowledge within the power electronics industry, they can network and exchange ideas about current developments and applications.

View the conference program for detailed information with all sessions, tutorials and seminars.

www.mesago.de/de/PCIM/Die_Konferenz/Englisch/index.htm

Broadcom Optocouplers

Take the Risk Out of High Voltage Failure!

Optocouplers are the only isolation devices that meet or exceed the IEC 60747-5-5 International Safety Standard for insulation and isolation.

Stringent evaluation tests show Broadcom optocouplers deliver outstanding performance on essential safety and deliver exceptional High Voltage protection for your equipment. Alternative isolation technologies such as magnetic or capacitive isolators do not deliver anywhere near the high voltage insulation protection or noise isolation capabilities that optocouplers deliver.

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BROADCOM®

SiC Seminar at APEC 2017 for Power Design

USCi and Richardson Electronics, Ltd. invite you to join us at an exclusive event to present the best way to streamline your power and energy design with Silicon Carbide technology.

APEC is the premier global event in applied power electronics. APEC 2017 continues to be a leader, engaging all sectors of the industry while maintaining one of the lowest registration costs of any IEEE conference. The conference will be held at the Tampa Convention Center, in beautiful Tampa, FL, March 26-30, 2017.

Enjoy a presentation of the must-know technology for Silicon Carbide and engage in a one-on-one session with USCi's Vice President of Engineering, Dr. Anup Bhalla, and Director of Applications Matt O'Grady. Come to discover how this next generation power semiconductor takes advantage of a wide bandgap to deliver inherent strength and durability that is well suited to your power applications.

March 27, 2017 @ 12:00pm-1:30pm,
Tampa Marriott Waterside Hotel & Marina,
Meeting Rooms 5 & 6, 700 South Florida Ave, Tampa, FL 33602

Numbers are limited at this exclusive event, however, we value highly referrals and your guests are always welcome.
Please RSVP at: www.rellpower.com

For more information on USCi, please visit USCi at

www.UnitedSiC.com

International's Enduring Partnership Continues

Vincotech, a supplier of module-based solutions for power electronics, pledged €12,000 to support an educational project for women in central Java. This grant is in lieu of the company's traditional seasonal gifts to business partners. The funds are earmarked to support vocational training sponsored by Plan International Deutschland e.V.

Jobs are few for young people in this region. Many women never learn a trade. This project aims high in the hopes of affording disenfranchised youth the opportunity to acquire the skills needed to find a job commensurate with their qualifications and aspirations.

Vincotech's social commitment runs deep. The company has long partnered with Plan International, an NGO dedicated to ending child poverty, and will continue to track and report on this latest project's progress.

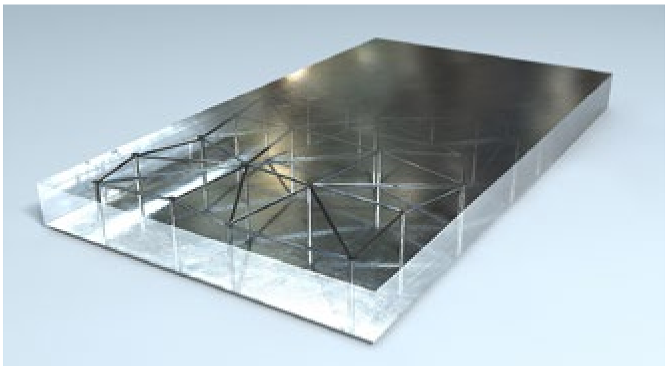
www.vincotech.com/Eur12000-to-Plan

www.vincotech.com/plan

Featuring InFORMS® Reinforced Solder Preforms at APEC 2017

Indium Corporation will feature its reinforced solder alloy fabrications, InFORMS®, at APEC 2017, March 26-30, in Tampa, Fla.

InFORMS are reinforced solder preforms that increase lateral strength and stability. As a result, improved thermal cycling reliability can be achieved.



In one study where InFORMS were used to solder a DBC to the baseplate of an IGBT, the following were achieved:

4x improved thermal cycling reliability compared to a solder preform-only approach

2x improved thermal cycling reliability compared to a solder preform + Al wirebond stitch approach

Low-voiding of <1%

Lower cost of ownership – an InFORM is a drop-in replacement for a standard preform or solder paste, requiring no additional process steps or equipment

For more information about InFORMS, visit Indium Corporation at APEC booth #525.

www.indium.com/informs

LinkSwitch-XT2 Offline Flyback Switcher IC Family Delivers High Accuracy and Efficiency

Rugged new ICs enable excellent no-load performance and are ideal for low-power applications including appliances, IoT, metering and industrial bias power.

Power Integrations, the leader in high-voltage integrated circuits for energy-efficient power conversion, introduced its LinkSwitch™-XT2 family of offline, low-power converter ICs offering high accuracy, high efficiency and excellent no-load performance. LinkSwitch-XT2 ICs target isolated and non-isolated flyback applications in which accurate regulation of output voltage and current are important. The new ICs can deliver up to 6.1 watts in wide-input range designs, and up to 9.2 watts for 230 VAC open-frame applications.

Designed for flyback topologies, the LinkSwitch-XT2 family delivers designs that exhibit current and voltage regulation of better than -/+ 3% and typical efficiency above 80%. LinkSwitch-XT2 ICs consume less than 10 mW in no-load conditions. High (132 kHz) operating frequency enables the use of small power transformers, while the programmable current limit (ILIM) function enables further transformer optimization.

LinkSwitch-XT2 converters combine a 725 V power MOSFET with control circuitry on a single silicon die. Integrated safety and reliability features include input overvoltage protection, hysteretic thermal shutdown for over-temperature protection, and auto-restart for output short-circuit, overvoltage and open-loop protection.

Comments senior product marketing manager Silvestro Fimiani: "The accuracy, small size, efficiency and excellent no-load performance of LinkSwitch-XT2 ICs makes them ideal for small appliances such as microwave ovens, IoT applications, utility meters, industrial and smart-home installations."

LinkSwitch-XT2 ICs come in three packages: P-package (DIP-8C), D-package (SO-8C), and G-package (SMD-8C) and are priced at $0.40 in 10,000-piece quantities. More information, including reference design DER-578, which details a 5 V 500 mA power supply, is available from the Power Integrations website at www.power.com/products/linkswitch-xt2/.

About Power Integrations

Power Integrations, Inc. is a leading innovator in semiconductor technologies for high-voltage power conversion. The company's products are key building blocks in the clean-power ecosystem, enabling the generation of renewable energy as well as the efficient transmission and consumption of power in applications ranging from milliwatts to megawatts. For more information please visit:

www.power.com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cde.com/MLSHSlimpack

Win a BM64 Bluetooth Audio Evaluation Board

Win a Microchip BM64 Bluetooth Audio Evaluation Board (BM-64-EVB-C2) from Bodo's Power.

This board enables easy development with Microchip's new IS206X of SoC devices and modules which offer Bluetooth Low Energy (BLE) capability. Uniquely engineered for speakers, headsets and gaming headphones, the IS206X flash-based platform offers flexibility and powerful design features, allowing audio manufacturers to easily incorporate wireless connectivity in streaming music and voice command applications.

The BM64 Bluetooth Audio Evaluation enables the user to evaluate and demonstrate the functionality of the BM64 Class 2 stereo audio module. The BM-64-EVB-C2 includes an integrated configuration and programming interface for plug-and-play capability, and also has status LEDs which enable rapid prototyping and faster time to market.

Along with the BM-64-EVB-C2, software tools and applications are provided to demonstrate the Bluetooth connections to the on-board BM64 stereo audio module and to optionally configure or program it. Microchip's highly-integrated module solutions are self-contained, low-power, and fully-certified for designers seeking to develop wearable or IoT devices without any Bluetooth Low Energy IP Stack or RF experience

The BM64 EVB has two USB ports that can be connected to the host PC using a micro-USB cable. Other BM64 Bluetooth Audio Evaluation Board features include:

- Based on the fully-certified Bluetooth 4.2 BM64 Class 2 stereo audio module
- Powered by a PC host using the micro-USB cable or by connecting a Li-Ion battery
- Built-in 3W Class-D stereo audio amplifier
- Built-in Near Field Communication (NFC)
- Stereo audio output for high-quality audio
- Easy access to I/O pins
- Connection and data status LEDs

For your chance to win a Microchip BM64 Bluetooth Audio Evaluation Board, visit www.microchip-comps.com/bodo-m64blue and enter your details in the online entry form.

www.microchip-comps.com/bodo-m64blue

System Benefits of Using G1 Series Intelligent Power Modules (IPM)

Mitsubishi Electric integrates several key technologies into one power module in order to deliver the best possible overall system performance. The G1 IPM concept addresses three areas crucial for inverter designers – [1] Easy design, [2] High efficiency and [3] High reliability.

Easy design: The G1 IPM is provided with an internal gate drive unit, multiple integrated protection functions and a failure output signal for easy facilitation of failure recognition. The incorporation of these functions into the G1 IPM relieve the inverter designers from extensive verification tests as all functions are fine-tuned to the built-in 7th gen IGBT/FWDi-chip set and which are 100% tested by the module manufacturer. Another feature going in favor of the design process is the busbar design flexibility option: the 'A' package variant (refer Figure 2) offers two possible main terminal positions. One option is where the AC output side is placed in parallel with the DC input terminal and another option is where the DC input terminal is placed at a 90° angle to the AC output terminal (with both variants available in either screw type terminal or solder type terminal).

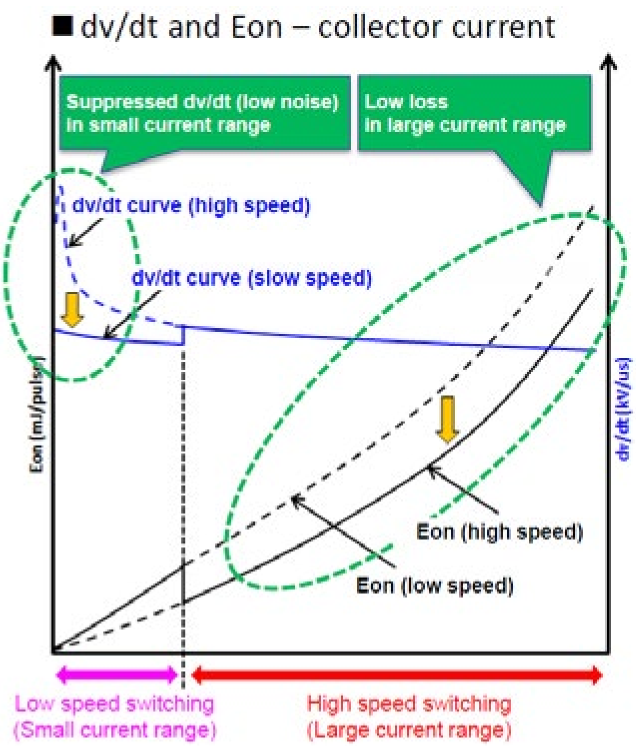


Figure 1: dv/dt and Eon control in G1 IPM

High efficiency: The IGBT chip is based on a special internal gate design optimized for the IPM's 'short circuit capability versus losses' trade-off, and as a result the ON state loss behavior is significantly lower than a conventional IGBT device and the Vcesat versus Eoff characteristic is also superior in comparison with a conventional IGBT device. In combination with this special gate design, this improved IGBT chip is provided with a monolithically integrated current mirror to implement a current sensing scheme. There are two main benefits offered by such a current sensing scheme. Firstly, an effective SC protection can be realized which is based on the instantaneous device current Ic. The trip level of such an SC-protection can be established independent of the IGBT-desaturation, thus being much faster than the conventional desat-protection. Secondly an innovative switching speed control can be established depending on the actual value of the device current Ic. This means - a reduced speed (for Low EMI) turn-on at low Ic values and a high speed turn-on (low turn-on loss) at high Ic values can be achieved (refer Figure 1). These key features ensure a significantly higher inverter efficiency and good EMI performance.

	Small-Pkg. (A-Pkg.)	Middle-Pkg. (B-Pkg.)	Large-Pkg. (C-Pkg.)
Outline of Package			
650V 6in1	50A, 75A, 100A	50A, 75A, 100A, 150A, 200A	200A, 300A, 450A NEW
650V 7in1	50A, 75A	50A, 75A, 100A, 150A,200A	200A, 300A, 450A NEW
1200V 6in1	25A, 50A	25A, 50A, 75A, 100A	100A, 150A, 200A NEW
1200V 7in1	25A	25A, 50A, 75A, 100A	100A, 150A, 200A NEW

Figure 2: Line-up of the G1 IPM modules

High reliability: The module packaging design and chip design have been established with 'product reliability' assuming utmost importance. The module consists of built-in functions which aid in failure detection, module's self-protection activation and facilitates failure-type recognition. An important feature is that the IGBT is provided with an on-chip temperature sensor to detect an over temperature directly in the silicon. There is a power supply under-voltage protection system and an innovative short-circuit protection scheme. The G1 module packaging technology aims to improve the withstand capability against stress factors causing degradation/aging of the module. The module employs the SLC (Solid Cover) technology along with an innovative IMB (Insulated Metal Baseplate) structure. As a result, the module exhibits superior thermal cycling behavior while providing lower thermal resistance.

www.mitsubitchichips.eu

Mind the Gap! – WBG Semiconductors are Gaining Importance

By Dr. Peter Friedrichs, Senior Director SiC and Steffen Metzger, Senior Project Director GaN, Infineon

Dr. Peter Friedrichs

Steffen Metzger

Designers of power supplies, motor control and inverter systems, RF circuitry, photovoltaic circuits and a variety of other power switching schemes are under unprecedented pressure to improve application performance while increasing power density, reducing board space and driving down component count. To address these seemingly conflicting challenges, engineers are increasingly looking to deploy solutions based on wide band gap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN).

The attraction of using WBG materials is clear. Switching at higher frequencies than conventional silicon can improve power density by shrinking the size of passive components. It can also help to save energy on cooling the overall system. Low charge and excellent dynamic performance in reverse conduction compared to silicon alternatives can enable more efficient operation in today´s applications at existing frequencies. And the much higher breakdown field strength and thermal conductivity of SiC devices allows manufacturers to create devices that outperform silicon alternatives across a range of temperatures – a key concern in areas such as photovoltaics, industrial motor drives, traction and electromobility.

But before WBG materials start to gain a significant share in the market, engineers need to take stock of a number of important issues. These range from the technology itself, through large scale manufacturing and supply chains to the support infrastructure that is behind it.

Silicon-based semiconductors may have been around for almost sixty years but they are not ready to be written off just yet. Manufacturers continue to invest heavily in silicon R&D and a large proportion of power applications can still be addressed using the latest advances around this ‘conventional’, reliable and highly cost-effective technology.

That said, there is no doubt that there are a growing number of demanding applications where silicon devices can simply no longer address the target requirements. Take, for instance, RF power.

Many RF applications are now heading towards frequencies where the efficiency of silicon devices is no longer good enough. To address this, semiconductor manufacturers are developing WBG solutions designed specifically for RF applications. Solutions such as Infineon’s comprehensive family of GaN-on-SiC RF power transistors that operate at frequencies of 1.8GHz and higher. These devices enable cellular amplifier designers to build smaller, more powerful and more flexible transmitters. And as the world moves towards 5G infrastructures, the role that GaN technology can play in this field is set to become even more important.

RF power is actually a relatively well-established market for WBG solutions when compared to the market for more general switching power applications including power supplies and inverters. And, as with many less mature markets, a lot of startups and small players are emerging with highly innovative solutions that compete in the key areas of price and performance. However, price and performance are far from the only issues to consider. Alongside the issue of not yet having manufacturing capabilities at a larger scale or an established supply chain and support infrastructure, a key challenge for some of these smaller companies is reluctance on the part of OEMs to buy a yet relatively unproven technology. Part of this reluctance relates to unknowns regarding product reliability.

Indeed, careful consideration of reliability should be at the forefront of the engineer’s mind when evaluating technologies for a power application that will be expected to operate, trouble-free, for many years. One of the issues is that a GaN structure, for example, is fundamentally different to a superjunction silicon structure. Because of this it is likely to exhibit different failure modes. This, in turn, means that the established tests for reliability such as those based around the JEDEC standards may no longer offer a fair reflection of lifetime reliability.

In order for GaN to achieve widespread acceptance and credibility in the market for power applications it will be absolutely vital for the industry to identify and support relevant, new reliability standards. Infineon, as one of the most established players in the GaN sector, is pushing for such standards at the same time as providing its own reliability data for its WBG portfolio to ensure that customers understand exactly how devices will operate in real-life applications.

Looking to the future, advances in silicon will ensure that this remains the dominant semiconductor material for at least the next ten years and, in most likelihood, a lot longer. SiC will continue to increase its market share – especially with the availability of SiC MOSFETs raising the benefits from SiC technology to a new level. New solutions supporting energy savings will be realized by the designers in many applications, among them photovoltaic inverters, energy storage systems and chargers for electromobility. And GaN will consolidate its position with respect to RF power and see future growth in more general power switching applications – especially as more robust reliability tests come online.

Within this market, we believe that Infineon occupies a unique position. As a supplier of both silicon and WBG semiconductors, the company is 'material-agnostic' and can take a holistic view when it comes to identifying the optimum solutions for customers in terms of performance, price and reliability. A strong history in silicon means an in-depth understanding of silicon's sustainability and the future possibilities and limitations of conventional semiconductors.

At the same time, the company has well-established and proven SiC and GaN capabilities built up over many years. Infineon will actively improve the cost/performance ratio of WBG technologies and accelerate the market introduction of WBG-based products. Because, after all, we are aiming at making life easier, safer and greener – with technology that achieves more, consumes less and is accessible to everyone.

www.infineon.com/power

Modern Magnetics Design

This article discusses one of the most difficult aspects of magnetics design and analysis: winding proximity loss. Without understanding proximity loss, there is a roadblock to reducing the size of the magnetics components.

By Dr. Ray Ridley, Ridley Engineering

The Size of Modern Magnetics

In the last ten years, tremendous strides have been made in semiconductors to increase the performance of high-frequency power supplies. New wide-bandgap technologies, and new packaging techniques have led to unprecedented levels of power density and converter efficiency. The future for power conversion has never been so exciting.

However, one component has stubbornly continued to defy proportional miniaturization—the magnetics. Invented in 1831, the power transformer remains a larger component than anticipated, and it does not seem to follow any version of Moore's Law.

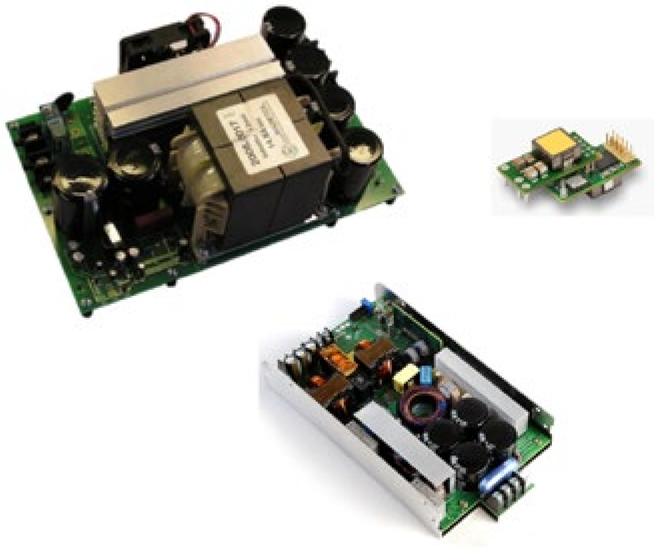


Figure 1: Modern Power Converter Size is Dominated by the Magnetic Components

Figure 1 shows modern power converters for different applications. A PFC circuit, LLC, and a point-of-load converter all feature prominent magnetics. In some cases, we find that the semiconductor devices no longer even need a heatsink and have disappeared from view underneath the circuit board. This emphasizes even more the need to work harder on the magnetics if we are to continue making progress with size reduction.

When starting a series of articles on magnetics design, it is customary to start at the beginning with design basics. Considerations of turns counts, saturation, core materials, and design optimization are usually at the forefront. You can learn more about some of these issues from our magnetics videos [1].

However, in this article, we are going to start with an advanced topic which causes severe problems for many designers. We will see in the example used in this article that conventional analysis of winding loss indicates that there will be just over 1 W of dissipation. However, detailed proximity loss analysis shows that, in reality, there is almost 15 W of power loss.

Forward Converter Design Example

Figure 2 shows an example forward converter running at 360 W. The converter runs at a switching frequency of 100 kHz. We will look at the detailed design of the transformer and show that it demonstrates excessive winding loss, despite initially good performance calculations.

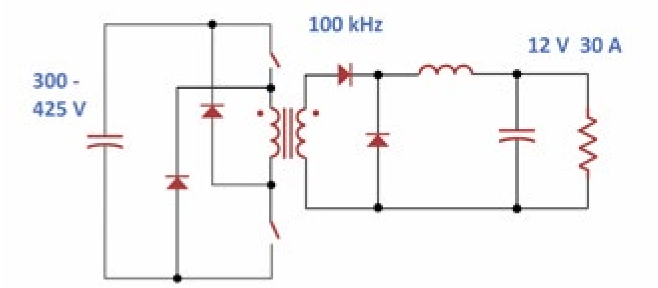


Figure 2: Two-Switch Forward Converter for 360 W Output

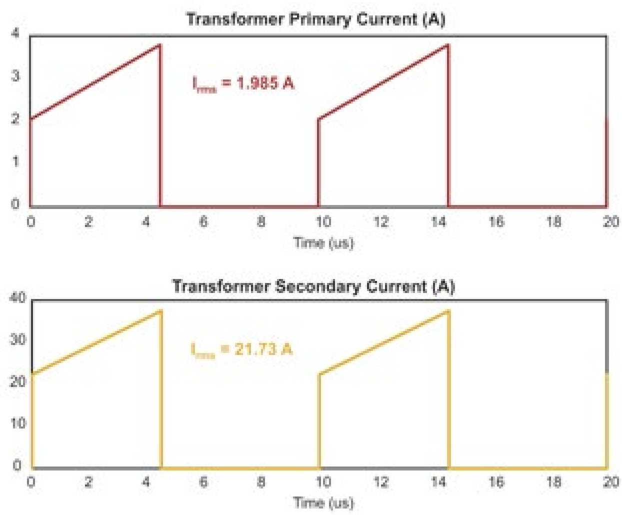


Figure 3: Transformer Currents for the 2-Switch Forward Converter

Figure 2 shows the simulated currents in the transformer [2]. The primary current has a peak almost 4 A, and an RMS value of 1.985 A. Notice that there is a dc component of the current. (This can be a surprise to power supply novices. Transformers are not ac-current devices, they are ac-voltage devices.) There are also ac frequency components at 100 kHz, 300 kHz, and higher order odd harmonics. As we will see later, different analysis techniques can include these ac components to calculate the total winding loss accurately.

The secondary waveforms reach a peak of almost 40 A, with an RMS current of 21.73 A. If you look closely at the waveforms, you may notice that the primary slope is slightly higher than the secondary slope. This is due to the addition of magnetizing current in the primary winding. This component is not seen on the secondary side.

Figure 4 shows the detailed winding construction of the transformer in a cross-sectional view.

The primary is composed of 3 layers of 20 awg wire, comprising a total of 51 turns. The total dc resistance is 97 mOhm, and the calculated rms dissipation is 0.38 W.

Figure 4: Forward Transformer Design Details and Calculated Winding Dissipations

The secondary is wound with 10 mil foil. This results in 0.146 mOhm dc resistance, with a calculated dissipation of 0.69 W. This total dissipation looks really good, and most engineers will be happy to take this to a prototype design for testing in their project.

AC Resistance Calculations

Most engineers in power are familiar with the fact that the resistance of a conductor changes with frequency. Some advanced math, long established, introduces us to the concept of skin effect where currents at high frequencies move to the surface, or skin, of a conductor. Manufacturers of early high-power distribution transformers were painfully aware of this effect when their transformer windings became hotter than expected.

While most engineers are aware of skin effect, very few of them are familiar with proximity effect. (Skin effect is actually a subset of proximity effect.) With proximity, the currents in a conductor do not flow evenly around the surfaces of a conductor. When wrapped in a helix around a core, the currents will concentrate unevenly on the inner and outer surfaces. With multiple layers of windings, circulating currents are produced. This is similar to induction heating, and the losses can become very large.

The mathematics, involving Dowell's famous equations, are very complex for calculating ac resistances. The main body of this work was completed in 1961, and is readily available to all engineers. Due to its complexity, less than 1% of power electronics engineers take advantage of this work.

Figure 5 shows the profound results that arise from properly applying Dowell's equations to the primary windings of the forward converter power transformer. This graph, on a log-log scale, shows the rising resistance of the wire with frequency, plotted from 10 Hz to 10 MHz.

At low frequencies, the resistance is equal to the calculated dc value, 97 mOhms. At around 7 kHz, the skin depth is equal to the thickness of the primary wire, and we see the resistance start to rise at about 2 kHz. At the switching frequency, 100 kHz, the wire thickness is 3.75 times the skin depth. However, we see that the resistance has risen far more than that. It is now 2.42 ohms, or about 24 times the dc resistance.

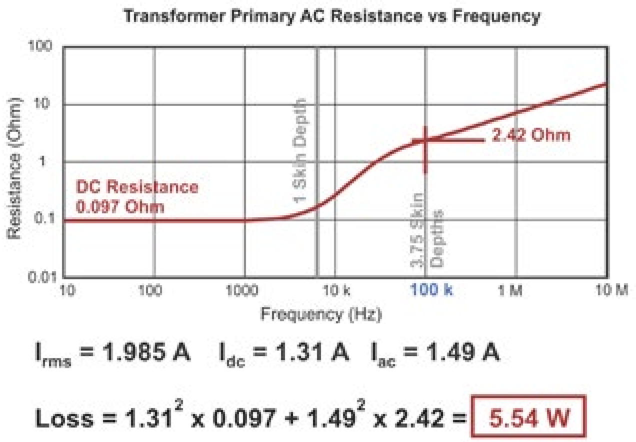


Figure 5: AC Winding Resistance Versus Frequency for the 3-Layer Primary Winding

We can use this information to approximate the total loss in the wire. This is done by taking the dc component of the current, squared, multiplied by the dc resistance. To this we add the total ac current squared times the ac resistance at 100 kHz. The result is an astonishing 5.5 W of loss, while conventional analysis suggests only 0.38 W.

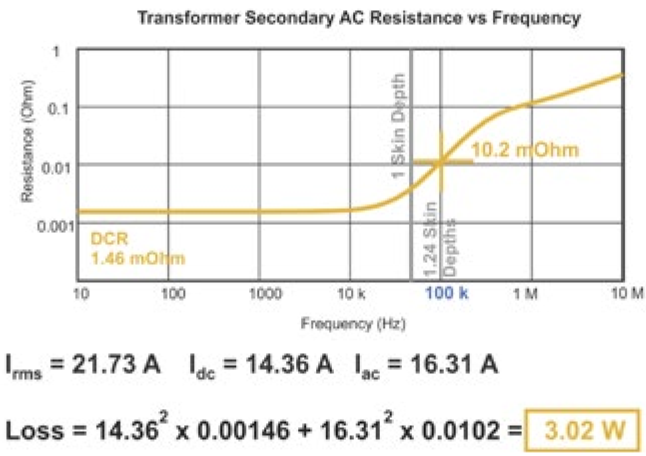


Figure 6: AC Winding Resistance Versus Frequency for the 5-Layer Foil Secondary Winding

We can repeat this process for the secondary winding. Figure 6 shows the ac resistance of the 10 mil foil versus frequency. This is a much thinner winding than the primary, and the skin depth is not reached until we get to about 65 kHz. You can see, however, that the resistance starts to rise well before this frequency, due to the multiple layers of foil. At 100 kHz, the foil is only 1.24 skin depths, but you can see that the ac resistance is about seven times higher than the dc resistance. When we separate the current into ac and dc components, the loss calculates to be about 3 W—almost five times bigger than the calculation without proximity effects included.

Many designers would be misled with this secondary design. An old rule of thumb is that you have to stay below 2 skin depths to avoid problems with your windings. In this case, it doesn't help. The increased resistance is still a factor of five higher than expected.

Circuit Models Reduce Calculations and Increase Accuracy

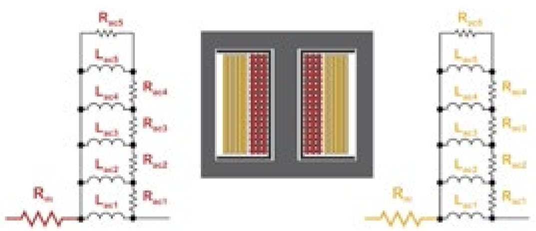
Even though the proximity calculations described so far indicate greatly increased losses, they still fall short of the real circuit losses. This is because all of the ac current is assumed to be at the switching frequency. In reality, there are higher harmonics, and the losses will increase further with the increasing resistance.

The difficult and time-consuming way to solve for the winding loss is to extract all of the harmonics from the current waveforms and to calculate the losses due to each frequency component. However, there is a simpler and more powerful way to do this.

The ac resistance versus frequency plots of figures 5 and 6 can be modeled with R-L ladder networks as shown in Figure 7. A sequence of 5 branches is sufficient to follow the curve accurately from 10 Hz to 10 MHz. These linear circuit models can then be simulated in LTspice, or any other circuit analysis package.

The inspiration for the R-L ladder network is drawn from Dr. Vatché Vorpérian's paper on frequency-dependent core loss [3]. In this landmark paper, he showed how simple circuit models could be used to simulate very complex loss equations, and the same can be done for proximity losses.

The circuit simulation will automatically steer the transformer current through higher resistances at high frequencies, and no calculation of harmonic content is needed. This happens automatically in the time-domain simulation.



Transformer Primary Proximity Model		
Rac1	1.36	mΩ
Rac2	243.10	mΩ
Rac3	3046.88	mΩ
Rac4	6833.99	mΩ
Rac5	22192.73	mΩ
Lac1	42.93	uH
Lac2	42.60	uH
Lac3	31.00	uH
Lac4	9.17	uH
Lac5	2.65	uH

Transformer Secondary Proximity Model		
Rac1	0.00	mΩ
Rac2	0.13	mΩ
Rac3	12.27	mΩ
Rac4	130.62	mΩ
Rac5	290.69	mΩ
Lac1	0.253	uH
Lac2	0.253	uH
Lac3	0.247	uH
Lac4	0.159	uH
Lac5	0.035	uH

Figure 7: Linear Circuit Networks Are Sufficient to Properly Simulate Proximity Losses

Despite the apparent complexity of the winding equivalent circuits, LTspice does not have any trouble in simulating at a reasonable speed. The results are very revealing. As can be seen from Figure 8, the primary winding loss climbs to 8.46 W, and the secondary to 6.27 W. The resulting 14.7 W is far from the initial loss estimate of about 1 W.

Many designers run into this difficulty with their transformer designs. The excess loss greatly lowers efficiency, and the power supply may not meet its specifications. Furthermore, the 14.7 W loss will raise the temperature of the windings significantly, resulting in still higher winding resistance and loss.

Transformer Dissipation		
RMS Calculation	0.38	W
Proximity Fundamental	5.54	W
LTspice Simulation	**8.46**	W
RMS Calculation	0.69	W
Proximity Fundamental	6.02	W
LTspice Simulation	**6.27**	W

Figure 8: Calculated Winding Losses Using RMS Calculation, Proximity with Fundamental Frequency Only, and LTspice Simulation with Full-Frequency Proximity.

Summary

Dowell's equations are essential to arrive at the real dissipation in transformer windings. If these calculations are not done, the magnetics winding loss can be an order of magnitude higher than expected. Most engineers do not make these calculations, however, due to the difficulty in understanding the process. Fortunately, modern software [2] is available to automate the entire process of model generation ready for circuit simulation. All that is needed is a description of the winding structure to generate accurate LTspice models. It is then easier, with any level of experience, to accurately predict dissipation and temperature rise in a transformer.

Even more importantly, a transformer can be redesigned with less layers to improve the dissipation in the windings. This will be illustrated in a future article.

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[5] Join our LinkedIn group titled Power Supply Design Center. Noncommercial site with over 7100 helpful members with lots of theoretical and practical experience.

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Step Up to Half-Bridge GaN Power ICs

Half-bridge circuits are essential building blocks in the power electronics industry, used in everything from smartphone chargers and laptop adapters, to TVs, solar inverters, data centers and electric vehicles.

By Santosh Sharma, Dan Kinzer, Jason Zhang, Marco Giandalia, Stephen Oliver, Navitas Semiconductor

The Ubiquitous Challenge

Operating these half-bridge circuits – i.e. providing power and signal to a floating high-side switch - at very high frequencies can shrink magnetics and enable a dramatic reduction in size, cost and weight while delivering faster charging. However, such frequency increases have eluded the industry for decades as silicon devices have been too slow and suffer from parasitic impedances between the driver, high-capacitance silicon FETs and poorly performing level-shifter / isolators. As a result, most converters still run at 65-100 kHz. From the original opto-couplers, we have seen the introduction of hybrid-technology level shifters (capacitive coupling, inductive coupling) which enabled somewhat higher frequencies but are expensive and inefficient. Finally, lateral monolithically-integrated half-bridge Gallium Nitride (GaN) Power ICs have been introduced to enable a 30x increase in switching frequency.

Figure 1: Broad range of applications using half-bridge power topologies

Scope: Power and Topologies

The focus of this article is on half-bridge applications (Figure 1) with power levels from 20 W to 300 W+, and where 650 V functional (not galvanic) isolation is required to separate the ground-referenced control IC PWM signals from the high-side gate, and allows a switching node typically between 0 V and 400 V bus rail. Extended power range can achieved by the use of full-bridge circuits and interleaving half-bridges.

In topology terms, and for high switching frequency, this includes soft-switching circuits such as active clamp flyback (ACF) (20 W – 65 W), LLC converters (80 W – 300 W), Totem-Pole PFC (>=200 W) and inverter topologies (>=200 W). In response to new regulations such as DoE Level VI and European CoC[1] with tough efficiency standards, combined with the interfacing specifications like USB-Type C, we may also see adoption of 'PFC+ACF' for USB-PD up to 100 W, as 'PFC+LLC" may be limited in output voltage range[2].

As mentioned earlier, high speed (i.e. high switching frequency) power conversion means the opportunity to shrink magnetic circuit elements (transformers, inductors). Many core options are available for 50-500 kHz operation and recent introductions by TDK (N59)[3] and Hitachi Metals (ML91S)[4] are optimized for 1-2 MHz.

Monolithic Integration: High Speed, Small Size and Low Cost

Opto-couplers are large (>50 mm^2) and require separate floating power supplies, plus drivers, FETs, etc. to create a half-bridge, so can be ruled out for high density systems. Similarly, Si-based 600 V half-bridge drivers are limited to ~200 kHz before junction temperatures exceed 125°C so must be excluded. Hybrid-isolators are multi-component modules (Si and SiO_2 or polyimide), and also require separate bootstrap diodes (vertical Si, SiC) and FETs (Si, GaN). This disparate bundling of technology limits speed, increases losses, component count, PCB space and costs. A homogeneous technology platform is the key to high speed, small size and low cost at a component level (Figure 2), and continues to bring benefits at the system level (Figure 3). AllGaN™[5] is the only JEDEC-qualified[6] 650 V lateral GaN Power IC technology, and is used to create monolithic die with integration of driver, logic and FET plus essential high-side functions such as level-shifting, isolation and bootstrap charging.

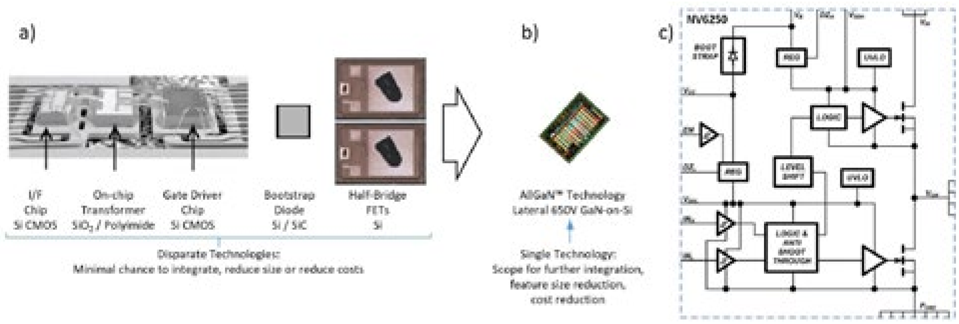

Figure 2: Integration is the key to small size, low cost. a) Multiple technologies: Hybrid isolator / driver with discrete powertrain, b) Homogeneous platform: Lateral GaN-on-Si, NV6250 Half-Bridge GaN Power IC. (Images are representative of technology, not specific die, not to scale).

In a half-bridge converter, there are three losses which are eliminated or minimized by monolithic integration[7] (and are FET size independent):

1. Driver loss - gate driver loop parasitic inductance is eliminated and matched driver-FET current capability means driving losses are negligible over frequency,
2. Bootstrap supply - GaN has low equivalent V_F and zero Q_{rr},
3. Level shifter - extremely fast and low power level shifter allows multi-MHz operations and short propagation delay.

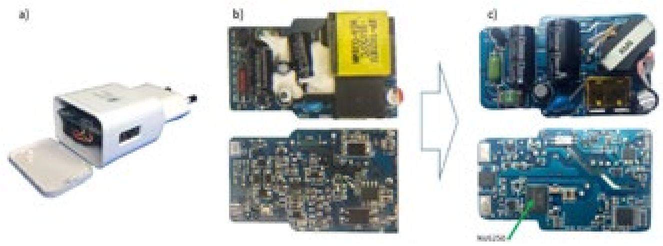

Figure 3: Half-Bridge GaN Power IC enables increase in switching frequency, 66% increase in power density. a) Original 15 W AC charger case, Original 15 W, Si-based QR Flyback, ~100 kHz, c) Upgraded 25 W, Half-Bridge GaN Power IC ACF, ~400 kHz.

High Performance GaN Power ICs

Developed from a prototype demonstrated at APEC 2015, the 650 V-rated NV6250 is the world's first half-bridge GaN power IC, packaged in a 6x8 mm QFN complete with dual drivers, level shifter, dual 560 mΩ power FETs, bootstrap and extensive protection features. Simple, low-power digital PWM inputs switch the half-bridge effortlessly at frequencies up to 2 MHz. The NV6250 offers significant ease-of-use and layout flexibility for the power system designer, and is compatible with a wide range of analog and digital controllers from multiple control IC providers.

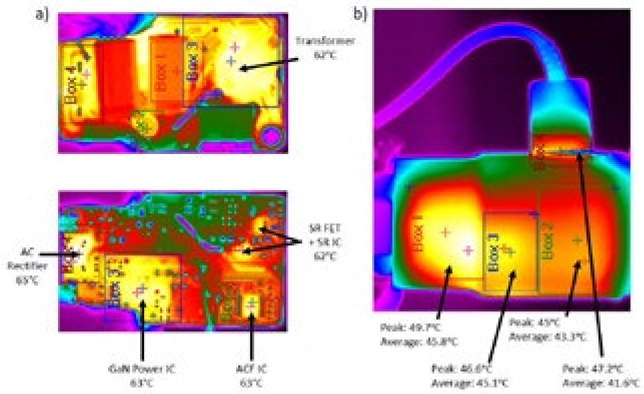

Figure 4: 25 W AC charger – thermal performance. a) No case, 25°C ambient, full load, 90 VAC input, no heatsinking, b) Cased, 25°C ambient, full load, 90 VAC input, no heatsinking.

In legacy discrete systems, the datasheet 'headline' delay is specified from the incoming PWM_H signal to a 10% change in the level-shifter's own output, with no consideration for downstream FET speed (charge), gate resistor, etc. For the half-bridge GaN Power IC, propagation delay is measured from PWM_H signal to a 10% change in high-side FET V_{DS}., i.e. the true, complete 'digital-in, power-out' timing. For the NV6250, the propagation delays are extremely fast – as low as 15 ns.

High Efficiency, High Density Conversion

As smartphone customers demand more features like Quick Charge™ [8] with "5 hours of talk time in 5 minutes of charging", this increases maximum charging current, so more power is needed but with a parallel goal to maintain the charger case size – i.e. increase power density - and limit costs.

A benchmark 15 W Si-based smartphone charger is shown in Figure 3. Moving to 25 W with the same low frequency, quasi-resonant (QR) flyback topology and no increase in efficiency means a 1.4x increase in case size. Using the soft-switching ACF topology[9] and with only a small increase in switching frequency to 400 kHz, yields a 25 W NV6250-based solution *in the original case* – a 66% increase in power density.

As size is reduced, efficiency must be increased to maintain a constant external case temperature. OEM specifications vary in the maximum allowable case temperature but there are cases where the limit is only 50°C (average over a 2x2 cm area). Here, to achieve the temperature rating, the system efficiency required an upgrade from ~89% to >92%.

Higher Powers, Higher Frequencies, Higher Performance

The AllGaN platform offers great flexibility for additional features / functions and also in alternative die sizes to optimize $R_{DS(ON)}$ for specific application power levels. MHz-switching topologies have been implemented from 25 W to 3 kW using DSP controllers. New, faster ASICs will come to market during 2017 to increase switching frequencies beyond the example 400 kHz – and so further reduce sizes – for high volume, cost-sensitive, consumer applications. By integrating the critical level-shifting, bootstrap and dual drive functions, all in GaN, the half-bridge challenge has been met and the path to MHz high-voltage power systems has been cleared.

(Endnotes)

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Dry Film Capacitors for High-Frequency Power Electronics

Dry plastic-dielectric (film) capacitors offer high-reliability and low-loss characteristics desirable in power electronic applications. They offer tight capacitance shift versus temperature and frequency, lightweight, no oil or electrolyte, and flexible packaging options.

By Joseph A. Bond, President & Director of Engineering, Electronic Concepts, Inc.

They are efficient and cost effective, and metallized film capacitors offer self-healing leading to soft failure modes over a long service life. Film capacitors are particularly well suited to high power applications in low to medium voltage markets.

Power electronic applications include voltage transient snubbing, coupling and decoupling, DC links, feed-through and EMI line filters, and inverter AC output filters. The industry is continually evolving to increase energy density, reliability, and efficiency while decreasing size, weight, and cost. The days of throwing bulk capacitance at applications as an afterthought of the design are long gone. Film capacitor designers use a toolbox of materials and techniques to optimize the capacitor performance characteristics for a given application. Capacitor designers must develop innovative materials, construction technologies, and packaging methods complementing the state-of-the-art in power circuits.

This article discusses the requirements for power capacitors in systems seeking advantage in state-of-the-art high-frequency designs. Comparison of system design versus capacitor design approaches highlight the advantages of each approach discussed. ECI power capacitors designed specifically to meet the challenges of increasing switching and harmonic filtering are presented.

Background

Wide band gap (WBG) materials for power electronic semiconductors increase switching, harmonic, and EMI frequencies. Capacitors used in high-frequency applications must meet the increased performance requirements relative to the increased bandwidth of frequencies. Higher frequencies have positive influence on reducing the capacitance needed for hold-up energy in filtering applications; however, the capacitors require lower ESL and ESR with increased resonant frequency. The system requirements challenge traditional capacitors using solid leads in these applications due to higher ESL and skin depth limitations of lead surface and cross sectional conducting area.

Electronic Concepts Inc. (ECI) is a vertically integrated capacitor manufacturer with unique capabilities including advanced plastic-dielectric manufacturing, metallizing and converting, state-of-the-art machine shops, materials research labs, and environmental and performance testing labs. These capabilities allow the development of innovative film capacitors delivering advantage to customer systems. ECI provides power designers the ability to realize optimal performance in systems employing the latest circuit components and technologies.

High-Frequency Design Concerns

The circuit designer and capacitor designer have methods to address certain aspects of operating at higher switching and harmonic frequencies. The general principle is to cancel the ESL of capacitors through mechanical configuration of opposing current flows, and increase conductor surface area relative to skin depth and operating bandwidth. Understanding those comparative approaches allows the circuit designer to choose the correct combination of circuit and capacitor designs to optimize performance and cost. It is also essential to understanding capacitor specifications, and the impact of specification requirements on capacitor design and cost.

Skin Depth

Current flows along the surface of a conductor at a depth relative to frequency referred to as skin depth. Figure 1 shows skin depth δ around the perimeter of round and flat conductors. Skin depth is the effect of increasing conductor resistance by decreasing conducting depth as frequency increases. As skin depth decreases, the conducting cross sectional area decreases, and the effective AC resistance of the conductor increases. The capacitor terminations and internal conductors must provide sufficient surface area for the best performance. At high frequency, typical solid lead wires can exhibit increased resistance and heating. The capacitor designer can provide multiple leads or flat copper conductors to offset skin depth. Conductor current required defines the cross sectional conducting area needed to prevent overheating. The proper conductor design results when the DC and AC resistance of the conductor are equal at the required frequency. In general, the conductor should operate at full current rating up to the resonant frequency of the capacitor.

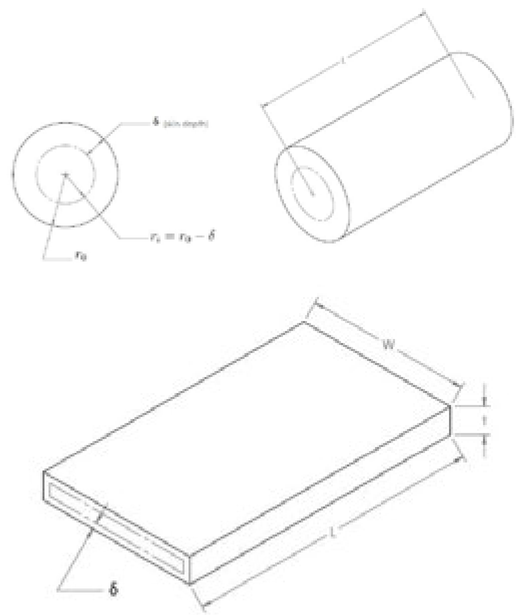

Figure 1: Skin depth δ around the perimeter of the conductor in round (top) and flat (bottom) conductors.

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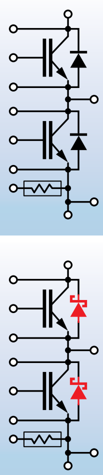
TECHNOLOGY		V_{CE}	I_C	V_{ISO}
All Silicon Module Si-IGBT & Si-Diode		1700 V	1000 A	4.0 kV
		3300 V	450 A	6.0 kV
Hybrid Module Si-IGBT & SiC-Diode (Hybrid SiC)		1700 V	1000 A	4.0 kV
		3300 V	450 A	6.0 kV

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Table 1 shows the equation for skin depth calculation as
$\delta = \sqrt{\rho / (\pi f \mu)}$.
As the resistivity of the conductor increases for different metals, the skin depth required increases. Figure 2 shows the skin depth of copper and aluminum conductors versus frequency in thousandths of an inch (mils). At 1 kHz the skin depth of copper is approximately 87 mils, at 100 kHz it decreases to less than 9 mils, and again to less than 3 mils at 1 MHz. The skin depth must be less than the radius of a round conductor or half the thickness of a flat conductor to maintain low resistance at high frequency. The threshold or crossover maximum frequency occurs when the skin depth equals the radius or half thickness. Above this threshold frequency, the conductor will get hotter as the conducting cross section is insufficient and the resistance increases. The resonant frequency of the capacitor must be less than the threshold frequency.

Symbol	Description	Units	Equation/Note
ρ	Resistivity of conductor at temperature T	$\Omega \cdot m \times 10^{-8}$	$\rho(T) = \rho_0[1 + \alpha(T-T_0)]$
ρ_0	Reference resistivity of conductor at temperature T_0	$\Omega \cdot m \times 10^{-8}$	
α	Temperature Coefficient of resistivity	1/°K	
μ	Absolute magnetic permeability of a conductor at temperature T	H/m	$\mu = \mu_0 \times \mu_r$
μ_0	Permeability of free space at T_0	H/m x 10^{-6}	$\mu_0 = 4\pi \times 10^{-7}$
μ_r	Relative magnetic permeability	None	Vacuum = 1
T	Conductor temperature	°C	
T_0	Reference temperature for ρ_0 and μ_0	°C	
f	Ripple frequency	Hz	
σ	Conductivity (inverse of resistivity) in Siemens	S/m x 10^{7}	$\sigma = 1 / \rho(T)$
π	Relationship of a circle's circumference to it's diameter	None	π = Circumference / Diameter
δ	Skin depth of conductor based on AC frequency	mm	$\delta = \sqrt{\rho / (\pi f \mu)}$

Table 1: Equations and variables of skin depth calculations

As the ESL of the capacitor decreases, the resonant frequency increases. The capacitor designer must increase the surface area of the conductors until the total cross sectional conducting depth is sufficient to maintain low resistance over the extended operating bandwidth. Multiple leads per capacitor termination, hollow bushings, tubes, flat foils, or tab conductors are typical methods. All ECI capacitors intended for high frequency operation like resonant capacitors, snubbers, feed-through capacitors, and EMI filters employ these increased surface area conductors for terminals and internal construction.

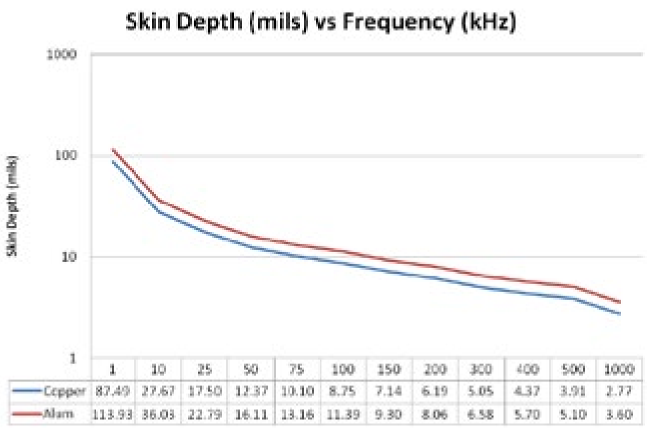

Figure 2: Skin depth versus frequency for aluminum and copper conductors

Circuit Strategies

Increasing switching frequency decreases the capacitance required as a function of acceptable voltage deviation and capacitor self-resonant frequency. In lower power applications, a double-sided PCB with multiple parallel capacitors arranged for equal and opposing current flow provides inductance cancellation at board level. This method uses lower cost standard box or wrap and fill capacitors. The double-sided PCB provides further inductance cancellation and the result is a low ESL apparent to the circuit. Figure 3 shows a snubber circuit using this technique.

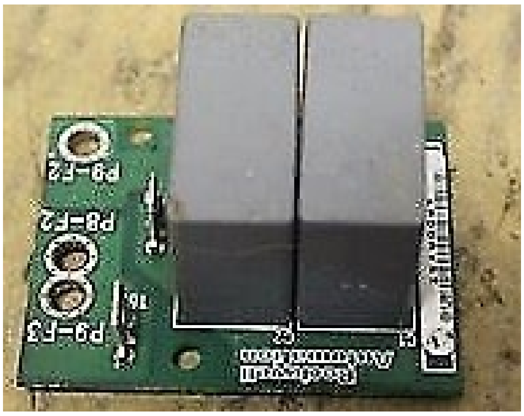

Figure 3: Snubber circuit with reversed current flow in box capacitors

This approach however requires higher component count and the additional cost of the PCB and assembly. In high power systems, it may be more cost effective to use larger power capacitors designed and manufactured to provide low ESL as a standalone module. The choice of which strategy to employ depends on a cost-benefit analysis at the system level.

Tools Available to the Capacitor Designer

Designing film capacitors for high-frequency applications requires the capacitor designer to employ mechanical techniques of winding geometry and assembly cancellation technologies. Plastic dielectric capacitors are rolled windings of two or more dielectric layers. Figure 4 shows the components of a wound capacitor including the fixed inactive aspects of margin and offset. The area required to provide the needed capacitance dictates the length of dielectric rolled into the winding. By decreasing the material width, the fixed inactive aspects of the winding decrease the volume efficiency. However, narrower material widths increase the peak and RMS current capacity.

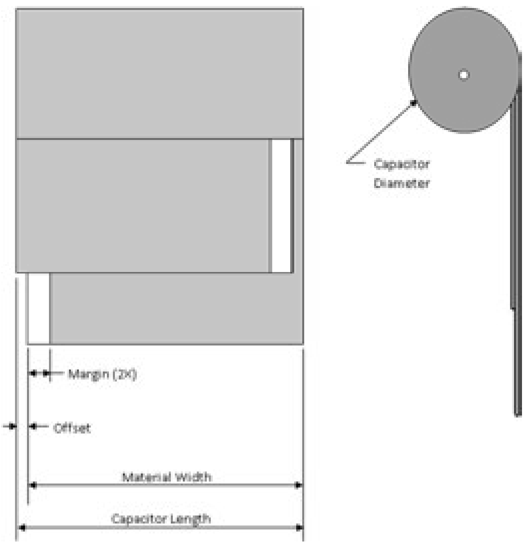

Figure 4: Components of a wound capacitor

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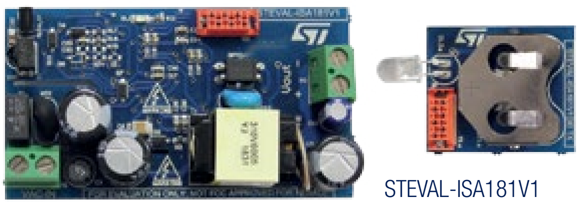
Evaluation board	Core product	Description	Standby consumption (mW)	Input voltage (V_{AC})	Output voltage/current (V/A)	Output power (W)
STEVAL-ISA181V1	VIPER0P STM32	Non-isolated flyback with zero-power standby and remote control	5	85 - 265	12 / 0.5	6
STEVAL-ISA177V1	VIPER01	Non-isolated flyback converter	10		5 / 0.8	4
STEVAL-ISA178V1	VIPER01	Buck converter	20		5 / 0.2	1
STEVAL-ISA180V1	VIPER0P	Isolated flyback converter	17		12 / 0.5	6
STEVAL-ISA182V1	VIPER38	30 W peak power isolated flyback converter	25	85 - 132	12 / 0.7 2.5 A for 10 ms	8.5 30 peak
STEVAL-ISA175V1	VIPER26	Ultra-wide input voltage isolated flyback converter for smart meters	30	85 - 440	16 / 0.5 5 / 0.1 3.3 / 0.2	9.5
STEVAL-ISA171V1	VIPER35	Quasi-resonant isolated flyback converter		90 - 265	12 / 1.25	15
STEVAL-ISA081V1	VIPER26	All primary side flyback converter	45	85 - 265	12, 3.3 / 1	12



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Capacitor Geometry

The geometry of the rolled capacitor winding greatly affects the peak and RMS current capacity, and reliability as a factor of thermal performance. Capacitor windings with a high diameter to length ratio (narrow dielectric width wound to a large diameter) perform better than capacitors of a low ratio (wide dielectric width wound to a small diameter). Certain aspects of the wound capacitor are fixed such as the inactive margin and offset necessary to provide voltage clearance and metal end spray connection. Long thin capacitors have better volume efficiency but worse thermal performance then short fat capacitors due to the fixed aspects as a percent of the capacitor length.

Since capacitance is only a factor of active area for any given voltage, the capacitor designer selects the best dielectric width providing the optimal ratio of performance to volume efficiency. Table 2 shows a comparison of capacitor performance parameters as a function of dielectric material width. The dielectric thickness is five micron, and only the dielectric width varies between 50 mm and 100 mm. Capacitor windings without ESL cancellation techniques have an inherent inductance of approximately 14 nH per inch of capacitor length.

5µm BOPP Dry Film Capacitor Winding		
Capacitor Parameters		
CAP (µF)	100	100
DIELECTRIC (FILM) WIDTH (mm)	50	100
FIXED MARGIN / OFFSET WIDTHS (mm)	5 / 1	5 / 1
CORE DIAMETER (mm)	9	9
CAPACITOR DIAMETER (in)	2.601	1.744
DIAMETER:LENGTH RATIO	1.30 : 1	0.44 : 1
CAPACITOR SURFACE AREA (in^2)	26.8	26.4
CAPACITOR VOLUME (in^3)	10.7	9.5
ESR (Ω at F-res)	0.00206	0.00929
PEAK CURRENT I-pk (Amps)	3,256	1,427
DV/DT (V/µs)	32.6	14.3
RMS CURRENT AT 45°C AMBIENT (AMPS)	53.7	21.3
RMS CURRENT AT 85°C AMBIENT (AMPS)	34.6	13.7
THERMAL COEFFICIENT R_{th} (°C/W-dissipated)	8.20	11.60
ΔT AT 20 AMPS, 40 kHz	6.8	43.1
HOT SPOT IN 45°C AMBIENT	51.8	88.1
PROJECTECD LIFE AT HOT SPOT (Hrs.)	636,838	51,439
ESL & F-res - Standard Commercial Design		
ESL (nH at F-res)	28.1	55.7
RESONANT FREQUENCY F-res (Hz)	94,914	67,455
ESL & F-res - Low ESL Construction		
ESL (nH at F-res)	5.0	10.0
RESONANT FREQUENCY F-res (Hz)	225,079	159,155

Table 2: Comparison of 100 µF windings at 50 mm and 100 mm dielectric widths

The comparison shows when the material width is halved, the resonant frequency increases 42% from approximately 67 kHz to 95 kHz. The power advantages of half the material width are also apparent. The ESR drops 78% from 9.29 mΩ to 2.06 mΩ, and the peak and RMS current capacity more than doubles. The lower ESR and thermal coefficient result in much less internal heating and over a magnitude increase in life projection. The plastic dielectrics used are organic and follow the 10°C rule where every 10°C decreases doubles the life. Furthermore, using construction techniques, the ESL drops to 5-10 nH, and the resonant frequency more than doubles, thus increasing the operational bandwidth significantly.

ECI Design Strategies

ESL and ESR of a capacitor are functions of geometry and mechanics employed by the capacitor designer. The geometry of the capacitor winding influences the peak and RMS current capacity as well as loss factors like ESR as shown previously in the Table 2 comparison. ECI design methods for low-ESL high-power film capacitors include concentric winding, wide copper terminations, integrated laminate buss structures, conductor shielding, and internal current reversal in winding arrays.

Figure 5 shows a concentric wind. ECI has the ability to wind one discrete capacitor over another on various open cores. A barrier layer of insulation film separates each capacitor in the winding. Several configurations are possible including individual capacitors isolated from each other, parallel connected for higher capacitance, or series connected for higher voltage and corona inception. For each configuration, the terminations and internal connections reverse current direction through each capacitor in the winding. This forms a true coaxial winding effectively cancelling the inductance of the completed unit. Double or triple concentric wound capacitors are possible on open cores ranging from 9-38 mm diameter. ECI provides additional cancellation techniques for the terminals exiting the package to realize ESL down to 5 nH as provided in the LH3 product series, and optionally offered in UL3 and MP3 DC link series.

Figure 5: Triple concentric winding of a true coaxial capacitor

Figure 6 displays a few of ECI capacitors series using some of the various techniques discussed.

Figure 6: MP88 series Low ESL snubbers (top left), 5PT46 series board-mount resonant capacitors (top right), UP38 series low ESL board-mount ripple filters (bottom left), and LH3 low ESL DC links (bottom right).

Understanding Capacitor Specifications

Many times specifications given for capacitor performance reflected in literature are “in circuit” assuming the use of certain board-level inductance cancelling practices. For instance, board mountable DC links with multiple leads are stated by some manufacturers as having very low ESL below 10nH. These units consist of multiple independent capacitors and lead pairs packaged into a single housing, but require the circuit designer to use a PCB design reversing the current flow through each of the individual capacitors. The user should verify if the specification is the standalone component ESL or the installed in circuit ESL.

A capacitor design incorporating multiple discrete insulated capacitor windings into a single housing with multiple lead sets exiting the package facilitates board soldering. Each lead set is a separate capacitor isolated from the others in the package but paralleled tightly together. The circuit PCB design then connects the parallel capacitors forming a single apparent capacitance to the circuit. If the PCB design reverses current direction through each capacitor in the package, the minimum effective capacitor ESL occurs. The net effect is realizing the total bussed capacitance and the minimum circuit ESL. However, if the PCB design simply busses all of the leads together on each side of the capacitor package, the resulting ESL is much higher as the individual capacitor currents couple by flowing parallel in the same direction. The double-sided PCB has cancellation affects that may mask the capacitor ESL at board testing, but the capacitor itself will not function as desired with increased resonant frequency and operational bandwidth.

Electronic Concepts offers product series addressing either board level cancellation by the user or as packaged assemblies. A wide range of terminal alternatives offered allows the user to choose single leads, multiple leads, multiple pins, flat terminals for solder or bolt down options, or units incorporating coaxial windings with laminate busses into the package with bolt down, or bolt through options. ECI capacitors meet very low ESL specifications as standalone devices through specific winding and internal cancellation techniques. The principles of coaxial design and laminate buss structures employed by ECI capacitor designers provide low ESL capacitors with high resonant frequency. ECI capacitor specifications represent the standalone values without additional system level cancellation practices.

The consideration for the circuit designer is which approach is most cost effective. The designer may choose to design the PCB to provide parallel bussing and inductance cancellation. Alternatively the designer may use a capacitor specifically designed and manufactured to provide inductance cancelling internal to the package. As the capacitance and current requirements increase, larger capacitor modules designed for high frequency operation are more cost effective. At a system level, buss work is minimized, and the low component count increases reliability and decreases installation labor.

Summary

Advances in wide band gap materials for semiconductors deliver higher switching, harmonic, and EMI frequencies. Capacitors used for snubbing, ripple filtering, and resonant applications must meet the demands of new power circuits. Decreasing capacitor ESL and increasing resonant frequency allows the capacitors to operate over a higher bandwidth. The capacitor designs must account for conductor heating resulting from insufficient cross-sectional conducting area due to skin depth at high frequency. Choosing the capacitor technology providing the optimum combination of cost and system performance is a user choice of system and capacitor design options.

Electronic Concepts Inc. is a vertically integrated capacitor company designing and manufacturing dry plastic-dielectric capacitors meeting the challenges of high-frequency power applications. ECI internal research and development efforts develop technologies delivering system performance advantages of low power loss over a high operating frequency range. ECI product lines range from axial leaded board mountable capacitors to sophisticated low ESL designs incorporating cancellation techniques of coaxial winding and laminate buss structures giving power system designers optimum performance and value.

ECI engineering will work with system designers to provide the best design solutions for each requirement. Contact us with your design challenges and we will recommend the correct product series or design a specific solution delivering the best performance and value for your application.

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Operation of and Power Silicon for Cascade Cell Based MV Motor Drives

For standard low voltage (≤690Vac) motor drives the IGBT based voltage source 2 level topology dominates the landscape. However at higher voltages (≥2400Vac) the situation changes and there is a plethora of different topologies, each one with unique technical and/or economic advantages. One of these topologies, often referred to as cascade, or Cascade H Bridge (CHB), has increased in popularity in recent years. This article will explain the basic operating principles of the CHB drive and showcase some new power modules matched to this type of converter.

By David Levett and Tim Frank Infineon Americas with Márcio Sari WEG, Uwe Jansen and Klaus Vogel Infineon Germany

Introduction

For Medium Voltage Drives (MVD's), there are several competing technologies: three level Neutral Point Clamp (NPC) type 1 using high voltage power modules (1), current source designs using reverse blocking semiconductors (2), five level T type (3), and Modular Multi-Level (M2L) (4), to name some of the more common types available today in the market. The history of the CHB topology is that it was invented in the early 1970's but first commercially brought to the market by Robicon USA (now owned by Siemens) in the early 1980's. In recent years numerous companies have introduced CHB based MVD's. The overall topology of one phase is shown in Figure 1 and a more detailed schematic for an individual cell in Figure 2.

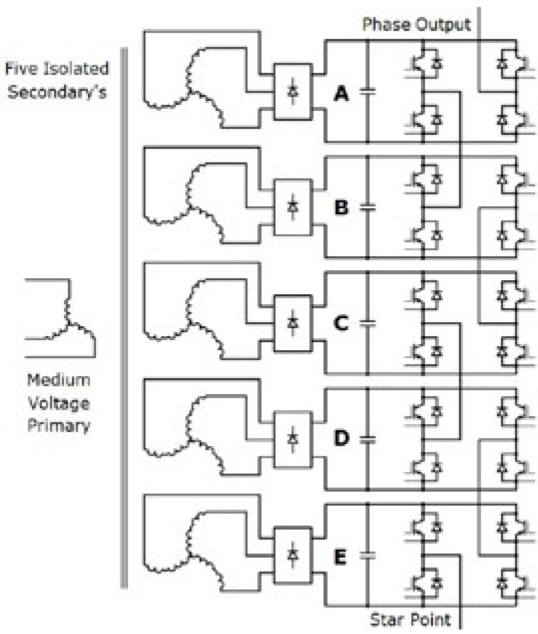


Figure 1: Overall schematic of one phase of a 5 cell per phase CHB converter.

Cascade Topology

The key to the cascade topology is a multiphase isolation transformer, see Figure 1, here shown with a medium voltage primary and 5 isolated secondary windings, in this example each rated at 750 Vac. Each transformer secondary powers a single cell and the 5 cells are "daisy chained" together in series to make a complete phase. Two other phases are used to build a complete three phase drive with a total of 15 isolated secondary windings. See Figure 4.

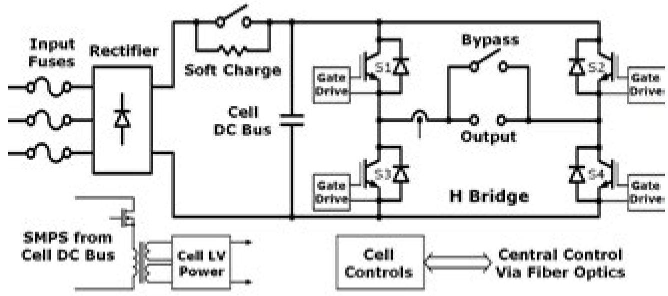
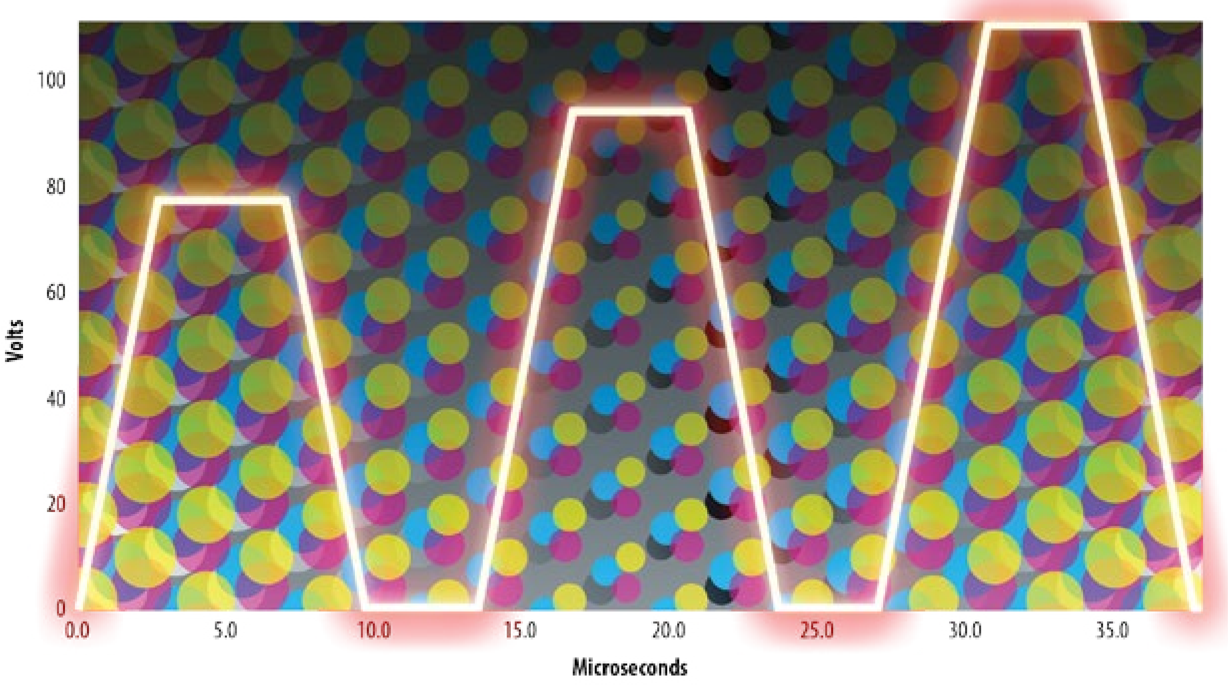


Figure 2: Example of a typical CHB cell schematic.

The detailed schematic of a typical cell is shown in Figure 2. It comprises of:

- A three phase input uncontrolled rectifier with a circuit to provide "soft" charging of the capacitor bank when the main power is applied. Note this soft charging can be performed with a separate winding on the main transformer, this allows the drive to be "control powered" without the grid three phase medium voltage being applied to the primary of the transformer.
- A capacitor bank to smooth out the rectified waveform and create a stable DC voltage source supply.
- An "H bridge" using 4 IGBT's and anti-parallel diodes. These can be switched in sequence to apply either positive, zero or negative voltage to the output terminals and the total phase voltage is the sum of the voltage of all 5 cells.



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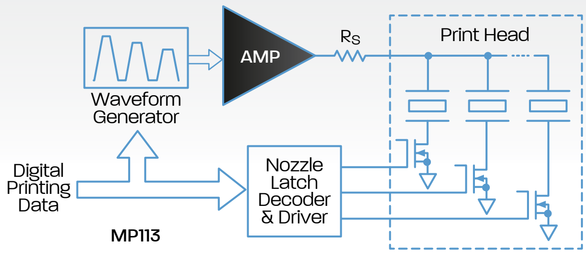

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- The low voltage supplies required for the gate drivers and controls can be generated locally using a SMPS powered from the DC bus. Control signals to and from the drive central controller are via fiber optic cables for voltage isolation. This allows the complete cell electronics assembly to “float” with respect to earth potential.
- The heat sink cannot be connected to earth potential as the IGBT modules and other components do not have the required isolation rating. Typically the heat sink is connected to either to an artificial center point of the DC bus or to the DC negative bus, often using a low ohmic resistor to damp out any potential high frequency oscillations. For liquid cooling it is required to use deionized water to prevent leakage current and electro corrosion and deposition effects. An alternative is to use phase change cooling (5).

Figure 3a shows a typical converter with transformer and 18 cells. Figure 3b shows an individual cell.

Figure 3a: MV3000 a 4160Vac 1500hp drive from WEG. Switchgear and transformer on the left and 18 cells (shown in detail in Figure 3b) in the center.

Figure 3b: Air cooled cell showing rectifier modules (black) in the center and 62mm modules(white) on the right and left.

Advantages
- From Figure 2, it can be seen that the power cell design is very similar to a standard AC drive except that only two half bridges are used. This allows for the use of components that are manufactured in high volume for lower voltage converters.
- Modular design allows for flexibility, as the output voltage can be increased by adding more cells and transformer windings.
- Cells can be bypassed to allow for redundancy. See Figure 4. If one cell is inoperable for any reason, it can be shorted out using a bypass switch, see Figure 2. This switch can be mechanical or semiconductor based using a pressure contact technology based thyristor module. As long as there is some voltage margin, the drive can still operate either in an unbalanced condition, or by also shorting out one cell on the other two phases, in a balanced condition.
- Very low input harmonics as the transformer secondary windings can be phase shifted using, for example, a zig zag transformer design.
- Motor current harmonics are very low and the dv/dt applied to the motor windings is reduced. The H bridge operates at low switching frequencies typically 500Hz – 1kHz as the number of cells multiplies the effective switching frequency seen by the motor windings.
- Simplified maintenance as the individual cells can be light enough to be handled by two people and made pluggable, see Figure 3b. Also as each cell is identical it reduces spare parts inventory.

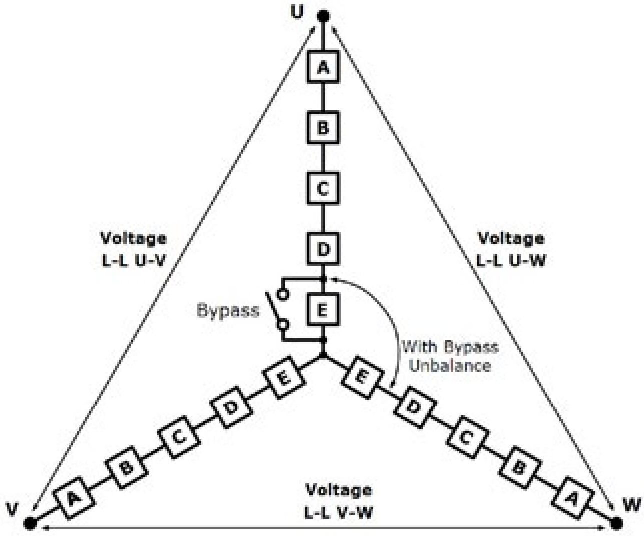

Figure 4: Three phase system and showing unbalance with one phase being bypassed.

Disadvantages
- The transformer is large and complex. See Figure 3a.
- Cells need to be isolated from each other and ground. This adds mechanical complexity and size to meet clearance standards.
- Requires a high value of smoothing capacitance due to the single phase operation of the cell H Bridge.
- More complex liquid cooling.

Switching Pattern

The H bridge can be switched to generate three different voltages at the output, for a positive voltage, S1 and S4, see Figure 2, are turned on, for a negative voltage S2 and S3 are turned on. For a zero voltage state, either S1 and S2 or S3 and S4 can be turned on.

In the simplest mode of operation the output sine wave can be built up by, for example, firing each cell on in sequence with Cell E first, then D all the way up to A with each step increasing the output voltage by ≈1000 VDC and PWM switching used at each level to shape the waveform to a sine wave. This is referred to as a level shift modulation, but it has the drawback that the power semiconductors in each cell do not see equal losses and the transformer windings do not draw equal current which does not minimize the input harmonic currents.

Another method, referred to as angle or phase shift modulation, is shown in Figure 5, and does create equal losses across the cells. The pattern uses a standard common sine wave reference for all cells, but phase shifts the PWM reference by a factor of the number of cells divided by 180°, in this case with 5 cells, 36°. This staggers the PWM patters and prevents two cells switching at the same time, it also shares the zero voltage states equally between the two possible choices. Figure 5 shows the phase shift between cells A and D at 3 x

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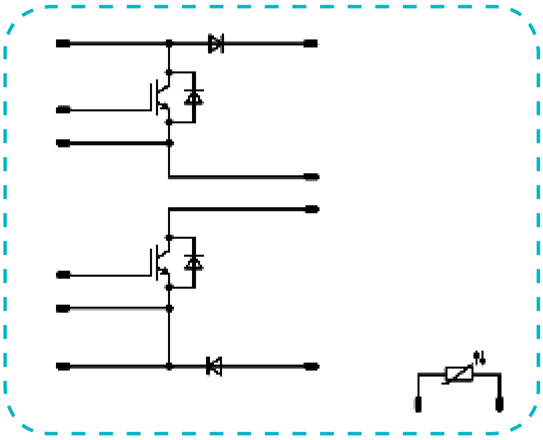

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36 = 108°. Now as with regular drives there are numerous nuances of PWM pattern generation, such a space vector modulation, all with targeted technical advantages.

Loss Calculation

The losses are dependent on the type of switching pattern used. However a simple approximation to the losses can be made using an on line tool such as the Infineon's Iposim, and estimating the losses assuming a single phase operation. A rough "rule of thumb" is that at a 60Hz fundamental output frequency, 1 kHz switching frequency on an air cooled heat sink the IGBT modules should be capable of an RMS output of 0.6 - 0.7 x DC current rating of the module. So for a 300A module the RMS current can be ≈ 180 – 210 ARMS.

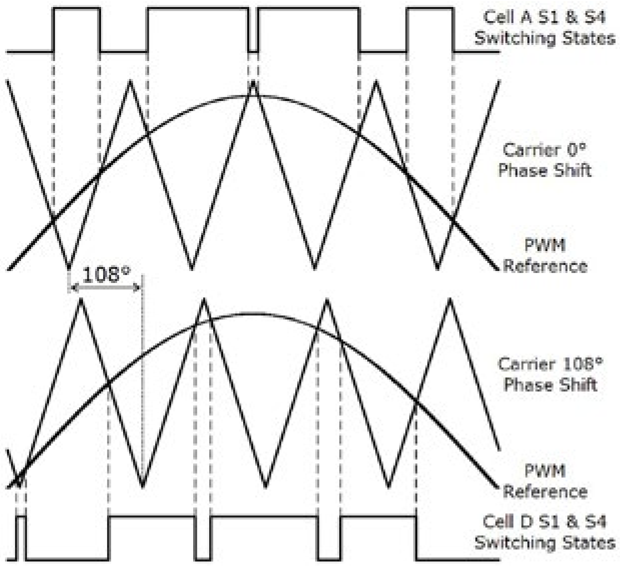

Figure 5: Angle or phase shift cell switching pattern for a half positive sine wave.

Power Silicon Options

For the three phase rectifier standard 20mm, 34mm and 50mm dual diode modules are available in both solder bond and pressure contact technology. See Figure 6.

Figure 6: Infineon 20mm, 34mm and 50mm Rectifier modules.

For the H bridge, 1700V IGBT's devices are often selected as this allows a higher cell voltage, up to a maximum of ≈1200Vdc enabling fewer cells in series. At the same time, 1700V silicon and peripheral components such as rectifiers and bus capacitors are readily available due to their use in 690Vac rated drives. Infineon has increased its portfolio of IGBT modules in industry standard packages to match the requirements of CHB drives as shown in Figure 7. Dual modules in the 62mm or EconoDUAL™3 packages are available up to 600A and complete H bridges, for a more compact design, are available in the EconoDUAL™3 and Econo 3 packages. The later suitable for PCB based designs using press fit technology.

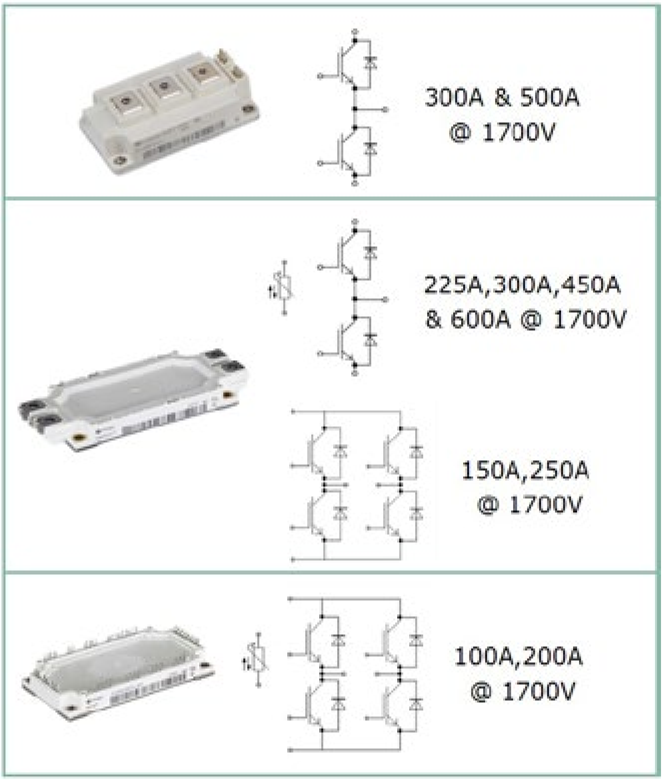

Figure 7: Modules options offered by Infineon tailored for a cascade cell H bridge.

Conclusion

For the power electronics design engineer, the use of a CHB topology has provided a lower technical entry point into the MVD market by utilizing the basic power converter components manufactured in higher volume for the lower voltage converter market. This and the performance advantages listed have fueled the growth of this topology in the MVD market.

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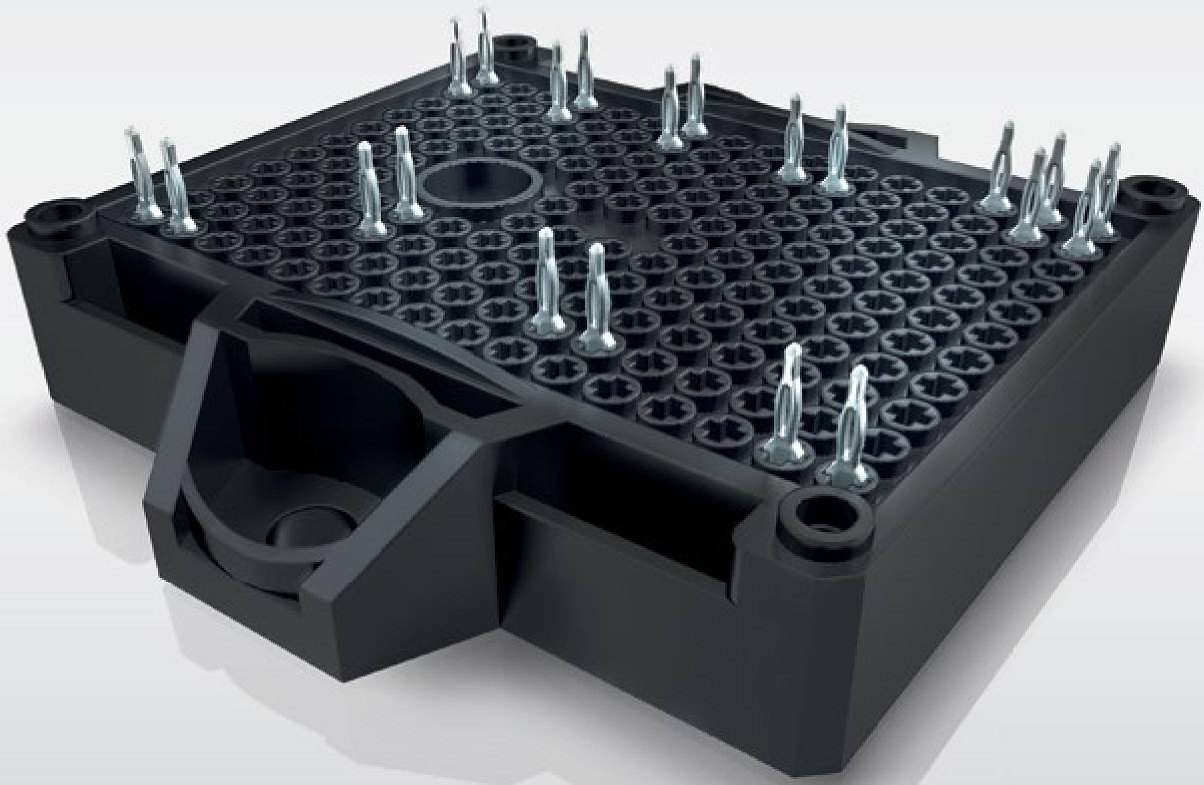

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Powerful Simulation Tool

Fuji IGBT SIM 6 – with X-Series IGBT

By Daniel Hofmann, Assistant Manager - Application Engineering; Fuji Electric Europe

During the development of a power converting system (PCS) commonly highest efficiency is required. Consequently preliminary studies are necessary in order to predict the generated system loss. As the IGBT power module is one of the key components of a PCS it gains special focus in terms of analysis and predictions. Of course, predictions and simulation results need to be confirmed by measurements of the complete system but helps to save development time and provides first indications of the performance of the chosen power module.

The new loss and temperature simulation tool FUJI SIM 6 combines powerful functions and a high degree of accuracy of IGBT modules utilizing the latest chip generation – X-Series.

Fuji Electric's X-Series power semiconductors achieve higher current density and a shrink in die size leading to powerful IGBT modules for the power electronic market by the increased power density.

Fuji Electric's semiconductors cover a wide range of power from 15A up to 3600A available in different voltage classes with particular attention on 600V/650V, 1200V, 1700V and 3,3kV.

The scope of application is fairly diversified such as white goods, small drives, drives, photovoltaic, wind power and traction etc.

The stand-alone operation of the software avoids an installation of the software to your operating system. A simple double click starts the simulation tool. The user interface of FUJI SIM 6 is well-arranged and kept simple for easy applicability. A total of four tabs provide the prospects of selecting a power module, performing static simulations or dynamic simulations and amending the heat sink to define the thermal conditions.

Module Selection

There are several ways to select a power module. The user can rather select the module by its name by clicking on the drop down menu "Module Name". A list of all available products appears. The number of eligible power modules is quite high so that it is helpful to define attributes such as current and voltage rating in advance. Additionally the desired chip technology or module topology can be preselected as well. In Figure 1 the 7th generation PIM (Power Integrated Module) in a common package with the dimensions of 62x122mm was selected. A PIM configuration combines a 3-phase rectifier bridge, break chopper circuit and 3-phase inverter bridge utilizing the Fuji's latest chip generation.

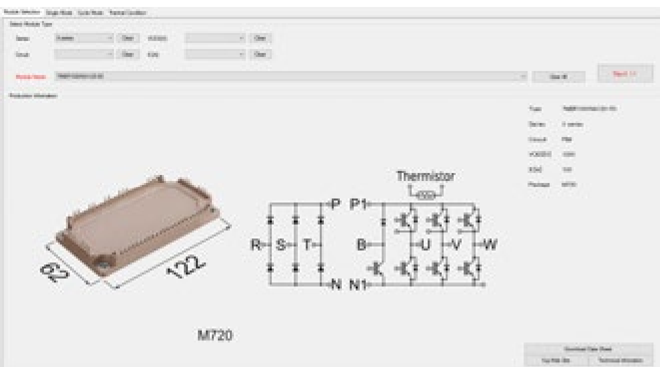

Figure 1: Module selection

Single Mode

After selecting a power module the simulation parameters must be predefined in the "Single Mode" tab (figure 2). The single mode describes a static operation point of the running system und regular condition.

First make sure what kind of circuit topology will be simulated. Not only a 3-phase 2-Level inverter circuit is available but also DC chopper mode and 3-Level I-type configuration is available. In this case, 3-phase 2-Level and DC chopper mode can be selected. The chosen circuit is displayed in the **"Explanation"** area of the interface. For convenience a fixed **heat sink temperature** can be defined. If more detailed cooling conditions are desired the user can define the heat sink parameters using the "Thermal Condition" tab or clicking on the "Detail Temperature Condition" button. Before entering the parameters to simulate loss and temperature of the inverter systems verify the pulse width modulation (PWM) method. Plenty of different modulation modes are on hand such as sinusoidal, space vector and many more.

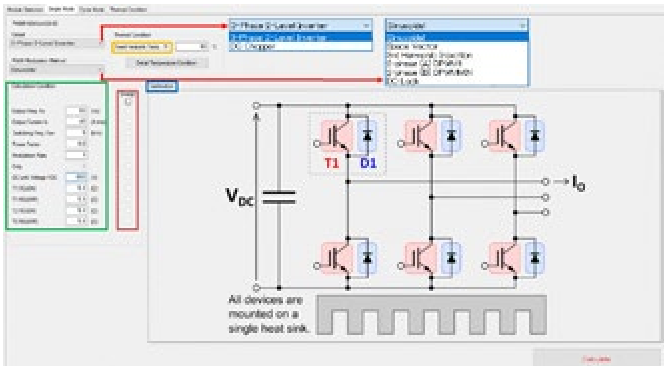

Figure 2: Static mode - parameter input

Fill in your simulation parameters into the **"Calculation Condition"** section such as output frequency f_o, carrier switching frequency f_{sw}, output current I_o, DC-link voltage V_{DC} and so on. The standard gate resistor values are already implemented but can be amended by the user.

Checking the **"Sweep"** box provides the possibility that loss and temperature values are displayed as a function of the selected parameter. The simulation tool traverses up to very high values of the selected "Sweep" parameter which is not representative for real applications but to get a feeling of the loss and temperature behavior over a wide range.

Figure 3 demonstrates the loss and temperature results of a certain operation point. On the right hand side the upper graph represents the loss curve while the lower graph shows the temperature on a time base with respect to the output frequency (e.g. 50Hz = 0,02s). The raw data of the graphs can be exported to a *.csv file by pressing the **"Data Export"** button. To save the displayed simulation results in *.bmp/*.tif/*.jpg format press **"Save Image"**. Total loss and temperature values are shown in the "Loss" and "Temperature" sections.

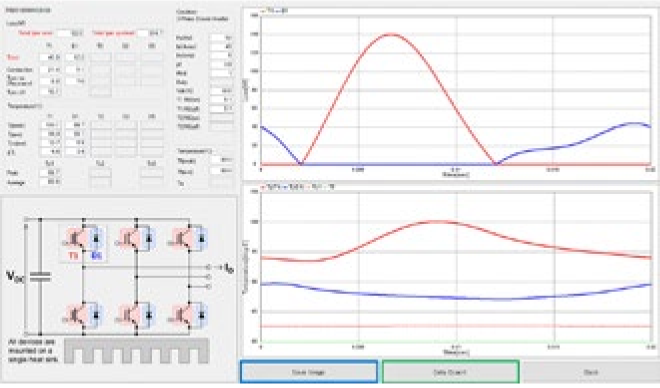

Figure 3: Static mode – temperature and loss results

Cycle Mode

While the single mode represents a static operation point a more dynamic solution is provided by the cycle mode. A customized profile according to the user's application can be entered. Figure 4 emphasizes the possibilities of the cycle mode. A fixed heat sink temperature can be chosen or a more detailed heat sink parameter can be defined by the "Detail Temperature Condition" button. The input of the desired gate resistance values is located next to the "Thermal Condition" section as well as the "Boundary Condition". The **"Cyclic"** boundary condition represents that the inputted cycle data occurs before and after the actual shown results of the simulation while the "1 shot" runs through the inputted data of "Cycle Data" section.

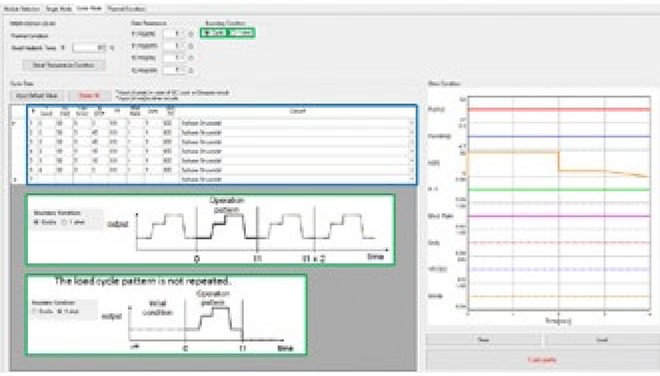

Figure 4: Cycle mode – parameter input

As shown in figure 4 a simple profile was entered in the **"Cycle Data"** section. An initial condition was used with zero output current. Starting from this initial condition at t_0 a ramp up of the current from 0A to 45A within 1second (t_1) takes place. The system operates for 1 second at 45A (t_1 to t_2) with a following decline of the output current to 10A (t_4) which operates for another second (t_4 to t_5) until the soft shut-off of the system to 0A output within 1 second (t_5 to t_6).

The results of the simulation are shown in figure 5. Similar to the results screen from the single mode the loss and temperature values are presented on the right hand side. The entered parameters are diagramed on the lower left side. The demonstrated graphs represent the loss and temperature trend over time like the in the single mode. The upper graph shows the loss curve of the transistor and diode according to the profile entered. The center one demonstrates the generated temperatures by the power semiconductors where the dotted line belongs to average values and straight lines to the maximum temperatures. Additionally, the case temperature Tc which is the temperature of the IGBT module's package and heat sink temperature Tf is simulated. The heat sink temperature is extracted in the lower graph as well. Same functions as in the single mode are present such as printing, saving the visible image or exporting the results to a text file is possible.

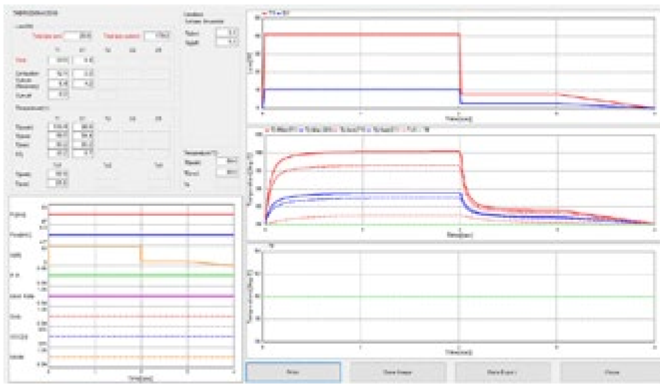

Figure 5: Cycle mode – temperature and loss results

Conclusion

Latest IGBT/FWD chip generation can be simulated in terms of loss and temperature behavior which provides an indication for the user's system. Many functions such as the detailed heat sink parameter definition allow quite precise thermal simulations. The selection of different PWM methods enable high complexity of calculation methods for accurate results in a single mode as well as cycle mode.

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Extremely Efficient Energy Storage Based on Three-Level Silicon Carbide Power Module

SiC makes the difference – both consumers and energy providers benefit from high-efficiency energy conversion between decentralized energy storage and the main power grid. The attraction for cost-effective and environmentally sustainable energy storage peaker plants is unlimited.

By Alexander Streibel, Roger Cooper, Ole Mühlfeld, Danfoss Silicon Power

Decentralized battery energy storage systems (BESS) reduce the reliance on fossil fuels and allow a wide range of other powerful benefits. Power grids need sufficient extra capacity to work properly during peak demand periods and to satisfy reliability requirements. This disadvantage is strengthened by the fact that the energy sources the energy providers prefer to use are only available with different time lags. In order to counteract large immediate peak demands, energy providers implemented pricing structures that led to a common use of combustion turbines (CT) in the past providing instantaneous energy. The benefit-side of the overall cost-benefit analysis will make energy storage more attractive to customers. If a proper analysis is done, not only acquisition costs, but also operating costs must be taken into consideration. The price for battery cells plus peripherals and the inverter competes against the acquisition and operating costs of CT plants.

Flexibility of CTs versus energy storage

The well-known output characteristics, acquisition and operating costs of CTs led to high acceptance in the world for adding peak power capacity to the main power grid. Furthermore, they were historically proven to be very reliable. However, when discussing the good points of CTs, the benefit of meeting shorter-duration peaking capacity requirements compared to coal or nuclear plants needs to be moved from the benefits of CTs to the ones of energy storage: Compared to energy storage, CTs are turtles in start and ramp-up phases. In addition, distributed energy storage facilitates the integration of variable wind and solar resources. The California Public Utilities Commission (CPUC) reported the negative impacts on grid stability occurred primarily due to solar PV. The potential of energy storage has been discussed in "Guide to procurement of flexible peaking capacity: Energy storage or combustion turbines" (by Chet Lyons, Energy Strategy Group, 2014): Flattening system load with energy storage synergistically reduces the need for all major categories of utility asset investment, including generation, transmission and distribution.

Year	Power	Energy
	$/kW	$/kWh
2016	$2,194	$549
2017	$1,390	$348
2018	$974	$244

Table 1: Projected costs (price) for a 1-MW, 4-hour redox flow battery (Source: ViZn Energy (used by Chet Lyons))

Cost-benefit analysis

CTs are often chosen to be the most cost-effective solution due mainly to their huge acceptance. At the same time, temperature, air pressure and humidity have a huge impact on the efficiency of those air-polluting machines. The CPUC defined use cases for storage in the California energy market that are described by Chet Lyons in more detail. In this paper, a 1-MW 4-hours redox flow battery is compared to a conventional simple cycle CT with a Capex of $1,390 per kW assuming mid-range CT costs since there are so many on the market. By 2017, storage can be roughly competitive with many conventional simple cycle CTs. More advantages can significantly increase the cost-effectiveness. The modular architecture of energy storage improves asset reliability and system resiliency through redundancy. The Electric Power Research Institute (EPRI) found out that distributed storage has higher value than central station storage mainly due to added distribution upgrade deferral and circuit stability control. Simply deferring capacity investments, regardless of type, lowers capital investment risks and improves total return on assets. The cost trend of energy storage as environmentally sustainable zero emissions energy resources that is dropping confirms the added value.

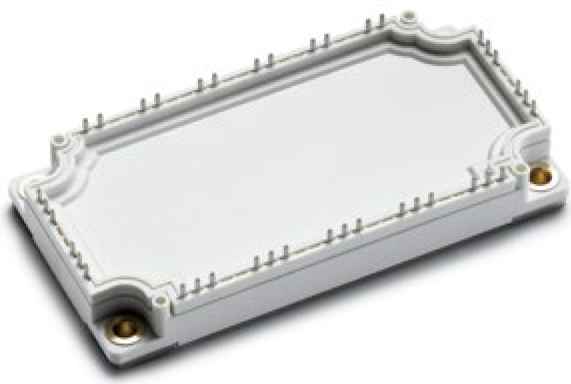

Figure 1: Exemplary E3 power module for a 60-kW solar inverter on IGBT basis (footprint: 62 mm x 122 mm)

High operational savings with three-level topology

Three-level advantages with compact NPC2 topology lead to high-efficiency inverter solutions due to smaller output voltage steps, reduced switching losses and doubly effective switching frequency. The design with the newest SiC technology allows a very high switching frequency of greater than 50 kHz that minimizes the required output filter dimensions. In addition, only SiC-type gate drivers are needed for the inverter. Due to its physical nature, the use of MOSFETs offers further advantages in the partial load area compared to IGBT solutions and in a reduced package size (by more than 35%) from E3 to E2 as shown in Figure 1—2. In conclusion, the E2 power module in Figure 2 and its circuit in Figure 3 is the first battery storage power module using SiC technology. The great amount of energy that is transferred through the inverter has a high impact on the operational cost savings resulting from the high efficiency. This benefit should be kept in mind to perform a proper costs-benefit analysis of power modules.

Figure 2: Exemplary E2 power module for a 60-kW energy storage inverter with SiC MOSFETs (footprint: 45 x 107,5 mm)

Customer-specific pin-out

The E2 module design has high flexibility to adjust switching characteristics due to a great amount of internal surface-mounted components. Therefore, MOSFETs can be easily replaced, and the power can slightly be up- or downscaled by minor changes to optimize system costs. Low temperature operation through improved thermal stack by using an AlN substrate leads to cost-efficient bonding and joining technologies that can be applied while still meeting the high lifetime requirements!

Outlook

The use of SiC power modules might only be beneficial if the battery stack costs (2017: approx. \$350/kWh) are high compared to the inverter costs. Although the price for battery cells is soon expected to drop below \$100/kWh, especially due to SiC components, high inverter efficiency is beneficial for the cost-benefit analysis to lower the attraction of CTs as peak capacity is added. Furthermore, as mentioned by Chet Lyons, simply overlaying storage on a central station basis won't maximize grid performance or cost reduction. In addition, storage can increase the importance of decentralized independently operating micro-grids that are disconnected from the main grid in emergency situations. Beside energy storage, this E2-SiC module can additionally be used for compact designs of high-efficiency solar inverters.

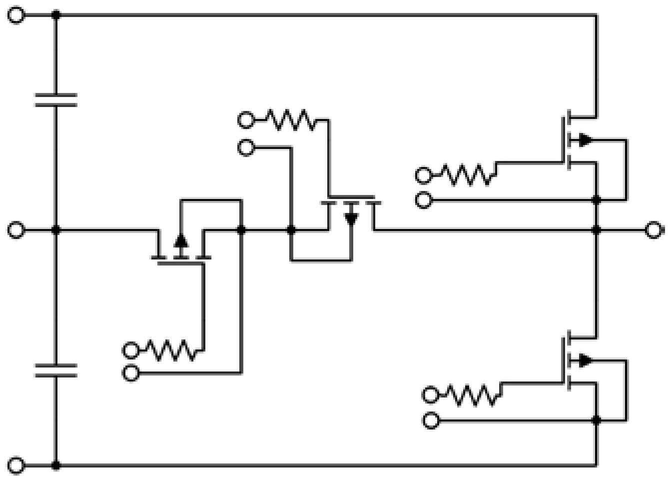

Figure 3: One NPC2 leg for a 60-kW three-phase energy storage inverter with SiC MOSFETs and internal resistors to adjust switching characteristics

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IGBT/SiC-FET Driver Design Tips to Prevent False Triggering

When designing IGBT or SiC FET bridge circuits, proper design of the gate drive circuitry is at least as important as transistor selection to ensure high reliability

By Andrew Leake, Dengrove Electronic Components

Concern for the environment is a major force behind trends such as renewable energy, smart industry and e-mobility. These in turn are driving greater demands for high-efficiency electric power converters and motor drives. These systems must be extremely reliable, and are often required to operate for lifetimes of up to 10 years or more.

To ensure high reliability, designers will choose very carefully when selecting the power transistors for a circuit such as the H-bridge of an inverter or motor drive. However, for best results, they should pay equal attention to designing and laying out the transistor gate-drive circuitry to prevent false triggering of the transistors, which can allow shoot-through currents. These short circuit currents can shorten the lifetime of transistors or, in the worst case, cause immediate destruction. Other undesirable results can include electromagnetic interference that may prevent equipment from meeting EMC regulations.

False triggering can result from poor management of the currents flowing in the transistor's parasitic capacitances and inductances, which are shown in figure 1.

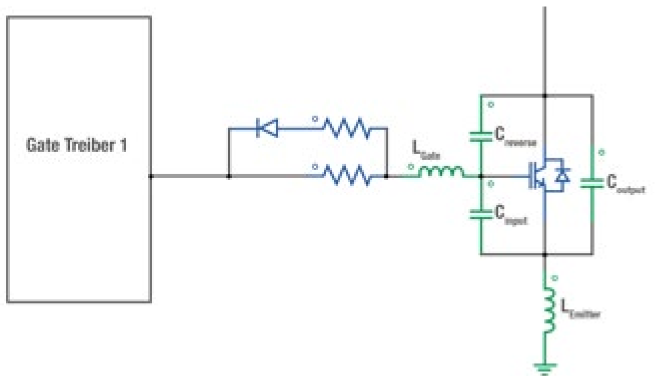

Figure 1: Parasitic effects and associated currents can disrupt control of the gate voltage

Parasitic Capacitances and False Triggering

Consider the flow of charging currents between Creverse and Cinput. If the collector-emitter voltage rises when the transistor is turned off, current flows into Creverse according to the following equation:

$$I_{Creverse} = C_{Reverse} \times dV_{CE}/dt$$

Referring to figure 1:

$$I_{Cinput} = I_{Creverse} – I_{Driver}$$

Hence a charging current flows into Cinput that can charge the parasitic capacitance to a voltage above the gate-emitter threshold voltage, causing the transistor to turn on. Idriver depends on gate resistances, and on the inductance Lgate in dynamic operation. The latter depends on circuit layout and the package used.

The designer can adjust various aspects to try and minimise the possibility of false triggering due to charging current flowing from the Miller capacitance. One solution may be to limit $dV_{CE/dt}$ to flatten the switching ramps and $I_{Creverse}$ curve. One disadvantage of this approach is to increase switching losses as a side-effect. Alternatively, optimising the circuitry to reduce the parasitic inductance Lgate can effectively reduce the voltage rise at the gate. However, a more predictable solution is to apply a negative gate-emitter voltage to widen the safety margin up to the threshold voltage.

Effects of Parasitic Inductance

False triggering can also result from the effects of parasitic inductances such as Lgate and Lemitter. When switched on, the load current flows through the transistor, and therefore also through Lemitter. If the load current is turned abruptly off, Lemitter causes a negative voltage according to the equation:

$$-V= L_{Emitter} \times dI / dt$$

This tends to drive the emitter voltage below GND. When the driver acts to send the gate voltage to GND, the gate-emitter voltage becomes positive and thus can turn the transistor on.

In a bridge circuit, where all low-side transistor emitters are connected to the power ground, the effective Lemitter of each transistor is influenced by the inductances of other transistors and their ground connections. Perfect symmetry is difficult to achieve. Hence some transistors can be more susceptible to false triggering, and predictable performance cannot be guaranteed under all operating conditions.

Circuit inductances should always be minimised by keeping conductors and trace lengths as short as possible. However, by using an isolated gate driver for each transistor, the driver ground can be connected directly to the transistor emitter thereby eliminating the effects of layout inductances. The situation can be improved further by using transistors that provide a Kelvin connection to the emitter. Connecting the driver ground to this Kelvin connection effectively prevents Lemitter from influencing the turn-on behaviour.

In addition, using a gate driver that can apply a negative gate-emitter voltage, i.e beyond simply holding the gate at ground potential, to keep the transistor turned off increases the safety margin between the gate-emitter voltage and the transistor's threshold voltage. This can be highly effective in preventing false triggering.

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<table>
<tr><th>Part Number</th><th>Description</th><th>Integrated FETs</th><th>Supply voltage range (V)</th><th>Typical $R_{DS(on)}$ (Ω)</th><th>Maximun output current (A_{rms})</th><th>Quiescent current (nA)</th></tr>
<tr><td>STSPIN220</td><td>Microstepping driver featuring up to 256 microsteps per full step</td><td rowspan="4">Yes</td><td rowspan="4">1.8 - 10</td><td rowspan="3">0.2</td><td rowspan="3">1.3</td><td rowspan="4">< 80</td></tr>
<tr><td>STSPIN230</td><td>3-phase brushless DC (BLDC) motor driver</td></tr>
<tr><td>STSPIN240</td><td>Dual brushed DC motor driver</td></tr>
<tr><td>STSPIN250*</td><td>Single brushed DC motor driver</td><td>0.1</td><td>2.6</td></tr>
</table>

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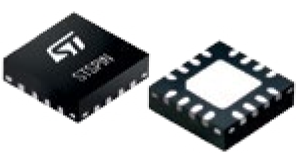

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Designing the Driver Circuit

The previous section has shown that the performance of the driver circuit has a major impact on the transistor's ability to resist false triggering.

When designing with IGBTs, typical gate-threshold voltages specified in transistor data sheets tend to be between +3V and +6V. These can decrease to 1 to 2V with increasing junction temperature. A gate-emitter voltage of +15V is generally accepted as the optimum turn-on voltage to ensure fast switching in commonly encountered operating conditions. As discussed, a negative gate voltage can be used to turn the IGBT off. A voltage of -9V has proved to be safe and effective in practice. Dual isolated DC/DC converters with asymmetric voltages at +15V and -9V are now often used as IGBT drivers.

Driving SiC FETs

In applications that demand high energy efficiency with small size and low weight, such as high-end industrial equipment, inverters, or electric vehicles, silicon carbide (SiC) MOSFETs are becoming increasingly popular. Ideal turn-on and turn-off voltages for SiC FETs are different to those recommended for IGBTs.

SiC FETs have significantly lower threshold voltages than IGBTs. Moreover, the voltage for a given SiC FET decreases with increasing temperature. Logically this would suggest that a greater negative offset voltage on the gate is needed to turn off the device and prevent false triggering. The threshold voltage decreases over lifetime. If the circuit is operated with a gate-source voltage of -5V, this decrease is typically between 0.2V-0.3V over a lifetime of a thousand hours. After this time the threshold voltage remains stable.

If the gate-source voltage is -10V, the change is around five times greater and the variations between transistors are large. The research found these variations to be so high that some devices were already "normal on" at 0V. Hence to ensure consistent performance over the lifetime of the equipment, designers should not apply gate offset voltage values more negative than -5V when working with SiC FETs.

On the other hand, a positive voltage of +15V, as used with IGBTs, would be theoretically possible. As the threshold voltage is substantially lower than for IGBTs, +15V should ensure reliable switching behaviour in SiC FETs. However, the output characteristics at different gate-source voltages have demonstrated that higher voltages would achieve a substantially lower on-resistance, RDS(ON). A gate-source voltage of +20V makes the most of a SiC FET's benefits. Hence a DC/DC converter running at +20V/-5V is a good choice for supplying the driver.

Moreover, the chosen DC/DC converter must also provide high isolation. Typical switching frequencies in the range 10kHz-50kHz for IGBTs, or over 50kHz for SiC FETs, can result in steep ramps that subject the converter's insulation barrier to repeated large stresses. Insulation that is too tightly dimensioned reduces the long-term reliability of the system.

Converters that are designed specifically to supply power transistor gate drivers, such as the RECOM RKZ1509 for IGBT applications, or RKZ2005 or RxxP22005 for SiC-FET applications, provide asymmetrical voltage outputs and high isolation rated up to 4kV or 5.2kV for the RxxP22005. Figure x and x show how these converters can be used to control IGBT or SiC-FET gate drivers.

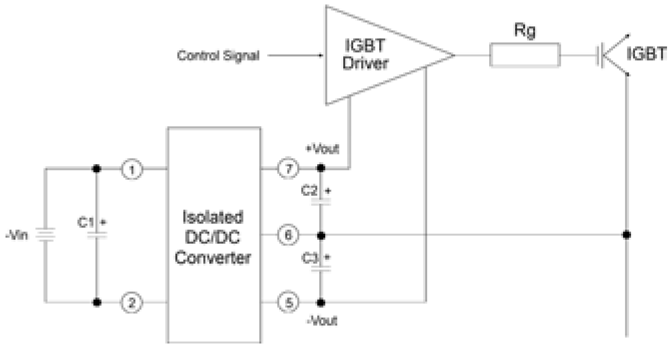

Figure 2: IGBT gate driver powered by dual asymmetrical isolated DC/DC converter

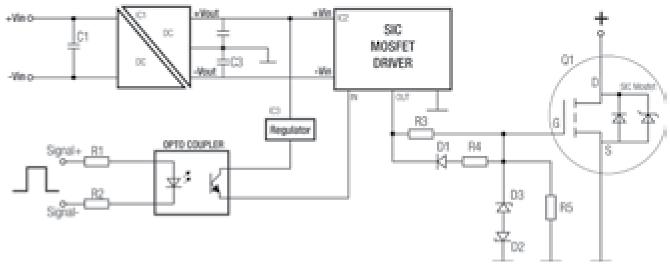

Figure 3: SiC-FET gate driver powered by dual asymmetrical isolated DC/DC converter

Conclusion

In systems that require a robust and reliable power-transistor bridge, proper design of the transistor gate-driver circuitry is at least as important as selection of the power transistor itself. Asymmetrical turn-on/turn-off voltages, with negative-offset turn-off, are known to be effective, and should be used in conjunction with best layout practice: keeping connections short to minimise inductances, and ideally (when designing an IGBT bridge) connecting the driver ground directly to the transistor emitter via a Kelvin connection.

The driver circuitry must be isolated to allow the driver ground to be connected directly to the transistor. Robust isolation is essential to ensure long-term reliability, both in the driver and in the dual asymmetric DC/DC converter used to power the driver.

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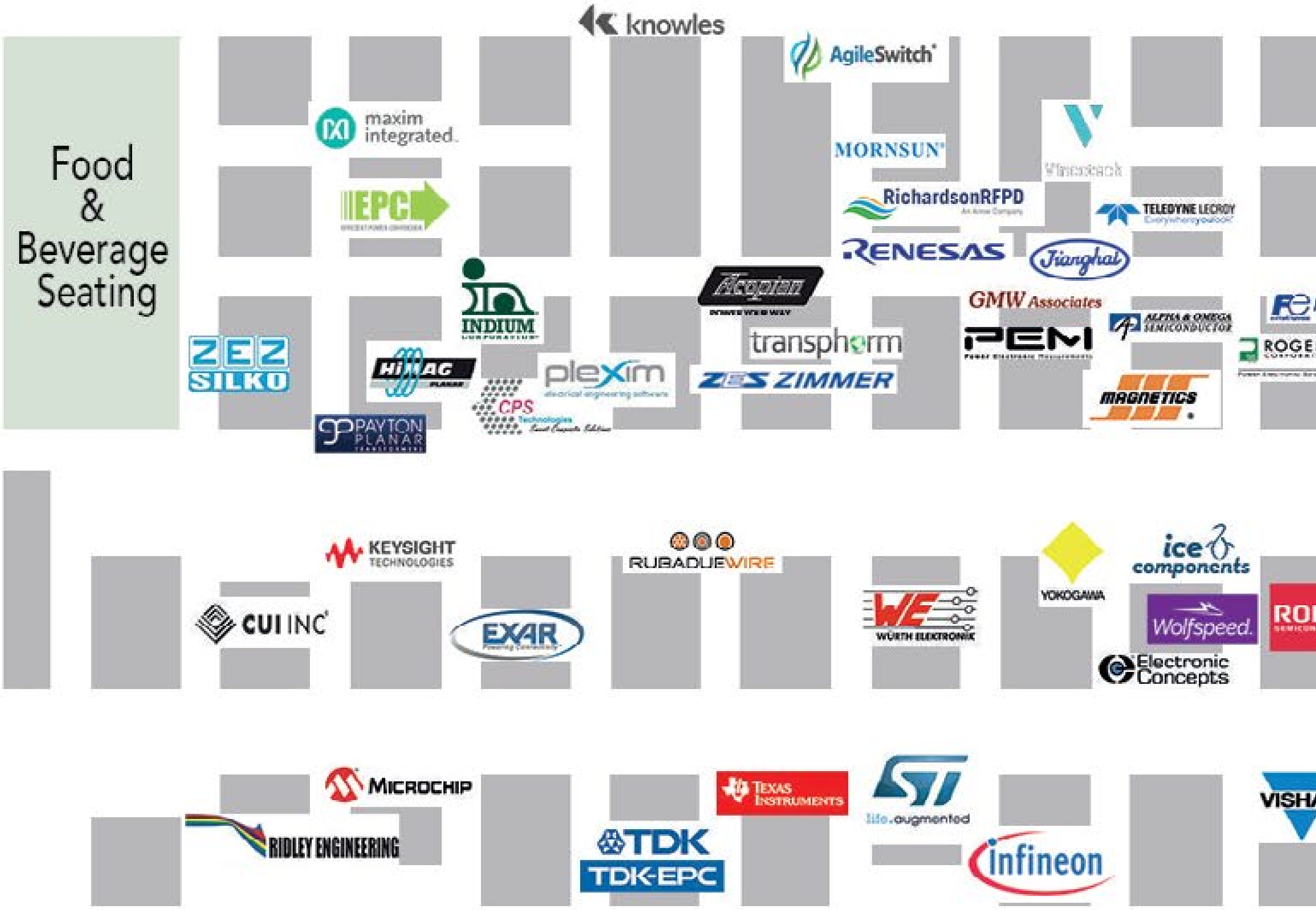

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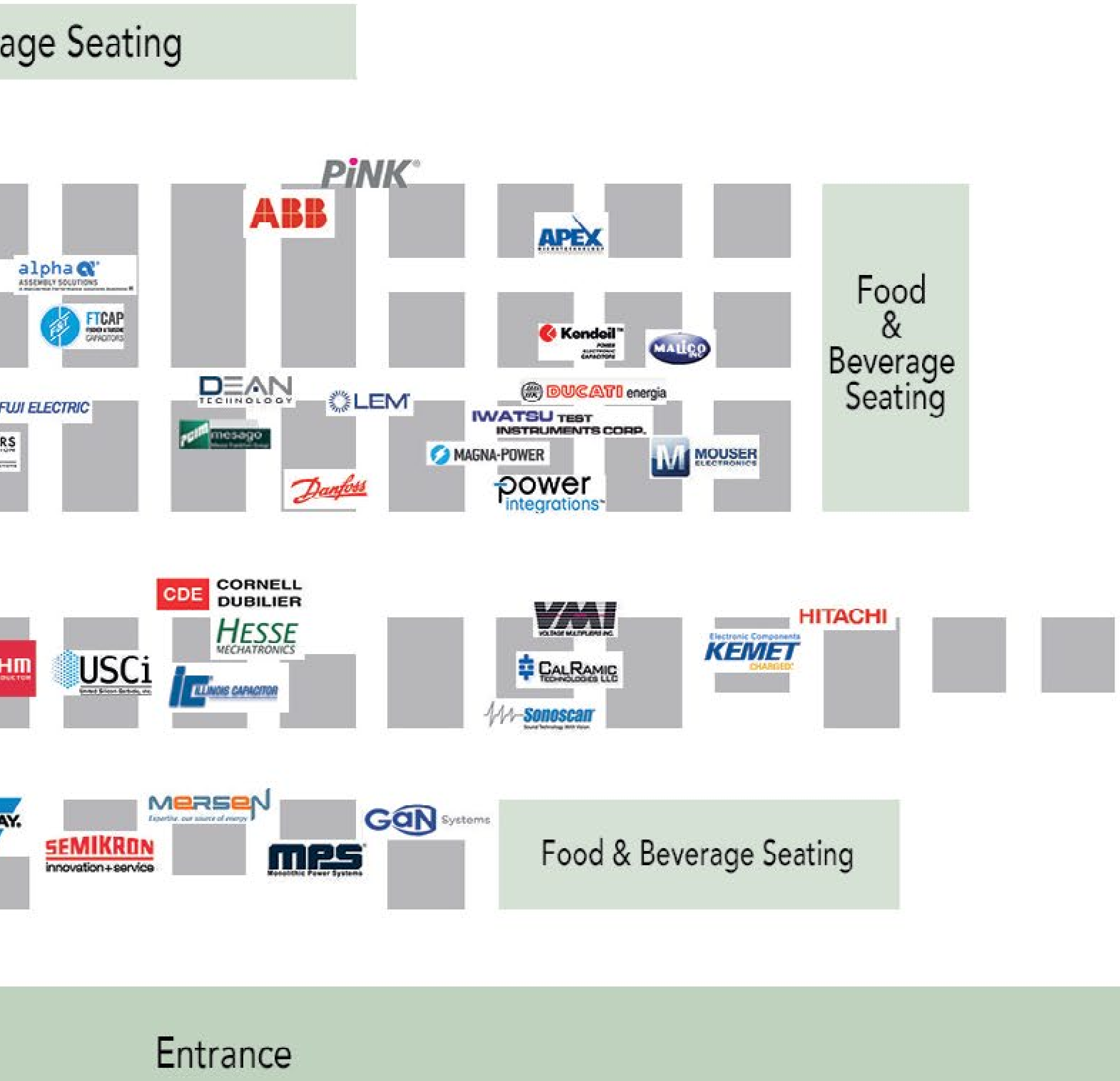

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Rethinking the Power MOSFET Figure of Merit

Sanjay Havanur, Sr. Manager System Applications, Vishay Siliconix

Comparing MOSFETs by their Figure of Merit (FOM) has become the ubiquitous industry practice. Along with current ratings and SOA curves, FOMs are being increasingly used as elements of MOSFET specmanship. The simplest and most widely used definition of the MOSFET FOM is the R_{ds} x Q_g product. Every new MOSFET product line is announced with an impressive reduction of at least 20 % in the FOM. The newer wide bandgap technology based devices go much further and claim up to 50x or even 100x reduction in the figure of merit. The end users are justifiably confused by the tall claims. What exactly is the benefit of using a switching device that has 50 times improved merit? Will it provide 50x less loss? If you have a power convertor with a silicon MOSFET dissipating 10 W, will the losses reduce to 0.2 W if it is replaced with another device that has “50x better Figure of Merit”? While even a 10 % reduction in losses is welcome, it would be somewhat underwhelming for a 50x improvement in the Figure of Merit.

A Brief History of FOM

The earliest mention of a Figure of Merit for power MOSFETs in switching applications appears in [1]. It defined the Baliga High Frequency Figure of Merit as

$$BHFFOM = 1 / (C_{in} \times R_{ds}).$$

C_{in} was later replaced by Q_g as the industry standard and the notion of an all-important, universally valid FOM was firmly established. Several modifications have been proposed to the definition, but the simple R_{ds} x Q_g continues to be the industry favorite even today. The logic behind the original FOM was rather simple. Lower R_{ds} reduces conduction losses, while lower Q_g reduces switching losses. Total losses are minimized if their product is minimized. How well does reality conform to this logic?

An evaluation was performed using a series of three design platforms, two with comparable R_{ds} x Q_g products, and the third from an earlier generation with much higher values, both for R_{ds} as well as the FOM. The different devices are identified by their FOMs in Table I. The test platform was a commercially available DC-DC quarter brick operating at 200 kHz using a ZVS bridge as the primary topology. Loss and efficiency results are shown in Fig. 1. *A 2.8x reduction in FOM with 5.8x reduction in Rds does not offer any performance benefit.* On the other hand, FET300, marginally worse than FET270, outperforms the other two, with nearly 1 % improvement in efficiency. Clearly, there is a

Device	R_{dson}	Q_g	FOM	R_{ds} Ratio	FOM Ratio
	mΩ	nC	mΩ-nC		
FET270	3.6	75	270	1.00	1.00
FET750	21	36	756	5.83	2.80
FET300	11	27.9	307	3.06	1.14

Table I: Comparison of parameters for devices with different Figures of Merit

disconnect between the real world performance of power MOSFETs, or any other switching device, and the figure of merit touted for them.

A closer look at [1] reveals a fundamental misconception about the nature of MOSFET losses. It explicitly states that the only switching losses in a MOSFET are due to gate charge and discharge. There is also an assertion that these switching losses are proportional to the square root of the switching frequency. V-I crossover losses were completely ignored, along with C_{oss} or body diode related ones. It is true that C_{oss} induced losses were not well understood in 1989 when the definition was proposed, and it was common practice to reverse connect external rectifiers to bypass the MOSFET body diode. However, the inductive switching mechanisms and the associated crossover losses were well known long before power MOSFETs were conceived. The omission of these known, major factors is quite surprising. What is not so surprising is the fact that the resulting FOM, which has practically no relevance to the application environment, is still religiously followed in the industry.

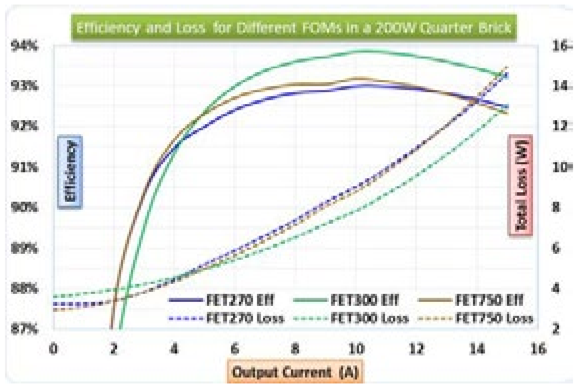

Figure 1: Loss and efficiency data for MOSFETs with different FOMs in a ZVS bridge converter switching at 200 kHz

Application Environment vs Device FOM

Fig. 2 shows the Plug to Processor power train for an AC-DC power supply and lists typical operating ranges for various parameters. As can be seen, each power stage requires a different technology as the operating conditions cover a wide range, typically over two orders of magnitude. Can a simple product of two device parameters predict

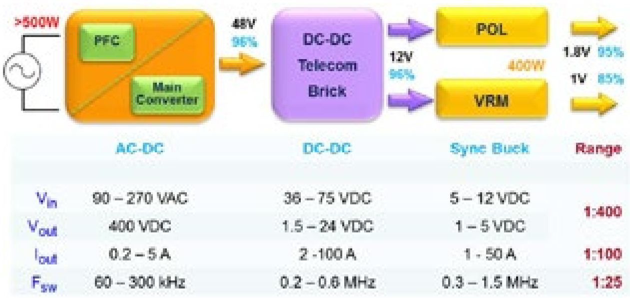

Figure 2: Plug to Processor power train with operating parameter ranges in each stage

which device will give the lowest loss performance under every one of these application conditions?

Several attempts have been made, [2] to [7], to improve upon the original FOM definition, replacing Q_g by Q_{gd} or Q_{oss}, or by more complex functions of capacitive charges associated with the MOSFET. However, none of these exercises have been able to overcome the limitations inherent to the very notion of an FOM at the product level. There are two issues with the basic concept of a universal figure of merit for MOSFETs that the users have to consider. First, the total losses incurred by a MOSFET are dictated not only by its own properties, they are equally dependent on how well they are matched to the system. No amount of adding and manipulating MOSFET parameters to the FOM will indicate how well it will perform in any given application. Put another way, *all* device based FOMs are completely blind to the application environment and therefore are only of marginal relevance to end users.

Instead of relying on lower FOM as a solution for improving performance, system designers need to go back to the basics of loss analysis. Today's switching circuits are quite complex, but the MOSFET losses in any application are still a combination of losses arising from

1. Conduction
2. Switching losses at turn on and turn off
3. Output capacitor charge and discharge
4. Diode conduction and recovery
5. Gate charge and discharge

Table II identifies the system specifications, design choices and combines them with MOSFET parameters to arrive at simplified expressions for estimating different loss components listed above.

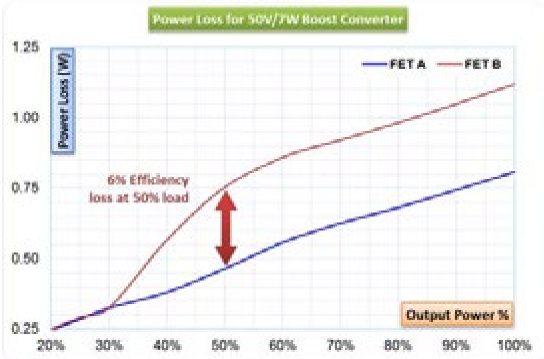

Figure 3: Loss data for MOSFETs with different FOMs in a boost convertor switching at 600 kHz

Combining all the loss components from Table II, a generic equation for total loss valid for any application can be written as below. Our purpose here is not to calculate individual losses with the highest degree of accuracy, but to understand the relation between MOSFET parameters and its operating environment to minimize the total losses.

$$K_{cond} \times R_{dson} + K_{sw} \times Q_{sw} + K_{out} \times E_{oss} + K_{bd} \times Q_{rr} + K_{fwd} \times V_{fwd} + K_{gate} \times Q_g \quad (1)$$

The losses are expressed here as the *weighted sum* of multiple MOSFET parameters, weightage factors being dependent on operating conditions listed in the last row of Table II. It should be clear that arbitrarily taking just two of them, R_{ds} and Q_g, and minimizing their *product* without any regard to other terms in the equation, will not translate directly to improved performance. Devices with lower FOM may indeed perform better in the real world, but such behavior is in no way predicated, nor predicted, by their R_{ds} x Q_g product.

The importance of matching multiple system parameters to a wider selection of MOSFET properties, instead of comparing FOMs, cannot be overemphasized. Another evaluation of a 600 kHz low power boost converter is shown in Fig. 3, where uniformly poor performance is observed even with a 1.5x reduction in FOM. At 50 % load the efficiency drops by nearly 6 % for the device with lower FOM. This converter operated with a low 11 V input and delivered a 52 V output at 135 mA. Table III below compares the relevant parameters of the two MOSFETs tested. C_{oss} induced losses dominate in boost converters and the 3x increase in E_{oss} clearly makes it the wrong choice for the application. Given the low power level, and the combination of high output voltage and switching frequency, it is not even necessary to do any detailed loss analysis.

Note that FET B by itself is not an inferior product. It was designed for a different application where C_{oss} losses did not come into play. MOSFET technology has advanced to a level where highly customized, application specific device platforms are possible. Choosing FET B over FET A because it has "better FOM", without any regard for system conditions, is a poor design practice. The fact that the MOSFET Figure of Merit excludes C_{oss} and E_{oss}, which can be the dominant source of switching loss for high voltage applications, makes it even more irrelevant to the system designers.

Platform vs. Product

By definition, any FOM refers to a technology platform. A large number of products can be derived in it, all having the same exact FOM. But end users do not need the whole platform. They are looking for that one device best suited to their application, which cannot be determined based on the R_{ds} x Q_g product. Device designers create a geometry that has specific R_{ds} and capacitances per unit active area of silicon. A multitude of MOSFETs are then created by literally cutting the silicon into dice of different sizes. The notion of a figure of merit applies to the geometry and not to any individual MOSFET, all of which have the same exact R_{ds} x Q_g product by definition. This can be illustrated further by applying the loss equation to a wide range of possible MOSFETs based on the FET270 platform. Fig. 4a shows the projected losses for three different power levels and design choices, as a function of R_{ds}. All R_{ds} values plotted on the x-axis are derived on the same FET270 geometry, assuming different active areas. MOSFET capacitances and charges were scaled higher or lower in inverse proportion to the same active area. In other words, all devices have the same FOM and yet can have widely different performances based on the application.

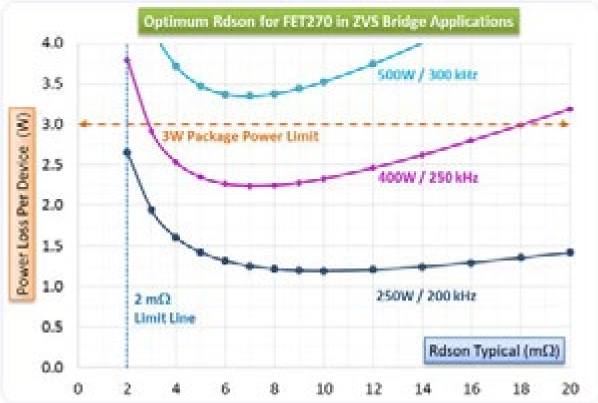

Figure 4a: FOM and optimum R_{ds} for ZVS bridge using operating parameters like P_{out} and F_{sw}.

Figure 4b: Loss component balance for the 250W, 200 kHz ZVS Bridge

The optimum choice of a MOSFET now reduces to finding the R_{ds} at which total losses are at the minimum. But finding that minimum, and the best device for the application, requires a knowledge of system parameters like output power and switching frequency, not device technology or FOM. Using simple loss analysis, Fig. 4b breaks down the loss components and explains the anomalous efficiency results. FET750 has a balanced composition of losses, conduction losses are almost the same as switching losses, and matches FET270 for total losses. FET300 is not as well balanced as FET750 but has better technology and its absolute losses are lower, which makes it the best

Loss Component	Conduction	Switching	Output	Diode	Gate Charge
System Specs	V_{in}, P_{out}	V_{in}, P_{out}, F_{sw}	V_{in}, F_{sw}	F_{sw}	F_{sw}
Design Parameters	Duty	I_g	-	T_{dead}	V_{gs}
Circuit Parameters	I_{rms}	I_{pk}, V_{in}	-	I_{pk}	-
MOSFET Parameters	R_{dson}, TCR	Q_{gd}, Q_{gs}, Q_{sw}	E_{oss}	V_{sd}, Q_{rr}	Q_g
Loss Equation	I^2_{rms} x R_{dson} x TCR	½ x V_{in} x I_{pk} x F_{sw} x (Q_{sw} / I_g)	E_{oss} x F_{sw}	V_{sd} x I_{pk} x T_{dead} x F_{sw}	V_{gs} x Q_g x F_{sw}

Table II: System, circuit, and MOSFET parameters required for application specific Figures of Merit choice among the three devices. Looking at Fig. 4a again, if a device with the optimum R_{ds} = 10 mΩ was chosen from the FET270 platform, it would be the best choice yet for this application. It should also be noted that the lowest R_{ds} achievable at 2 mΩ is not an optimum solution for any operating condition.

Device	R_{ds} @ 4.5 V	R_{ds} Ratio	Q_g @ 4.5 V	FOM	FOM Ratio	E_{oss} @ 50 V
	mΩ		nC			µJ
FET B	24	63 %	8.7	209	69 %	300 %
FET A	38		8.0	304		

Table III: Comparison of parameters for devices in a boost convertor

The point here is that the FOM number is only an indirect pointer, covering a broad range of products, but lacks the insight needed to choose a specific device optimally matched to the application. Nor is such insight gained by running circuit simulations. There is no alternative to writing down a detailed loss equation for the application under its specified operating conditions, fill in the values for different MOSFETs under consideration, and evaluate which of them will have the lowest loss. The method is illustrated for PFC circuits in [8].

Most system designers today understand that “lowest R_{ds} money can buy” is never the right criterion for selecting their MOSFETs. At the same time, the other rule of thumb, “device with the lowest FOM available in the market” needs to be re-evaluated, in view of its lack of application focus. The MOSFET Figure of Merit is a designers’ tool, useful for comparing one design platform to another. But there is no such thing as a figure of merit for a specific product. It is not a question of whether definition x for the FOM is more relevant than definition y. The very notion of a Figure of Merit does not have any validity at the individual device level, and by logical extension, to the system designer.

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Robust AC- Film Capacitors for Power Electronics

AC film capacitors are an important part of filters in modern power electronics. Investigations have shown that reliability of these components is not always guaranteed under harsh environmental conditions.

By Dieter Burger, COMPOTEC / Germany - the European sales-office of BM / China

In order not to thwart the efforts to achieve a world with green energy, smart homes and with decarbonized transportation, the robustness of the applied EMI- and AC- filtering Capacitors play an important role. If the AC Capacitors should face a degradation during operation, the electronic device might pollute the environment with inacceptable levels of EMI-noise and feed high ripple currents into the grid. Under such circumstances, this electronic devices could lose their acceptance in the public.

Film Capacitors on the AC-side of power electronics

AC Film Capacitors are being used in power electronics as X- and Y-capacitors for EMI-noise suppression, or for AC-filtering to remove the switching ripple from the mains current.

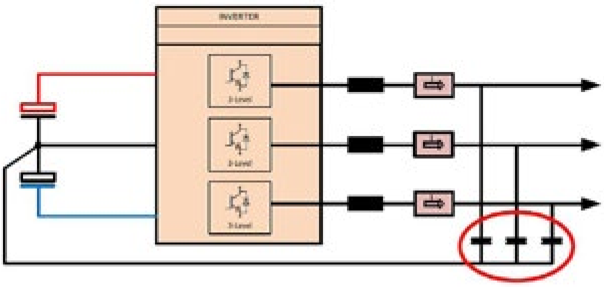

Figure 1: AC-filtering capacitors in output sine filters of inverter applications. The connection is between phase and neutral of the output.

Usually, a degradation of an EMI- and AC-filtering capacitor doesn't cause the electronic device to stop its operation, as these capacitors are not connected in series to the line. The electronic device keeps on operating without the initial characteristics of this capacitors.

Consequences of degrading AC Capacitors

If AC Capacitors degrades while the electronic device keeps on operating, there are following consequences:

- Increase in the electronic device's emission potential to cause electromagnetic disturbances.
- Decrease in its immunity to interferences.
- Rise in ripple currents on the mains.

Figure 2 shows a simplified topology of a grid connected inverter. The inductor limits the ripple current and the X capacitor limits the ripple voltage. Under ideal conditions it short-circuits the ripple. When the mains impedance is low, or the X capacitor impedance is high because of degradation, then a large fraction or the whole ripple current will be fed into the public grid. Today the impedance of the public grid is influenced already by the capacitive load of distributed power electronic devices and their EMC filter capacitors [1]. Even in grids with higher impedances, the current source behavior of the filter inductors will feed a high ripple current into the grid if the filter capacitance is reduced because of degradation.

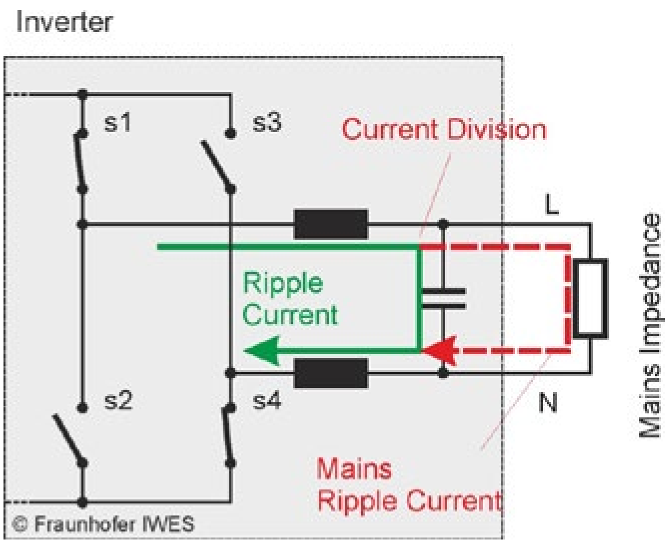

Figure 2: If the filter capacitor face an inacceptable degradation, the ripple current on the mains increases – not only in a low impedance grid but also in a high impedance grid, because the coils act as current source when the semiconductor bridge is chopped.

In the case of a degraded X capacitor, the mains ripple current can rise to levels which can harm or influence other electric apparatuses. Mr. Kirchhof, research engineer at Fraunhofer IWES, points out that cases have been well documented where inverter ripple currents on the lines influence the current measurement circuit of smart meters in a way that additional energy measurement errors of 20 % and more occur [2] [3]. Moreover, ripple currents at frequencies of several kilohertz will stress isolators, varistors, power capacitors and other electronic devices and reduce their lifetime as well.

Negative effects of increased ripple currents in the grid

An increase of the ripple currents in the grid due to degraded AC Capacitors may have following impacts:

- The end-of-life of components or electronics nearby could be caused due to their increased power-loss.
- The measuring results of Electricity Smart Meters could be falsified.
- Measurement circuits of the inverter could be affected because of decreasing internal EMC behavior.
- Powerline communication could be disturbed.

- Communication lines close to the AC cabling could be affected by capacitive and inductive coupling between these lines.
- The propagation of conducted disturbances does not stop at the border of the own branch.
- The inverter regulation can become unstable which may lead to a malfunction of the inverter.
- This negative effects can be prevented by using AC Capacitors with a high robustness to withstand a degradation in the field.

The power quality of the grid has an impact to the lifetime-expectancy of AC Capacitors

It must be taken into account that the stress to AC Capacitors in the application keeps on increasing as the power quality at higher frequencies is getting worse:
The climatic changes cause more and stronger surge-pulse events in the AC mains, e.g. from lightning strikes.

The continuous increase of switched-mode power supplies, converters, inverters and active PFC‘s cause additional stress to AC capacitors at frequencies above the mains frequency and its harmonics. The switching process of these devices leads to continuously repeated low amplitude pulse loads.

Such pulses provoke capacitance-consuming self-healings and challenge the capacitor's endspray-contacts with high pulse-currents:

$$\text{Current } i(t) = C \times dV/dt$$

A voltage pulse in the mains with e.g. 100V/µsec leads in a 1µF AC capacitor to a pulse-current of approx. 100A/µsec.

The increasing amount of converter, decentralised grid feed-in or fluctuating loads generate more temporarily over-voltages in the mains. If this temporarily over-voltages are above the rated voltage of the AC capacitor, the dielectric's breakdown voltage strength may suffer.

Furthermore, unconsidered resonant-circuits may arise when several switched-mode sources/sinks begin to resonant against each other: together with the individual power entry-filter, the wire-length of the device creates a resonant frequency. If this resonant frequency is close to the device's switching-frequency, such resonances lead to high currents between the individual filter-capacitors.

With an inductance per unit length of 1 µH/m for a single wire and some 20 µF distributed between two points at a line of 200 m length, resonances can occur within the chopper frequency range of modern power electronics. A resonance circuit can also act as a voltage transformer. In this case, the voltage stress on a device at the other end of the line can be larger than the stress of the same device connected in proximity to the disturbance source. Once the capacitance of the filter capacitor decreases, such resonances are even more likely.

Temperature rise of AC Capacitors

High ripple currents in the AC mains cause very high power-losses ($P = I^2 \times ESR$) of AC Capacitors. The temperature-rise of a capacitor corresponds to the increase of its power-loss. The formula shows that the power-loss from a capacitor with e.g. 500mA is 100 times higher than from the same capacitor with 50mA.

With a degradation of the metallization layer (electrode), the ESR of the AC Capacitor keeps on rising. A steadily increasing ESR in combination with increased currents in the AC mains accelerates the temperature-rise and finally the end-of-life of AC Capacitors.

What are the main root-causes for a degradation of film capacitors used in AC voltage?

The root-causes of a degradation of film capacitors under AC operation are mainly:
- Partial Discharges (Corona)
- Humidity Corrosion of the film metallization (electrodes).

Partial Discharge (PD, or so called Corona-Discharge)

During the production of the capacitors, a bad winding-process and an insufficient hot press-process create air-gaps between the film-layers. When the electrical field in the capacitor is higher than the breakdown-strength of the air in the gaps, a local breakdown occurs which results in an ionization of this air (= Partial Discharge/Corona). With this discharge, small electric arcs occur locally, creating high currents and triggering capacitance-consuming self-healings. This process cause a local evaporation of the metallization.

It is important to note that under a given voltage, the electrical field in a thin film is higher than in a thick film. Example:

230Vac/5µm film = 46V/µm; 230V/7µm film = 33V/µm, equals to 40% difference. This is like an accelerating factor corresponding to 1.4 of the rated voltage.

With a higher electrical field, breakdowns occur much faster and more breakdowns can be observed within shorter time. Generally, for AC capacitors larger physical dimension means a higher robustness.

The highest concentration of the electrical field in a capacitor is at the metallization edges (major disturbance of the electrical field homogeneity) [3].

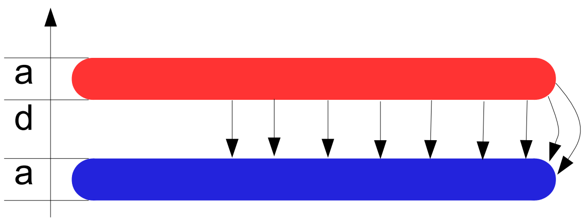

Figure 3: Electrical field in a film capacitor; a = electrode thickness; d = dielectric film thickness.

Therefore PD/Corona usually starts at the metallization-edges on the outside. It evaporates the metallization in a quite straight movement from the free margin side of the film towards the inside. PD/Corona is mostly present under AC operation (change of the electrical field).

Figure 4: Demetallized electrodes by corona arcing in the air gap between the films

A PD/Corona-process is comparable to a glow discharge. With applied voltage, this process might kept alive until there is no more electrode to apply an electrical field. No more electrode means no more capacitance.

Humidity Corrosion

The winded film element of the capacitor might get in contact with humidity either during the production-process or during the time in the field. The plastic box and the epoxy-potting provides a humidity-protection for the winded film element. However, there are significant quality-differences in the materials for the box and the epoxy.

Usually the very thin metal coating of the plastic film is either Zinc or Aluminium, or a mixture of both. The combination of humidity (water = dipol) and applied voltage reacts with both materials (Zinc ++, Aluminium+) and leads to a corrosion-process.

Figure 5: Electrode corrosion due to the presence of humidity

When humidity corrosion occurs in the film metallization, the metallization coating breaks down. This results in a thinning of the metal layer and ultimately loss of conductive electrode surface area - with a corresponding loss of capacitance and rise of ESR.

Manufacturer of AC Film Capacitors offer series with extended robustness

Considerable efforts can be seen from manufacturers of AC Film Capacitors to offer products with a long lifetime-expectancy. Such products are named e.g. industrial grade-, heavy duty- or THB- capacitors. This capacitors are specified to pass humidity-robustness test with simultaneously applied temperature, humidity and voltage. By means of lifetime-calculation formulas (e.g. Hallberg-Peck equation), the result in such a test can be used to calculate the minimum lifetime-expectancy under load.

Generally, very good achievements for AC Capacitors with a high robustness to Partial Discharge (Corona) and Humidity Corrosion can be reached with:

- A complete In-line production process, with an overall control of the ambient conditions.
- An intensive drying-process of the winded element before epoxy-potting.
- Applying high-end epoxy resin.
- Using a box material with low permeability to humidity.
- Dielectric: preferably PP due to its higher dielectric strength, lower loss-factor and lower humidity-coefficient than PET.
- Electrode metallization: avoiding Zinc in the active metallization area, as it is highly sensitive to the presence of humidity.
- Capacitor element: with inner series connection, thus reducing the AC voltage stress per connection by half. The Partial Discharge Inception Voltage (PDIV, Corona Starting Voltage) is significantly higher compared to capacitors without series connection.
- Optimization of the layer pressure.
- Increased strength of the contacts between lead-wires and winded element.

Next to the robustness, also Fail-safe and the active and passive flammability are important characteristics for AC Capacitors.

BM's new series B43 of extremely robust AC Capacitors

The company BM from Shunde/China has launched the series B43, which combines the above criteria. As a result, the average ΔC/C In a humidity robustness test with 85°C, 85% RH and applied voltage for 1.000 hours is outstanding 5% at most. Thus, this series not only meets entirely the requirements for highly robust EMI- and AC filtering- capacitors in power electronics. The narrow tolerances of degradation also permits a controlled current supply, e.g. in capacitive voltage-dividers and capacitive power supplies.

Also for DC-link capacitors BM offers very robust designs, with excellent results in accelerated lifetime-tests (THB-test; temperature, humidity, biased voltage).

Conclusion

There are different quality-levels of AC Capacitors in the market. Same as doing it already e.g. for electrolytic capacitors, the R&D engineer should only select such AC Capacitors which have at least the same lifetime-expectancy like the electronic device itself. Otherwise – as descripted in this article - the consequences when the electronic device keeps on operating while the AC Capacitors face a degradation are too serious.

Further information can be found under:

www.compotec-electronics.com

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High Voltage Ceramic Chip Capacitors Evaluated Acoustically

The internal structural defects that cause high-voltage ceramic chip capacitors to fail in service typically begin as some form of gap, which may be called a delamination or a void or a non-bond. The gap, filled with air, may by itself be harmless, but thermal stresses will eventually generate cracks extending from the gap into the adjacent dielectric.

By Tom Adams, consultant, Sonoscan, Inc.

The cracks themselves may also be harmless for a time, and thus have no electrical signature. Eventually they may reach an adjacent electrode, at which time the path created by the cracks causes the high-voltage capacitor to fail (sometimes explosively).

High voltage capacitors are often imaged acoustically to pinpoint internal gaps. If a capacitor is sectioned physically through a gap found by ultrasound, tiny ceramic fragments may fall from the sectioned face. These were created by numerous cracks in the dielectric. A crack-generating non-bond may have been caused by surface contamination that prevented bonding. A void may be an air bubble trapped by the fluid ceramic or the artifact left behind by a dust particle that was trapped during fabrication and then incinerated during firing of the ceramic.

There is value to assemblers in identifying those high-voltage capacitors that harbor internal gaps in order to remove those capacitors from the assembly process. The gaps are not amenable to x-ray inspection.

But they are ideal targets for acoustic micro imaging tools. In the most frequently used imaging mode in Sonoscan's C-SAM® acoustic micro imaging tool series, ultrasound is pulsed into a capacitor and the return echoes from the non-bond, void or other gap become bright white pixels in the acoustic image of the capacitor. The ease and speed with which an acoustic micro imaging tool can find and image these defects can in part be explained by three parameters:

- 6,000 m/s - the speed of ultrasound through a typical high-voltage ceramic chip capacitor
- very close to 100 percent - the percent of arriving percent of ultrasound reflected by a solid-to-air interface such as a gap
- 0.02 micron - the minimum gap thickness needed to reflect virtually all of an ultrasonic pulse

The imaging process is this: the moving transducer is coupled to the top surface of the capacitor by an accompanying column of water, needed because high-frequency ultrasound does not travel through air. The transducer launches a pulse of ultrasound through the water column into the capacitor. The pulse travels through the capacitor until it strikes a material interface, where it will be in part reflected back to the transducer as a return echo signal. The most highly reflective interface is that between the ceramic (or any solid material) and the air in a gap. Interfaces between solids are various shades of gray.

Suppose that a very thin gap such as a non-bond lies 1mm below the surface of a high-voltage ceramic chip capacitor. If the height of the water column is 4 mm, the time for the pulse to travel from the transducer to the capacitor and return to the transducer will be about 6 microseconds. Moving at a speed that can exceed 1 m/s, the transducer collects the return echo signal from thousands of x-y locations per second. The critical imaging of a tray holding multiple capacitors, or of a single capacitor, is thus achieved quickly.

Apart from air- or gas-filled gaps, all internal material interfaces in any sample being imaged by a C-SAM tool are solid-to-solid interfaces. The percentage of ultrasound reflected by these interfaces can range from a few percent to above 95 percent. If a pulse strikes an interface where, say, 50% of the ultrasound is reflected and the other 50% transmitted across the interface, the transmitted portion will travel through presumably homogeneous material (ceramic, mold compound, metal) toward the next material interface. Here it will again be partly reflected and partly transmitted. If 70% is reflected and 30% transmitted, what is transmitted is only 15% of the original pulse. It it strikes a third interface, the reflected portion must return by the same route through the same interfaces,, and will incur the same losses. If a particular sample has enough layers. there comes a point when the reflection from a deep interface is too weak to reach the surface and the transducer.

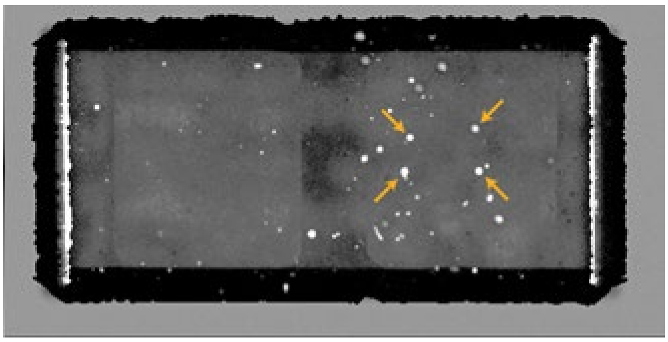

Figure 1: Small white features in this acoustic image are air-filled gaps at various depths

How, then, can meaningful echoes be received from the bottom layers of a high-voltage ceramic chip capacitor having dozens or even hundreds of layers? One would expect the return echo signals to be received only from the handful of layers nearest the top surface. The answer lies in the details of the reflection process. Every material has an acoustic impedance value - acoustic impedance being the product of the acoustic velocity (in meters per second) and density (grams per cubic centimeter) of the material. The percents of reflection and transmission are determined by the difference between the products of these two values in the two adjacent materials.

Very occasionally, however, the product is the virtually the same in both materials, even though the individual values for acoustic velocity and density are very different. It is a peculiarity of ceramic chip capacitor that the two materials - dielectric and electrode - fit this unusual pattern. Ultrasound pulsed into the top surface is reflected only minutely by each internal interface. Echoes from highly reflective structural defects can be read from any interface within the capacitor.

Figure 1 is the top-view acoustic image of a multi-layer ceramic high voltage capacitor. The image was made using a C-SAM imaging tool with a 50 MHz transducer. C-SAM transducers range from 10 MHz to 400 MHz in frequency. The purpose of the mid-range 50 MHz transducer is to provide good penetration and good resolution. This capacitor measured 33.27mm x 15.3mm x 5.33mm.

Very faintly visible at right and left are the two stacks of electrodes and dielectric within the capacitor. Each stack is roughly square, and they are separated by the irregular dark regions at the center of the part.

The return echo signals were gated on the whole thickness of the stacks - meaning that return echo signals from any depth would be displayed in the acoustic image. Gates of any thickness can be set, as well as multiple gates that will produce multiple images. In this image made by a wide gate, the depth of a particular feature cannot be determined.

The scattered small white features within the image are voids - small air bubbles that were trapped during fabrication. They are white because the interface between the capacitor (a solid) and the air (a gas) reflects essentially all of the ultrasound pulsed by the transducer. Much larger white features are sometimes seen in high voltage capacitors. They are variously called non-bonds or delaminations, and are much less common than they were a few decades ago.
The danger posed by the voids seen here is that any of them can generate a crack that will grow until it creates a pathway between two adjacent electrodes. Because of the high power levels, high voltage capacitors typically explode when the dielectric is breached. Lower power ceramic capacitors simply stop functioning.

To make Figure 2, the 5.33mm thickness of the capacitor was divided into eight equal gates, each 0.66mm thick. Gate 7 is the top image in Figure 2, and gate 8 is the bottom image. The area covered by each of the two stacks obviously changes from gate 7 to gate 8. To make these images, the transducer accepted only return echo signals from with the gate, and ignored all echoes from above or below the gate.

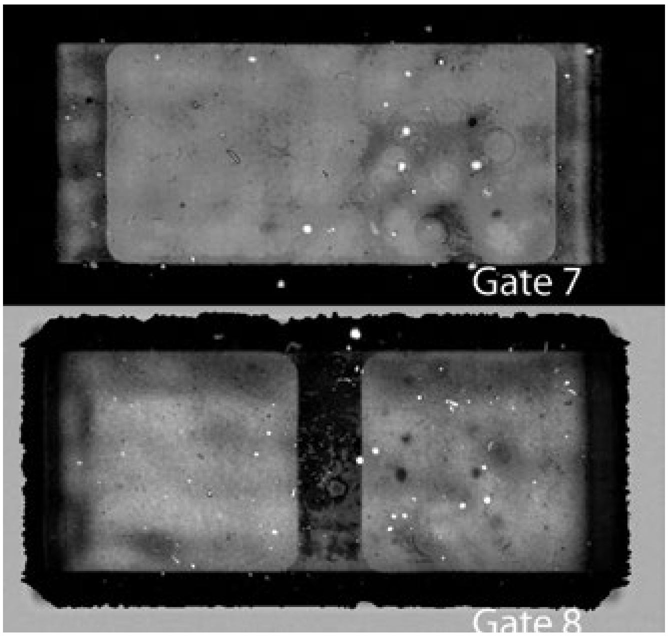

Figure 2: Of the three gaps marked by arrows in Figure 1, three are in gate 8, while the fourth is gate 7 above gate 8, and is imaged as a dark acoustic shadow

In the right half of Figure 2 are the four voids marked by arrows in Figure 1. One of the voids, however, is now black rather than white. This void lies somewhere above gate 7. Echoes returning from the gated depth are locally blocked by this void. The resulting black acoustic shadow marks the location of the above-the-gate void.

In the image of gate 8, all four of the voids are black. The one that lies an unknown distance above both gates is also somewhat more faint. The white voids in the gate 8 image all lie within gate 8.

The same capacitor was also imaged by the Q-BAM™ imaging mode, developed and patented by Sonoscan. The purpose of Q-BAM is to produce a nondestructive cross section through a part. In Figure 3, the top view is essentially the same as Figure 1; it is used here to select the vertical plane through which nondestructive imaging will be made. In Figure 1, the line between the two arrows marks the vertical plane. The part can be rotated as desired and imaged through as many planes as desired.

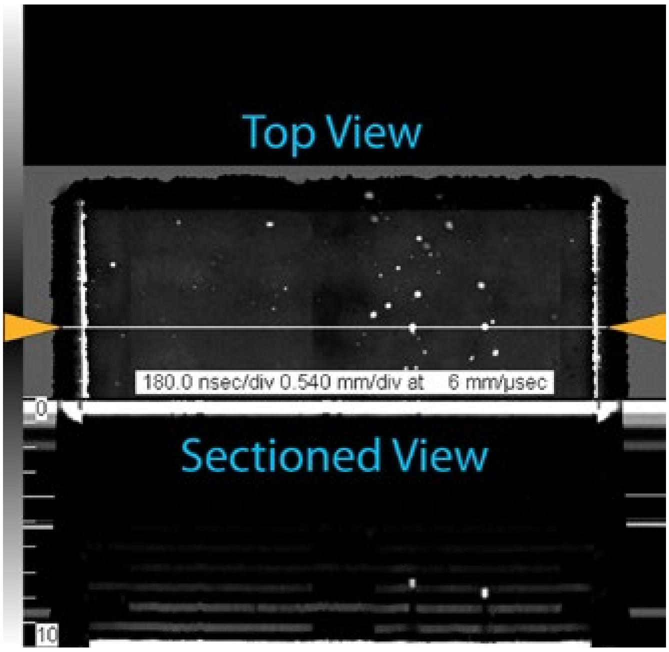

Figure 3: Line between arrows shows plane for Q-BAM nondestructive sectioning; sectioned view below shows depths of the two gaps intersected by the line

The transducer scans back and forth along this line, first collecting images from a very thin gate at the bottom of the capacitor, and then moving fractionally upward at each scan. The line of travel was chosen to include two of the voids seen in Figures 1 and 2, and to show their respective depths. Although they are both in gate 7 in Figure 2, the Q-BAM image shows that the void in the left lies slightly higher.

Several other acoustic imaging modes have been developed by Sonoscan for screening lots of high voltage capacitors or for diagnostic analysis of individual capacitors. In all cases the purpose is the same: to keep defective capacitors out of production.

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Dynamic Output Voltage Adjustment

In some applications a variable or adjustable supply voltage is a requirement. This can be for example the supply of a DC motor, when PWM modulation is not possible due to EMI reasons. Another example are power supplies for audio amplifiers. Especially Class A and A/B amplifiers with only little load have large losses. By decreasing the supply voltage these losses can be reduced significantly.

By Matthias Ulmann, Texas Instruments

Also for amplifiers working in Class D, a reduction of the supply voltage at low power increases the efficiency. This article describes different implementations how to add the feature of adjusting the output voltage to nearly any switch mode power supplies.

Analog Approach

Each switch mode power supply has an error amplifier integrated. This can be a normal operational amplifier like shown in Figure 1 or a transconductance amplifier. The function is always identical and the implementation of the output voltage adjustment can be done in the same way, too. The error amplifier compares the voltage of the feedback voltage divider (VFB) with its internal reference (VREF) and sets the duty cycle (PWM) such that the difference is zero. As the reference voltage is typically in the range of a few hundreds of millivolts up to single volts, the output voltage is divided by the feedback voltage divider (R1, R2). Between the input (FB) and the output (COMP) of the error amplifier, the compensation network is connected. Properly designed, it ensures good regulation of the output voltage under all line and load conditions.

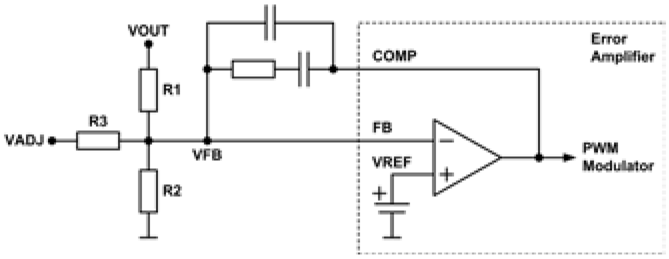

Figure 1 - Error Amplifier

These external components are typically fixed, as a converter is designed for a non-variable output voltage. By applying an external voltage (VADJ) to the feedback of the error amplifier with a defined resistor (R3), an additional current is injected which flows via the low-side resistor (R2) to GND causing an additional voltage drop. This means, the voltage on the op amp's input (FB) rises and the error amplifier reduces the duty cycle to get it back to the value of its reference voltage. This approach is called "analog" as an analog voltage is used to adjust the output voltage. Well implemented, the output voltage of the power supply is proportional to the analog adjustment voltage.

A short example shows the calculation of the three resistors.

Minimum output voltage	$V_{OUTmin} = 5.0V$
Maximum output voltage	$V_{OUTmax} = 12.0V$
Minimum adjustment voltage	$V_{ADJmin} = 0.0V$
Maximum adjustment voltage	$V_{ADJmax} = 3.3V$
Reference voltage	$V_{REF} = 0.6V$

When VADJ is set to 0.0V, resistor R3 is practically in parallel to R2. This means, the output voltage has its maximum value. When VADJ is set to 5.0V, resistor R3 generates an additional current which superimposes to the current of R1. In this case the output voltage reaches its minimum value. Important to keep in mind that the minimum output voltage is limited by the reference voltage and cannot be lower than this value.

The three resistors can be easily determined in four steps:

First, the minimum current ($I_{R1,min}$) through the high-side resistor R1 needs to be selected. Very low currents are susceptible to noise and very high currents cause needless losses. A typical value is 100µA which is used in this example as well.

Now, the high-side resistor of the voltage divider is calculated.

$$R_1 = \frac{VOUT_{min} - VREF}{I_{R1.min}}$$

$$R_1 = \frac{5.0\,V - 0.6\,V}{100\,\mu A} = 44.0\,k\Omega$$

The closest value of 44.2 kΩ is selected.

The next step is the calculation of resistor R3, which connects the external voltage with the feedback of the error amplifier.

$$R_3 = \frac{R_1 \cdot VADJ_{max}}{VOUT_{max} - VREF - R_1 \cdot I_{R1,min}}$$

$$R_3 = \frac{44.2\,k\Omega \cdot 3.3\,V}{12.0\,V - 0.6\,V - 44.2\,k\Omega \cdot 100\,\mu A} = 20.9\,k\Omega$$

The closest value of 21.0 kΩ is selected

As R1 and R3 are known, the missing resistor R2 can be determined.

$$R_2 = \frac{R_1 \cdot R_3 \cdot VREF}{R_3 \cdot VOUT_{max} - R_3 \cdot VREF - R1 \cdot VREF}$$

$$R_2 = \frac{44.2\,k\Omega \cdot 21.0\,k\Omega \cdot 0.6\,V}{21.0\,k\Omega \cdot 12.0\,V - 21.0\,k\Omega \cdot 0.6\,V - 44.2\,k\Omega \cdot 0.6\,V} = 2.62\,k\Omega$$

The closest value of 2.61 kΩ is selected.

The external voltage for adjusting the output voltage of the power supply can be generated in several ways. Most commonly a smoothened PWM signal or the output of a digital-to-analog converter (DAC) is used like shown in Figure 2.

The first method is often used because it's very simple and inexpensive. If an adjustable output voltage is needed, usually a microcontroller is somewhere in the system anyway. An output with pulse-width-modulation (PWM) capability generates a rectangular waveform, which is filtered by a low pass filter to convert it into the average DC voltage. To achieve a smooth analog voltage, the bandwidth of the low pass filter should be one decade or less below the frequency of the PWM signal. The step width of the adjustable output voltage depends directly on the resolution of the PWM signal. Another method is the usage of a DAC like the DAC5311. If different adjustable power rails are needed and the amount of PWM outputs on a microcontroller is limited, several digital-to-analog converters can be controlled in parallel by the SPI bus. Here the step width also depends on the resolution of the DAC. This family of digital-to-analog converters offers a resolution from 8 bit (DAC5311) up to 16 bit (DAC8411), so it can cover any demand regarding resolution of an adjustable output voltage for a switch mode power supply.

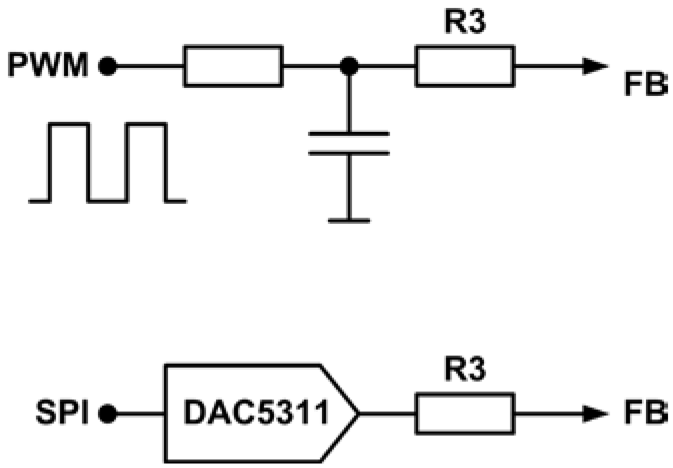

Figure 2 - Analog voltage generation

Digital Approach

For the "digital" approach, digital signals like the outputs of a microcontroller are used to directly change the output voltage of a power supply without the detour by a DAC for example. The idea behind this is pretty simple. By changing the resistance either of the high-side (R1) or the low-side resistor (R2), the output voltage can be manipulated. It is important to notice, that the high-side resistor has an impact on the compensation, more precisely on the gain. If the value of this resistor is changed, the gain of the compensation network changes which can lead to instability and different behavior dependent on the output voltage. Besides that it is also not easy to change its resistance as it is floating and not referred to ground. The better method is manipulating the low-side resistor. It has no impact on the compensation and thus the behavior of the converter will always stay the same. Additional resistors, which can be switched by logic-level FETs are put in parallel to the fixed low-side resistor (R2). The example in Figure 3 shows a so-called VID interface (Dynamic Voltage Identification) with two bits. If a FET is driven by the digital output of a microcontroller, the corresponding resistor is switched in parallel to the fixed resistor R2. The overall resistance decreases and therefore the output voltage increases. With two bits, four different voltage levels can be set. Dependent on the demands, more steps can be added.

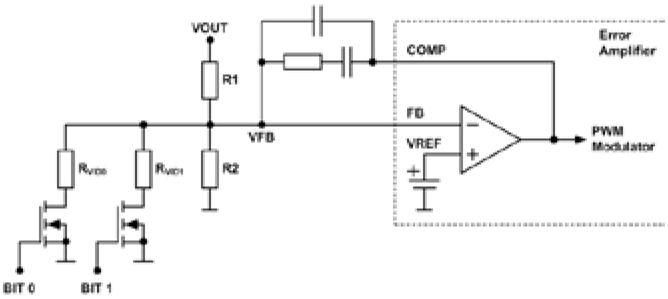

Figure 3 - VID Interace

For this example the specification of the analog approach is used again:

First, the minimum current ($I_{R1,min}$) through the high-side resistor R1 needs to be selected. 100µA is also used here.

Now, the high-side resistor of the voltage divider is calculated.

$$R_1 = \frac{VOUT_{min} - VREF}{I_{R1,min}}$$

$$R_1 = \frac{5.0\,V - 0.6\,V}{100\,\mu A} = 44.0\,k\Omega$$

The closest value of 44.2 kΩ is selected.

R2 is the fixed low-side resistor which is always connected between the feedback of the error amplifier and ground.

$$R_2 = \frac{R_1 \cdot VREF}{VOUT_{min} - VREF}$$

$$R_2 = \frac{44.2\,k\Omega \cdot 0.6\,V}{5.0\,V - 0.6\,V} = 6.03\,k\Omega$$

The closest value of 6.04 kΩ is selected.

The number of steps depend on the number of bits of the VID interface. As example, four bits (0, 1, 2, 3) enable 16 steps. A single step is calculated with the following equation.

$$VSTEP = \frac{VOUT_{max} - VOUT_{min}}{2^{BITS} - 1}$$

$$VSTEP = \frac{12.0\,V - 5.0\,V}{2^4 - 1} = 467\,mV$$

Theoretically, this calculation has to be done for each bit, so four times in this example (BIT 0, 1, 2, 3). But it is sufficient to do it only for bit 0 and then just use 1/2, 1/4 and 1/8 for the other three remaining values.

The closest value of 56.2 kΩ is selected
With the four switchable resistors parallel to the fixed resistor R2, the output voltage can be set between 5.0V and 12.0V in 16 steps.

A similar, but more integrated solution can be implemented with a digital potentiometer like the TPL0401A-10 shown in Figure 4.

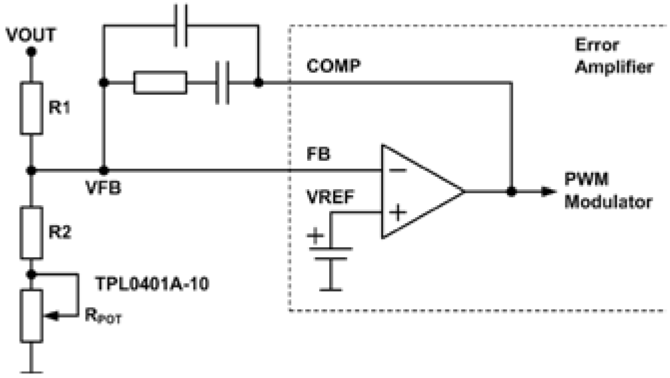

Figure 4 - Digital Potentiometer

The potentiometer RPOT is in series with the low side resistor R2 and controlled by either I2C or SPI. This specific device has 128 taps, so its functionality is similar to a discrete VID interface with 7 bits. It is important not to use it as the feedback voltage divider itself, otherwise the high-side resistance will change dependent on the output voltage and thus have an impact on the compensation as explained at the beginning.

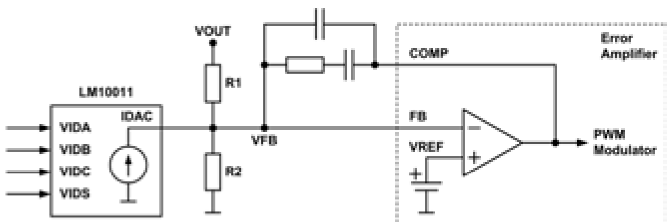

Figure 5 - LM10011 VID Programmable Current DAC

Digital-Analog Approach
The third approach is the "digital-analog", which uses a combination of both solutions shown. It is based on Texas Instruments LM10011V VID programmable current DAC. This device has four logic inputs, which are driven in the same manner like described in the digital approach. The output of the device is not a voltage, but a current, which

is fed directly into the low-side resistor R2 of the voltage divider as shown in Figure 5. Similar to the analog approach, this programmable current in the range of 0 to 59.2 µA causes an additional voltage drop on the low-side resistor and thus controls the output voltage of the power supply.

It can be used either in 4 bit or 6 bit mode, thus providing 16 and respectively 64 steps for adjustment of the output voltage. The advantage is the smaller solution size compared to a discrete setup and it's compatibility to TI's TMS320 DSPs which control their supply voltage autonomously dependent on the load.

Conclusion

Typically, a power supply provides only a fixed output voltage. But in some applications it is neccesary or desirable to change this voltage in a certain range. This article describes three different approaches of expanding this functionality to practicallly all power supplies. Almost any signals like PWM, simple logic, SPI/I2C or dedicated VID interfaces can be used. The speed of change of the output voltage depends mainly on the bandwidth of the converter and less of the control circuit.

Matthias Ulmann was born in Ulm, Germany, in 1980. He was awarded a degree in electrical engineering from the University of Ulm in 2006. After working for several years in the field of motor control and solar inverters (specialized in IGBT-drivers), he joined TIs' Analog Academy for a one year trainee program. Since 2010 he has worked in the EMEA Design Services Group as a Reference Design Engineer in Freising, Germany. His design activity includes isolated and non-isolated DC/DC converters for all application segments. He was elected "Member, Group Technical Staff" in 2015

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Increasing Power Density and Improving Efficiency

While the creation of SiC substrate wafers was described in part 1 in BPS January 2017 and possible structures of SiC devices were the subject of part 2 in BPS February 2017, this third part will focus on the finished products.

By Aly Mashaly, Manager Power Systems Department, Rohm Semiconductor GmbH

Packages for SiC Semiconductors

Basically, SiC diodes and MOSFETs can be used for all kinds of standard packages (discrete devices and modules). Discrete devices can be grouped into two categories: THT devices (through hole technology) and SMDs (surface-mounted devices). For package design, it is necessary to understand and consider the physical properties of SiC. For instance, parasitic inductances within the package are more significant in SiC semiconductors than in Si IGBTs because of the faster switching times of SiC devices. Therefore, Rohm makes intensive efforts to reduce the parasitic inductances within the discrete devices and modules.

Rohm began mass-producing of initial commercial SiC products in 2010. Since then, the company expanded its product lines across different power categories in order to meet the requirements of industrial and automotive applications. Rohm's product offering includes discrete devices (THT and SMD) as well as modules. As a semiconductor manufacturer, Rohm also provides its products as SiC wafers (bare die) and co-operates with major module manufacturers to expand the worldwide SiC market.

Rohm's offering of second-generation SiC-SBDs currently includes 650V products from 5A to 100A as well as 1200V and 1700V versions for up to 50A. In 2016, Rohm started volume production of third-generation SiC-SBDs for 650V and currents up to 10A.

In the SiC MOSFET segment, Rohm's product portfolio is even larger featuring two different technologies (planar and double trench). Planar technology is already available in discrete devices and modules for 650V, 1200V and 1700V and current levels up to 300A.

Rohm starts its volume production of third-generation SiC MOS products with discrete devices and full-SiC modules based on its proprietary double trench technology, which will expand the existing MOSFET product family and contribute to the evolution of highly efficient, highly reliable power electronics.

New 1700V SiC MOSFETs for SMPS Applications

Switch-mode power supplies (SMPS) are among the most important elements of all power electronic systems. After all, it is impossible to implement the functionality of the main system without a suitable power supply. Basically, the SMPS subsystem acts as the internal power supply for all electronic subassemblies of a power electronic system, providing the necessary supply voltages for the microcontroller, the sensors and the drivers of the main power semiconductors. As the industry's most popular SMPS topology, fly back converters of up to several hundred Watts transfer electrical energy between a DC input and a galvanically isolated DC output. In practical applications, a Si MOSFET is used as the main switch with switching frequencies typically ranging between 16kHz and 500kHz. Higher switching frequencies enable the use of smaller inductors, although high losses in the Si MOSFET and the diode are a limiting factor. Rohm's new 1700V SiC MOSFET is excellently suited for these applications because of its efficient switching behavior and low Rdson. Rohm provides the 1700V SiC MOSFET in the TO-3PFM and the TO268-2L package (see Figure 1).

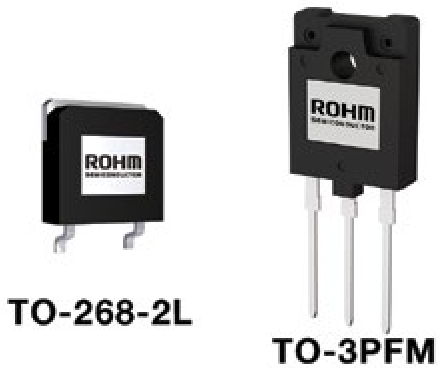

Figure 1: Rohm's 1700V SiC MOSFET is available in two different package options

Thanks to its high electrical field strength, the SiC MOSFET maintains its low on resistance per chip area even at high breakdown voltages. Figure 2 shows a comparison between Rohm's newly developed 1700 SiC MOSFET and the best in class Si MOSFET available in the market, which is typically, used in fly back applications. The 1700V SiC MOSFET features a much lower on-state resistance (Rdson) than the 1500V Si MOSFET. Values of 0.75Ω/1.15Ω have been achieved with the SiC MOSFET, while the Si MOSFET features 9Ω, although the SiC MOSFET's die size is 17-times smaller than the die size of the Si MOSFET.

Using the 1700V SiC MOSFET (SCT2H12NY) in a TO268-2L package greatly improves the on-state resistance and the current capability compared to the Si MOSFET with the same package. Thanks to the SiC MOSFET's very low capacitance values (Ciss and Coss), switching frequencies beyond 100kHz can be used without any thermal problems, enabling a miniaturization of the inductive components and the space of printed circuit board. Furthermore, automated board assembly using a SMD line is enabled by the use of the TO268-2L SMD package, resulting in a significant reduction of production costs and finally total costs. In order to achieve optimum switching behavior of the SiC MOSFET in a flyback topology, Rohm designed a special driver (BD768xFJ-LB) with a dedicated controller in a SOP-J8S package.

In a three-phase 400VAC industrial application, two series-connected Si MOSFETs are typically used for flay back converter as the main switch to provide sufficient voltage headroom for the main switch in

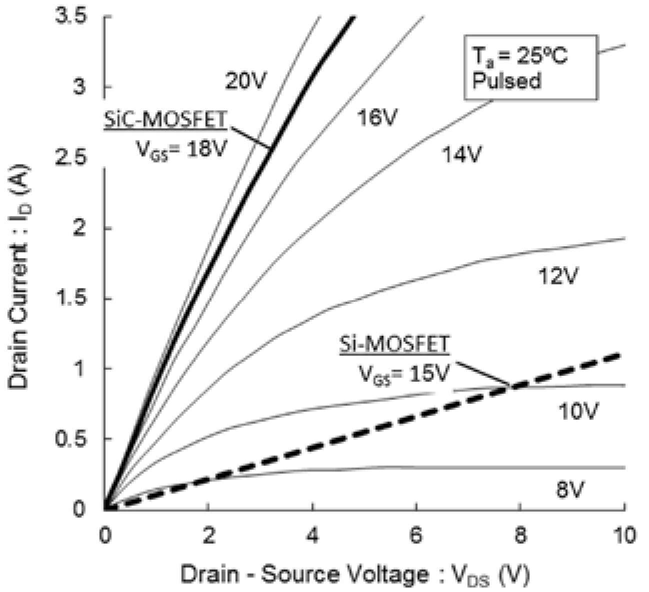

Figure 2: Conduction behavior of Rohm's 1700V/1.15Ω SiC MOSFET compared to a 1500V/9Ω Si MOSFET

the off state. Thanks to the availability of Rohm's new 1700V SiC MOSFET, the two Si MOSFETs can be replaced by a single SiC MOSFET.

High Efficiency in Drive Applications
Industrial applications including drive inverters, which require sine filters at the output of the inverter, can benefit from the advantages provided by SiC. Examples include motor drive inverters whose power is in the double-digit kilowatt range. The motor and the inverter can be connected by cables of up to 100 meters in length. A sine filter is often used at the output of the inverter in these applications.

Output filters of this kind enable the use of unshielded cables, which reduces total equipment costs dramatically. As an additional advan-

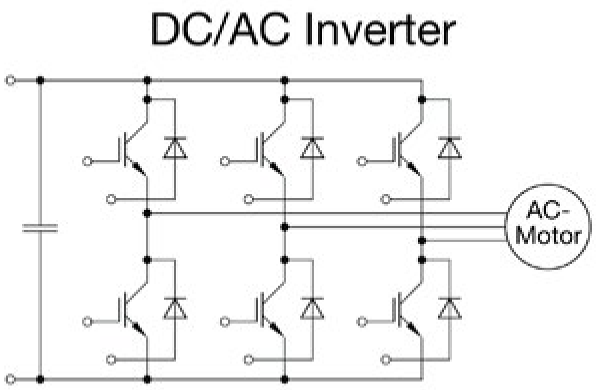

Figure 3: Standard topology of a drive inverter

tage, these filters lead to much lower high-frequency currents in the motor windings, which in turn results in reduced power losses in the motor. This, in consequence, will improve the motor's thermal behavior and reduce its noise level significantly. All in all, a sine filter will have a positive impact on the lifetime and reliability of the entire system. However, in high-power equipment the sine filter will account for most of the application's volume. It would therefore be an interesting proposition to reduce the filter's size and cost, which can be basically done by increasing the switching frequency of the semiconductors in the inverter.

By default, Si IGBT technology is used in these applications at switching frequencies around 10kHz. IGBTs cannot be used in applications with elevated switching frequencies due to the high power losses and the resulting thermal stress in the inverter.
With its excellent physical properties, SiC opens new doors to this kind of sophisticated applications. In particular, SiC enables the use of high switching frequencies without causing excessive thermal stress in the inverter.
Two benefits result from using high switching frequencies: The output filter can be smaller and the resonance behavior of the entire system will improve accordingly.

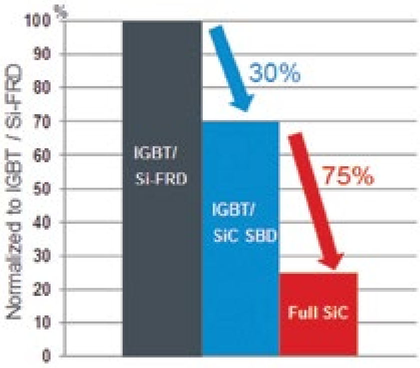

Figure 4: Comparison between a Si IGBT, a hybrid configuration and a Rohm full-SiC module

Figure 4 compares the switching losses of a Si IGBT technology and Rohm's SiC technology in a standard inverter topology (see Fig. 3). The comparison is based on a DC link voltage (Vdc) of 600V, a motor phase current (Imotor) of 200A and a switching frequency (Fsw) of 10kHz.

For the data in Figure 4, the loss was normalized to the combination of Si IGBT and Si FRD (black bar). In a hybrid configuration consisting of a Si IGBT and a SiC SBD as an antiparallel freewheeling diode, switching losses will be 30% lower (blue bar). If a full-SiC module from Rohm (SiC MOSFET and SiC SBD) is used in this topology, switching losses will be reduced significantly (red bar).

Figure 5: Full-SiC module based on Rohm's trench technology

The world's first full SiC module based on Rohm's newly developed trench technology is shown in Figure 5. Featuring a breakdown voltage of 1200V, the module supports a drain current of 180A. Rohm is increasing its line up from Modules continuously and offers now modules up to 600A.

Reverse Conduction of SiC

As described in part 2 of this article series, a parasitic inverse PN diode (body diode) is present in every SiC MOSFET. In commutation loops of power electronic systems with series inductors, some current flows in this body diode when the SiC MOSFET is in the off state. Like all PN diodes, a forward voltage occurs at the diode when a current is flowing through it. Physical properties of SiC MOSFETs include a wide band gap, which results in a high voltage drop at the body diode. During the design phase of a system, power electronic designers should explore how often the body diode will be used during switching transitions. The high voltage drop results in high thermal losses if a large share of the current flows through the body diode. In addition, switching time plays an important role in thermal design.

As one of the options available to eliminate this high voltage drop, it is possible to benefit from a specific physical property of SiC MOSFETs called reverse conduction (see Figure 6). The mechanism behind reverse conduction is based on the fact that the channel of a SiC MOS-

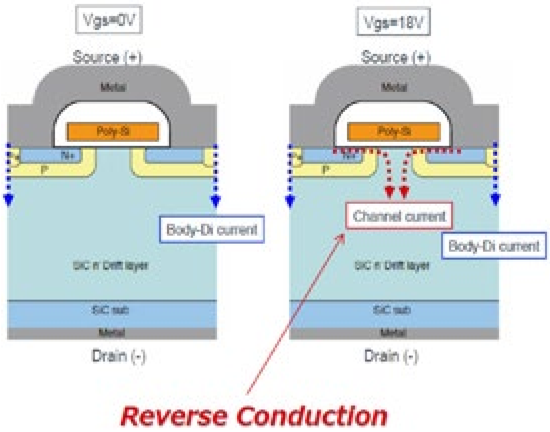

Figure 6: Reverse conduction of SiC

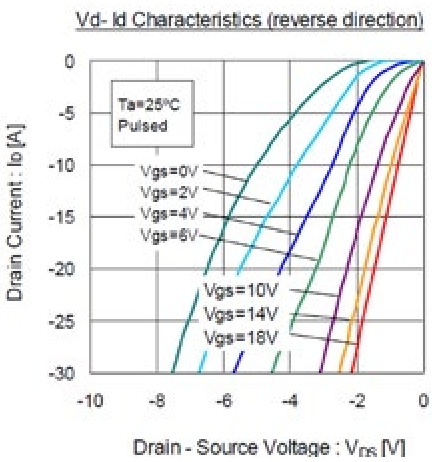

Figure 7: The voltage drop will decrease when the MOSFET channel is turned on again

FET can be turned on again even if the MOSFET is reverse biased. The reverse current will then flow through the SiC MOSFET channel instead of the body diode. As depicted in Figure 7, the voltage drop between drain and source will decrease if the gate voltage increases. A gate voltage of Vgs = 18V will yield optimum results.

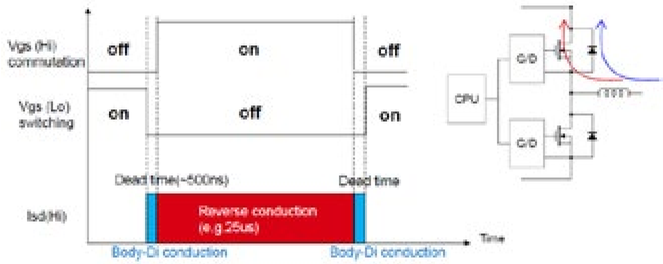

Figure 8: Using reverse conduction in the half-bridge topology

How can this reverse conduction effect be used and adjusted in applications based on half-bridge configurations?

The half-bridge configuration is a very popular topology in power systems including inverters and DC/DC converters. It consists of two switches or SiC MOSFETs (high-side switch and low-side switch). In the half-bridge topology, the complementary driver signals generated by the microcontrollers are adapted to the MOSFETs by gate drivers to ensure the functionality of the system. A dead time must be inserted between the transitions of both switches to prevent a short circuit in the DC link. The current will flow through the body diode during the dead time. After the dead time, the MOSFET, which previously was in the off state, can be turned on again although it is reverse-biased. As shown in Figure 8, the current will flow through the body diode only during the dead time (blue arrow) before the MOSFET channel is turned on again to let the current flow though the MOSFET channel (red arrow). This reverse conduction can be implemented via the software running on the microcontroller.

About Rohm Semiconductor

Rohm Semiconductor is a leading supplier of systems, LSIs, discrete devices and modules. Using latest semiconductor process technologies and state-of-the-art automation technology for proprietary manufacturing systems, Rohm can maintain its leading position through high operative expertise and outstanding product quality.

In 2015, the Rohm Group recorded sales of 3 billion dollars with 20,843 employees. Rohm provides a wide portfolio of IEC-Q-qualified products for the automotive industry, ranging from standard products including transistors, diodes, EEPROMs, operational amplifiers, comparators and LDOs to ASIC and ASSP products including LED drivers, motor drivers and optimized gate drivers for engine control units (ECUs).

Furthermore, Rohm provides leading technologies for the new generation of power products, resulting in breakthrough performance with respect to efficiency, heat generation and compactness. New products and materials like SiC MOSFETs and full-SiC modules were developed for this purpose.

Rohm makes unmatched contributions with its energy-efficient, future-oriented solutions especially tailored to meet the requirements of the automotive market.

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State of the SiC MOSFET

Device evolution, technology merit, and commercial prospects

By Kevin M. Speer, PhD, Littelfuse Inc.
Dr. Sujit Banerjee, PhD, and Kevin Matocha, PhD, Monolith Semiconductor Inc.

Introduction

It is highly unlikely that anyone reading this article is unfamiliar with the insulated gate bipolar transistor (IGBT). This disruptive power transistor, first commercialized in the early 1980s, has had an enormous positive impact on the power electronics industry, enabling innovative converter design, improved system efficiencies, and worldwide energy savings. Indeed, some estimates suggest the IGBT has helped forestall 75 trillion pounds of CO2 emissions over the past 25 years [1].

Much as the IGBT was revolutionary in the 1980s, today the wide band gap semiconductor silicon carbide (SiC) shows increasing promise for revolutionizing the power electronics world once again. The IGBT gave us a transistor simultaneously capable of blocking high voltages with low on-state (i.e., conduction) losses and well-controlled switching. The device is limited, however, in how fast it may be switched, which leads to high switching losses, large and expensive thermal management, and a ceiling on power conversion system efficiency. The advent of SiC transistors all but eliminates an IGBT's switching losses for similar on-state losses (lower, actually, at light load) and voltage-blocking capability, enabling unprecedented efficiency in addition to reducing the overall weight and size of the system.

Like most disruptive technologies, however, the evolution of commercial SiC power devices has traveled a tumultuous road. This article is intended to put the evolution of the SiC MOSFET in context, and – along with an abridged history of the device's advancements – present its technology merits today and its commercial prospects for the future.

Early days of silicon carbide

Although device-related SiC materials research had been underway since the 1970s, the promise of SiC for use in power devices was most formally suggested by Baliga in 1989 [2]. Baliga's figure of merit served as additional motivation for aspiring materials and device scientists to continue advancing SiC crystal growth and device processing techniques. In the late 1980s, intense efforts were underway around the world to improve the quality of SiC substrates and hexagonal SiC epitaxy – needed for vertical SiC power devices – at places ranging from institutes like Kyoto University and AIST in Japan to the Ioffe Institute in Russia to the University of Erlangen and Linkoping in Europe to SUNY-Stony Brook, Carnegie Mellon, and Purdue University in the United States, to name just a few. The improvements continued throughout much of the 1990s, until the first commercial device was released in 2001 in the form of a SiC Schottky diode by Infineon.

For a few years following their release, SiC Schottky diodes experienced field failures that were traced to material quality and device architecture. Rapid and drastic progress was made to improve the quality of substrates and epitaxy; meanwhile, a diode architecture known as the junction barrier Schottky (JBS) was used which more optimally distributed the peak electric field. In 2006, the JBS diode morphed into what is now called the merged p-n Schottky (MPS) structure, which maintains optimal field distribution but also allows for enhanced surge capability by incorporating true minority carrier injection [3]. Today, SiC diodes are so reliable that they have demonstrated even more favorable FIT rates than silicon power diodes [4].

MOSFET alternatives

The first SiC power transistor released to the market came in 2008 in the form of a 1200 V junction field effect transistor (JFET). SemiSouth Laboratories followed the JFET approach because, at the time, the bipolar junction transistor (BJT) and MOSFET alternatives had impediments that were thought to be insurmountable. Although the BJT had impressive current-per-active-area figures, the device had three major shortcomings: First, the high current required to switch the BJT

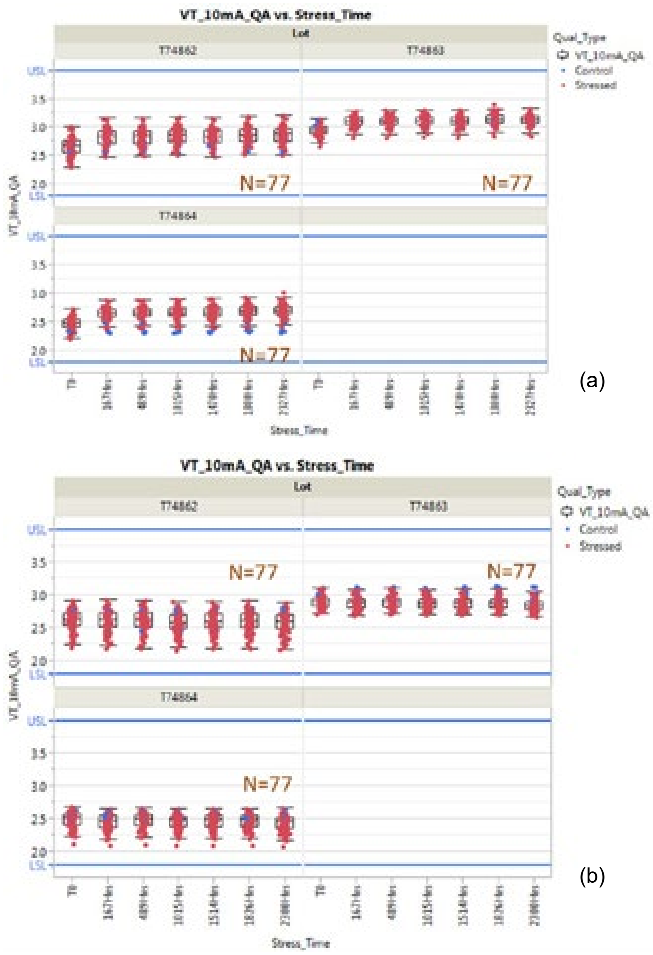

Figure 1: (a) Positive, VGS = +25 V, and (b) negative, VGS = -10 V, high-temperature gate bias (HTGB) stress tests performed at 175°C on 77 devices from three different wafer lots out to 2300 hours. Negligible diviation in threshold was observed.

was frowned upon by many designers accustomed to using voltage-controlled devices like the MOSFET or IGBT. Second, the BJT's drive current is conducted across a base-emitter junction with a large built-in potential, leading to substantial power losses. Third, because of the bipolar action of the BJT, it was particularly susceptible to a device-killing phenomenon known as bipolar degradation [5].

The JFET, on the other hand, is hindered by the fact that it is a normally on device, which can scare away many power electronics designers and safety engineers. Of course it is possible to design around this, but simplicity and design elegance are underrated virtues in the engineering world. SemiSouth also had a normally off JFET, but it proved far too difficult to manufacture in volume. Today, USCi, Inc. offers a normally on SiC JFET co-packed with a low-voltage silicon MOSFET in a cascode configuration [6], an elegant solution for many applications. Nevertheless, the holy grail of SiC power devices has always been the MOSFET due to its similarity in control to the silicon IGBT – but with the aforementioned superiority in performance and system benefits.

Evolution of the SiC MOSFET

The SiC MOSFET has had its share of issues, most of which are directly related to the gate oxide. The first signs of trouble were observed in 1978 when researchers at Colorado State University measured a messy transition region between the pure SiC and the grown SiO_2 [7]. Such a transition region was known to have high densities of interface states and oxide traps that inhibit carrier mobility and lead to instabilities in threshold voltage; this would later be proven true by too many research publications to name. Many in the SiC research community spent the late 1980s and 1990s further studying the nature of various interface states in the SiC-SiO_2 system.

Research in the late 1990s and early 2000s led to remarkable improvements in understanding the sources of interface states (whose density is abbreviated Dit), as well as reducing them and mitigating their negative effects. To mention a few noteworthy discoveries, oxidation in a wet environment – that is, using H_2O as an oxidation agent instead of dry O_2 – was observed to reduce Dit by two to three orders of magnitude [8]. Also, the use of off-axis substrates was found to reduce Dit by at least an order of magnitude [9]. Last but certainly not least, the effects of post-oxidation annealing in nitric oxide – a process commonly called nitridation – were first discovered by Li and co-workers in 1997 to reduce Dit to very low levels [10]. This was subsequently affirmed by six or seven other groups, a set of work that is nicely summarized in a paper by Pantelides [11]. It would be an egregious omission, of course, not to underscore the seminal contributions made by the bulk growth and wafer research community, who have taken us from mere Lely platelets to 150 mm wafers that are virtually free of device-killing micropipes.

Published research progress on the SiC MOSFET slowed somewhat over the next few years, as hopeful suppliers were busy making advancements they wanted to commercialize. However, the stage had been set for final improvements directed at further tightening threshold voltage stability as well as process enhancements and screening to ensure reliable gate oxides and completion of device qualification. In essence, the SiC community was getting ever closer to finding the holy grail.

Today's MOSFET quality

In just the past two years, commercially available 1200 V SiC MOSFETs have come a long way in terms of quality. Channel mobility has risen to suitable levels; oxide lifetimes have reached an acceptable level for most mainstream industrial designs; and threshold voltages have become increasingly stable. What is equally important from a commercial standpoint is that these milestones have been reached by multiple suppliers, the importance of which is saved for a later section. Here we substantiate claims of today's SiC MOSFET quality, including long-term reliability, parametric stability, and device ruggedness.

Using accelerated time-dependent dielectric breakdown (TDDB) techniques, the oxide lifetime of Monolith Semiconductor's MOS technology has been predicted by researchers at NIST to exceed 100 years, even at junction temperatures higher than 200 °C [12]. The NIST work used lifetime acceleration factors of applied electric field across the oxide (greater than 9 MV/cm) and junction temperature (up to 300 °C); for reference, oxide electric fields used in practice are around 4 MV/cm (corresponding to VGS = 20 V), and junction temperatures during operation are typically lower than 175 °C. It is also worth noting that while a temperature-dependent acceleration factor is commonly seen in silicon MOS, it had not been seen by NIST for SiC MOS prior to their work with devices from Monolith Semiconductor.

Next, threshold voltage stability has been convincingly demonstrated, as seen in Figure 1.High-temperature gate bias (HTGB) was performed at a junction temperature of 175 °C and under negative (VGS = -10 V) and positive (VGS = 25 V) gate voltages. As dictated by JEDEC standards, 77 devices from three different wafer lots were tested, and no significant shift has been observed.

Still another parameter set proven to be stable over the long term is the blocking voltage and off-state leakage of our MOSFETs. Figure 2 shows high-temperature reverse bias (HTRB) test data. More than eighty samples were stressed for 1000 h at VDS = 960 V and

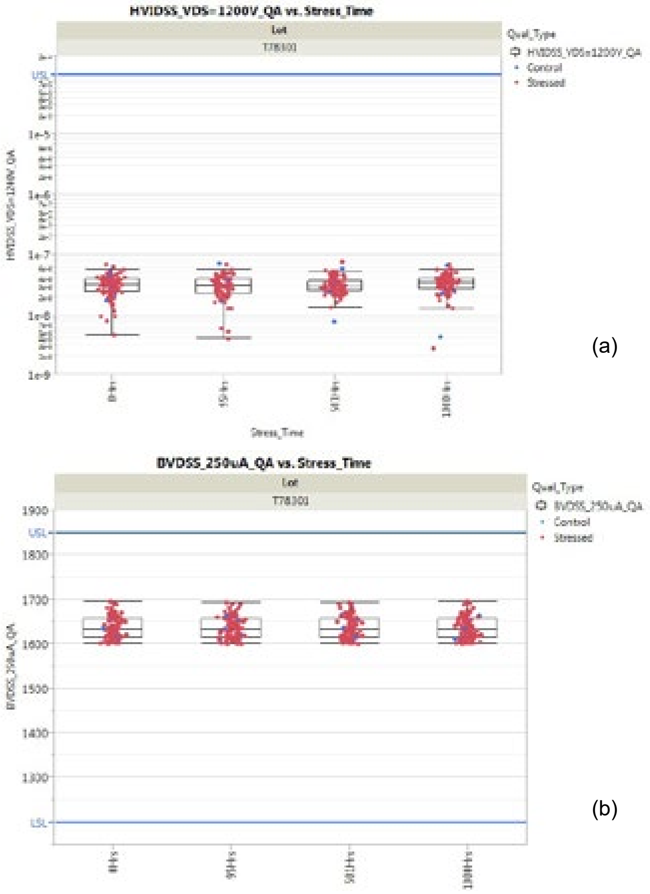

Figure 2: High-temperature reverse bias test data on 82 samples after 1000 h of stress at VDS = 960 V and Tj = 175 °C, illustrating no change in (a) drain leakage at VDS = 1200 V or (b) blocking voltage at ID = 250 µA.

Tj = 175 C, after which post-stress measurements revealed no change in drain leakage or blocking voltage . With respect to device ruggedness, preliminary measurements shown in Figures 3 and 4 reveal a short-circuit withstand time of at least 5 microseconds and an avalanche energy of 1 J.

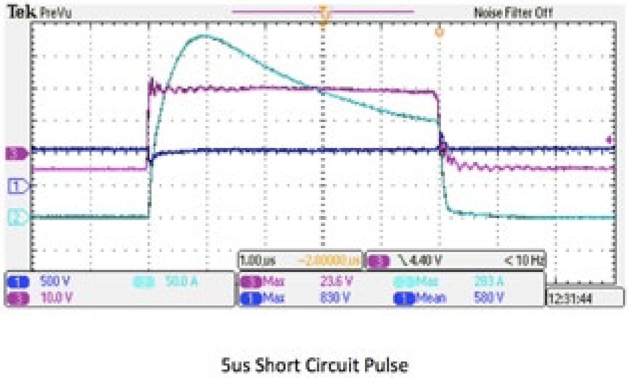

Figure 3: Short-circuit testing of a 1200 V, 80 mΩ SiC MOSFET at a dc link of 600 V and VGS = 20 V, indicating a withstand time of at least 5 µs

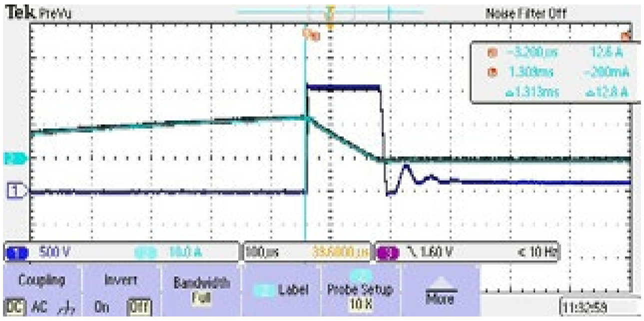

Figure 4: Avalanche ruggedness test on a 1200 V, 80 mΩ SiC MOSFET, showing that 1.4 J of energy was safely absorbed in the device with Ipeak = 12.6 A and L = 20 mH.

Although we cannot speak to the long-term reliability or ruggedness of other manufacturers' products, we can say that based on our evaluation of commercially available SiC MOSFETs, there now appear to be multiple suppliers in the marketplace capable of supplying production-level quantities of SiC MOSFETs. These devices appear to have acceptable reliability and parametric stability, which will surely encourage mainstream commercial adoption.

Commercial prospects

In addition to quality improvements, the past few years have seen tremendous commercial progress. Multiple SiC MOSFET suppliers are available to satisfy customers' second-source concerns in addition to creating a competitive landscape that is good for both suppliers and users. As previously mentioned, the fact that multiple SiC MOSFET suppliers have adequately reliable devices has been an enormous advancement, given the device's lengthy evolution. Figure 5, reproduced with permission from Yole Développement's "2016 Power SiC" report [13], shows the status of SiC MOSFET activities from various suppliers as of July 2016. Commercially available parts have been released from Wolfspeed, ROHM, ST Microelectronics, and Microsemi; the community can expect offerings soon from Littelfuse and Infineon.

Multi-chip power modules are also a hot topic in the SiC world among customers and suppliers alike. Figure 6, also taken from Yole's Développement's 2016 report [13], shows the status of SiC module development activities. We believe many bright opportunities remain for SiC MOSFETs in discrete packages, as best layout practices of both the control and power circuits can easily extend the applicability of discrete solutions to tens of kilowatts. Higher power levels and the motivation to simplify system design will drive SiC module development efforts, but the importance of optimizing parasitic inductance from the package, control circuit, and surrounding power components cannot be overstated.

The final elephant in the room when it comes to the commercial prospects of the SiC MOSFET is price. Our view on price erosion is favorable, largely due to two aspects of our approach: first, our devices are manufactured in an automotive-grade silicon CMOS fab; second, the process is run on 150 mm wafers. This is explained in greater detail in a separate work [14], but suffice it to say that the central advantages of utilizing existing silicon CMOS fabs are the absence of capital expenses and an optimization of operating expenses, both of which would otherwise be passed to the end customer. Furthermore, manufacturing on 150 mm wafers produces more than double the devices as compared to 100 mm wafers, which dramatically impacts the per-die cost. Some indication of pricing is given in Figure 7, based on a sur-

vey taken from commercially available SiC MOSFETs at Digi-Key. As an example, since the first announcement at Digi-Key six years ago, the price of a 1200 V, 80 mΩ device in TO-247 has fallen by more than eighty percent, even if the SiC MOSFET is still 2-3x more expensive than a comparable silicon IGBT. Designers are already viewing substantial system-level price benefits using SiC MOSFETs over Si IGBTs at today's price levels, and we expect SiC MOSFET pricing will continue to fall as economy of scale takes hold with 150 mm wafers.

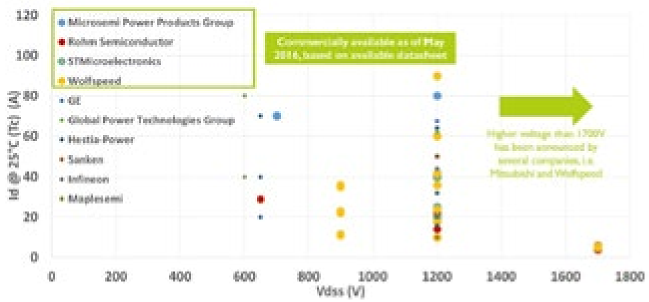

Figure 5: Status of SiC MOSFET development activities by various suppliers [13, reproduced with permission].

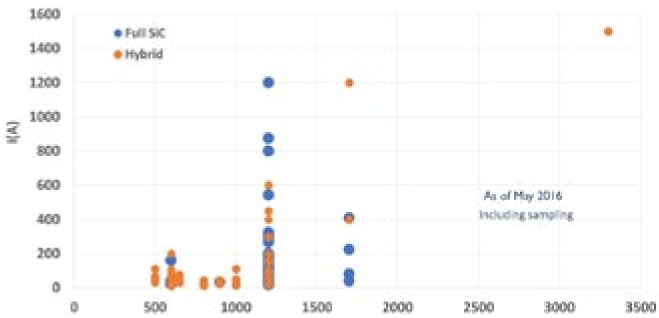

Figure 6: Status of SiC power module development activities [13, reproduced with permission]. Blue circles represent modules with only SiC devices, while orange circles depict modules that use silicon transistors and SiC diodes.

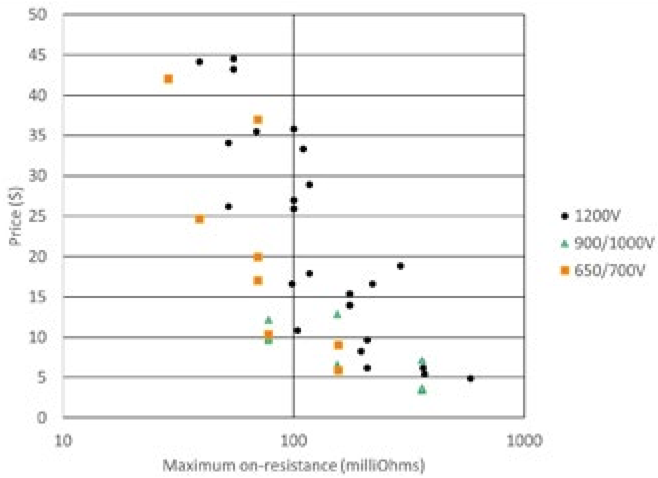

Figure 7: Price survey of commercially available SiC MOSFETs as seen at Digi-Key [www.digikey.com].

Conclusions

The silicon IGBT was an enormous positive disruption to the power electronics community in the 1980s, and it has been the workhorse of the industry ever since. The next revolutionary technology will be the SiC MOSFET. Today's state of the SiC MOSFET indicates resolution on major commercial impediments including price, reliability, ruggedness, and diversification of suppliers. In spite of a price premium over Si IGBTs, the SiC MOSFET has already seen success due to cost-offsetting system-level benefits; the market share for this technology will increase sharply over the next few years as materials costs fall. After more than forty years of development effort, at last the SiC MOSFET appears poised for widespread commercial success and a substantial role in the green energy movement.

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www.littelfuse.com

www.monolithsemi.com

High Current Welding Diodes for Demanding Industrial Applications

The specific requirements for resistance welding, even though it is not a high profile power electronics application, led to a continuous development of a family of application specific devices. In this article, we'll take a closer look at the application itself, the requirements the power semiconductors must meet the load cycle testing and the components which have been developed to meet these demands. Finally, trends in new product releases in the near future are discussed.

By Ladislav Radvan, ABB s.r.o. Semiconductors

Resistance welding

Resistance welding is a technique used mainly for joining sheets of metal. It involves the generation of heat by passing a current through the contact resistance between metal surfaces. Small pools of molten metal are formed at the weld area when the high current is passed through. Once the area is cooled down, a solid joint is established. Following Figure 1 is showing major real and parasitic resistances in the secondary loop of the weld transformer. It demonstrates importance of excellent diode forward characteristics. The welding diode must have a low resistivity in the circuit to be successful in terms of efficiency and life-time. Any additional losses lead to higher diode stress in the application.

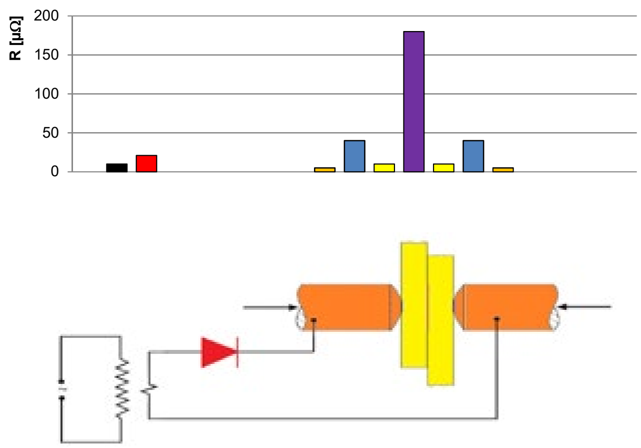

Figure 1: Weld circuit resistance. The colors represent the different parts and their respective resistances.

Compared to other welding methods, resistance welding is very efficient, as it causes little pollution and limited work piece deformation. It has high production rates, can easily be automated and requires no filler materials. Therefore, it is used extensively in the automotive industry, as most cars have several thousand spot welds made by industrial robots.

Welding circuit principle

The electrical circuit of the resistance welding system consists of 4 parts as shown in Figure 2:

- A frequency converter, which generates a single-phase, quasi-square wave voltage and current of the wished frequency from a 3-phase sine wave. Typically, welding units are assembled together with the IGBT inverter. The output from the inverter is connected to the primary side of the transformer. The wave shape is a PWM rectangular pulse pattern with the typical frequency of 1 kHz and an amplitude of 560 V.
- A transformer with a secondary voltage in the range of 6 – 20 V, with 10 V is the most common. The secondary current is often in the range of 10 – 20 kA but can be even higher for Aluminium welding.
- A diode rectifier to convert the quasi-square wave current to DC-current. This is done since the welding quality is much better when using DC instead of AC. The connection of choice is type M2 to reduce the number of diodes required for the rectification. When higher currents are needed, the capability is increased by having two or more diodes connected in parallel.
- A welding gun with water-cooled electrodes between which the metal sheets to join are pressed.

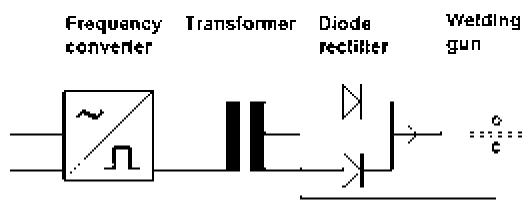

Figure 2: A typical welding circuit

Required performance of diodes for welding applications

For each car model, a customised welding system is designed. In the automotive industry, the transformer, the rectifier and the welding gun are often placed on a robot arm. Thus, size and weight is of great importance. Since increased frequency reduces the size of the transformer at equal power, the trend is to increase the frequency from the 1 kHz used today to about 10 kHz or possibly even 20 kHz.

Specific materials also need specific weld sequence and requirements. Each material has a so called plastic temperature range where it can be easily deformed, melted and joint under applied force. Steel materials and alloys feature a wide plastic temperature range and thus are easy to fusion weld. On the other hand, pure metals like copper and aluminum, which are highly conductive (thermally and electrically), have a narrow plastic temperature range. They require more precise timing, short weld time and higher current levels (see

Figure 3). Therefore, new 10 kHz welding systems were developed. All presented application aspects are reflected in the features of ABB welding diodes.

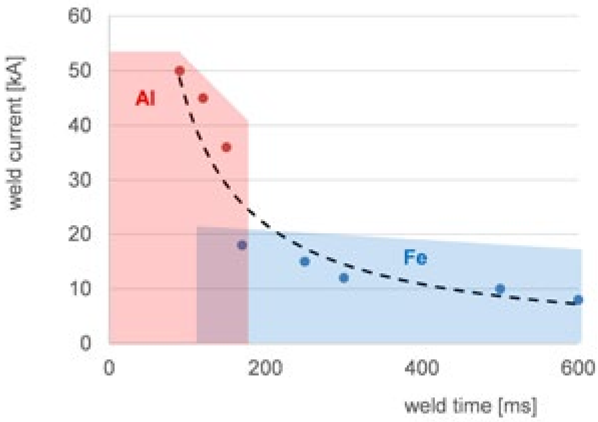

Figure 3: Weld parameters, specific material requirements

Load cycling capability

Application success in resistance welding equipment highly depends on the right choice of the welding diode and its correct operation. Each welding cycle represents a load cycle for the diodes and the expected lifetime is generally 10 million cycles or even more. This means that the load cycling capability of the diode is crucial for the choice of component and this capability is determined by the temperature swing the diode undergoes during the cycle.

Figure 4: Diodes are stressed by regulated short circuit during weld spot.


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To keep the temperature swing as low as possible during the welding cycle, the diodes must be designed for lowest possible losses and thermal impedance. During one weld spot the diode is stressed by fast current pulses (1kHz range) reaching from 10 to 50kA and lasting hundreds of milliseconds. The junction temperature is rapidly raising at that time, usually up to T_{jmax} (180°C). In summary, a welding diode operation is a combination of surge current, fast commutation and frequency load. The diode lifetime also strongly depends on construction of the diode, used materials and its fabrication quality.

ABB diodes combine all needed features for such extreme load and set new power cycling records for all power semiconductor devices in general.

Figure 5: Welding diodes from ABB

Standard WDs (up to 2 kHz)	I_{FAVM} (A)	Package* (mm)
5SDD 71X0400	7110	61 / 44
5SDD 71B0400	7110	63 / 44
5SDD 0120C0400	11350	75 / 57
5SDD 92Z0401	9250	53 / 47
5SDD 0105Z0401	10502	56 / 50
5SDD 0135Z0401	13500	64 / 57

High Frequency WDs (up to 10 kHz)	I_{FAVM} (A)	Package* (mm)
5SDF 63X0400	6266	61 / 44
5SDF 63B0400	6266	63 / 44
5SDF 0102C0400	10159	75 / 57
5SDF 90Z0401	9041	53 / 47
5SDF 0103Z0401	10266	56 / 50
5SDF 0131Z0401	13058	64 / 57

VRRM = 400 V

** Note: maximum diameter / pole-piece diameter*

Table 1: ABB’s Welding Diodes portfolio

ABB welding diodes

ABB has developed a comprehensive welding diode range that is shown below in Figure 5 and Table 1. We are offering standard welding diodes in hermetic package or even thinner versions called housing-less diodes. In this configuration the welding diode Silicon chip is bonded in one robust thin sandwich together with double side molybdenum discs and top copper electrode. This thin housing has the advantage of an even lower thermal resistance. An added advantage is the small size and low weight of the diodes, a welcome feature for equipment mounted on a robot arm.

The diode sandwich structure is proven by many power cycling tests done by ABB R&D testing laboratory and worldwide cooperation with main players in resistance welding applications. The successful diode testing were reaching significantly over 10M cycles without failed diodes or weld parameters degradation.

To meet the demands of higher frequencies, a new group of high frequency welding diodes with high current capability combined with excellent reverse recovery characteristics was developed. These new features will enable operation with high efficiency at frequencies around 10 kHz.

The welding Diode represents the most stressed component in the application. Diode reliability and lifetime performance represent key factor for application success. ABB welding diodes are considered as a worldwide benchmark.

www.abb.com/semiconductors

flowIPM 1C CIB 1200 V Drives Down Costs and Speeds up Assembly --

Vincotech, a supplier of module-based solutions for power electronics, announced the launch of a deeply integrated Intelligent Power Module for 1200 V applications. The flowIPM 1C CIB 1200 V achieves the deepest level of integration of any power module available on the market today to drive down systems' cost and speed up assembly.
The flowIPM 1C based on a CIB topology (converter + inverter + brake) features three inverter gate drives, including a bootstrap circuit for high-side power supply. Each leg of the inverter provides current-limiting for circuit protection.

The current rating of this new intelligent power module housed in the new flow 1C housing is also impressive: 14 A @ 80°C or 30 A @ 25°C heat sink temperature. The deeply integrated flowIPM 1C CIB 1200 V module enables manufacturers to slash their overall system's size, cost, and time to market. It also features a brake chopper with integrated gate drive as well as emitter shunts (30 mΩ) for vastly improved motion control.
Samples may be sourced on demand from our usual channels.
To learn more about Vincotech's flowIPM 1C CIB 1200 V, please visit: www.vincotech.com/IPM-1C
To see Vincotech's entire range of power modules, please visit: www.vincotech.com/products/by-topologies.html

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X8R MLCCs go Non-Mag with New Dielectric Formulation

Knowles Capacitors is pleased to announce that their ongoing material development process has qualified an X8R dielectric material to be Lead (Pb) free. This is part of Knowles environmental commitment to continuously develop materials that are more environmentally friendly, as well as ensuring continued compliance to the existing requirements along with potential future changes to the EU RoHS directive.
This dielectric material will replace the current X8R materials that contain Lead (Pb), though these remain available on request. The new material will be used for standard X8R Multilayer Ceramic capacitors (MLCCs) and AECQ200 MLCC X8R Multilayer Ceramic Capacitors for all voltage ratings (50V up to 3kV) and capacitance values 100pF up to 2.2uF. Case sizes from 0805 to 2225 are available. This gives Knowles Capacitors one of the widest ranges of voltage, capacitance and cases sizes available for an X8R product range in the industry.
Knowles Capacitors R & D centre has accumulated extensive reliability test data in order to verify that this new dielectric meets, or exceeds, all reliability and quality specifications. The TCC (capacitance variation with temperature) of the material also meets X8R specifications.
The range is qualified to AECQ-200 from 100V upwards and includes a range extension over the existing standard X8R range, which is manufactured to the same exacting standards for use in demanding applications. Knowles unique FlexiCap termination is available across all product types.

Data packs are available on request.
The current X8R Space grade (S02A or S03A), and IECQ ranges are not affected, nor are the non-magnetic parts, planar arrays, discoidals or EMI filter products.

www.knowlescapacitors.com

Technological Basis Set for High Performance Electronic Circuit Breakers

A German research team has explored the technological basis for reducing the energy losses in power grids and electric devices by more than half. This can be made possible through the use of direct current (DC). DC allows for smaller power losses when compared to the alternating current (AC) used today. The five project partners from industry and science investigated the foundations of a semiconductor-based and completely electronic circuit breaker that can be used for future DC power grids and applications. Such a circuit breaker will enable to use direct current wherever alternating current is used today.
The circuit breakers will be able to switch on direct current as quickly and safely as possible and, in case of emergency, switch it off quickest possible. They will enable to more efficiently feed electric energy from regenerative sources into power grids and energy storage and improve grid stability. With direct current it will also be possible to build much more compact electric devices. Infineon Technologies AG had the team lead and worked on the circuit breakers together with Airbus, E-T-A Elektrotechnische Apparate GmbH, Siemens AG and the University of Bremen's Institute for Electrical Drives, Power Electronics, and Devices (IALB). The European Center for Power Electronics e.V. (ECPE) provided further support. The ECPE is headquartered in Nuremberg, Germany.

www.airbus.com

www.e-t-a.de

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www.ialb.uni-bremen.de

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Integration, Efficiency, and Flexibility of Next-Generation IPMs up to 100W

STMicroelectronics has extended its SLLIMM™ nano series of Intelligent Power Modules (IPMs) for motor drives with more package options that help minimize overall size and complexity, extra integrated features, and greater efficiency leveraging the latest-generation 500V MOSFETs.

With a current rating of 1A or 2A, the new IPMs target applications up to 100 Watts, such as refrigerator compressors, washing-machine or dishwasher motors, draining and recirculation pumps, fans, and other drives running at less than 20kHz in hard-switching circuitries. Operation up to 150°C allows use in harsh environments.

The modules integrate a three-phase MOSFET bridge and gate-driver HVICs, with value-added features including an unassigned op-amp and comparator for functions such as over-current protection and current sensing. Additional built-in safety features include interlocking to prevent shoot-through currents from damaging MOSFETs of the bridge, a fault-status output, shutdown input, and smart-shutdown capability. An optional built-in thermistor helps simplify over-temperature protection.

In addition to the zig-zag lead option, the new series is also available in a line-lead package. These give designers extra flexibility to simplify the board layout and minimize controller size in mechatronic assemblies and other space-constrained applications.

The high thermal performance of the packages, combined with the superior efficiency of ST's latest 500V MOSFETs, enhances designers' freedom to minimize heatsink size or create heatsink-free solutions for lower-power applications. The low MOSFET on-resistance of 3.6Ω and 1.7Ω, in 2A and 1A variants, respectively, combines with low switching losses to ensure high overall energy efficiency. The MOSFETs have separate open-emitter connections to module pins, which simplifies use of three-shunt current sensing for field-oriented motor control (FOC) or single-shunt sensing for trapezoidal control.

The modules also integrate the bootstrap diodes needed to control the high-side MOSFET gates, further minimizing demand for external components.

www.st.com/ip

Breakthrough for Coreless Power Conversion Technology for High Magnetic Field Applications

Powerbox, one of Europe's largest power supply companies and a leading force for four decades in optimizing power solutions for demanding applications, has announced the release of its new coreless technology platform to power medical and industrial equipment operating in very high magnetic field environments such as magnetic

resonance imaging or particle accelerators. Using the latest technology in high-frequency switching topologies and digital control with proprietary firmware to optimize efficiency and voltage regulation,

Powerbox's GB350 buck-converter module is the first building block in its category that is able to operate safely when exposed to high radiation magnetic fields of 2 to 4 Tesla. GB350 delivers an output power of 350W and when higher power levels are required it can be paralleled using an interleaving mode thus reducing EMI.

Medical and industrial applications such as magnetic resonance imaging (MRI) and particle accelerators (PA) generate high magnetic fields to induce the RF energy required to activate the hydrogen nuclei in the case of imaging, or to accelerate particles in research and industrial equipment.

Modern MRI systems usually generate 1.5 to 4 Tesla, making conventional power supplies using ferrite material useless due to inductance saturation as a result of the MRI magnet disturbing the energy transfer. To prevent parasitic saturation, power supplies are traditionally positioned outside the shielded operation room. Installing the power supplies remotely requires long cables with subsequent power losses, and it is also a big challenge to power the latest generation of measuring equipment that require stable and tightly regulated voltages under fast transient load conditions.

www.prbx.com

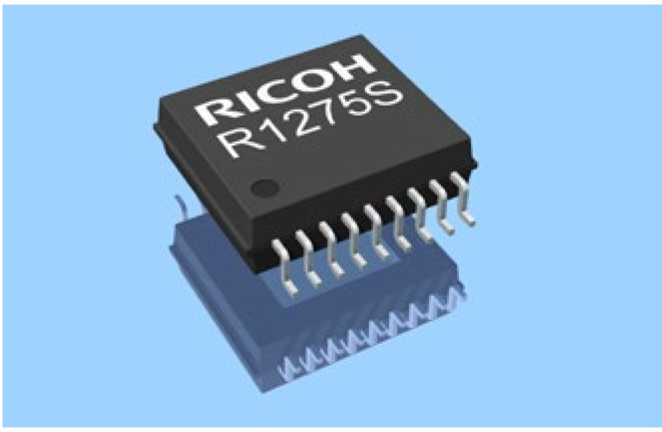
Large-Area C-SAM® Tool for the Production Floor

Sonoscan® has introduced the J610™, the latest member of its C-SAM® acoustic microscope line. The J610 is a semi-automated tool designed for production environments and has an unusually large scan area. Its key role is finding internal structural defects by screening trays of loose components, wafers, board-mounted components and other suitably sized items.

The 610mm x 610mm scan area can accommodate 6 JEDEC-style trays or one or more printed circuit boards. To reduce vibrations and maximize image quality, the system's patented inertially balanced linear scanner is counterweighted. The J610 can learn the x, y and z extent of specific user-defined areas of interest within a component. By comparing anomalies to the user's standards, it can automatically accept or reject components. Using Sonoscan's PolyGate™ software, it can create a separate image for each of multiple depths of interest in a given component, without increasing scan time. Using Sonoscan's proprietary Q-BAM™ module, it can create non-destructive cross sections through a component. When scanning printed circuit boards, the system accurately finds and scans a component even if the component is slightly out of place on the board. When defects repeatedly appear in the same component on multiple boards, steps can be taken to find and eliminate the cause.
J610 inspection permits replacement of board-mounted components that fail to meet the user's criteria.

www.sonoscan.com

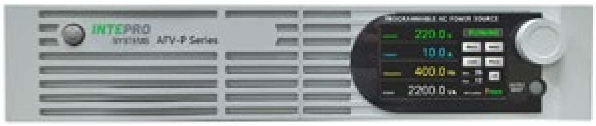
30V / 2A PWM DC/DC Converter with EMI Noise Reduction



Ricoh Europe (Netherlands) B.V. Semiconductor Support Centre has launched the R1275, a high-efficiency, 2A synchronous step-down DC/DC converter with a wide input voltage range up to 30V and has two options to minimize electromagnetic interference (EMI). It allows connecting to a variety of input sources, such as battery-powered portable devices, industrial supplies and automotive batteries.
There are many ways to reduce radiated and conducted EMI significantly, but few are as simple as using a Spread Spectrum Clock Generator (SSCG). The idea behind using SSCG is to modulate the clock frequency mildly, which results in spreading the EMI energy amongst many frequencies instead of concentrated at one frequency. This way, the amount of potential interference of the base frequency and its harmonics is reduced considerably.
The switching frequency is internally set to 2MHz, but it is also possible to synchronize with another DC/DC Converter by applying an external clock signal from 1.8MHz to 2.2MHz. Especially in case the power supply consists of multiple DC/DC converters, the individual switching frequencies can result in a significant noise in common ground wiring. By synchronizing all DC/DC converters to one frequency, the resulting noise is easier to filter out and will not interfere with the control of the converters.

www.e-devices.ricoh.co.jp/en/

Programmable AC Power Source Includes DC Output Capability



Intepro Systems, a market leader in power component and power system automated test equipment (ATE), introduces the AFV-P Series of precision, programmable AC/DC power sources. The compact rack-mounted AFV-P Series units are available in four power levels – 600VA, 1250VA and 2500VA (2U) and 5000VA (5U) – and provide clean power with distortion less than 0.3% at 50/60Hz. The AFV-P series delivers output voltage from 0 to 310 VAC and frequency from 40 to 500 Hz (15 to 1000 Hz with the high-frequency option). The devices can also be programmed to provide DC power from 300W to 2500W at 0-210/0-420 VDC. The units feature 300 µs slew rate (for 0-90% change in output voltage) and can deliver up to 4.5 times peak current (crest factor) from its max rated current. The APF-V Series is ideal for commercial, defense and aerospace test applications, from design verification and quality assurance to automated production testing. The AFV-P Series' graphical user-interface software makes it easy to set up complex testing sequences. Transient generation functions provide simulation of voltage variations, surges, drops and frequency disturbances with 1msec programming resolution. The five-inch touch screen with rotary knob allows quick adjustments and configuration of voltage, current and frequency. Users can remotely control the unit via standard interfaces of USB, RS232/RS485, LAN or optional GPIB and analog control. Free control software and LabVIEW driver are available for easy programming and remote control.

www.inteproATE.com

Programmable Linear Hall-Effect Sensor IC

The A1377 from Allegro MicroSystems Europe is a programmable linear Hall-effect sensor IC designed for applications that require high accuracy and high resolution without compromising bandwidth.

The device uses segmented, linearly interpolated temperature compensation technology which greatly reduces the total error of the device across the whole temperature range. As a result, it is ideally suited to linear and rotary position in automotive applications such as actuators and valves.
The A1377 is available in a through-hole, small form factor, single in-line package (SIP) and has a broad range of sensitivities and offset operating bandwidths. The accuracy and flexibility of this device is enhanced with user programmability, via the supply voltage (Vcc)and output pins, which allows it to be optimised to the application.
This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. The quiescent voltage output is user-adjustable from approximately 5% to 95% of the supply voltage. The device sensitivity is adjustable within the range of 1 to 14 mV/G.

www.allegromicro.com

Rectifier in DO-214AA Package Optimized for Space Constrained Applications

SMC Diode Solutions announced the availability a general-purpose high voltage SMD rectifier in low-profile (DO-214AA) size format. The SD560B rectifier uniquely combines a compact footprint and 2.5mm profile with an average rectified output current (IO) rating of 5A continuous and a reverse voltage (VRRM) rating of 600V. The component additionally provides a robust forward surge rating (IFSM) of 200A, making it well suited for switching and linear power supplies.
Primarily specified as an input rectifier to convert alternating line voltage to usable DC, the SD560B is appropriate in an extensive range of uses, such as a general-purpose rectifier, freewheeling diode, or reverse polarity protection device in applications where space is limited and long life and reliability are critical. The device is employed in an array of electronic devices and equipment, including high voltage regulated power supplies, switchmode power supplies, UPSs, AC-DC adapters/chargers, DC-DC converters, lighting circuits, industrial ballasts, temperature and motor speed control circuits.
SMC’s SD560B provides a low forward voltage drop (VF) of 1.2V max. (IF = 5A) to reduce heat dissipation and maximize energy efficiency, as well as a low idle current of 9µA max. (TA = 25°C, 600V)

to minimize reverse energy loss. Typical junction capacitance (Cj) is 50pF @ 4V, 1MHz.

www.smc-diodes.com

Switching Regulators to Supply Microprocessors from 4-20mA Loop

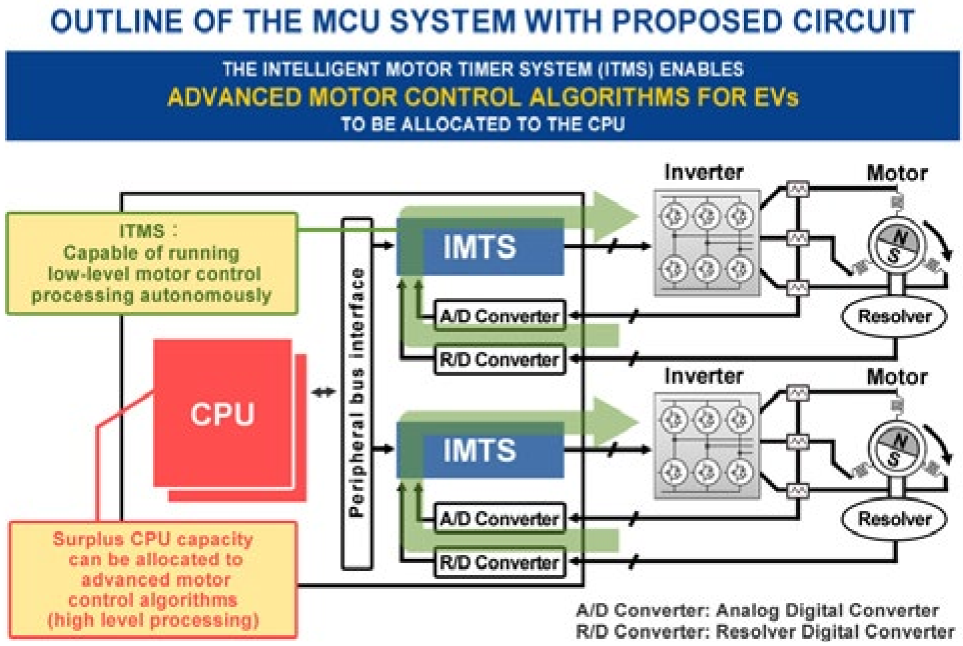
Recom R420-1.8/PL switching regulators were developed specifically for supplying microprocessors from 4-20mA loop. Characteristics of the flat module include extremely low idle power along with high efficiency.
As aged as it may be, the venerable analogue 4–20mA loop still represents the undisputed standard in process and control technology – not least due to the relatively simple two-wire technology, which is extremely reliable and easy to install. Supplying digital components from the unused portion of the loop current had become an issue with microprocessors processing raw data and HART (Highway Addressable Remote Transducer) modems ensuring that smart sensors keep sending a variety of data signals on the same loop.
Conventional switching regulator ICs are unsuitable as their high efficiency at full load drops so far at lower loads that they exceed the 4mA threshold. Low quiescent current in sleep mode cannot compensate as this shuts off the main output voltage altogether. Linear regulators are not ideal either; despite their perfectly decent quiescent

current levels at around 0.5mA, poor efficiency decreases available power by a factor of around three compared to switching regulators.

www.recom-power.com

Motor Control Circuit Technology for Automotive Microcontrollers

Renesas Electronics announced the development of a circuit technology dedicated for motor control that realizes green vehicles satisfying stricter automotive CO2 emissions requirements.
The developed technology is an Intelligent Motor Timer System (IMTS), a dedicated circuit block that next-generation high-speed EV motors with excellent energy efficiency and inverter systems with high-speed switching performance to drive them. Furthermore, the unique circuit also enables functional safety support required for the automotive powertrain field.



can be integrated into automotive microcontrollers (MCUs) for next-generation electric vehicles (EVs) and hybrid electric vehicles (HEVs). It performs field-oriented-control operations, which are essential to EV motor control, in a mere 0.8 microseconds (µs), the world's fastest rate, which is less than 1/10 the operation processing time of software implementation on a CPU running at the same operating frequency. This contributes to the realization of

With the increasingly stricter fuel efficiency requirements in the recent years, EVs, HEVs, and plug-in hybrid electric vehicles (PHEVs) have come to account for an increasing share of the total number of vehicles produced. To increase the range of such motor-driven vehicles, it is necessary to boost the energy efficiency of motor control.

www.renesas.com

Smart New Battery

Global battery manufacturer Ultralife Corporation is set to enrich the U1 lead acid battery market with the launch of its new 492Wh Lithium Iron Phosphate (LiFePO4) smart battery. The URB12400-

U1-SMB battery, which features accurate fuel gauging and integrated safety circuitry, is designed to replace and improve on traditional sealed lead acid (SLA) batteries in applications such as medical carts, wheelchairs, scooters, robotics & motor bots or uninterrupted power supply (UPS) systems.
The URB12400-U1-SMB battery has a nominal voltage of 12.8V and a capacity of 38.4Ah, with a low self-discharge rate of less than five per cent per month. The battery also functions fully at a wider temperature range than SLA batteries, from -20°C to +60°C.

www.ultralifecorporation.com

Class Accuracy 0.5 and Easy-to-Install Smart Current Sensors for Smart Cities

LEM upgrades "ART" Rogowski current sensor to measure current of up to 10000A AC and beyond with Class Accuracy 0.5. The ART achieves IEC 61869 Class 0.5 accuracy without the need for additional components like resistors or potentiometers, which can drift over time. In addition, the ART benefits from "Perfect Loop" technology, a unique patented coil clasp that eliminates the inaccuracy caused by sensitivity to the position of the conductor inside the loop as well as providing an innovative, robust and fast "Twist and Click" closure. An internal shield is provided as standard to guard against external fields, improving accuracy and optimising performance for small current measurements.

The ART series provides the same ease of installation as existing split-core transformers, but with the benefits of being thinner and more flexible.

Whatever the chosen dimension - 50, 70, 125, 175, 200 & 300 mm diameter for the aperture – the ART can be mounted very quickly by simply clipping on to the cable to be measured. Contact with the cable is not necessary, and the ART ensures a high level of safety as well as providing a high rated insulation voltage (1000 V Cat III PD2 - reinforced).

The ART also allows disconnection of the coil to be detected through the use of a security seal passed through a specially designed slot, making it really useful when used with a meter. It can be used in applications requiring a protection degree up to IP 67.

www.lemcity.com

Designed for High Dielectric Strength in Traction Batteries and Stationary Energy Storage

With its newly developed, shunt-based IVT-S measurement technology, Isabellenhütte is responding to the market, which now favours specified functions in current measurement systems. The main focus is on achieving dielectric strength that is as high as possible in line with the intended application. High dielectric strength must be guaranteed in battery-powered vehicles, for example.

To this end, Isabellenhütte is now introducing the IVT-S. The measurement system has a maximum dielectric strength of 1,000 volts. Its functional range includes the measurement of current and voltage. Isabellenhütte thus meets today's market requirements of traction battery systems or stationary, electrical energy storage devices. These lithium-ion batteries generate high energy density at which higher voltages can be applied with smaller currents. This is why the sensor's dielectric strength also has to be correspondingly high – a key quality feature that distinguishes IVT-S from competing products. For fast-charging battery systems, this performance feature is extremely important.

www.isabellenhuette.de/en/home

Compact Power Entry Module for Protection Class II Equipment

Schurter expands its wide range of power entry modules to include versions, without ground pin, for use in Protection Class II double-insulated applications. The 5145 power entry module is already popular for use in Protection Class I equipment, due to its circuit breaker and EMC filter functions integrated into one compact package. The new Protection Class II version is perfectly suited for medical equipment used at home where the medical standard prescribes the use of Protection Class II design.

The 5145 Class II version is according to IEC 60320-1, style C18. It is particularly well suited for use in medical equipment according to the IEC standard 60601-1-11, which outlines additional safety measures specific to medical equipment intended for use in the home. There is increasing demand for such equipment as populations around the world age and healthcare costs continue to rise.

The EMC filter is available in medical and low leakage, M5, versions. This integrated filter at the power input provides highly effective interference suppression, which results in optimized electromagnetic compatibility. Current ratings range from 1-10 A at 250 VAC. Versions with quick-connect or solder terminals are available.

www.schurter.com

Single-Chip Telematics/Connectivity Processors to Support Connected-Driving Services

STMicroelectronics has boosted performance and security in its latest Telemaco processors tailored to support richer connected-driving services.

Telematics systems that monitor on-board sensors and exchange information with the Cloud are becoming increasingly sophisticated to support high-value services including remote vehicle diagnostics, roadside assistance, and Over-The-Air (OTA) software updates. Infotainment features like location-based services and access to personal content and contacts add further benefit for end users. Over 72% of new cars globally will be fitted with factory-installed telematics systems by 2021, according to ABI Research, and there are opportunities for aftermarket systems, as well as OEM and independent telematics service providers.

ST's Telemaco concept helps maximize consumer access to these advanced connected-driving services through the cost-effective integration of the telematics processor, secure in-car connectivity, and sound boosting in a single chip. Unlike alternative devices, which are typically based on an application processor or a GSM modem with integrated CPU (Central Processing Unit), ST's latest Telemaco3 chips are tailored for telematics applications and give extra flexibility to choose the connection type, such as 2G, 3G, or 4G. At the same time, the secure interface with the in-vehicle network is enhanced with a hardware cryptographic accelerator, and connectivity extended with Gigabit Ethernet support and the option to host a Wi-Fi module that can be used as an in-car hotspot.

www.st.com

Online Store Now Includes all Former Atmel Products

Microchip Technology Inc. announced that all former Atmel products are now available on microchipDIRECT, Microchip's full service channel. For the first time, customers can purchase products such as AVR® and SAM® microcontrollers and development tools direct from the manufacture.

microchipDIRECT carries the largest available inventory of Microchip's products. The service offers pricing for all volume levels, ability to schedule orders up to 12 months in advance, order tracking, buffer stock and many payment options including credit lines. In addition, it is the first manufacturer–to-customer website that allows customers to upload their custom code on a microcontroller or memory device. It also offers true global support in 10 languages.

All products are now available on microchipDIRECT. For more information or to purchase products, visit

www.microchipdirect.com

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Ready-to-use solution for variable speed drives

iMOTION™ IRMCK099 – High performance sensor less motor control IC

Customer benefits:

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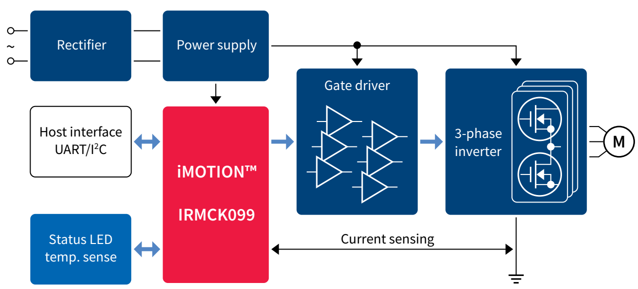
- Reduced BOM cost
- Patented and field proven Motion Control Engine (MCE) for sensorless field oriented control (FOC)
- Very wide speed range
- Integrated protection features
- Standby function
- Tiny 5 x 5 mm² QFN-32



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