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Bodo´s Power Systems®

Electronics in Motion and Conversion

July 2025

Calibration ensures Confidence in Current Measurement

DANISENSE

PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the
- **Incremental inductance** $L_{inc}(i)$ and $L_{inc}(\int Udt)$
- **Secant inductance** $L_{sec}(i)$ and $L_{sec}(\int Udt)$
- **Flux linkage** $\psi(i)$
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** B(i)
- **DC resistance**

Also suitable for 3-phase inductors

APPLICATIONS

Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**
- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

AVAILABLE MODELS

Model	max. test current	max. pulse energy
DPG10-100B	0.1 to 100A	1350J
DPG10-1000B	1 to 1000A	1350J
DPG10-2000B	2 to 2000A	1350J new model
DPG10-2000B/E	2 to 2000A	2750J new model
DPG10-3000B/E	3 to 3000A	2750J
DPG10-4000B/F	4 to 4000A	8000J
DPG20-10000B/G	10 to 10000A	15000J

Technological leader in pulsed inductance measurement for 20 years

www.ed-k.de

Content

Supporters & Friends

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

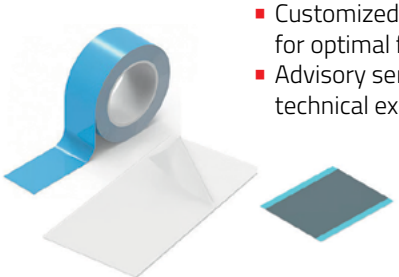
YOU'VE GOT BETTER OPTIONS THAN THAT

Check out our Thermal Management Solutions

Thermal management is crucial for developing durable and efficient designs. Our gap filling, heat spreading, and hybrid solutions deliver optimal thermal management solutions, ensuring your design achieves maximum durability and efficiency. Paired with our expert services and custom solutions, we provide the perfect fit for your application. Ready to keep it cool?

www.we-online.com/thermal

#THERMAL



Highlights

- Gap filling, heat spreading and hybrid solutions
- Customized components for optimal fit
- Advisory services from technical experts

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Munich is Calling

...and it's not for electronica this year! With PCIM behind us and summer holidays just ahead (or already in full swing), Bodo's team is now moving focus to this year's edition of the Wide Bandgap Event in Munich.

We're excited to be returning to our trusted venue, the Hilton at Munich Airport, on December 2nd and 3rd. Not only because we value continuity at Bodo's, but also because the venue delivers everything we need. Speaking of continuity, we're keeping the well-established format: a round table followed by a get-together on Day 1, and the conference with tabletop exhibition on Day 2. As in previous years, presentations will run in two parallel tracks. We'll do our best to publish the program on www.bodoswbg.com as soon as possible so that you can plan your visit and make sure not to miss what matters most to you and your team.

We're truly excited to be returning to Munich, but first, there's plenty of work ahead. Over the coming weeks, all previous partners, presenters, sponsors, and exhibitors will receive (or may already have received) an invitation. It's part of our DNA to honor those who helped to build this successful event by offering early access to these opportunities. That said, we also welcome new companies bringing fresh ideas and approaches. I can already give you a sneak peek: some exciting newcomers will be joining us this year. The event's growing reputation has led companies to reach out long before we even began planning.

If you think your company should be part of the WBG event, please send an email to me at holger@bodospower.com and let's see how we can work together. But don't wait too long. Tabletop spaces, for example, are limited!

Bodo's Magazine is delivered worldwide by postal service and remains the only magazine globally focused solely on technical content in power electronics. In North America, our distribution is supported by EETech, and for our Chinese-speaking audience (or the curious), check out www.bodospowerchina.com. Every issue is freely available in our online archive at www.bodospower.com.

My Green Power Tip of the Month:
We occasionally encounter postal delays in some regions. Why not solve two problems at once? The digital edition is always on time - and much kinder to the environment!

Kind Regards,

Events

3D-PEIM 2025
Golden, CO, USA July 8 – 10
www.3d-peim.org

Battery Show Asia 2025
Hong Kong, China July 15 – 17
www.thebatteryshow.asia

PEDS 2025
Penang, Malaysia July 21 – 24
www.ieee-peds.org

WiPDA Asia 2025
Beijing, China August 15 – 17
www.wipda-asia2025.org

EMC+SIPI 2025
Ralaigh, NC, USA August 18 – 22
www.emc2025.org

ECCE Europe 2025
Birmingham, UK August 31 – September 4
www.ecce-europe.org

PCNS 2025
Sevilla, Spain September 9 – 12
www.pcns.events

electronica India 2025
Bengaluru, India September 17 – 19
www.electronica-india.com

PCIM Asia 2025
Shanghai, China September 24 – 26
www.pcimasia-shanghai.com

Need a low range current sensor that offers high resolution?

HMSR DA series

The new HMSR DA family of integrated current sensors designed by LEM is the first to include an ADC with a sigma-delta bitstream digital output.

High-resolution, ease-of-use and an output that follows the increase or decrease of the input with configurable delay, makes it easier to develop a wealth of control systems.

This makes the HMSR DA the first choice for standalone servo drives, robotics, high precision machines, automated guided vehicles (AGVs) and CNC machine tools.

www.lem.com

- **Current range 6-30 A_{RMS} continuous at 125°C**
- **75 A peak current**
- **Digital bitstream output with 10 MHz clock**
- **More cost-effective and compact than discrete alternatives**

LEM

Life Energy Motion

APEC 2026: Call for Papers

August 15, 2025, is the deadline for submission of Technical Sessions digests for the 41st annual edition of the Applied Power Electronics Conference. APEC 2026, to be held in San Antonio, Texas, from March 22-26, 2026, continues the long-standing tradition of addressing issues of immediate and long-term interest to the practicing power electronics engineer. Interested authors wishing to present a paper must submit a digest for consideration by the deadline. To facilitate higher quality digest and final manuscript submissions, APEC 2026 offers significantly expanded submission windows for both the phases. Topics of interest are divided into fourteen tracks, each track with a diverse set of subtopics: AC/DC Converters, DC/DC Converters, DC/AC Inverters, Devices and Components, Magnetics, Power Electronics Integration and Manufacturing, Control, Modeling and Simulation, Motor Drives, Power Electronics for Utility Applications, Renewable Energy Systems, Wireless Power Transfer, Transportation Power Electronics, Power Electronics Applications. "APEC provides an ideal balance between academic and industrial research and is a meeting ground for these two areas, unlike any other power electronics conference," said Dhaval Dalal, APEC 2026 Program Chair. "APEC tops the list of the IEEE power electronics conferences for average paper citations — as of May 2025, 7.4 for APEC 2019 and 4.8 for APEC 2022." The Technical Sessions digest should explain the problem that will be addressed by the paper, its major results and how it is different from the closest existing literature. Technical Sessions papers presented at APEC must be original material and not have been previously presented or published.

www.apec-conf.org

PCIM booth raises €10,000 for a worthy cause

Vincotech staged a charity benefit at this year's PCIM Europe trade fair. The company and its partners pledged a donation for every visitor who competed in a virtual reality memory game, raising 10,000 € for a Plan International Germany project in Malawi called "Education Empowers Girls!" Vincotech has made a tradition of hosting engaging charity events at the fair. Activities such as wall climbing, Sudoku, and this latest VR memory challenge – a crowd favorite – attracted hundreds of enthusiastic fairgoers. This year's proceeds go to a Plan International Germany project aiming to improve access to education and outcomes for girls in Malawi's Lilongwe and Kasungu districts. Running from October 2022 to September 2026, the initiative goes to create inclusive, supportive learning environments where girls and boys can realize their full potential. In a statement Vincotech explains why it chose this charity project: "Empowering girls through education changes lives – and not just individuals'; it transforms entire families and communities for generations to come."

www.vincotech.com

Collaboration to support Battery Energy Storage System Platform

Arrow Electronics, in collaboration with Prime Batteries and NXP Semiconductors, is launching a next-generation Battery Energy Storage System (BESS) platform. Prime Batteries developed this solution with support from Arrow and NXP to advance energy industry and energy-saving technologies, addressing the increasing global demand for greater efficiency. By leveraging their combined strengths, the companies aim to establish new benchmarks in energy-saving technology and make a substantial impact across industries. According to Arrow the solution complies with the latest European safety regulations and "achieves unprecedented levels of energy storage capacity, making it ideal for a variety of BESS applications". The platform's versatility allows it to cater to different customer needs, with adjustable voltage and current parameters. It supports high voltages up to 1500 V, inline with current market trends for high-power equipment, and meets rigorous safety standards for critical applications, including ISO 26262, with the potential for ASIL D certification, if necessary. The system features multiple protection layers and continuous, independent cell monitoring. Designed with scalability and upgradability in mind, the BESS can meet the changing requirements of customers. Its low maintenance needs and optimized operating conditions extend its lifespan, thereby reducing the total cost of ownership. In this context NXP's 1500 V Battery Energy Storage System provides a modular and scalable reference design for utility, commercial, industrial and residential high-voltage applications.

www.arrow.com

ROHM SEMICONDUCTOR

EcoSiC

New High Power Density EcoSiC™ Modules

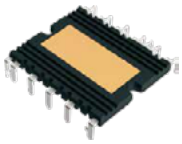
Compact high heat dissipation design sets a new standard for OBCs

ROHM has developed the new 4-in-1 and 6-in-1 SiC molded modules in the HSDIP20 package optimized for PFC and LLC converters in onboard chargers (OBC) for xEVs (electric vehicles). The lineup includes six models rated at 750V (BSTxxx1P4K01) and seven products rated at 1200V (BSTxxx2P4K01).

Lineup ideal for configuring high-power power supply circuit topologies such as PFC and LLC circuits

Adopting high thermal conductivity insulating materials ensures superior heat dissipation, facilitating insulation design

Delivers higher output compared to power modules of similar size

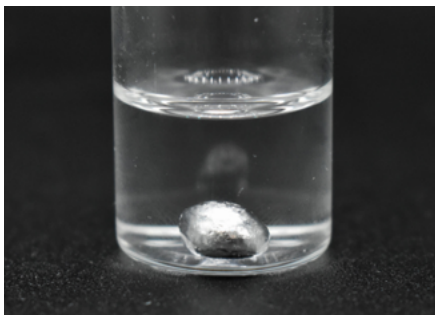
Part No.	Absolute Max. Ratings (Tj=25°C)			Topology	Module Package
	V_{DSS} [V]	$R_{DS(on)}$ [mΩ]	I_D[A]*1		
BST91B1P4K01	750	13	90	4in1	 HSDIP20 [38.0mm × 31.3mm × 3.5mm]
BST47B1P4K01		26	47		
BST31B1P4K01		45	31		
BST91T1P4K01		13	90	6in1	
BST47T1P4K01		26	47		
BST31T1P4K01		45	31		
BST70B2P4K01	1,200	18	70	4in1	
BST38B2P4K01		36	38		
BST25B2P4K01		62	25		
BST70T2P4K01		18	70	6in1	
BST38T2P4K01		36	38		
BST25T2P4K01		62	25		
BST70M2P4K01*2		18*3/ 36*4	70*3/ 38*4		

*1: Tc=25°C VGS=18V *2: Combines chips with different ON resistances
*3: Q1, Q4 pins *4: Q2, Q3, Q5, Q6 pins

www.rohm.com

Gallium: From Mining towards the Fab

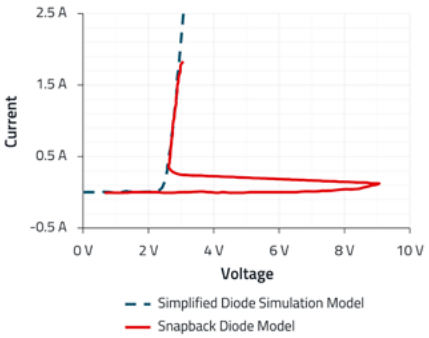
Indium Corporation and Rio Tinto have successfully extracted gallium from feed sourced at Rio Tinto's Vaudreuil alumina refinery in Saguenay, Quebec/Canada. This collaboration is a step in building a more robust global supply chain for gallium. A strategic North American supply will accelerate the development of the project towards commercialization of gallium-based technologies. Indium Corporation designed and developed this gallium extraction process in the United States at its research and development facility in Rome, New York state. Indium Corporation works towards establishing a 3.5-ton demonstration plant which would be located in Saguenay, Quebec, which might then eventually complemented by a commercial-scale capacity of 40 tons annually, addressing an estimated five to 10 percent of global gallium supply.



www.indium.com

LTspice Models for ESD Products

Würth Elektronik, in cooperation with the Institute of Electronics (IFE) at Graz University of Technology, now offers an LTspice model for its TVS diodes and ESD suppressors for ESD protection, based on real measurement data using TLP (Transmission Line Pulsing). This enables the actual behavior of the components to be measured under electrostatic discharge (ESD) conditions. The ready-to-use simulation files facilitate integration into SPICE-based analyses and help shorten design cycles and time-to-market. Conventional models of components for ESD protection typically rely on simplified approximations. The new models developed by Würth Elektronik and the IFE at Graz University of Technology, based on measurement data, however, reflect the actual transient properties, including snapback behavior. The snapback effect allows the voltage to be clamped to a lower level after a transient overvoltage than is possible with standard PN diodes. This is a key aspect of ESD protection, as it reduces both the overvoltage and the resulting thermal stress on sensitive electronic components, so the ability to simulate it is a critical improvement to the development process. LTspice models for realistic modelling of real component behavior during ESD



events for products from the WE-TVS and WE-VE product series are now available to download.

www.we-online.com

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High-accuracy **Power Analyzers** & **Current Sensors** from a single source.

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Semiconductor Partnership with Indian Government

Renesas has started a partnership with the Ministry of Electronics & Information Technology (MeitY), Government of India, to support local startups and academic institutions in the field of VLSI and embedded semiconductor systems. Renesas also celebrated the expansion of its offices in Bengaluru and Noida to accommodate its growing R&D teams, with inauguration ceremonies held in May 2025. India is a key market for Renesas, offering significant growth potential and access to a highly skilled talent pool. Renesas intends to generate over 10 percent of its global revenue from the Indian market by 2030. Recent collaborations include the OSAT factory project with CG Power and Stars Microelectronics in Gujarat and the MOU with IIT Hyderabad. Renesas is also expanding its operations in India, with plans to increase its headcount to 1,000 by the end of 2025.

www.renesas.com

CIPS 2026: Call for Papers

CIPS, the "International Conference on Integrated Power Electronics Systems" will take place March 10-12, 2026 in Dresden/Germany, and the organizers describe the basic framework as follows: In the next decades, power electronic system development will be driven by energy saving systems, intelligent energy management, power quality, system miniaturisation and high reliability. Monolithic and hybrid system integration will comprise advanced device concepts including wide bandgap devices, new packaging technologies and the overall integration of actuators/drives (mechatronic integration). Consequently, CIPS is focused on the three main aspects: Assembly and interconnect technology for power electronic devices and converters. The second aspect is the integration of hybrid systems and mechatronic systems with high power density, and the third aspect is the systems' and components' operational behaviour, reliability and availability. Basic technologies for integrated power electronic systems as well as upcoming important applications will be presented in interdisciplinary invited papers. Experts from industry, research institutes and universities wishing to present results of their recent research are cordially invited to submit a paper by September 29, 2025. Applications are wide spread over areas such as power supplies and drives to feed all kinds of loads like consumer electronics, industrial equipment, data centres etc. Applications are e. g. from the grid or to feed electrical energy from solar or wind generators to the grid but also in the transportation sector like railway, automotive and aircraft. The organizers explicitly encourage to "submit your contribution even if you can not find the appropriate topic for your contribution. All interesting contributions are welcome!"

www.cips.eu

1200 V SiC Diodes: Manufacturing Collaboration between Indian and Taiwanese Companies

RIR Power Electronics announces the successful production expansion and shipment of 1200 V SiC diodes from Taiwan. This was achieved through a strategic collaboration with a contract fab at Pro Asia Semiconductor Corporation (PASC), Taiwan and by leveraging technology IP that RIR Power had acquired from Sicamore Semi, USA. The product portfolio includes 1200 V Schottky Barrier Diodes (SBDs) ranging from 2 A to 60 A, addressing the most common ratings used across multiple applications and markets globally. Besides serving existing domestic Indian and the USA customers, shipping from Taiwan also provides improved access to strategic high-growth markets for SiC devices in the South East Asian region. RIR Power's SiC technology and portfolio are the result of a comprehensive technology transfer agreement signed with Sicamore Semi in October 2024. The agreement granted RIR Power exclusive rights to manufacture, market and commercialize SiC diodes, MOSFETs and IGBTs using Sicamore's proven IP and process know-how. Originally developed for 4-inch wafers, the technology has been successfully adapted for 6-inch wafer production. The scale-up was achieved with technical support from Vortex Semi, USA and PASC.

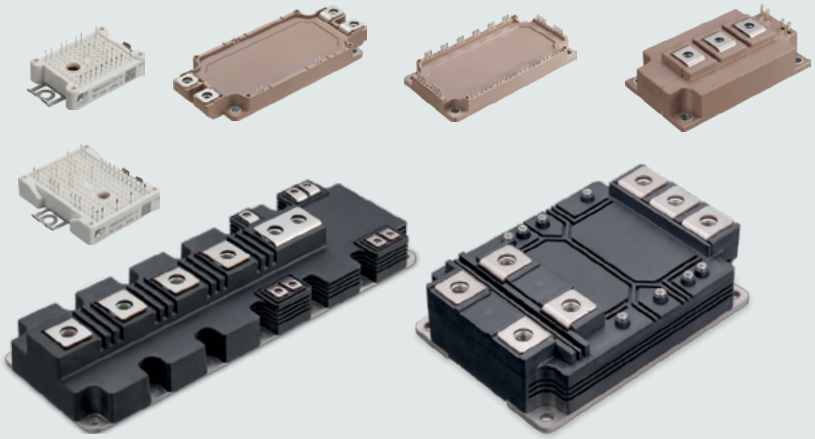
The 1200 V SiC diodes, produced at PASC's fabrication facility in Taiwan, have been shipped to India and validated to meet global industry standards. RIR Power has already secured purchase orders from key suppliers to the commercial, industrial and defence sectors. This achievement aligns with India's Make in India initiative, reinforcing the nation's semiconductor supply chain and reducing reliance on imports for critical defence technologies. RIR Power's new SiC semiconductor facility in Odisha, is set to further enhance India's indigenous manufacturing capabilities.

www.ruttonsha.com

Fuji Electric
Innovating Energy Technology

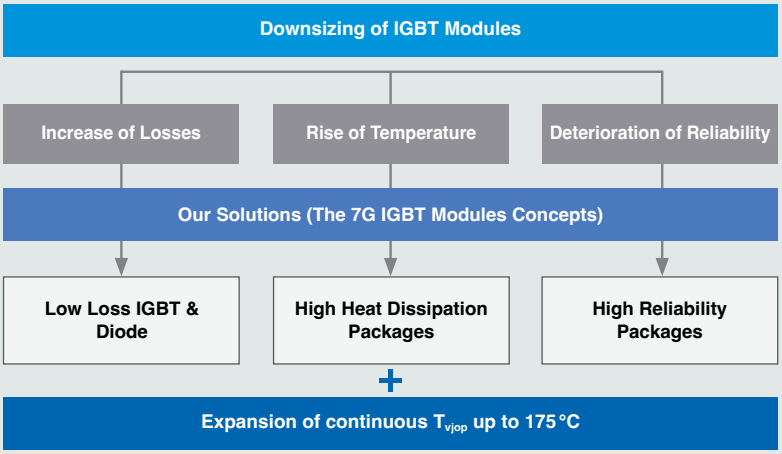
7th Generation X series

Top Class in Power Density and Reliability



MAIN FEATURES

- 7G IGBT & FWD
- New internal layout
- Higher reliability
- High temperature silicone gel
- Solder or press-fit pins
- Advanced bond wire design
- High thermal conductive ceramic substrate
- V_{iso} up to 4 kV
- Lower V_{cesat}
- Improved efficiency
- Available in various package types from low to high power ranges



www.fujielectric-europe.com

The smarter E Europe 2025: “We are the Energy System”

Despite a two-day overlap with PCIM in Nuremberg, The smarter E Europe 2025 in Munich – which naturally addresses a much larger target group – proved to be the almost customary successful event. Europe’s largest alliance of exhibitions for the energy industry turned the Bavarian capital into the epicenter of the global energy industry – and the numbers once again speak for themselves: On three days, 2,737 exhibitors from 57 countries presented their technologies, business models and mature solutions for an intelligent, integrated and fully renewable energy system.

By Roland R. Ackermann, Correspondent Editor, Bodo´s Power Systems

At the end of the day, around 107,000 trade visitors from 157 countries took the chance to take care of old contacts and establish new ones as well as to set up partnerships or initiate projects. Furthermore around 2,600 attendees visited the accompanying specialist conferences and side events.

Once again, the rising complexity, interconnectedness and integration of our energy systems became abundantly clear. Sectors and industries are no longer merely coupled — they are evolving together within a decentralized, digital, and intelligent framework. The outcome will be a dynamic, integrated system for the physical and economic realization of the energy transition.

Renewable energies are no longer just a nice add-on – in many markets they have become a force to reckon with, determining the way the energy systems will be structured. And they are expanding at a remarkable pace across the globe.

Positive feedback from organizers

Despite the challenges that some parts of the industry are facing right now, the general atmosphere at The smarter E Europe was extremely positive. It was abundantly clear that the gathered thinkers, doers and decision makers are brimming with passion and optimism as they work to advance the energy transition. The event once again highlighted the industry’s strong unity, as well as the enthusiasm and innovative power they put into driving the energy transition.

Markus Elsässer, CEO and founder of Solar Promotion GmbH, who organizes The smarter E Europe alongside Freiburg Wirtschaft Touristik und Messe (FWTM) was very positive about the three successful exhibition days: “Our four exhibitions complement each other, covering the key topics of the energy transition in both breadth and depth. Once again, The smarter E Europe provided the blueprint for the climate-neutral energy world of the future. The path has been laid out, the technologies and solutions needed to get there already exist. It is now about following that path unerringly. Because we are the energy system.”

Markus Elsässer mentioned a particular highlight of this year’s event: “I am absolutely delighted about the attention and positive feedback our special exhibit on bidirectional charging attracted. With the special exhibit we played to one of our major strengths, having our finger on the pulse and working with the renewables industry to highlight the right topics at the right time.

Innovations in Action:
The Winners of The smarter E AWARD 2025

On the eve of the official start, the winners of this year’s The smarter E AWARD were honoured at an official ceremony. Winners included visionary products, solutions and projects that pave the way for a renewable energy world with innovative technologies and smart concepts – pioneering, bold and relevant. Three equal winners were selected in each of the five categories, Photovoltaics, Energy Storage, E-Mobility, Smart Integrated Energy and Outstanding Projects – a strong indication of the industry’s innovative breadth and depth. The range they cover is truly impressive – from cloud-based planning software, optimized hardware components and novel storage technologies to projects of various sizes with an immediate social and ecological impact, both locally and globally.

Among the winners in the Energy Storage category was the German company CMBlu Energy: Their organic SolidFlow battery combines high performance with low environmental impact. Series production is set to start in 2026. The long-term storage system can store 200 kWh of electricity and have an output of 40 kW. The modular design means that the system is scalable up to the GWh range and can store energy for several days. The design follows circular economy principles by using no rare or problematic materials and by consisting of 100 percent recyclable components. The unique chemistry combines solid organic polymers with an organic, metal-free electrolyte. The company claims that the battery has in excess of 20,000 charging cycles and a DC-DC efficiency up to 90 percent. The panel of judges highlighted the impressive energy density, the innovative chemical composition and the economical, scalable operating principle of the organic SolidFlow battery.

Further examples are a Compressed Air Energy Storage from Canadian company Hydrostor or a 5-minute backup solution for UPS from Samsung SDI based on lithium-manganese-oxide (LMO) battery chemistry, which enables quick charging and discharging while maintaining a high level of thermal stability. Samsung SDI even received another award: in the E-Mobility categories. Hyunyoung Kwak, Samsung SDI’s Vice President, said: “The holistic approach of the exhibition – integrating storage, generation, digitalization, and grid solutions – aligns perfectly with our vision of a safe and sustainable future. Making renewables available 24/7 is no longer a distant goal; it is becoming a tangible reality, especially in Europe, where policy, technology, and market forces are rapidly converging to drive the energy transition.“

While the global deployment of renewable energies is in full swing, the next step will be to make the energy system more flexible, more digital and more integrated. The smarter E Europe will return to Munich from June 23–25, 2026.

www.thesmartere.de

Need a HIL simulator that handles the fast switching of your EV charger?

The RT Box is your answer.

Simulate your DAB, LLC, or PSFB with 4 ns step sizes on the RT Box

plexim
electrical engineering software

A New Era of Power Analysis for Automotive and Beyond

Introducing the AVL X-ion™ PA2 Power Analyzer - advanced versatile features in a seamless measurement solution

AVL List GmbH, renowned for its pioneering measurement devices, continues to revolutionize automotive and electrical testing. The latest addition to their product portfolio is the AVL X-ion™ PA2 High Precision Power Analyzer. This feature-rich device delivers unparalleled testing performance, from large electrical drivetrains to single components.

Key Measurement Features:

- Up to 8 power channels / 48 channels cascaded
- 12 MS/S, 18-bit sampling for power measurement
- 100 MS/S, 14-bit sync. transient waveform analysis
- 1000V RMS CAT III voltage inputs
- 2x rotor resolver or sine/cosine signal inputs

The AVL X-ion PA2 boasts high-voltage inputs up to 1000 V RMS, which are galvanically isolated and meet CAT III requirements. A standout feature is the split of the voltage signal after the high-voltage divider into a high-precision measurement path for electrical power calculation and a high-frequency 20 MHz oscilloscope-like snapshot path with sampling at 100 MS/s. This enables precise power calculations and transient waveform evaluations at the same time, which is essential for assessing switched power electronics, revealing overshoot, rise-time, ringing, and harmonic content. Additionally, the data is available on a common time-base for post-processing various operating points of electrical systems, enhancing efficiency and controller performance.

Originating from the automotive industry, the X-ion PA2 includes up to two optional direct resolver inputs to determine the rotor position of two electrical drives. This allows for field-oriented control calculations (Id, Iq) for 2x 3-phase machines with a single power analyzer.

AVL is launching the X-ion PA2 with matching high-precision closed fluxgate current transducers, featuring Transducer Electronic Datasheet (TEDS) technology.

Interface Features:

- Integrated current sensor supply and sensing
- TEDS recognition and configuration with AVL CFC
- Raw data streaming for post processing
- NVH input modules and hybrid testing by cascading
- PTP and AVL PUMA 2™ synchronization

With its multi-physics X-ion roots, the PA2 can be equipped with noise, vibration and harshness (NVH) inputs for measuring vibration sensors, strain gauges, accelerometers via IEPE and microphones in a modular fashion. Therefore, systemic correlations of electrical signals and NVH-phenomena can be made visible. Ensuring fully synchronized testing setups of hybrid systems, involving combustion engines and electrical motors, X-ion family devices can be cascaded.

Testbed integration with AVL PUMA 2™ automation software is seamless and world-class. Time-stamped data and results are delivered to the AVL toolchain to guarantee synchronization across different sampling speeds. Furthermore, the system can be integrated with third-party automation systems and Precision Time Protocol (PTP) connectivity.

The AVL X-ion™ PA2 comes with AVL BEAT™ measurement control and post-processing software. Complementary accessories for wiring and installation add to the completeness of the solution.

www.avl.com


Lukas Philipp, Daniel Rückert, Thomas Schulze und Steffen Knapp, GVA experts for development
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POWER ELECTRONICS EXPERTS

Calibration ensures Confidence in Current Measurement

The value – usefulness, if you prefer – of any measurement depends on the accuracy of the measuring equipment. For a test set up to be reliable and repeatable, the instruments used must be calibrated regularly in accordance with international standards.
But that process can be time-consuming, involving a lot of paperwork. More, during the calibration process, the equipment being calibrated is not available for the job it was intended to do in supporting development, production and operational tasks.

By Morten Birkerod, Calibration Laboratory Manager, Danisense

There is an increasing need for accurate current measurement. In the automotive EV industry, high performance, reliability and accuracy are key criteria for electronic components and systems. Test benches used to analyse the entire drive system can require several conversion stages – electrical and mechanical – and for a deep understanding of where losses occur, therefore high accuracy is required. Another significant market for current measurement is renewable energy. With traditional hydrocarbon-fuelled power plants it is relatively easy to monitor current levels because the energy flow is highly predictable and comes from a centralised source. With solar and wind the energy load is much more dynamic, with many more smaller power generation sources and unpredictable fluctuations as the weather conditions change. A third application is large physics institutions, such as CERN, where accuracy is an inherent requirement. These users are the most demanding, pushing for parts per million accuracy levels, whereas other applications might only require, essentially, a functional test.

Figure 1: For a test set up to be reliable and repeatable, the instruments used must be calibrated regularly in accordance with international standards

A measurement can only be as accurate as the instrument itself, and calibration provides a level of confidence in the veracity of that measurement. Essentially there are two aspects to calibration: a functional 'pass/fail'; and the accreditation traceability issue. Calibrations are performed to an international standard ensuring that results from anywhere in the world will be consistent. ISO/IEC 17025 is the international standard for testing and calibration laboratories, focusing on their competence, impartiality, and consistent operation. ILAC G8 assists laboratories in the use of decision rules when issuing statements of conformity to a specification or standard as required in the 2017 edition of ISO/IEC 17025.

All calibration relies on a comparison of the device under test (DUT) with a known good, or 'golden', reference. One of the issues with current sense transducers lies in ensuring the quality of the reference transducer. Reference instruments of sufficient quality are rare – so much so that Danisense has created its own which has been certified by the Federal Institute of Metrology METAS in Switzerland which serves as that country's National Metrology Institute (NMI).

Fundamentally, the calibration process is thus: a known reference current is passed through both the device under test and the reference, and a measurement is performed on each simultaneously. A burden (or reference) resistor is used to convert the current into a voltage, so it is also very critical to use the highest quality resistor, since resistors can suffer from instability.

We have discussed why it is important to have current sense transducers regularly calibrated. But what should the period between calibrations be? Danisense produces both voltage and current output sensing devices. Voltage output products employ a resistor module, and as such, may need calibrating more often than current output units which do not require the resistor module. Certified test houses are not allowed to give guidance on the frequency of calibration, however periods of one and even two years between calibrations is common. More often, companies have their own quality procedures which will state the frequency.

One of the greatest inconveniences caused by calibration is the length of time it can take. Test houses routinely quote four weeks turnaround. This may be because they are usually generalist companies that offer a wide range of test services. As such, they may not attract much business from the rather specialised current sense transducer sector, so when they do, they will have to set up from scratch each time.

Another challenge that faces current sense transducer users when they request a unit to be calibrated is that they may be asked a multitude of questions concerning the nature of the data that the user requires from the test. The person in charge of organising the calibration for the user is likely to be a quality manager who may not have specific knowledge of the measurements required, causing further delays and headaches.

To address these issues, current sense transducer manufacturer, Danisense, has created an ISO/IEC 17025-accredited calibration laboratory at its Taastrup headquarters in Denmark. Because the only calibration that the facility will undertake is current measurement equipment, the set-up is permanent. This means that the process has been streamlined and automated, so the company is promising a 10 working day turnaround service. When considering accuracy, Danisense created its own reference which benefits from

a very high accuracy, so customers can have a very high degree of confidence in the accuracy of the results. The Danisense lab is also able to help customers with the process of defining conformity limits which best suit their application.

Figure 2: Danisense has its own ISO/IEC 17025-accredited calibration laboratory and offers brand agnostic calibration services for current transducers

Intriguingly, the Danisense current measurement test facility is brand-agnostic and will accept equipment made by Danisense's competitors for testing, as well as the Danish company's own products.

Customers can use a new personal online portal[1] to book their ISO/IEC 17025-accredited calibrations. The portal provides customers with 24/7 availability of the calibration reports, regular online and email updates during the calibration process, and detailed order tracking as well as access to an online payment function.

Calibrating equipment is crucial to ensure the accuracy, reliability, and safety of measurements and operations. It maintains equipment within specified tolerances, preventing errors and ensuring consistent results, which is vital for quality control, regulatory compliance, and ultimately, saving money by reducing downtime and waste. When dealing with demanding applications, such as electric vehicles, power grid analysis and international research organisations such as CERN, it is of paramount importance that users can have the fullest confidence in accuracy and reliability of their measurements. Danisense's current sense transducers have been proven to be amongst the most accurate instruments of their type and the new independent calibration service will reduce time lost while instruments are being calibrated, as well as demystifying the process.

[1]: https://danisense.com/webshop/

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Structural Optimization and Performance of the new SiC-LV100 for 1.5 kV_{dc} Renewable Applications

The SiC-MOSFET module currently being developed utilizes body-diodes and realizes high current density. The target application is 1,000 V_{ac} / 1,500 V_{dc} 2-level inverters systems in renewable energy systems like solar and wind power. The optimized structure tackles the challenge of risks due to high current density and high-speed switching.

By Akiyoshi Masuda, Mitsubishi Electric Europe B.V., Ratingen, Germany and Tetsuo Yamashita, Mitsubishi Electric, Fukuoka, Japan

Introduction

As the share of renewable energy continues to grow, the demand for large capacity, high power density, and greater efficiency is increasing. Mitsubishi Electric is developing a power module utilizing SiC-MOSFET devices to meet these requirements.

SiC-MOSFET devices show high efficiency with low power losses by high-speed switching. The power module consists of only SiC-MOSFETs without separate diodes by utilizing the body-diode built-in the MOSFET in large capacity housing "LV100". This configuration realizes high current density and a current rating of 1,800 A (under development). Besides, the optimized voltage rating for excellent LTDS performance (, which matches the optimal solution for 1,000 V_{ac} and 1,500 V_{dc} systems as the recent link voltage standard for renewable applications.

High current density leads to significant heat generation, demanding excellent thermal performance for effective heat dissipation. SiC-LV100 consists of high thermal conductive components like Aluminum Nitride (AlN) substrate.

On the other hand, such high current density and high-speed switching could result in lower module robustness. This module integrates higher number of parallel-connected MOSFET chips than conventional modules with separated transistors and diodes chips. However, this setup makes it challenging to maintain uniform current distribution among all chips. Parallel-connected MOSFETs, which are designed to realize high-speed switching with low capacitance, can lead to gate voltage oscillation, potentially resulting in unexpected failures.

Accordingly, the design incorporates appropriate components and a well-optimized layout to ensure stable operation. The LV100 module shows high performance by SiC-MOSFETs, along with sufficient capability provided by its improved structural design.

Module configuration

Mitsubishi Electric adopted Solid Cover (SLC) technology with insulating metal baseplate and resin encapsulation for the 7th generation Si-IGBT modules, such as LV100 housing [1]. This packaging technology shows competent thermal resistance and an isolation voltage of 4 kV. Furthermore, it improves thermal cycling capability by eliminating the solder layer beneath the substrate. This is achieved by using an insulated metal baseplate (IMB) that integrates the insulating layer, circuit pattern, and baseplate as a single component. Electrical isolation from the baseplate is maintained by the resin-based insulating layer.

However, the new SiC-LV100 adopts a high thermal performance AlN substrate and cupper baseplate e with encapsulating gel to make full use of SiC-MOSFETs.

The following are the main features of SiC-MOSFETs:

1. High thermal conductivity, which enables efficient heat dissipation.
2. Wide bandgap energy, allowing stable operation at elevated temperatures.
3. High breakdown electric field, enabling a thinner drift layer and reduced on-resistance.

SiC-MOSFET enables higher current density than Si-IGBT due to these properties. As a result, high current density is a key selling point for SiC power modules. The LV100 module has been optimized for high current density with excellent thermal dissipation capability.

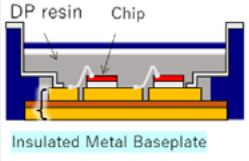
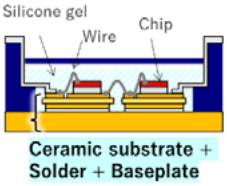
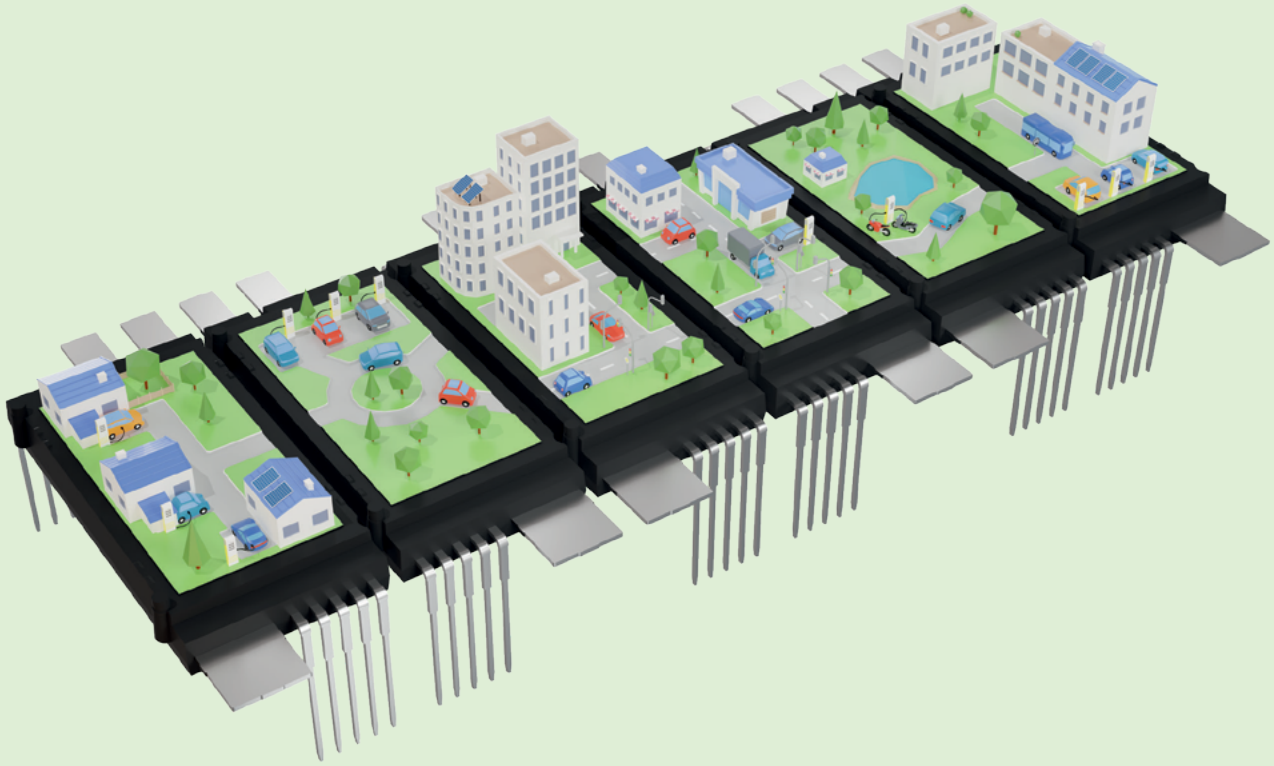
Structure	Si-LV100	SiC-LV100
Appearance		
Outline		
Sealing Material	Resin	Silicone Gel
Substrate	Insulated Metal Baseplate	Ceramic Substrate
Chip	IGBT,FWD	Only MOSFET

Table 1: Configurations of Si-LV100 and SiC-LV100

AUTOMOTIVE HOME APPLIANCES INDUSTRIAL POWER TRANSMISSION RENEWABLES RAILWAY



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// Supports both 800 V and 400 V battery systems with flexible configuration
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1. Utilizing the body-diode built-in the MOSFET

Only SiC-MOSFET devices are mounted on the SiC-LV100 module. The MOSFETs include intrinsic body-diodes, which function as freewheeling diodes for commutation during dead time operation. The MOSFET is bidirectional and can be turn-on to reduce conduction loss on freewheeling phase. The SiC-MOSFET naturally combines transistor and diode functions within a single device, leading to more constant heat generation and improved thermal dissipation. Moreover, the required mounting area for SiC-MOSFETs is smaller than that of a separate transistor-diode pair. As a result, more devices can be mounted on a single module, thereby increasing the current density of the module.

2. Ceramic insulation Structure with AlN substrate

Aluminum nitride (AlN)-based substrates are known for their excellent heat dissipation performance. In the SLC structure adopted in the Si-LV100 modules, the mounting area on the insulating metal baseplate can be increased compared to the conventional ceramic insulation structure [1]. However, since SiC devices achieve high current density per chip, mounting area is unlikely to become a bottleneck in thermal design or output power. Instead, improving heat dissipation becomes a more critical consideration. The use of AlN substrates further enhances the module's thermal performance.

Figure 1 shows a thermal analysis comparison between the SLC structure and the ceramic insulation structure with an AlN substrate, assuming the SiC-LV100 module. As can be seen from the figure, the ceramic insulation structure with an AlN substrate achieves a lower junction temperature (T_{vj}) in the simulation. Although the layout, chip size, and number of chips differ, the total mounting area was equal in both cases, minimizing the impact on thermal performance.

The images show the differences in internal layouts, chip size and chip count. However, the total chip mounting area was the same, so these differences have negligible impact on thermal performance.

Figure 2 shows the impact on the thermal resistances. $R_{th(j-c)}$, is defined from the chips to the case and $R_{th(c-s)}$ is defined from the case to the heatsink. Thermal resistance from the chips to the heatsink is 11 % lower in the ceramic insulation structure with a AlN substrate compared to the SLC structure.

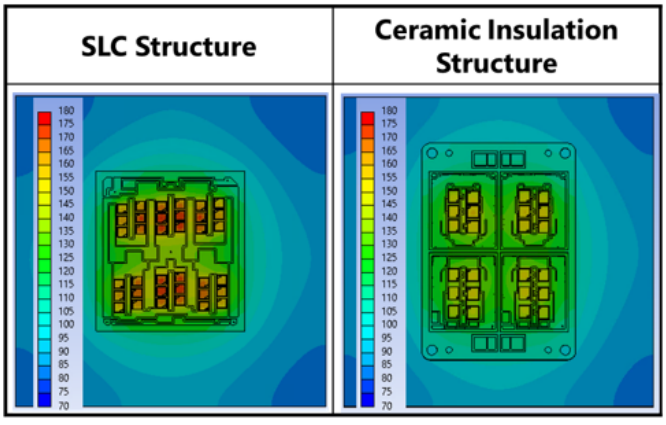

Figure 1: Temperature Distribution Comparison

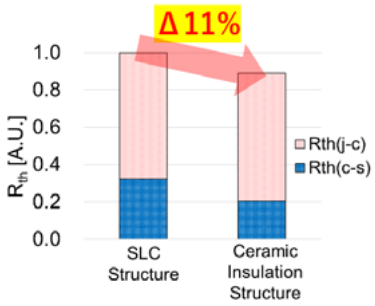

Figure 2: Thermal Resistance Comparison

Concerns with high current density and high-speed switching

SiC devices generally exhibit high-speed switching and low switching losses. Especially the SiC-LV100 adopted 2nd generation planar SiC-MOSFETs because it can reduce the capacitance and achieve the high-speed switching [2]. On the other hand, this module includes more parallel devices internally than conventional Si-IGBT modules to achieve higher current density. These features may lead to the following risks.

1. Uneven current distribution
2. Gate voltage oscillation

Parallel chips exhibit differences in impedance in both the gate and main current circuits. These impedance differences make it difficult to maintain balanced collector current among the individual parallel chips. Current concentration in specific chips may result in rapid current change (di/dt), which can degrade the module robustness due to surge voltage caused by stray inductance (Ls) and di/dt. In addition, a parallel chip layout often induces gate voltage oscillation, which becomes more pronounced as the number of parallel chips increases and the switching speed becomes higher [3]. This oscillation occurs because each chip forms an LC-resonant circuit, and these multiple LC circuits interfere with one another. To suppress gate voltage oscillation, the SiC-LV100 circuit layout is optimized to minimize impedance differences among the parallel chips.

Figure 3 compares source inductance between parallel chips for two different layout types. In the bottom graph of Figure 3, the source inductance of each of the six chips, based on analysis, is shown. The optimal layout minimizes the source inductance of each chip, and the variation is reduced by approximately 70 % compared to the conventional layout.

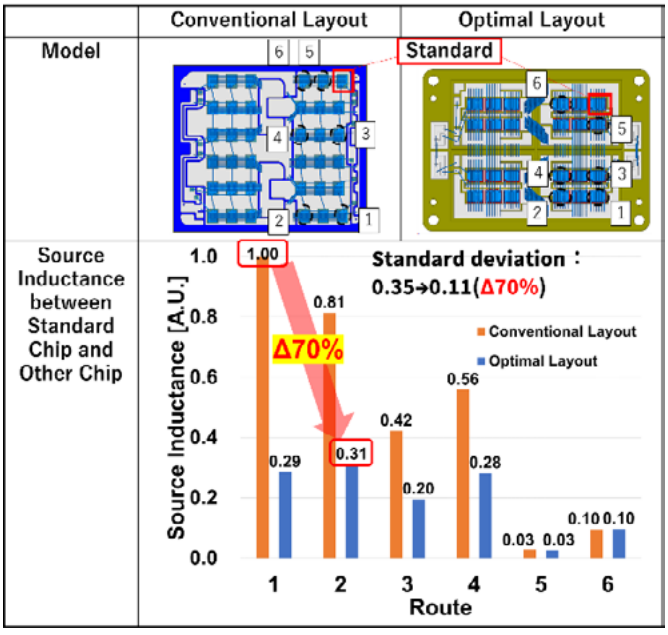

Figure 3: Models and Results of Source Inductance Analysis

Figure 4 shows a comparison of current distribution among parallel chips along the X axis. The optimal layout improves current balance across the chips and reduces the peak di/dt in the parallel configuration. This optimal design addresses the two risks mentioned above and ensures stable module performance.

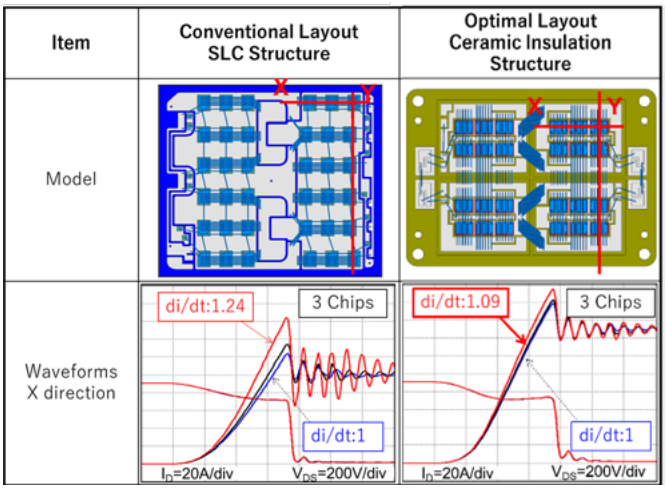

Figure 4: Models and results for current flow analysis between chips

Performance comparison

The SiC-LV100, which targets a voltage rating of 2,500 V, is designed for 1,500 V_{dc} link voltage applications using a 2-level topology. This module features an on-resistance of $R_{DS(on)}$ = 1.9 mΩ (under development) at T_{vj} = 150 °C.

Table 2 and Figure 5 present the performance comparison with two Si-IGBT-based solutions that are also suitable for 1,500 V_{dc} systems: a 7th generation 1,200V Si-IGBT module using a 3-level A-NPC topology, and a 7th generation 2,000V Si-IGBT module using a 2-level topology. In this comparison, the SiC-LV100 achieves more than a 100 % increase in output current compared to Si-IGBT module solutions.

Item	3-level A-NPC 7th Si-IGBT Module	2-level 7th Si-IGBT Module	2-level SiC-MOSFET Module
Type Name (Rating)	CM1200DW-24T (1200 V/1200 A)	CM1200DW-40T (2000 V/1200 A)	New-Module (2500 V/1800 A)
Number of Modules	3(1phase × 3modules)	3(1phase × 3modules)	3(1phase × 3modules)
f_c	2 kHz	4 kHz	4 kHz
Footprint		100% (Equivalent)	
I_o (at T_{vj}=150 °C)	100%	83%	**200%**

Table 2: Summary of Performance Comparison (Other conditions: V_{dc} = 1500 V, Power factor = 1, and a modulation index = 0.7)

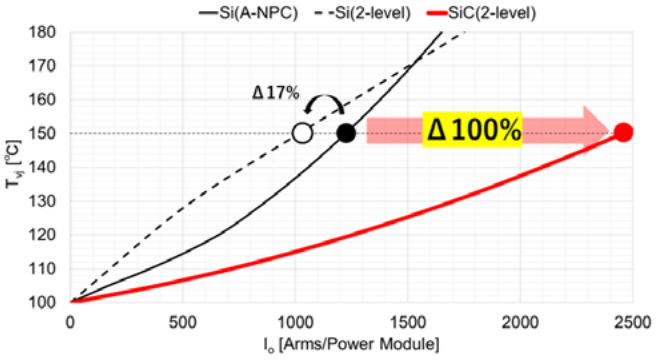

Figure 5: Correlation between I_o and T_{vj}

Conclusion

The new SiC-LV100, targets a voltage rating of 2,500 V, is developed for 1,000 V_{ac} / 1,500 V_{dc} 2-level inverters systems in renewable applications. In addition to the high thermal conductivity of SiC itself, this module employs the ceramic insulation structure with an AlN substrate to achieve both excellent heat dissipation and high current density. With this configuration, the thermal resistance from the chips to the heatsink becomes 11 % lower compared to the SLC structure adopted in the Si-LV100 modules. However, the high current density and high-speed switching introduce two key challenges: uneven current distribution and gate voltage oscillation. To address these issues, the module's internal layout has been optimized to minimize the source inductance of each chip.

In comparison with conventional 7th generation LV100 modules using both 2-level and 3-level A-NPC topology, the SiC-LV100 achieves over a 100 % increase in output current. By taking advantage of SiC-MOSFETs and an optimized structural design, the SiC-LV100 demonstrates outstanding performance and enhanced robustness.

References

[1] Takuya Takahashi et. al., "A 1700V-IGBT module and IPM with new insulated metal baseplate (IMB) featuring enhanced isolation properties and thermal conductivity", PCIM Europe 2016.
[2] Kenichi Hamano et al., "2nd generation High performance 4H-SiC MOSFETs with 1.7 kV rating for high power applications", PCIM Europe 2019
[3] Florian Sawallich et al., "Inter-chip Oscillation of paralleled SiC MOSFETs", PCIM Europe2023

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Galvanic Isolation And EMI/EMC Immunity between Switch and Controller in Mid-to-Large Drive Applications with Plastic Optic Fiber

Plastic Optic Fiber (POF) emerged in the late 1970s and found its first application in power electronics with the release by HP of connectors which provided a path to use POF as an isolation technology to provide both galvanic isolation between two PCBs as well as isolation from EMI/EMC.

By Michael O'Gorman, Application Engineering Manager, Firecomms

Today POF links are a key part of mid-range and large drives providing the protection needed by the controllers from the electronic noise generated by the switching technology of choice (Thyristors, IGBTs and SiC devices). Looking at the connectors it is not obvious that much has changed. The from factor looks identical but under the hood this technology has grown significantly to meet the demands of the 21st century Power Electronics Industry.

Under the hood new ASICs have revolutionized the performance taking the solutions from 40 kBd to 50 MBd with TX drivers fully integrated and enhanced EMI/EMC immunity.

Today this market is multi-sourced with four major manufacturers of the fiber (Mitsubishi-Rayon, Toray, Asahi-Kasei and Sino-Optic) as well as multiple global suppliers of the optical connectors/transceivers such as Firecomms. The RedLink connectors from Firecomms have seen significant developments that are not obvious to the casual observer. Comparing the original Plastic Optic Fiber and the original HP transceiver datasheets to the parts available today, the first item that a keen reliability engineer will spot is the increase in temperature range.

The original parts were limited to 0 to +70 °C. Today you have both fibers and transceivers rated to an industrial temperature range of operation in ambient temperatures of -40 to +85 °C and higher for some options. This development was driven by the demands of the applications. A locomotive sitting on a side-track in Alaska will experience severe cold while the same locomotive crossing the central desert of California at midday will need to tolerate very high ambient temperatures. This demand is equally relevant to Solar Energy farms located in deserts or Wind Farms located in our oceans not to mention HVDC technology in remote power plants as well as the SVG and SVC units required to balance the power lines in all of these installations. Thousands and thousands of hours of engineering and reliability testing has produced plastic optic fiber links suitable for use in 21st century Smart Grid applications.

A deeper dive under the hood will reveal that the majority of transmitters used today use RCLED technology instead of the original LED technology. The original LEDs were slow devices with long rise and fall times and they needed relatively high currents to generate the optical power needed to provide stable links with long lifetimes. With the arrival of commercially available industrial Resonant Cavity LEDs (RCLED) in the early 2000's the transceiver manufacturers were able to make faster devices which use a lot less current to achieve the same optical power levels. Today you can get 10 and 50 MBd transceivers that use a fraction of the current consumption required by the original 40kBd and 1MBd LED based transmitters to achieve the same optical powers. Reducing current is obviously important for saving the planet by reducing the energy demand of the devices built with these parts but also has a significant benefit to long term reliability as every reduction in current consumption results in a fourfold increase in transmitter lifetime. Increasing the product lifetime leads to lower OPEX and CAPEX, due to direct reduction in field maintenance costs. In summary the transmitters available today are faster, have less skew (less part to part variability), use less current to generate the same optical power, last longer and therefore require less maintenance.

The improvements are not limited to the transmitter side of the link. The receiver end of the POF link has also seen significant development in the last 15 years. Originally, the HP receivers were based on Bi-CMOS technology with a single integrated photo-diode. Firecomms ASICs are designed on pure CMOS process nodes, that allows for integration of more intelligence into the receiver solution. These custom Firecomms ASICs integrate all of the functions necessary to convert the optical signal to a digital output signal. At the front end the physical interface uses a dual-photo-diode scheme to detect the light. A photo diode detects the light and a mirror photo-diode is screened from the light, both elements experience all of the electronic and magnetic fields emanating from the nearby switches, e.g. an IGBT.

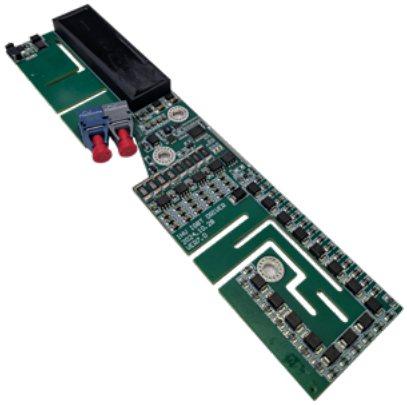

Figure 1: Insulated-Gate Bipolar Transistor (IGBT) Drive Board

The photo-diode signals are fed into a differential amplifier which cancels the common electronic/magnetic noise and as a result forwards the clean optical signal now converted to a clean electrical signal. The electrical signal is amplified, put through a comparator and finally through a line driver stage conditioning it for release to a TTL, LVTTL or LVDS data bus as a standard electronic signal. The receivers available today feature dual operation from both traditional 5V power supply rails as well as 3.3V supplies and can therefore interface directly to older TTL logic ICs as well as modern standard 3.3V based Micro-controllers, FPGAs, ASICs and PHY ICs. In summary, the receivers available today compared to an historic ROSA leverage CMOS based ASICS that have excellent EMI immunity thanks to the differential photo-diode front end, the fully integrated signals path and the ability

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- Low thermal resistance

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- Lower loss characteristics than Si IGBT module
- High channel temperature ($T_{ch,\,max}$ = 150°C)
- Low stray inductance
- Low thermal resistance

Featured Products

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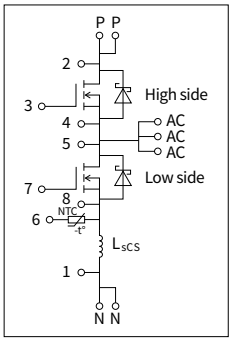
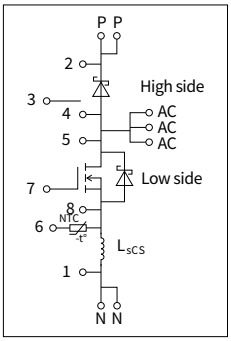
  600A – MG600Q2YMS3
- 1700V 250A – MG250V2YMS3
  400A – MG400V2YMS3
- 2200V 250A – MG250YD2YMS3

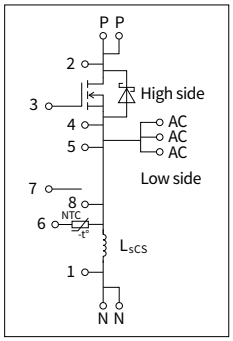
Internal circuit options



Half bridge

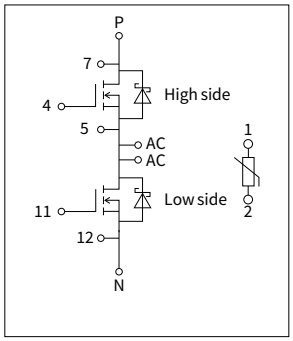


Chopper low



Chopper high

Internal circuit option



Half bridge

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to adapt automatically to the supply line and output the correct logic level for the next step in the signal path.

Fundamentally with the introduction of CMOS ASICs into both the transmitter to drive the RCLED and the receiver to cleanly detect the light, the POF transceiver today provides a true digital bridge from one electronic bus to another across a plastic optic fiber giving galvanic, electrical and magnetic noise field immunity from DC to 50 MBd with a minimal application circuit.

The introduction of ASICs integrated into the optical components, the digital bridges offers customers the possibility to use POF for galvanic isolation and EMI rejection not just in the equipment layer of their system but as illustrated in all three of the system layers from the equipment, to the networking of drives and with the Fast Ethernet devices even out to the IT layer providing protection between the drive network and the wider IT network.

At a PCB level the digital bridges automatically configure to match the power rail available and by extension the correct logic levels of the PCB that they sit on. They can be used for alarm signals holding a static light on or light off for years and years without error or can be used in the traditional way for PWM delivery from drive controller to switch. However this technology has wider scope with the new higher speeds which can also be used to network the drives helping to co-ordinate multiple drives across a network of devices.

The new generation of DC-50 MBd devices have extended the benefits of noise immunity beyond singular IGBT or SiC control to include the networking of multiple controllers with superior noise immunity that traditional copper wire cannot provide. The simple connectivity of POF with proven reliability can network any number of drives.

Beyond 50MBd, it is also important to note that POF can also support higher speed such as Fast Ethernet and right up to 250 MBd.

Figure 2: Silicon Carbide (SiC) Core Driver Board

The majority of FPGAs used today support a native LVDS port operating at 200 Mbps and this will interface directly to a POF transceiver offering fully duplex datacomms links supporting real time monitoring of power systems in locomotives, smart grids, and power monitoring in data-centers. The datacomms links over POF support real time protocols such as EtherCAT and Profinet as well as proprietary links.

To summarize, Plastic Optic Fiber and the humble HP connector have come a long way. Today, it can support not just a basic PWM signal between driver controller and thyristor but an array of IGBTs and SiC devices. The POF link can also be used in the next levels of control hierarchy, to network a number of drive controllers together for higher efficiency and again in the third layer where the drive network controller meets the wider IT system network. POF can offer real-time compatible links operating at internet speeds providing complete galvanic isolation between the IT systems and the electrical plant. All three layers of operating come with proven reliability, simple and robust fiber termination, eye safe visible red light, low current consumption and operation over industrial temperatures in harsh environments. Plastic Optic Fiber links are, therefore, ideal for use in 21st century Smart Grids.

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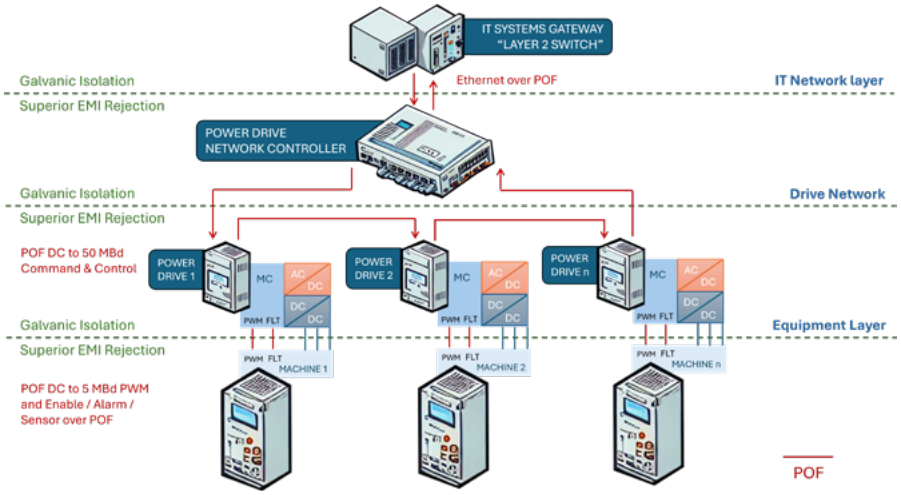

Figure 3: Galvanically Isolated Smart Grid Networking Solution

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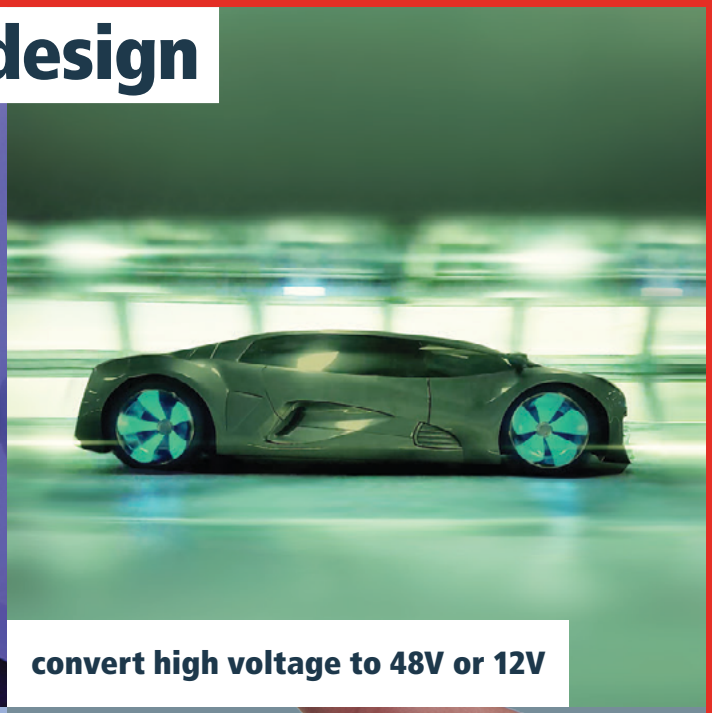

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Advanced SiC Trench Gate MOSFET Technology for Automotive Applications: High Performance Meets High Robustness

SiC trench gate MOSFETs deliver superior performance in terms of both switching and conduction losses. To maintain this performance advantage while meeting the robustness and lifetime requirements of automotive applications, careful attention must be paid to the device design. The example of Bosch's dual-channel SiC trench gate MOSFETs shows how this can be achieved.

By Jens Baringhaus, Steffen Beushausen, and Klaus Heyers, all Robert Bosch GmbH

Dual-Channel SiC Trench Gate MOSFETs: Enablers of High Performance

The introduction of the trench architecture marked a significant advancement in SiC device technology. The low switching losses and low specific on-resistance of SiC trench gate MOSFETs instantly made them an ideal choice, particularly for automotive converter applications such as traction inverters, on-board chargers, and DC-DC converters. However, classic planar MOSFETs were initially considered a better match for automotive applications due to their greater robustness – particularly of the gate oxide – and their simpler manufacturing process.

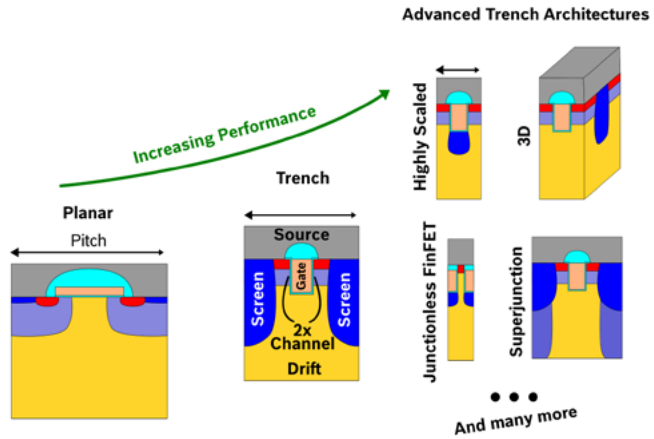
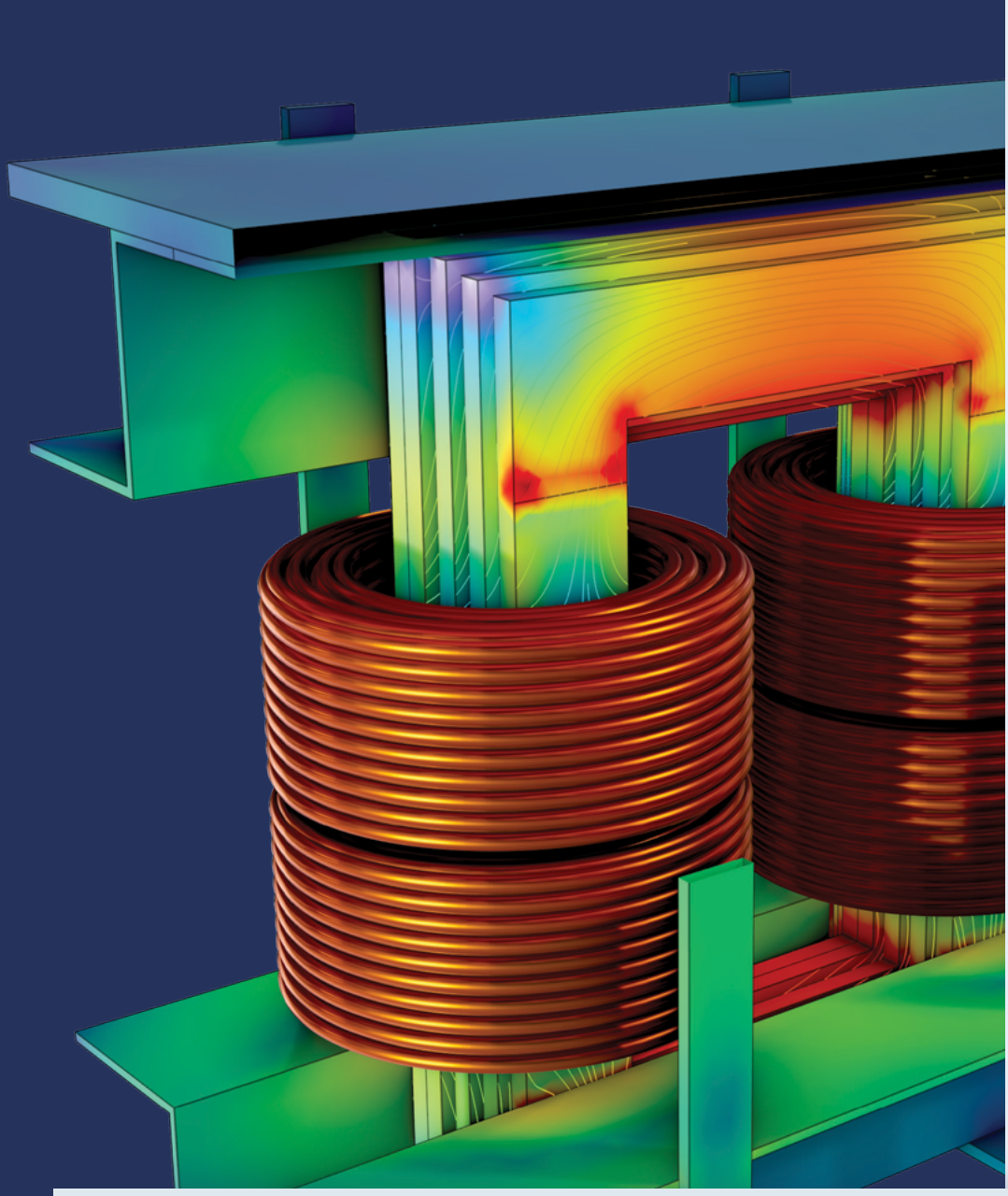


Figure 1: Advancement of SiC MOSFET device architectures over time.

Today, advancements in device design and manufacturing have closed the robustness gap, allowing SiC trench architectures to offer superior performance while matching the robustness and yield of their planar counterparts. Consequently, SiC trench gate power MOSFETs are now an excellent fit for all high-voltage systems in electric vehicles. With the upcoming transition to more advanced architectures, SiC trench gate MOSFETs are set to soon surpass planar architectures in both performance and robustness. Their smaller cell pitch, which results in lower conduction and switching losses, will make trench gate architectures a more desirable choice. Bosch is one of the only manufacturers of SiC trench gate MOSFETs to date, combining high performance with solid robustness.

The evolution of SiC power device architectures over time (see figure 1) illustrates the transition from conventional planar to trench and subsequently to advanced trench architectures. Bosch's self-developed dual-channel trench design allows for two electron channels in each unit cell, effectively halving the contribution of channel resistance to total on-resistance compared to single channel architectures. Since channel resistance is one of the most important resistance contributions in the voltage classes typically used in electric vehicles (750 V and 1,200 V), the full utilization of the channel area yields a significant advantage.

In the future, advanced trench architectures can further reduce this key resistance contribution by lowering pitch size and increasing channel density. Additionally, these designs target JFET and drift zone resistance. Key trends include ultra-narrow pitch designs, the development of 3D structures by extending p-type contact regions and shielding regions into the third dimension, junctionless FinFET architectures, and trench superjunction devices. Today's trench designs should therefore be viewed as a starting point for the development of new MOSFET designs, which will ultimately achieve the lowest possible conduction losses and enhance the robustness of SiC power devices.



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Reliability in Dual-Channel SiC Trench MOSFETs: Adding more Design Freedom

Key aspects of improving reliability in SiC trench gate architectures for automotive applications include the gate oxide quality as well as its robustness against cosmic rays. Figure 2 (top) shows the simulated electric field during off-state operation of a Gen2 Bosch dual-channel trench MOSFET. Bosch's Gen1 to Gen3 utilize deep p-type ion implantation to push the electric field deep into the semiconductor. This additional degree of design freedom is not present in planar SiC MOSFETs. Adapting the implant profile (doping, energy, implant angle) makes it possible to tailor the deep p-type screening and the current spreading regions, which constitute the JFET area. The electric field can thus be shaped to diminish electric field peaks, reducing both the electric field in the gate oxide and the field in the SiC itself.

A primary factor in ensuring the gate oxide's long-term reliability is proper shielding against the reverse bias field, which is a main source of hole injection. The gate oxide of a SiC MOSFET is inherently more vulnerable than that of silicon-based counterparts. The higher defectivity at the SiC/SiO2 interface and the resulting larger number of extrinsic defects makes a significant gap between application and screening voltage essential. This gap can be increased significantly with a thicker gate oxide. Since the cell pitch of trench gate MOSFETs is much smaller (and power density therefore higher), a thicker gate oxide can be implemented by sacrificing a small fraction of the on-state performance improvement. This increased gate oxide thickness enhances screening efficiency.

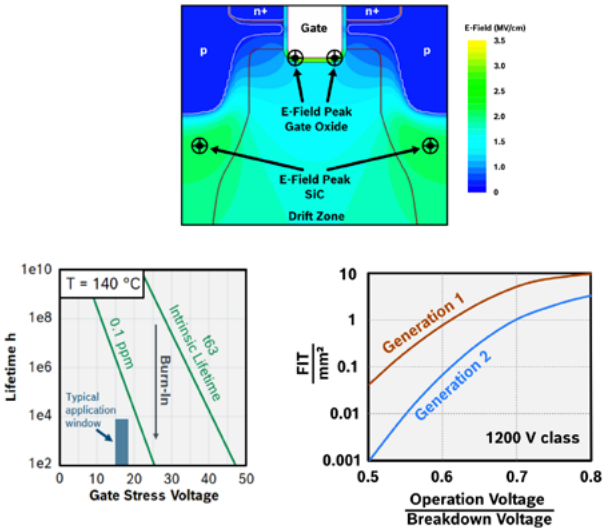

Figure 2: Top: Simulated electric field in a dual-channel trench gate MOSFET during the off-state. Left: Intrinsic lifetime of the gate oxide in Bosch's SiC trench MOSFETs. Right: FIT rate dependency on blocking voltage for Gen1 and Gen2 SiC MOSFETs from Bosch.

Figure 2 (left) presents the intrinsic lifetime (t63) of the gate oxide in one of Bosch's SiC trench gate MOSFETs, and the 0.1 ppm lifetime curve achievable through screening. Both the high intrinsic lifetime and the 0.1 ppm curve – which is well above the typical operating regime – demonstrate the excellent robustness of the gate oxide in this trench architecture.

The benefits of sophisticated shielding structures will be further enhanced with the introduction of advanced trench architectures. Since more compact designs enable more effective shielding, the gate oxide can be made even more robust, and gate oxide reliability in trenched devices is soon expected to surpass that of planar SiC MOSFETs.

While the intrinsic robustness of SiC trench gate MOSFET devices can achieve very high levels, factors such as cosmic ray impact cannot be overlooked. SiC devices are inherently susceptible to single-event burnout due to the high electric fields present during the off-state. Since cosmic ray impact cannot be avoided entirely, it must be mitigated to a level low enough to ensure low FIT rates. Therefore, both the electric field shape and the definition of the breakdown voltage must be optimized. Here again, trench architectures present an important advantage: the JFET area below the trench can be tailored to reduce electric field peaks during blocking mode, leading to enhanced robustness against cosmic rays with little $R_{on}A$ penalty.

Figure 2 (right) illustrates the FIT rates for Bosch's Gen1 and Gen2 1,200 V SiC trench gate MOSFETs with respect to the applied voltage.

By improving the electric field shape and increasing the breakdown voltage by 60 V, a 40x improvement in the FIT rate was achieved for operation at 50% of the breakdown voltage. The high cosmic ray robustness additionally makes it possible to utilize overvoltage transients (above the rated device voltage) for faster switching and lower switching losses.

Designing Future Generations

While transitioning from planar to trench and advanced trench gate MOSFETs is the best solution for applications with high power levels, the impact of these new designs on parallel operation in power modules needs to be carefully considered. In general, it is essential to avoid parasitic turn-on of a device in a power module while acting as a commutation partner. A high Miller ratio (C_{GS} / C_{GD}) is therefore generally favorable, which can be easily achieved in trench gate and advanced trench gate SiC designs as narrower pitches and more compact designs will typically push C_{GD} further down. The example in figure 3 shows the active turn-on/turn-off as well as passive turn-off of a future generation Bosch SiC MOSFET power module design study. Switching 1,000 A at 920 V in a module with four 40 mm² dies as physical switches demonstrates the complete omission of parasitic turn-on.

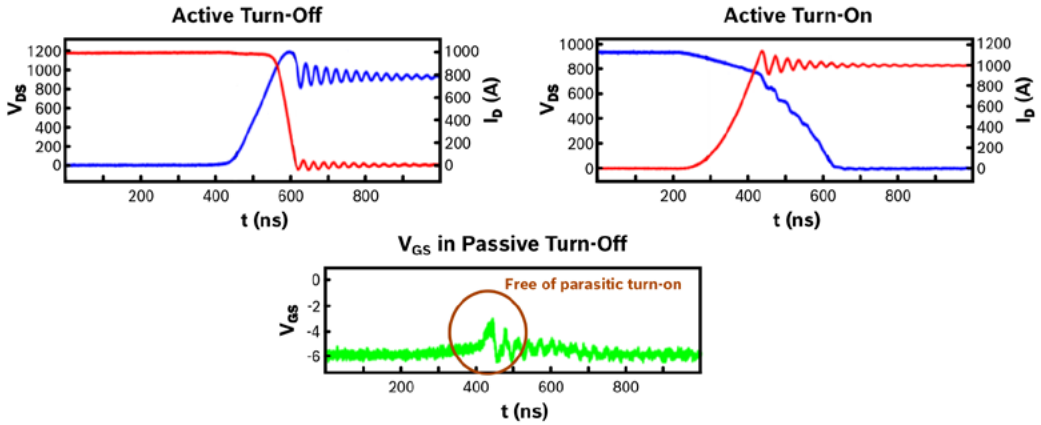

Figure 3: Switching characteristics of engineering samples of Bosch's Gen3 SiC MOSFETs in a power module setup (920 V, 1,000 A).

However, reducing C_{GD} can lead to unwanted self-excited oscillations in power modules, if they lack sufficiently low parasitic inductances in between parallel dies and exhibit a certain asymmetry for static and dynamic current sharing. In such modules, the power devices form an *LCR* circuit with the module inductances, leading to self-excited oscillations with the power MOSFETs acting as amplifiers. Damping these oscillations is possible by increasing the internal gate resistance per die. However, this has negative consequences on system level, e.g. increased switching losses. Therefore, SiC MOSFETs should be designed to prevent these oscillations in the first place. This can be achieved by reducing the C_{DS}/C_{GD} ratio. However, this leads to a design trade-off, as a higher C_{GD} is needed to dampen the oscillations, while a lower C_{GD} is beneficial to avoid parasitic turn-on.

The full power density benefit of novel SiC trench gate MOSFETs can be exploited with modern power module architectures based on advanced assembly and interconnection technology (AIT). Figure 4 (top) shows the switching of a SiC MOSFET with a C_{GS} /C_{GD} ratio of 25 and a low $R_{G,int}$ of 2 Ω in a standard bond wire module. In this conventional module, self-excited oscillations are clearly visible in the gate-source voltage, drain-source voltage, and drain current. Any further increase in the DC-link voltage or switched current can lead to catastrophic failure, even though the SiC MOSFETs are still far below their nominal current and voltage handling capabilities. When switching to an advanced AIT module such as the Bosch Gen6 power module (figure 4 right), these oscillations can be completely mitigated. Switching is consequently possible at much higher currents and DC-link voltages without any self-excited oscillations (figure 4, bottom).

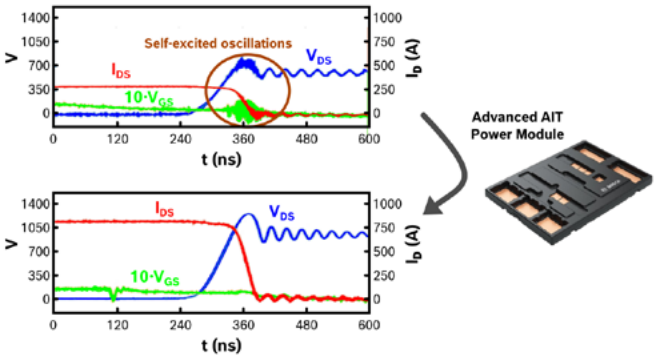

Figure 4: Turn-off switching characteristics for a standard bond-wire module and an advanced AIT power module. SiC power transistors with high CDS / CGD ratios were used to provoke self-excited oscillations in case of the standard bond-wire module.

Conclusion

SiC trench gate MOSFETs offer substantial benefits for both automotive and non-automotive applications, combining superior static and dynamic performance with high robustness unlike any other SiC power device technology. While today's trench architectures already present a benchmark in terms of achievable power density, advanced trench-gate-based SiC architectures will further enhance this figure of merit, making trench gate MOSFETs the best choice among SiC devices.

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PCB Embedding of Semiconductor Dies: Enabling Next-Generation Power Electronics

The embedding of semiconductor dies, particularly GaN and SiC MOSFETs, into PCB structures provides multiple system-level benefits. This advanced packaging technique significantly improves performance by optimizing circuit layouts, reducing parasitics, and enhancing thermal management.

By Sam Aldhaher, Power Electronics Lead, RAM Innovations & Simon Stringer, Power Electronics Consultant, Gipfel EDS

With reduced parasitics and improved thermal management, power converters can operate at higher efficiencies and power densities. The ability to push semiconductor devices closer to their absolute maximum ratings, as specified in their datasheets, allows for better utilization of their capabilities. These improvements lead to lower energy consumption, reduced heat generation, and more compact and cost-effective power electronic solutions.

Optimized Layouts for High-Speed Switching

Embedding semiconductor dies within a PCB enables a more compact and optimized circuit layout, drastically reducing power loop inductances and associated parasitic effects. This reduction is crucial for achieving faster switching speeds without the risk of excessive switch node ringing. In conventional PCB designs, external packaging and wire bonding introduce inductive parasitics that limit switching performance and can lead to voltage overshoot. By embedding the die directly into the PCB, designers can minimize these detrimental effects and unlock the full high-frequency potential of wide-bandgap semiconductors.

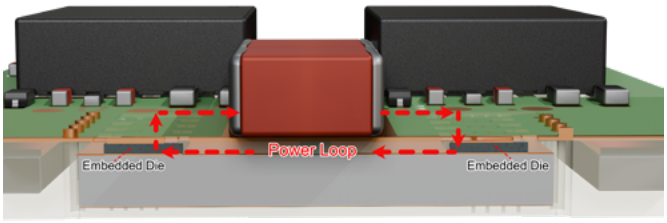


Figure 1: Embedding unlocks the "z-axis," allowing components to be placed vertically and reducing power loop parasitic inductances.

Thermal Management with Embedded Ceramic Tiles

One of the key advantages of die embedding is the ability to integrate a ceramic AlN (aluminium nitride) tile within the PCB, onto which the die is sintered. AlN provides excellent thermal conductivity while maintaining electrical isolation, ensuring efficient heat dissipation from the semiconductor device. This method effectively reduces thermal resistance, allowing the embedded MOSFETs to operate at higher power levels without excessive temperature rise, improving reliability and longevity.

Improved Clearance and Creepage for Higher Power Density

By embedding semiconductor dies, the pollution degree of the environment is effectively reduced, allowing for more relaxed clearance and creepage requirements. This means that dies can be placed closer together, increasing overall power density. The compact arrangement enables more efficient power conversion in applications requiring high power output within a small footprint, such as automotive and aerospace power electronics.

Unlocking 3D Circuit Design Capabilities

Traditional PCB layouts are constrained to a two-dimensional plane, limiting circuit optimization. With embedded dies, the design paradigm shifts to a three-dimensional approach where the z-axis becomes available for further enhancements. High-frequency ceramic decoupling capacitors can be placed directly on top of the embedded die, minimizing the power loop, and improving transient response. Similarly, shunt resistors for current sensing can be positioned directly atop the die, significantly reducing parasitic inductance, and enhancing signal integrity for precise current measurement.

Reliability and Mechanical Integrity

Embedding reduces mechanical stresses on semiconductor dies by eliminating traditional wire bonding, which can be a common point of failure due to vibration and thermal cycling. Enhanced mechanical robustness makes embedded power modules ideal for harsh environments such as automotive, aerospace, and industrial applications.

Integration of Current sensors, Gate Drive and Protection Circuitry

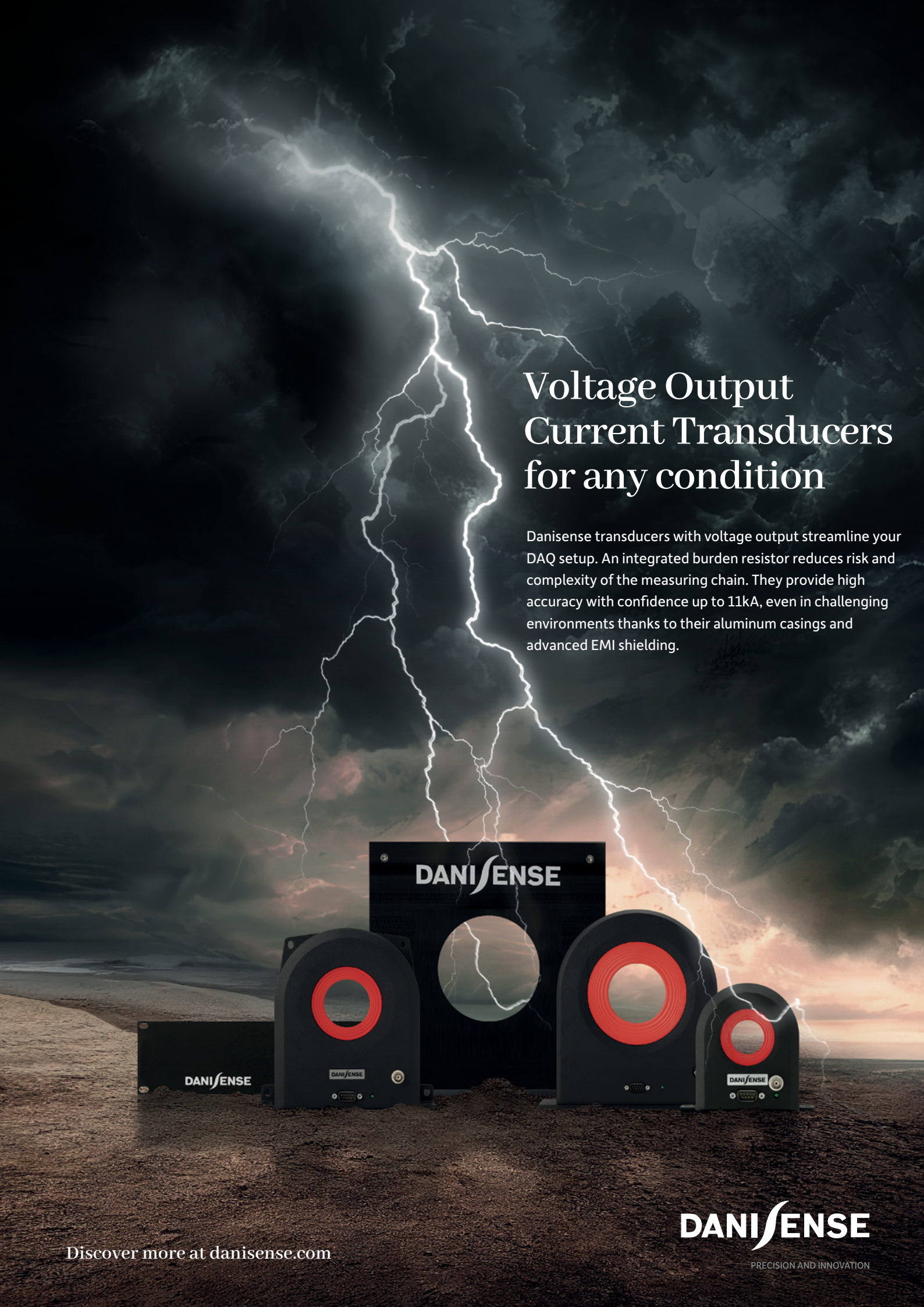
Embedding allows for the co-packaging of current sensors, gate drivers and protection circuits (such as overcurrent and overtemperature protection) close to the power switches, minimizing delays and improving switching performance. This tight integration enhances system reliability and further reduces parasitic effects.

Reduction of EMI and Noise

The shorter interconnects and reduced loop areas lead to significantly lower electromagnetic interference (EMI), improving compliance with EMC regulations. This allows for simpler filtering requirements, reducing the need for bulky and expensive external components.

Advanced Manufacturing Techniques and Challenges

Manufacturing methods such as laser drilling, sequential lamination, and sintering enable reliable embedding. However, challenges such as yield rates, thermal expansion mismatches, and inspection/testing difficulties compared to traditional PCB manufacturing must be addressed.



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Impact on System Cost and Manufacturing Scalability

While embedding increases initial manufacturing complexity, it can reduce overall system costs by eliminating bulky heat sinks, reducing PCB layers, and minimizing external packaging requirements. This technology's scalability for mass production is improving as advancements in PCB manufacturing make it more accessible.

RAM Innovations

With a focus on advanced solutions for wide band gap semiconductors in power applications, RAM Innovations concentrates on heterogeneous PCB embedded die packaging, which means that bare die WBG semiconductors are embedded directly within PCBs—rather than mounting them on the surface. This reduces power loop lengths, minimises parasitic inductance, enhances circuit efficiency, lowers energy consumption, and significantly reduces module size and weight—critical advantages across a wide range of high-performance applications.

While optimised for WBG semiconductors, the technology also supports embedded magnetics, RF, and optoelectronic dies. Applications span automotive, aerospace, space, defence, and medical sectors, where the inherent EMI shielding and reliability of embedded packaging are particularly advantageous.

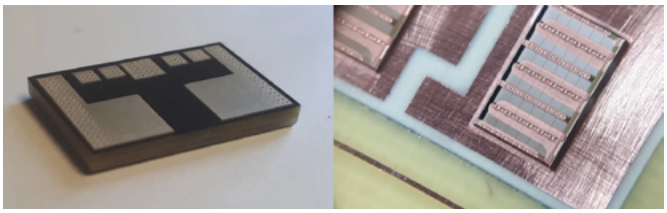

Figure 2: Example of RAM's embedded power modules.

The GT1 Power Module

A first demonstrator product is a 100 V/90 A half-bridge power module featuring an embedded GaN die (100 V, 7 mΩ). The module also includes an embedded AIN ceramic tile onto which the GaN dies are silver sintered. The AIN ceramic provides galvanic isolation and a low thermal resistance path to an external heat sink. Additionally, embedded copper terminals are also included for a low electrical resistance path from the DC bus and the switching phase to the GaN die.

The GT1 half-bridge module includes self-powered galvanically isolated gate drivers and DC link decoupling capacitors. The capacitors are directly placed above the GaN die in order to lower the impedance path to the GaN die. This can only be achieved with embedding as it unlocks the z-axis.

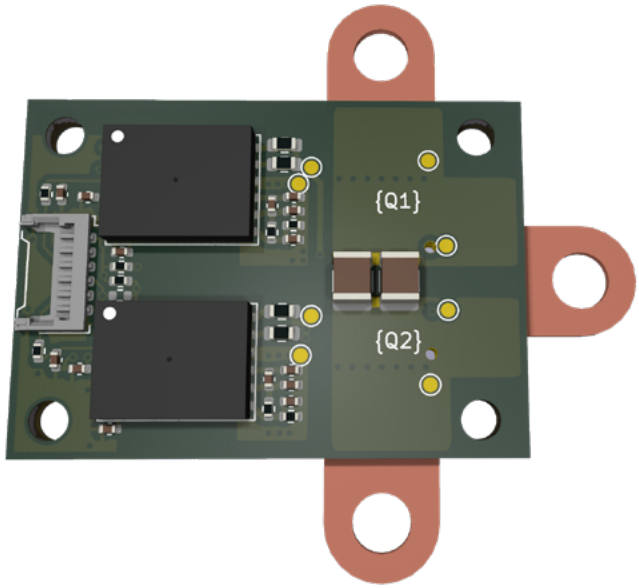

Figure 3: The GT1 Power module with embedded 100 V/7 mΩ GaN die.

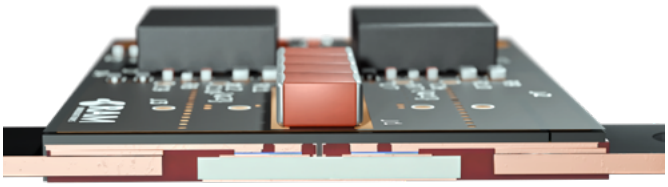

Figure 4: Cross section render of the GT1 Power Module.

Test Boards and Evaluation

Two 500 W buck 48 V-to-12 V DC/DC converters using 100 V/ 7 mΩ GaN devices demonstrate the effectiveness of PCB embedding of power semiconductors compared to traditional surface mount designs. One design utilizes the GT1 half-bridge power module and other uses discrete packages that are surface mounted.

This shows that more power can be obtained from a circuit with embedded components and an AIN ceramic tile, offering higher power densities in a given volume. This is because embedding results in lower thermal resistance from die to ambient, which means that the temperature can be closer to the heatsink temperature whilst also providing galvanic isolation. Additionally, embedding reduces parasitic inductance resulting in switching waveforms with sharper rise and fall times with less ringing. This lower switching loss and allows for reliable and efficient operation at higher switching frequencies.

To perform an "apples to apples" comparison, the DC/DC converters for both embedded and non-embedded design share the same input and output decoupling capacitors, power inductor and heatsink. Both are designed to convert 48 V to 12 V at up 20 A of load current at a switching frequency of 500 kHz. The discrete version is designed using best layout practices to minimise as much as possible the parasitic inductances of the power loops. Notice that for the design with discrete GaN, thick thermal pads are required to provide electrical isolation. This increases the thermal resistance and will consequently limit the amount of power that can be obtained, this is the main limitation of using discrete surface mount devices.

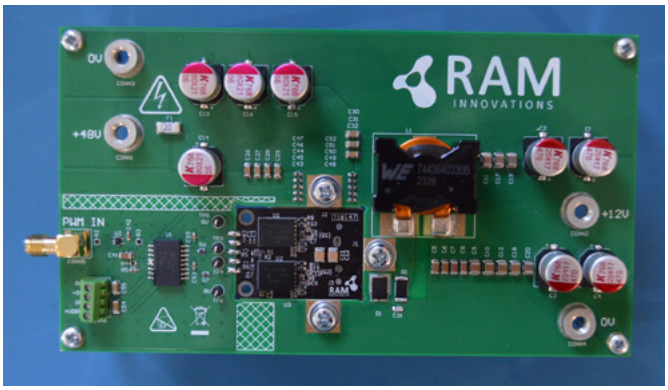

Figure 5: DC/DC Converter with RAM's GT1 Half-Bridge GaN module.

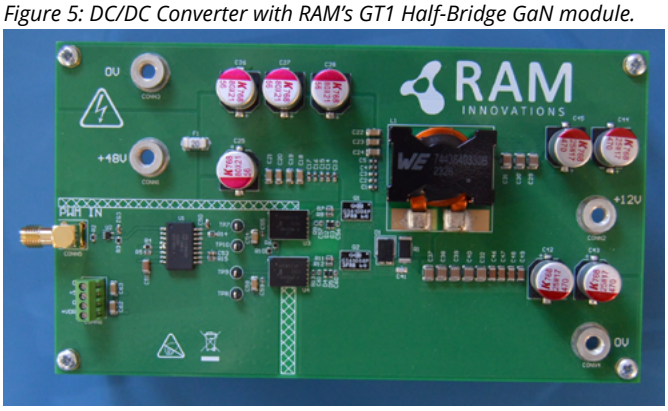

Figure 6: DC/DC Converter using traditional surface GaN components.

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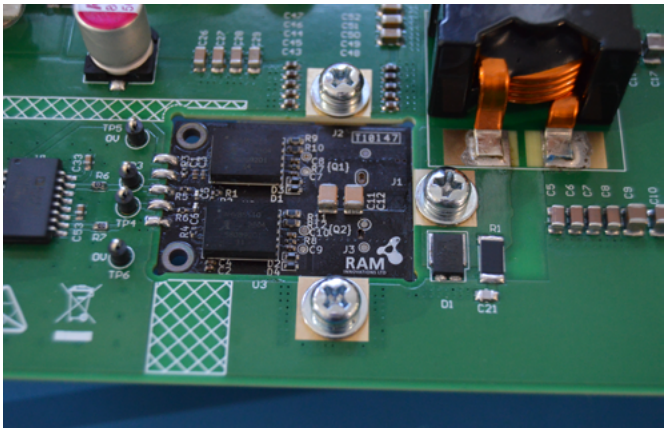

Figure 7: Close-up of the installed GT1 GaN Half-Bridge Module.

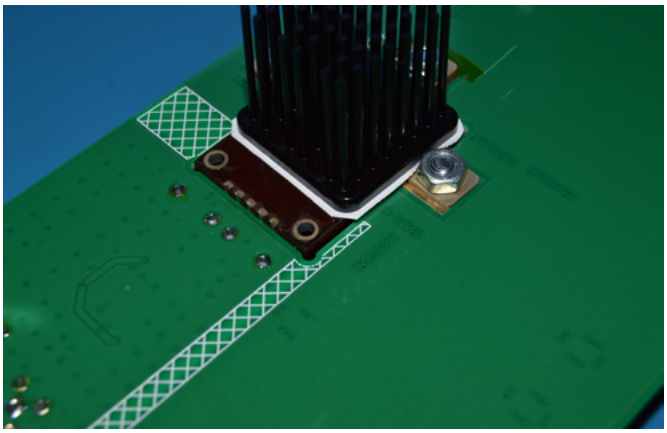

Figure 8: Heatsink attachment for both board designs.

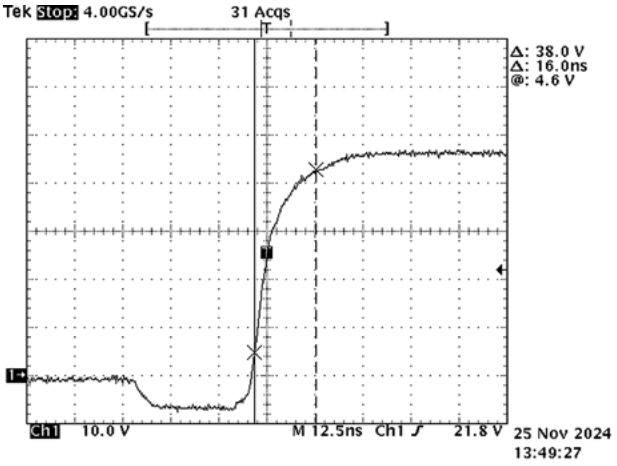

Figure 9: GT1 Module turn-off switching waveform.

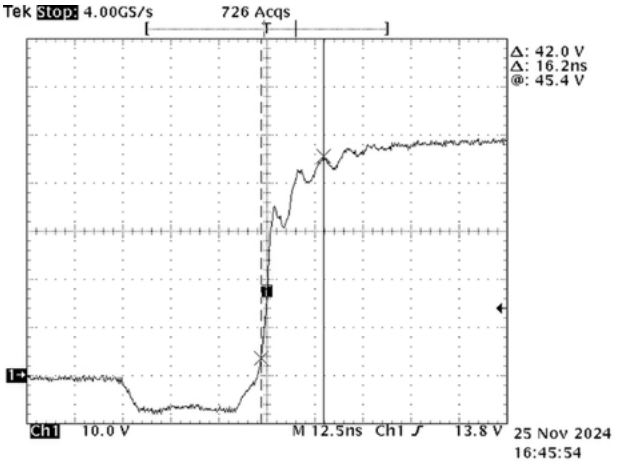

Figure 10: Discrete design turn-ff switching waveform.

Switching waveforms

The first result to compare is the switching node waveform at turn-on and turn-off. With embedding it is expected to have less parasitic inductance in the power loop so the switching waveform should have little to no ringing, overshoots and undershoots. For this comparison both designs are operating at approximately 17 A of load current at 500 kHz switching frequency.

The images 9 and 10 show how the turn-off switching waveform of the GT1 half-bridge module provides a clean and smooth rise of the voltage and turn-off. Whereas the turn-off switching waveform of the design with the discrete design shows higher frequency ringing and oscillation riding along the waveform. The consequence of better switching waveforms is that better EMC performance and less noise can be expected. This, in turn will impact the entire system as less filtering components are needed.

Maximum Load Current & Efficiency

Next comparison is the efficiency versus load current, here we would expect the efficiency to be almost identical between the two designs. The curves below show how the efficiency varies with load current for the two designs, the difference between both curves is negligible or within margin of error of the measurement equipment and operating parameters. For the discrete solution, the maximum achievable load current was approximately 15 A at 12 V before reaching the thermal limit of the discrete GaN devices. There was a temperature of approximately 131 °C on the low side GaN device, and the heatsink reached a temperature of 84 °C. This means there is a temperature difference of approximately 47 °C between the GaN device and the heatsink indicating a large thermal resistance.

Whereas for the GT1 Module the maximum load current that was achieved was approximately 17 A at 12 V – with a surface temperature of 134 °C and the heatsink reached a temperature of 120 °C. It was expected that the actual temperature of the embedded die would be slightly higher than 134 °C, however, the heatsink temperature was just 120 °C which is only 14 °C lower than the topside of the module.

This result confirms that the low thermal resistance achievable with embedding along with RAM's patented LAC technology, the die temperature can be closer to the heatsink temperature which therefore allows the system to deliver more power compared to discrete GaN solution with the same thermal and heatsinks. Since the volumes of the two solutions are the same and power is proportional to current squared this already represents a 27 % improvement in power density.

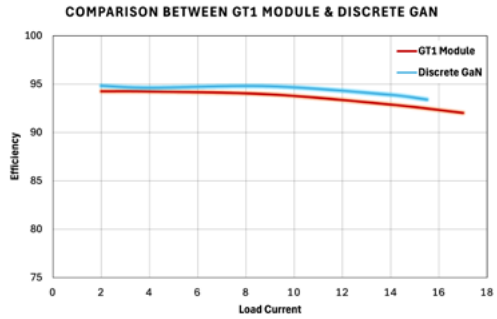

Figure 11: Efficiency comparison between GT1 module and discrete GaN at 12 V output.

The result above shows that the embedded design still has the capability to deliver more output power if the thermal design is changed and optimised. As mentioned previously, since the embedded GaN dies are galvanically isolated due to the internal AIN tile, there is no need for a thermal interface or pad from the surface of the power module to the heatsink, and so a large copper standoff can be used to interface the module to the heatsink and

therefore the total thermal resistance can be reduced significantly. Additionally, since the heatsink that was used did have a temperature of 120 °C which was close to the surface temperature of the module, this means a larger heatsink can be used to allow for more power dissipation

Figure 12 shows that the GT module is now able to deliver up 36 A of output current with the optimised thermal design using die embedding and the internal galvanic isolation.

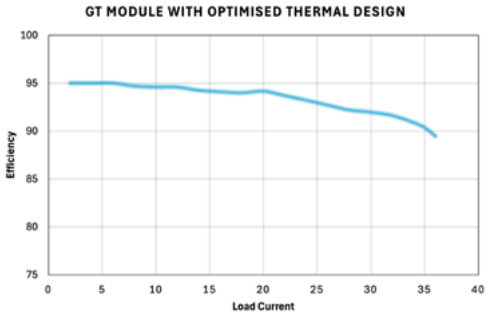

Figure 12: Efficiency measurement of the GT1 module at higher loads.

Maximum Power Dissipation and Current Evaluation

Embedding and the LAC technology allow for lower electric impedance and thermal resistances to be achieved, thus allow power semiconductors to operate closer to their absolute maximum ratings as specified in their datasheets. To test the absolute maximum current and power ratings of the GT1 Module, a water-cooling set-up with a heat exchanger mounted to the bottom side of the GT1 Module was attached for heat extraction, and both, the top and the bottom embedded die, were turned on at gate voltage of 5 V. A current limited power supply was used to conduct current through both dies and the surface temperature was monitored continuously. Image 13 shows the cooling setup for this single test, figure 14 shows the absolute surface temperature rise of the GT1 module whilst conducting a constant current of 55 A. The voltage drop measured directly across the positive and negative terminals was 1.992 V indicating a power dissipation of approximately 110 W. It is expected that both dies will have equal power dissipation of 55 W.

Since the GaN dies are embedded inside the PCB structure, it might not be feasible to measure their temperature directly. By referring to the manufacturer's datasheet it is estimated that under the operation conditions of this specific test and the cooling setup the junction temperature of the dies has reached approximately 150 °C.

The initial estimates, based on these preliminary tests and FEM simulation, were that the thermal resistance from the embedded die to the bottom surface of the GT1 Module is 0.2-0.4 °C/W. The next product generation of the GT1 Module will include an embedded thermistor which will provide a temperature reading that is close to the body temperature of the die, which will therefore allow providing an accurate calculation of the thermal resistance.

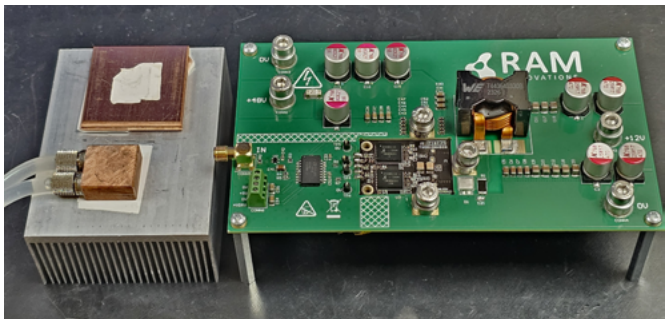

Figure 13: Heatsink for extended power and thermal testing of the GT1 module.

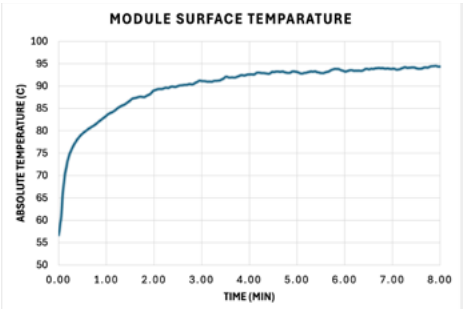

Figure 14: GT1 module temperature measurement.

Conclusions and Next Steps

Preliminary results have proved that embedding reduces the power loop parasitics resulting in "cleaner" switching waveforms and increased power density compared to a traditional "2D" design with surface discrete components. A next step will be building a new design iteration of the GT1 module which will include an embedded thermistor and current sensor. RAM has also designed and built a 650 V 60 A GaN module and plans to build 900 V GaN and 1200 V SiC versions.

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Three-Phase Systems in LLC and CLLC Switching Power Supply Technology

In LLC and CLLC converters the output capacitor (or battery) is charged in a pulsating manner, placing a high load, while the input is subjected to a pulsating current. However, a three-phase circuit in LLC and CLLC technology ensures a nearly continuous energy flow.

By Heinz Schmidt-Walter, Professor Emeritus at Darmstadt University of Applied Sciences, Germany

The three-phase electrical system is one of the greatest inventions in electrical engineering. Although the three phases carry alternating current, meaning each phase has a power output pulsating at twice the grid frequency, the power input or output of a three-phase system with a symmetrical load is without power pulsation. As a result, for example, the turbines in a power plant are loaded with constant torque, and three-phase motors deliver a torque that is constant over time.

Switched-mode power supply technology has not yet taken advantage of this behavior of a three-phase system. Instead, switched-mode power supplies operate with high-frequency controlled switches that deliver power in pulsating fashion at the output or absorb it at the input. The resulting pulsation is buffered by capacitors, ensuring a sufficiently continuous power output.

LLC and CLLC Converters (state of the art)

LLC and CLLC converters are resonant converters, with the switching transistors turning on at zero voltage (zero voltage switching, ZVS). This results in minimal losses in the transistors and consequently in minimal heating during operation. Efficiencies of >98% could be realized. Modern GaN transistors achieve switching frequencies of >500 kHz to 1 MHz at power levels of several kW and voltages in the 500 V range. The transformers are often designed as so-called matrix transformers, in which windings are distributed across multiple legs to minimize their size. In this technology, converters with a power output of several kW are reduced to the size of a cigarette pack.

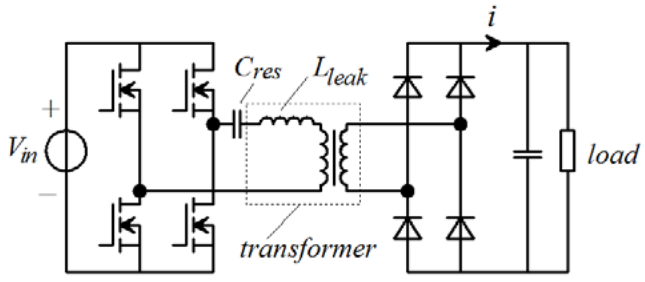

Figure 1: LLC converter with pulsating power transmission.

The LLC converter conducts energy in only one direction. The CLLC converter can conduct energy in both directions, thus being capable of regenerating energy. Figure 1 shows an example of the LLC converter.

Both converters have the problem that the output capacitor is charged in a pulsating manner, thus subjecting it to high loads. Likewise, the input is loaded with a pulsating current (see figure 2). LLC and CLLC converters are state-of-the-art when it comes to high efficiency and compact size.

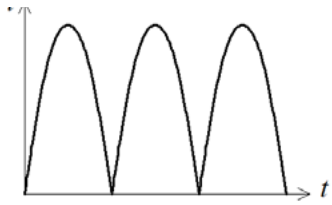

Figure2: Example of the pulsating current i from Figure 1.

The resonance capacitor C_{res} and the leakage inductance of the transformer L_{leak} form a series resonance with the resonance frequency f_{res} equal to the switching frequency f_{sw}.

(Formula 1): $$f_{res} = \frac{1}{2\pi\sqrt{L_{leak} \cdot C_{res}}} = f_{sw}$$

The transistors are switched with a duty cycle of 50%. At resonance, the current in the transformer is sinusoidal. The output capacitor is charged with pulsed half-sine waves. The output voltage is controlled by frequency variation. At switching frequencies f_{sw} lower than f_{res}, the output voltage increases; at frequencies higher than f_{res}, the output voltage decreases. The control range of LLC and CLLC converters is quite narrow. Typically, the transformer has an air gap. This is dimensioned so that L_p / L_{leak} = 3...5 (see relevant literature).

The LLC converter in three-phase design

The converter described below (Figure 3) distributes the transmitted power using a three-phase transformer in such a way that the power flow is largely continuous, allowing the output capacitor to be reduced to a very small value (see figure 4). The supply source is also loaded with approximately a direct current. This is especially important when both the source and load are batteries.

The bridge outputs are controlled with a 120° phase shift. This creates a three-phase voltage system that generates approximately sinusoidal currents in the three-phase transformer, offset by 120°, see figure 5. A three-phase rectifier is located on the output side. It does not have to consist of diodes; instead, active rectifiers using

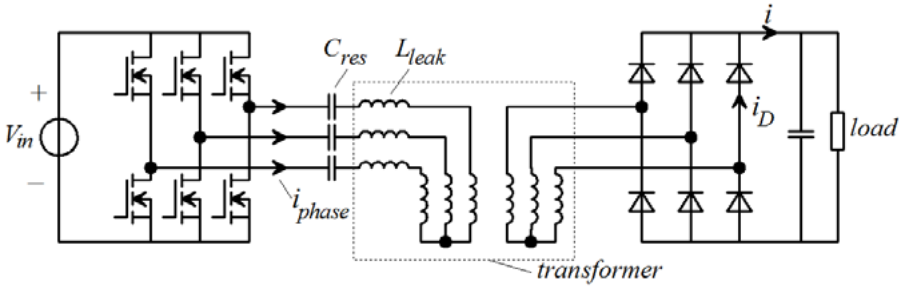

Figure3: Basic circuit of the LLC three-phase converter.

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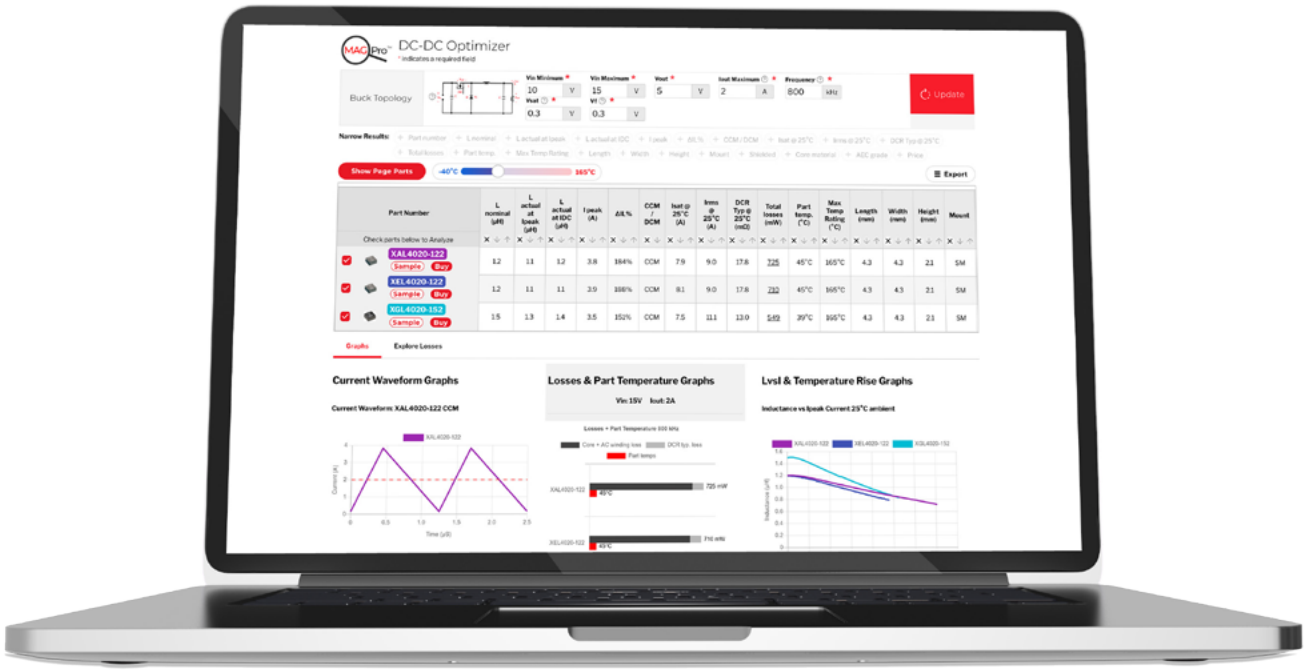

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transistors are used today. In the CLLC converter, the primary and secondary active transistor bridges must be used due to the symmetrical power transmission. The star point of both the primary and secondary sides must remain free.

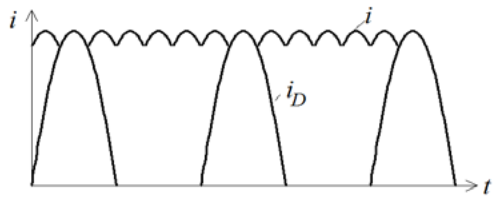


Figure 4: Current i and current i_D in a rectifier diode.

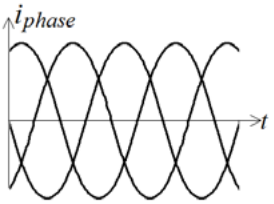


Figure 5: Primary currents in the transformer.

The magnetic volume of the three-phase transformer is slightly smaller than that of an LLC converter of the same power. The total switching capacity of the transistors remains the same.

Three-phase transformer

The three-phase transformer has three legs, which, thanks to the ferrite core design, can be arranged symmetrically. This results in identical magnetic conditions for all three legs (figure 6).

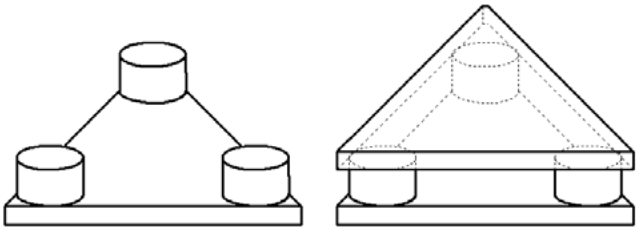


Figure 6: Ferrite core with base and legs (left side) and core with cover plate (right side).

However, the traditional geometry of a three-phase transformer is also possible (figure 7). In this case, however, the magnetic ratios of the three legs are not entirely identical, which can affect the leakage as well as the resonance capacitor.

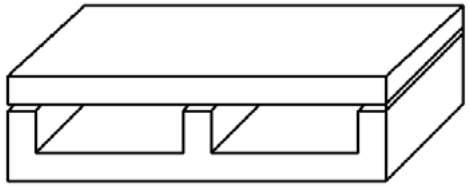


Figure 7: Three-leg planar core.

The respective primary and secondary windings are applied in the same way to the three legs with the same winding direction, see figure 7a.

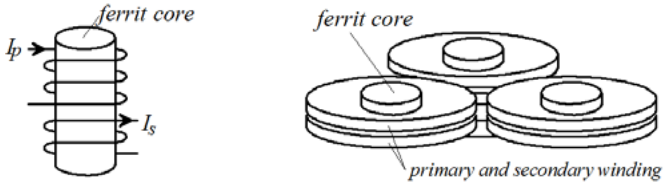


Figure 7a: Winding direction (left side) and physical view of the windings (right side).

Calculation example for the transformer

Several parameters are taken into account when calculating the transformer. Therefore, we speak of a transformer "design", which includes core parameters, winding parameters, switching frequency, and insulation distances. The designer has many options, but of course, physical laws must also be taken into account.

The following LLC three-phase converter serves as an example for calculating the transformer:

Input voltage V_{in}=400 V,
Output voltage V_{out}=24 V,
Power P=1.5 kW,
Switching frequency f_{sw}=500 kHz.
Further definitions:
B_{max}: Maximum magnetic flux density in the ferrite within the winding
A_{fe}: Cross-sectional area of the ferrite
A_N: Cross-sectional area of the winding
Φ: Magnetic flux
S: Current density in the winding
N: Number of turns
T: Period of the switching frequency f_{sw}
Subscripts *1* and *2* stand for primary and secondary

For the calculation, we assume a current density S=5 A/mm² in the copper and a B_{max}=100 mT in the ferrite. B_{max}=100 mT results in approximately 1 mW/mm³ in the aforementioned ferrite (1 kW/m³=1 mW/mm³). We consider this acceptable with respect to transformer heating with slightly forced ventilation.

Figure 8: Primary phase-element voltage – the voltage between the output of the transistor bridge and the primary star point.

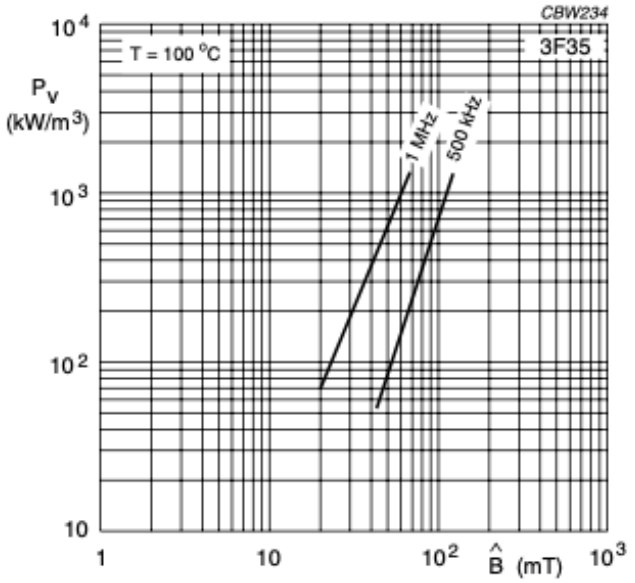
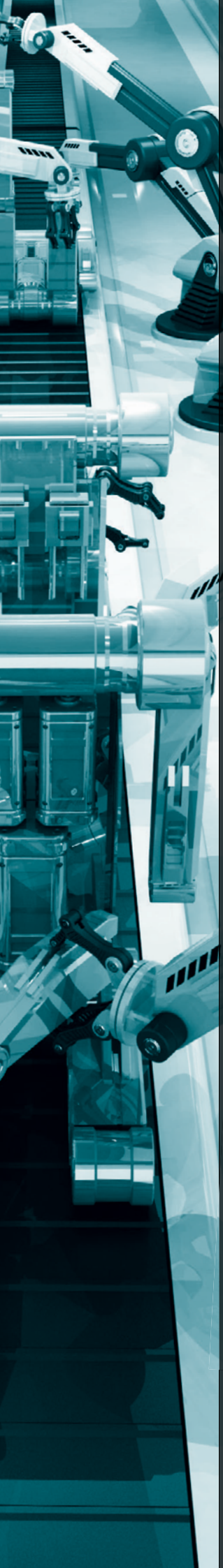


Figure 9: Power losses within the ferrit 3F35 (Ferroxcube) at 500 kHz, $\hat{B}$ corresponds to B_{max}.



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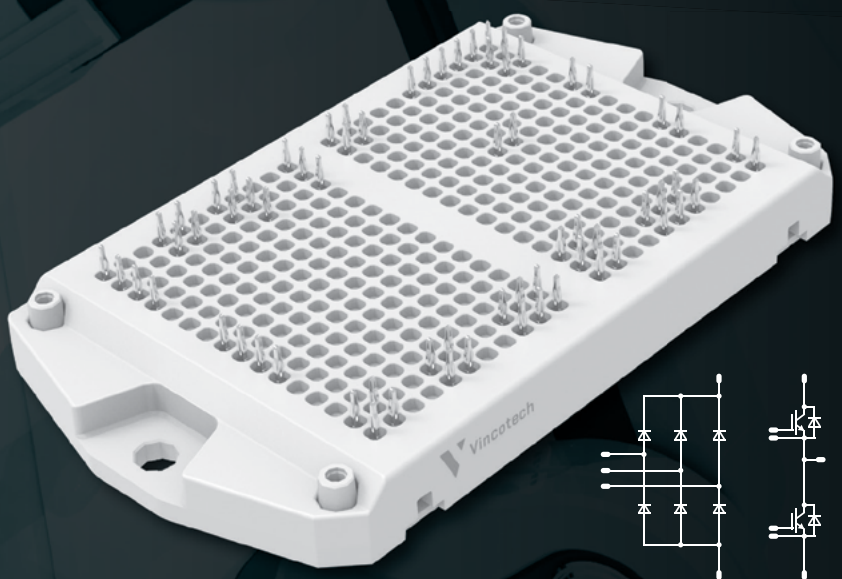

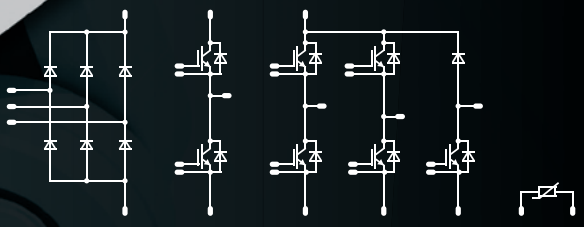

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The basis for further calculation is Faraday's Law of Induction:

(Formula 2): $V = N \cdot \mathrm{d}\Phi/\mathrm{d}t$.

From this it can be seen that the voltage and the number of turns determine the suitable cross-section of the ferrite core.

It follows:

(Formula 3): $\frac{1}{N}\int V \cdot \mathrm{d}t = B \cdot A_{fe}$

The integral (Formula 3a) $\int V\,dt$ describes the voltage-time area, which determines the magnetic flux or magnetic flux density (see figure 9). For positive voltage, the flux increases; for negative voltage, it decreases.

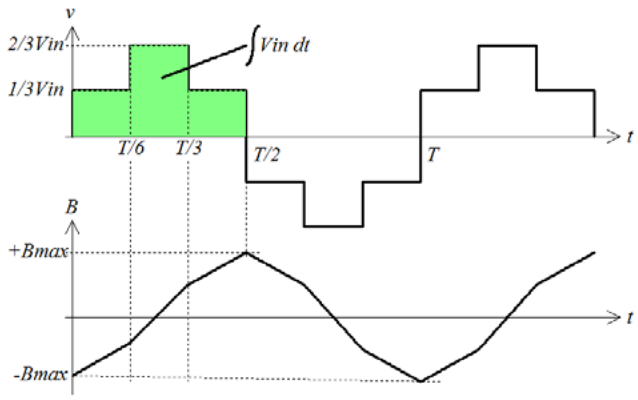

Figure 10: Phase-element voltage and corresponding magnetic flux density B.

With a free star point, the phase-element voltages describe a step function, each step of which is $V_{in}/3$ for each $T/6$. The voltage-time area per half-cycle is $4 \cdot V_{in}/3 \cdot T/6$, see figures. 9 and 10. This causes the magnetic flux density to run from $-B_{max}$ to $+B_{max}$ and vs. in the steady state.

Applying Faraday's Law of Induction now leads to:

(Formula 5) $\frac{1}{N} \cdot 4 \cdot \frac{V_{in}}{3} \cdot \frac{T}{6} = \frac{1}{N} \cdot \frac{2}{9} \cdot \frac{V_{in}}{f} = 2B_{\max} \cdot A_{fe}$

Since the voltages in the transformer are proportional to the number of turns, this calculation applies equally to the input voltage V_{in} and the output voltage V_{out}:

(Formula 6) $\frac{1}{N_1} \cdot \frac{2}{9} \cdot \frac{V_{in}}{f} = 2B_{\max} \cdot A_{fe} = \frac{1}{N_2} \cdot \frac{2}{9} \cdot \frac{V_{out}}{f}$

Due to the high frequency, the secondary number of turns in our example can be very small. The number of turns must also be an integer. Therefore, we first choose N_2 to calculate the required cross-sectional area of the core.

(Formula 7) $A_{fe} = \frac{1}{N_2} \cdot \frac{2}{9} \cdot \frac{V_{out}}{f} \cdot \frac{1}{2B_{\max}}$

Now you can iteratively determine which number of turns seems suitable:

a) N_2=1 leads to (Formula 8) $A_{fe} = \frac{1}{N_2} \cdot \frac{2}{9} \cdot \frac{V_{out}}{f_{sw}} \cdot \frac{1}{2B_{\max}} = 53.3\mathrm{mm}^2$
b) N_2=2 leads to 27 mm² or
c) N_2=3 leads to 18 mm²

The primary number of turns is then $N_1/N_2 = V_{in}/V_{out}$ for:

a) N_2=1 → N_1=16
b) N_2=2 → N_1=32
c) N_2=3 → N_1=48

Next, the required winding space can be determined. The current determines the wire cross-section; the more turns, the larger the winding cross-section. The number of turns should be as small as possible to minimize copper losses. On the other hand, the winding space should be proportionate to the core volume. In the example, N_2=1 and N_1=16 are selected. A secondary number of 1 turn is particularly favorable for the layout of the subsequent rectifier stage.

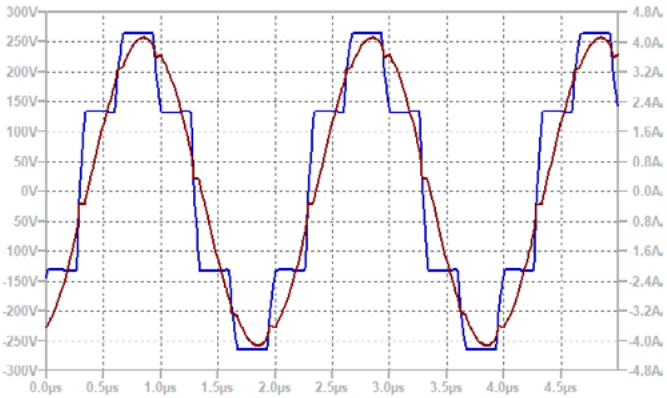

Figure 11: Primary phase-element voltage (blue) and phase current (red.)

The phase-element voltages on the primary side are approximately V_{1peak} =270 V and V_{1RMS} = 190 V.

Each phase delivers P_{phase} = 500 W. This results in a primary phase current of I_1= 500 W/190 V = 2.65 A (slightly higher in the simulation because the voltage drop in the inverter stage and the power loss of the secondary rectifier are taken into account).

The phase currents on the secondary side are therefore $I_2 = N_1/N_2 \times I_1$ = 42.5 A.

The current density S = 5 A/mm² should not be exceeded. A fill factor of 0.7 is assumed for the windings. The primary and secondary windings require the same winding cross-section. This results in the following for the primary and secondary windings:

a) N_1=16, N_2=1:

(Formula 9)

$$A_N = 2 \cdot \frac{N_2 \cdot I_S}{S} \cdot \frac{1}{0.7} = 2 \cdot \frac{42.5\mathrm{A}}{5\mathrm{A/mm}^2} \cdot \frac{1}{0.7} = 25\mathrm{mm}^2$$

b) N_1=32, N_2=2: A_N=50 mm²

c) N_1=48, N_2=3: A_N=75 mm²

Note: The winding windows in the core must accommodate the primary and secondary windings twice.

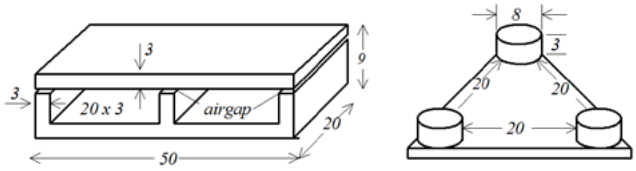

Figure 12: Two possible core-designs for N_1=16 und N_2=1.

Figure 12 shows two core designs. Figure 12 left shows the traditional three-phase transformer design, right a symmetrical triangular core design (cover plate not shown). The windings count 16 and 1. The windings would protrude at the sides, creating an entire transformer area of 70 x 40 mm² on the left design and a triangular area with 56 mm edges on the right one. With the triangular solution, the base and cover plates could be reduced to 1.5 mm thickness because the magnetic fluxes would partially cancel each other out due to their phase shift. An air gap can be inserted between the cover plate and the lower core.

Summary

LLC and CLLC converters are currently state-of-the-art when it comes to high efficiency and compact size. However, both converters have the problem that the output capacitor (or battery) is charged in a pulsating manner, placing a high load. Likewise, the input is subjected to a pulsating current.

The three-phase circuit in LLC and CLLC technology ensures a nearly continuous energy flow. This is particularly advantageous when the converters are powered by DC sources, such as batteries or solar cells, and/or have batteries as a load.

At the same time, the three-phase transformer is a particularly advantageous design because the three magnetic fluxes in the legs cancel each other out, so that the flux from one leg is absorbed by the other two. The transformer therefore has a smaller footprint than a single-phase converter of the same power and frequency.

The transformer must be connected in a star configuration with a free star point. The stepped voltage curve supports the sinusoidal current.

In case the load is resistive, the output capacitor can be selected to be approximately 40 times smaller than with the single-phase LLC and CLLC converter, with the same voltage ripple.

The author has filed a patent for the LLC and the CLLC three-phase solution, and he can also provide the simulation file for LTSpice upon request. The ferrite transformer can be ordered from Blinzinger Elektronik, Forchtenberg/Germany.

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How to accurately estimate IC Junction Temperature

This article serves as a comprehensive guide to accurately estimate the junction temperature of semiconductor devices. It explains the significance of thermal parameters, such as thermal resistance (θ) and thermal characterization parameters (ψ), and their roles in effective thermal management. The article highlights the differences between these parameters and provides guidance on their correct application in IC junction temperature estimation. Additionally, it discusses common mistakes in junction temperature estimation and offers insights to improve the accuracy of thermal measurements.

By Ankul Gupta, Senior Engineer Automotive Power, Analog Devices

Accurately estimating the junction temperature is essential for ensuring the reliability, performance, and longevity of semiconductor devices. Junction temperature has a direct influence on the efficiency, stability, and safety of electronic components. This article serves as a comprehensive guide to techniques for estimating junction temperature, with a focus on utilizing thermal resistance and thermal characterization parameters. By following these techniques, engineers can implement effective thermal management strategies, enhance device performance, and mitigate the risk of overheating-related failures. The document provides a thorough explanation of fundamental thermal parameters, highlights the key differences between thermal resistance and thermal characterization parameters, and introduces practical methods for estimating junction temperature. It also includes case studies to validate the accuracy of these approaches. Whether you are developing new electronic systems or optimizing existing designs, this article equips you with the essential knowledge and tools to achieve precise thermal measurements and maintain device reliability.

Thermal Parameters Overview

Understanding thermal resistance and characterization parameters is crucial for evaluating and comparing the thermal performance of electronic packages. These parameters play a key role in effective thermal management and accurate junction temperature estimation. Table 1 shows an overview of the five primary thermal parameters.

Thermal Resistance vs. Thermal Characterization Parameters

Thermal resistance (θ) and thermal characterization parameters (ψ) are often confused because they both relate to the thermal performance of electronic packages and involve similar concepts of heat dissipation and temperature differences. However, they serve different purposes and are derived under different conditions. Thermal resistance measures the temperature difference between two points (for example, junction to ambient, junction to case) divided by the power dissipation, and is highly dependent on specific conditions like PCB design and airflow. It typically considers a single dominant path of heat flow, making it useful for comparing the thermal performance of different packages and designing cooling solutions. On the other hand, thermal characterization parameters measure the temperature difference between the junction and a specific point (for example, top of the package, board) divided by the power dissipation, considering the combined effect of various heat conduction paths. These parameters are less dependent on

Thermal Parameter	Description	Influenced By	Primary Use
θ_{JA} (Junction-to-Ambient Thermal Resistance)	Thermal resistance from the device junction to the ambient air.	Factors such as PCB design, airflow, and package type.	Comparing the thermal performance of different packages in a standardized environment and junction temperature estimation.
θ_{JC} (Junction-to-Case Thermal Resistance)	Thermal resistance from the device junction to a specific point on the package case. Indicates the efficiency of heat transfer from the die to the case considering heat flow in a single direction.	Package materials (for example, lead frame, mold compound, die attach adhesive) and design features (for example, die thickness, exposed pad, internal thermal vias).	Comparing the thermal performance of different packages in a standardized environment. Estimating junction temperature where heat sink is used.
θ_{JB} (Junction-to-Board Thermal Resistance)	Thermal resistance from the IC junction to a specified point on the PCB.	Factors such as PCB design, including copper area, thermal vias, and board stack-up.	System-level thermal modeling, as it quantifies the heat flow path from the junction to the board.
ψ_{JT} (Junction-to-Top Thermal Characterization Parameter)	Temperature difference between the IC junction and the top surface of the package. Accounts for heat conduction through multiple paths.	Factors such as package design and the effectiveness of the heat conduction paths.	Estimating junction temperature in real-world applications when the top surface temperature and power dissipation are known. Only used for cases where heat sink is not used.
ψ_{JB} (Junction-to-Board Thermal Characterization Parameter)	Temperature difference between the IC junction and the board. Includes the combined effects of heat conduction through multiple paths.	Factors such as PCB design and the effectiveness of heat conduction paths within the system.	Accurate estimation of junction temperature in real-world applications.

Table 1: Thermal Parameters

specific conditions, providing more accurate junction temperature estimations in real-world applications.

As an example, the junction-to-case (top) thermal resistance parameter extraction considers all the package losses to be dissipated through the top side of the package with heat flowing through a single dominant path. The parameters are extracted through simulation and, hence, a condition is created in simulation where they force all the heat to be dissipated from the top side. This would not occur in a real-world application as heat would be dissipated through different paths in the IC. On the other hand, the junction-to-case (top) thermal characterization parameter is derived by considering that, for losses occurring in the IC, only a portion of the heat flows through the top of the package. It accounts for all possible heat flow paths as they occur in real-world conditions, making it more suitable for estimating junction temperature in practical applications. Figure 1 provides a simplified visual representation to illustrate the difference in the heat flow path for the extraction of these two parameters. Note that this diagram is intended for ease of understanding and does not accurately depict the actual parameter extraction process nor the precise heat flow path inside the package.

The confusion between these two metrics arises because both involve temperature differences and power dissipation, but they are applied in different contexts and have distinct dependencies. Understanding these differences is critical for accurate thermal estimation and management.

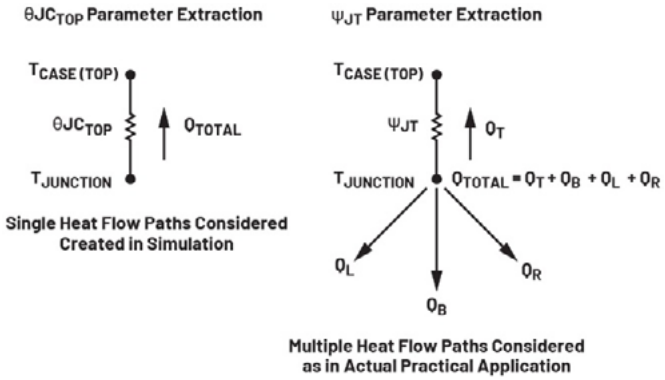


Figure 1: Representation of a heat flow path in θ_{JC} and ψ_{JT} parameter extraction.

Techniques for Junction Temperature Estimation

There are multiple techniques available that can be used to estimate the package junction temperature. It is critical to use the right thermal parameter to ensure accurate temperature estimation. The two dominant methodologies that can be easily applied on the experimental setup for junction temperature estimation are discussed.

Method 1: Using Junction-to-Ambient Thermal Resistance (θ_{JA})

This is a good method for getting a ballpark figure of junction temperature without the need of any specialized equipment by just having an idea of the losses in the package. As a Requirement the value of the package for the specific PCB under test as well as the ambient temperature of operation and accurate losses in the package need to be known.

$$T_{JUNCTION} = T_{AMBIENT} + \theta_{JA} \times Losses \quad (1)$$

It is a challenge that the θ_{JA} value is highly dependent on PCB design and airflow, which can lead to inaccuracies if not properly accounted for. Another challenge is the accurate measurement of ambient temperature and IC losses is another critical aspect.

Method 2: Using Junction-to-Case (Top) Thermal Characterization (ψ_{JT})

This method is accurate in estimating junction temperature but needs additional equipment to measure the package case temperature. It cannot be used to estimate junction temperature when a heat sink is used on the package. In terms of requirements the ψ_{JT} value of the package for the PCB under test is needed together with an accurate measurement of the case top temperature and power dissipation of the package.

Two of the commonly used methods for package case temperature measurement are described here – using a thermal camera and using a thermocouple. A thermal camera can be employed to observe the case temperature. This method is suitable for room temperature measurements. Accurate measurement depends on thermal camera accuracy as well as package losses.

A thermocouple can be attached to the package case top to measure the case temperature. This method is suitable for measurement at all temperatures especially when the package needs to be placed in a thermal chamber. Accurate measurement primarily depends on the thermocouple and multimeter used.

$$T_{JUNCTION} = T_{CASE} + \psi_{JT} \times Losses \quad (2)$$

The accurate measurement of the package case temperature is critical for precise junction temperature estimation, and attaching a thermocouple to the package case top for temperature measurement can be challenging.

The two methods discussed in this article are verified through bench validation. To test the accuracy of the measurement, the MAX25255 is employed, which features a temperature sensor pin to monitor the IC die junction temperature. This provides a reference point for the actual junction temperature of the IC and how accurately each method estimates the junction temperature.

Thermal Parameters	4-Layer JEDEC Board	4-Layer EV Kit
Junction-to-Ambient Thermal Resistance (θ_{JA})	27.2 K/W	18.5 K/W
Junction-to-Case (Bottom) Thermal Resistance (θ_{JCb})	4.8 K/W	5.5 K /W
Junction-to-Board Thermal Resistance (θ_{JB})	6.9 K/W	7.9 K/W
Junction-to-Case Thermal Characterization (ψ_{JT})	0.56 K/W	0.58 K/W
Junction-to-Board Thermal Characterization (ψ_{JB})	7 K/W	7.9 K/W

Table 2. MAX25255 Package Information

The different thermal parameters for the IC package for both the JEDEC board and EV kit are specified here. In internal tests the 4-layer MAX25255 EV kit was used for bench validation.

The operating condition for the test case is as follows:

- V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 8 A, f_{sw} = 2100 kHz, T_{amb} = 25 °C
- Efficiency = 92.3 %, IC losses = 1.7 W
- Die junction temperature (as measured by the TEMP pin) = 57.3 °C

The different techniques are used to estimate the junction temperature to see how well they match to the actual die temperature.

Case 1: Using θ_{JA}

No specialized equipment is needed to calculate the package junction temperature for this method, which reduces the chances of measurement error due to wrong equipment calibration. Simply equate the different parameters in the equation to calculate the junction temperature. For the IC under test, the estimated junction temperature with this method is as shown in Equation 3.

$$T_{JUNCTION} = 25°C + 18.5°C/W \times 1.7\ W = 56.45°C \quad (3)$$

The junction temperature estimated here is 56.45 °C, which is close to the actual junction temperature measured by the TEMP pin. The error in measurement is about 0.85 °C (1.5 %). The accurate measurement of ambient temperature and IC losses is critical here to minimize the error in junction temperature estimation. For example, even miscalculating the IC losses by 0.1 W would result in the junction temperature to vary by 1.85 °C (3.3 %).

Case 2: Using ψ_{JT} Along with a Thermal Camera for Case Measurement

For this method, a thermal camera is used to measure the IC case top temperature. The thermal camera used here is E60BX, which has an accuracy of ±2 °C or ±2 % (whichever is greater). Allow the converter to operate for 15 to 20 minutes to ensure the IC junction temperature is stable. The maximum case temperature captured for the IC is shown in Figure 2.

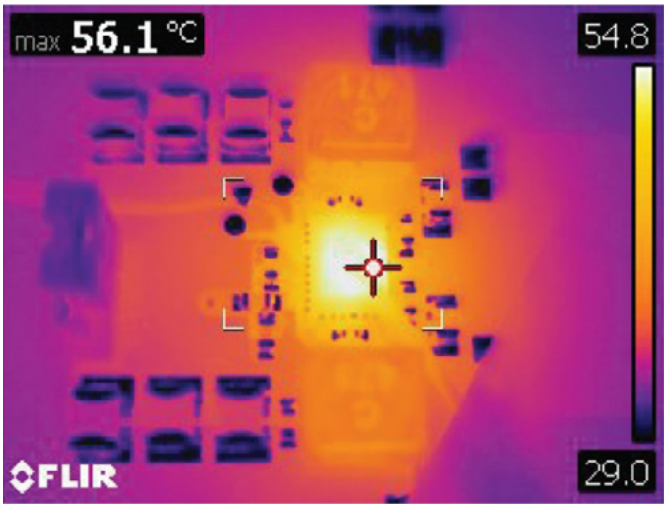


Figure 2: Thermal image captured for the MAX25255 IC case top temperature measurement.

The case temperature measured by the thermal camera is 56.1 °C. Equation 4 is used to calculate the junction temperature.

$$T_{JUNCTION} = 56.1°C + 0.58°C/W \times 1.7\ W = 57.09°C \quad (4)$$

The junction temperature estimated here is 57.09 °C, which is very close to the actual junction temperature measured by the TEMP pin. The error in measurement is about 0.21 °C, which is around 0.37 %. The error within the accuracy of the thermal camera used for measurement. Estimating the case temperature accurately is more critical than IC loss calculation here. For example, even if the IC loss calculation is off by 0.5 W, the junction temperature measurement would be off by 0.29 K/W (0.5 %). This is a big advantage of using ψ_{JT} over θ_{JA}.

Case 3: Using ψ_{JT} Along with a Thermocouple

Compared to case 2, this method uses a thermocouple to measure the package case temperature. A suitable thermocouple needs to be selected based on application specifications. In this case, a Type K thermocouple is selected, which has an accuracy of 2.2 °C or 0.75 % (whichever is greater). Attaching the thermocouple to the package case is critical to ensure proper measurement—either a thermal paste or thermal glue can be used. Ensure the thermal paste or glue is rated for a temperature higher than what the package needs to be tested for. In this case, thermal compound TC3-1G is used. Attach the thermocouple to the top of the IC using thermal paste to ensure good thermal contact (Figure 3).

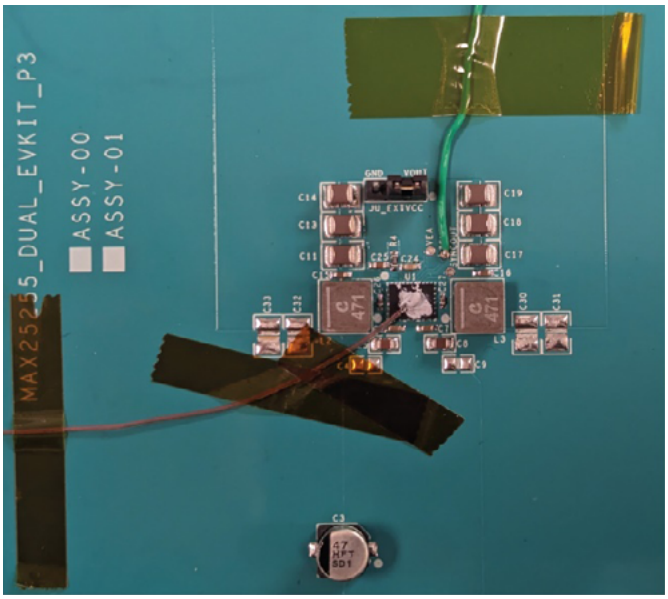


Figure 3: Thermocouple attachment to the MAX25255 IC case top using thermal paste.

The thermocouple is connected to a Fluke 52 II thermometer, which has an accuracy of ±[0.05 % + 0.3 °C]. Allow the converter to operate for 15 to 20 minutes to ensure the IC junction temperature is stable and take the reading on the thermometer. In this case, the thermometer reading was 58 °C. Equation 5 is used to calculate the junction temperature.

$$T_{JUNCTION} = 58°C + 0.58°C/W \times 1.7\ W = 58.98°C \quad (5)$$

The junction temperature estimated here is 58.98 °C, which is not as accurate as the previous two techniques. The error in measurement is about 1.68 °C, which is around 2.93 %. The reason for the increased error in case temperature measurement is due to the addition of equipment involved in this technique (thermocouple, thermal paste, and thermometer). This is still within the combined measurement accuracy of different equipment involved. An advantage of this technique is that it can be used to estimate the junction temperature when the package is placed in the thermal chamber as well.

The three case studies validate the discussed package junction temperature estimation techniques. While using θ_{JA} offers a good method to get a ballpark figure without specialized equipment, ψ_{JT} provides a more accurate estimation. The parameters offer a more precise estimation of junction temperature in real-world applications compared to θ_{JA}, which is highly dependent on PCB design. A good example to highlight this difference is by comparing the values for θJA and ψ_{JT} for the MAX25255 for the JEDEC board and EV kit in Table 2. Note the variation in θ_{JA} for the two boards is close to 9 K/W, whereas ψ_{JT} only varies by 0.02 K/W.

Conclusion

This article provides a comprehensive overview of the key thermal parameters, including thermal resistance (θ) and thermal characterization parameters (ψ), and their roles in accurate thermal estimation. The story detailed two primary methodologies for estimating junction temperature of a package without a heat sink: using junction-to-ambient thermal resistance (θ_{JA}) and using junction-to-case (top) thermal characterization (ψ_{JT}). Each method has its specific requirements, procedures, and challenges. The case studies demonstrated the practical application of these methods, highlighting the importance of accurate measurements and the impact of different techniques on the estimation accuracy. For accurate measurements, using ψ_{JT} is the preferred method in real-world applications compared to θ_{JA}.

Common mistakes in junction temperature estimation, such as misunderstanding thermal parameters, incorrect use of θ_{JA}, errors in loss calculation, and improper case temperature measurement, were also discussed. By avoiding these pitfalls, designers can improve the accuracy of thermal assessments. In summary, the techniques discussed in this article might not be able to determine the package temperature with absolute precision, but with a thorough understanding of thermal metrics and careful selection of estimation techniques, we can improve the accuracy of thermal measurements.

www.analog.com

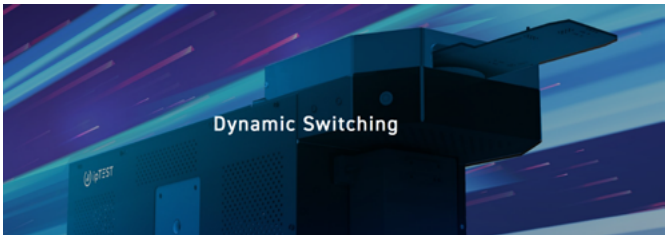
1700 V Switcher IC for 800 V BEVs

Power Integrations announced five new reference designs targeting 800 V automotive applications based on the company's 1700 V InnoSwitch™3-AQ flyback switcher ICs. Spanning power levels from 16 W to 120 W, the designs leverage both wound and low-profile planar transformers and target automotive applications such as DC/DC bus conversion, inverter emergency power, battery management and power supplies for auxiliary systems. The designs feature Power Integrations' wide-creepage InSOP™-28G package, which supports 1000 V_{DC} on the primary side while providing appropriate creepage and clearance between pins in pollution degree 2 environments. Power consumption is less than 15 mW at no-load. The ICs also incorporate synchronous rectification and a valley switching, discontinuous/continuous conduction mode (DCM/CCM) flyback controller capable of delivering greater than 91 % efficiency. The company provides three reference designs, which are all isolated flyback converters based on the 1700 V-rated CV/CC InnoSwitch3-AQ switcher ICs. The three reference designs kits (RDKs) and two design example reports (DERs) are RDK-994Q (35 W ultra-low-profile traction inverter gate-drive or emergency power supply with 40-1000 V_{DC} input and 24 V output), RDK-1039Q (18 W power supply with planar transformer for traction inverter gate driver or emergency power supply), RDK-1054Q (120 W power supply with planar transformer, designed to shrink or eliminate heavy, bulky 12 V batteries), DER-1030Q (20 W four-output power supply) and DER-1045Q (16 W four-output power supply).

www.power.com

Test Generator for up to 2 kA

The Microtest Group introduced the M2 DS5 Quasar, "the smallest 2 kA low inductance dynamic switch test generator, for the test of all types of products on one platform". The tester is suited for high-volume semiconductor production. The M2 DS5 Quasar is designed to test power chips, and the latest WBG (Wide-bandgap) devices made from Silicon Carbide and Gallium Nitride, materials commonly found in consumer power supplies, electric vehicles including trains and battery electric hybrid, industrial motors, HVAC systems and many other applications in the green energy, automotive, power markets, as well as rad-hard (radiation-hardened) devices for space and defence. The tester was developed by the UK subsidiary ipTEST. It is eight times more efficient in overcurrent protection, with a typical response time of under 300 ns. The parasitic inductance has also been reduced by 85 % to 30 nH.



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SiC Superjunction Technology

Infineon Technologies has introduced a trench-based SiC superjunction (TSJ) technology concept. This expansion will encompass a diverse range of package types, including discretes, molded and frame-based modules, as well as bare dies – for a broad spectrum of applications, targeting both the automotive and industrial sectors. The first products based on the new technology will be 1200 V in Infineon ID-PAK for automotive traction inverters and combine the advantages of trench technology and superjunction design. This scalable package platform supports power levels of up to 800 kW, enabling system flexibility. Key benefits of the technology include increased power density, achieved through an up to 40 percent improvement in $R_{DS(on)}$* A, allowing for more compact designs within a given power class. Additionally, the 1200 V SiC trench-superjunction concept in ID-PAK enables up to 25 percent higher current capability in main inverters without compromising short-circuit capability. As an early customer, Hyundai Motor Company development teams will use the trench-superjunction technology in electrical vehicle drivetrains.

www.infineon.com

Multiphase Power Controller

Alpha and Omega Semiconductor (AOS) announced its AOZ98252QI 2-output, 8-phase controller with 2.5 mA quiescent power. Featuring AMD SVI3 high-speed and SMBus digital interfaces, the AOZ98252QI is engineered as a key component in a complete system power solution with AOS' DrMOS products for graphics and desktop systems. The AOZ98252QI digital controller provides two output rails in flexible 8+0 to 4+4 GFX/SOC and Vcore/SOC output rails. Using the A2TM (Advanced Transient Modulator) feature, designers can achieve fast response times and adequate current balance for transient and DC loads. The device is shipped in a QFN 6x6-52L package.

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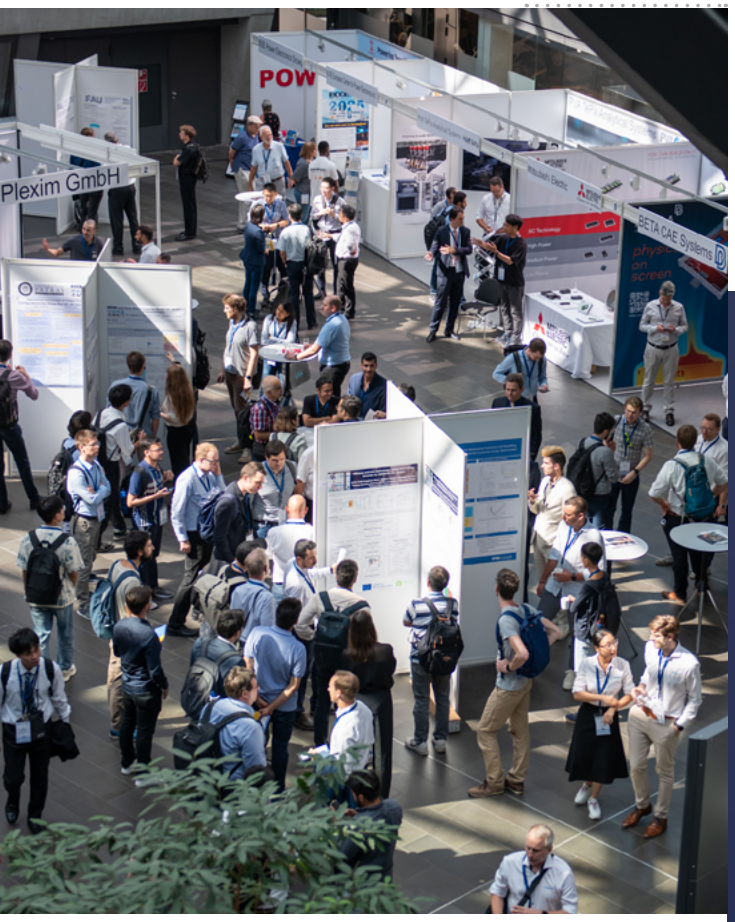

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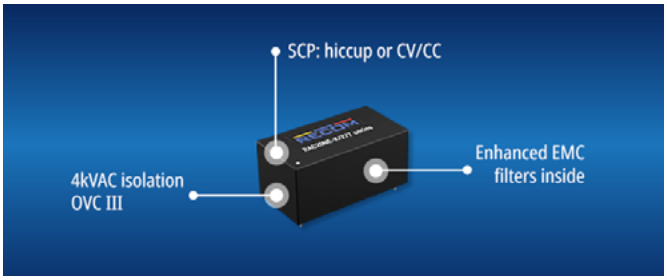
Series of Gate Drive Transformers

ITG Electronics has introduced a series of gate drive transformers comprising a range of products for various needs. The company's T201213 Series of Gate Drive Transformers spans lower-current items for general applications – such as a 200 V direct current version – to products offering up to 450 V_{DC} for higher-voltage applications. Gate drive transformers are specialized pulse transformers used to deliver high-power, fast-switching signals to the gates of power translators like IGBTs and MOSFETs, while also providing galvanic isolation. Essentially acting as barriers between power translators and controlling drive circuits, gate drive transformers are essential to applications such as power converters and motor drives for efficient and consistent switching. The T201213 Series activates or deactivates switching devices, and provides floating supply and level shifting for switching signals. The series is designed for frequencies from 20 – 300 kHz, and each gate drive transformer in the portfolio meets medical safety isolation requirements.

www.ITG-Electronics.com

AC/DC Power Supplies delivering 20 W

In new energy applications, AC/DC power supplies increasingly must operate over nominal supply values from 100 V_{AC} to 277 V_{AC}. The recently launched RAC20NE-K/277 from Recom matches this with 20 W available at optional 12, 24, or 36 V_{DC} outputs. Encapsulated versions are available with constant voltage or constant current limiting characteristics and a constant voltage open frame type with 12 or 24 V_{DC} output. The RAC20NE-K/277 series allows reliable operation at full load to 60 °C ambient, and to 85 °C with derating. The parts are Class II insulated, OVC III rated to 3000 m altitude (OVC II/5000m) and meet EN 55032 'Class B' EMC requirements with a floating or grounded output. Standby and no-load power dissipation meet Eco-design requirements. The RAC20NE-K/277 board-mount, encapsulated parts are sized 52.5 mm x 27.6 mm x 23.0 mm while the open frame parts with Molex connections measure 80.0 mm x 23.8 mm x 22.5 mm.



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Enhanced Thermal Performance Package Technology

WeEn Semiconductors has introduced SiC MOSFETs and Schottky Barrier Diodes (SBDs) in thermally efficient TSPAK packages. These packages will enable engineers to improve efficiency, reduce form factors, extend reliability and lower EMI across a variety of high-power applications. Providing effective heat dissipation from a thermal pad on the surface of the SiC device rather than via a PCB substrate, the company's top-side cooling TSPAK technologies can reduce J-A (junction-to-ambient) thermal resistance by up to 16 % compared to conventional devices. As a result, the packages help to simplify thermal management design, lower losses and increase power density. EMI reduction derives from the fact that the circulating current that creates the magnetic field is no longer blocked by the thermal vias necessary in conventional bottom-side cooling designs and can return to the source directly, minimizing magnetic interference. WeEn's TSPAK SiC technologies are suited to on-board chargers and high-voltage-to-low-voltage DC/DC converters in electric vehicles, automotive HVAC compressors, vehicle charging stations, photovoltaic renewable energy systems and power supplies for computing and telecom servers. TSPAK MOSFETs offer voltage ratings from 650 V to 1700 V and on resistance ratings from 20 to 150 mΩ. TSPAK SBDs are available with voltages from 650 V to 1200 V and current ratings of 10 A to 40 A.

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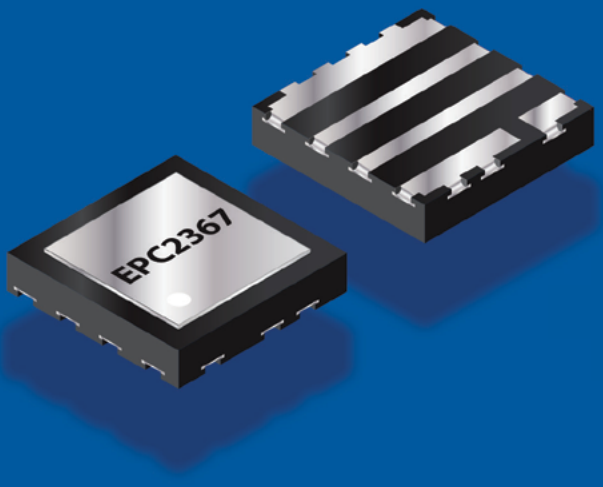

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