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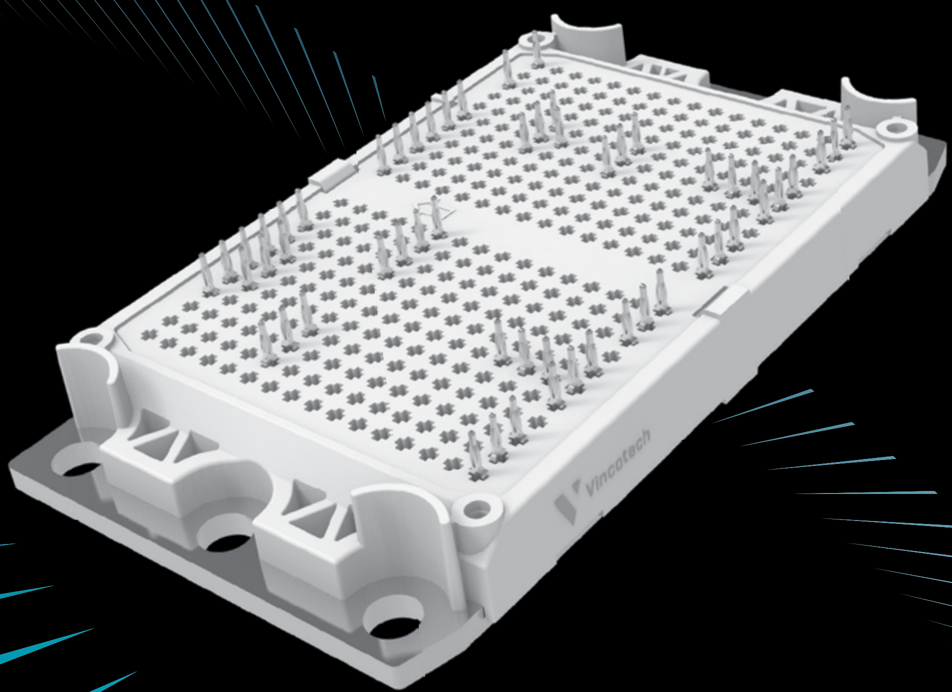
Bodo´s Power Systems®

Electronics in Motion and Conversion

November 2025

ADVANCING INDUSTRIAL POWER CONVERSION WITH SILICON CARBIDE



ed-k

PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES WITH 3-PHASE EXTENSION UNIT

Inductance measurement on 1~ and 3~ reactors from 0.1 A to 10 kA

3-PHASE EXTENSION UNIT

- Easy and quick measurement of 3-phase inductors
- Automatic measurement of all windings without reconnecting the terminals
- The software considers the different magnetic flux conditions in the core with 3-phase sinusoidal currents and corrects the measurement results
- The measurement result is equivalent to a conventional measurement with 3-phase sinusoidal mains voltage

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

APPLICATIONS

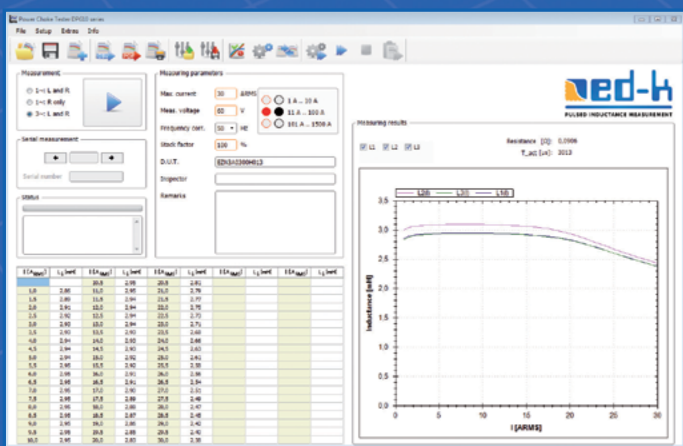
Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**

- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

KEY FEATURES OF THE DPG10/20 SERIES

Measurement of the

- **Incremental inductance** $L_{inc}(i)$ and $L_{inc}(\int Udt)$
- **Secant inductance** $L_{sec}(i)$ and $L_{sec}(\int Udt)$
- **Flux linkage** $\psi(i)$
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** $B(i)$
- **DC resistance**



ed-k

Technological leader in pulsed inductance measurement for 18 years

www.ed-k.de

Content

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Getting Wide Bandgap Semiconductors done

Earlier this month I took the train from Neubiberg/Germany (where Infineon is headquartered) to Villach/Austria. However, I neither want to talk about the great weather there while we had a grey autumn sky in Munich, nor about the greatest view at the I alps I ever had from a meeting room, which can be distracting during a Q&A session. Villach is the center of gravity for Infineon's power semiconductor development, and it was very impressive to see POWER semiconductor manufacturing on 300 mm wafers during my tour in a bunny suit through the fully automated wafer fab.

In power semiconductor manufacturing we talk more about 100 nm than 3 nm technology, but one fact really fascinated me: In GaN semiconductors the GaN layer is added to a silicon wafer in an epitactical process, however, there is a huge problem, because the crystal lattice of Si and GaN have a 17 % mismatch. Across the diameter of a 300 mm wafer (Infineon now manufactures GaN on 300 mm) this results in pressure forces in the GigaPascal range. 1 GPa is roughly 9 times the pressure that exists at the deepest point on earth, in the Mariana Trench in the western Pacific Ocean almost 11 km below sea level. Despite this enormous pressure, the GaN-on-Si wafers undergo over 1,000 individual process steps involving numerous heat/cold cycles before becoming the finished product you can use in your designs.

You too may marvel at this, but at Bodo's Wide Bandgap Event we will go one step further, because then it's a question of how GaN and SiC components can be best used and integrated into end product designs.

On the second day of Bodoswbg.com, which takes place on December 2 &3 at the Munich Airport Hilton, you will be able to listen to more than 40 live-presentations from industry experts in two parallel, synchronously clocked tracks on GaN and SiC. Every 10-minute presentation is followed by 5 minutes of Q&A. So it'll be a powerful, intensive and very useful day providing many practice-oriented inputs.

One of my personal highlights is the panel discussion on day 1, where six high-level executives from major SiC and GaN manufacturers as well as the director of the inverter department at one of the leading automotive tier-1 manufacturers will discuss with Bodo and myself how we can make wide bandgap designs happen.

If you still register in the first days of November, you will be eglible for the discounted early bird offer. Furthermore, some very few companies have the opportunity to present their solutions and services in the table-top exhibition.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive, of every issue of the magazine, is available for free at our website bodospower.com.

My Green Tip of the Month:
Check out footprintcalculator.org and think about the result. If you live in the US, you might want to visit epa.gov/ghgemissions/carbon-footprint-calculator, where they also provide an offline calculator in spreadsheet format.

Alfred Vollmer

Events

Batteries Event 2025
Lyon, France November 4 – 6
www.batteries-event.com

WiPDA 2025
Fayetteville, AR, USA November 10 -12
www.wipda.org

DMC 2025
Fayetteville, AR, USA November 17 – 19
https://attend.ieee.org/dmc-2025

productronica 2025
Munich, Germany November 18 – 21
www.productronica.com

SEMICON Europa 2025
Munich, Germany November 18 – 21
www.semiconeuropa.org

SPS 2025
Nuremberg, Germany November 25 – 27
https://sps.mesago.com

cti symposium 2025
Berlin, Germany November 2 – 3
www.cti-symposium.world/de

Bodo's WBG Event 2025
Munich, Germany December 2 – 3
www.bodoswbg.com

PCIM Asia New Delhi 2025
New Delhi, India December 9 – 10
www.pcim.in

Lift motor developed using Ferrite Magnets – without Rare Earth Materials

Ziehl-Abegg claims to be "the first company worldwide to develop a high-performance synchronous lift motor that operates entirely without rare earth magnets – without compromising on power output". The new lift motor, which uses ferrite magnets, eliminates the need for critical raw materials such as neodymium and dysprosium, which have traditionally been considered indispensable for high-performance drives due to their power density. These rare earth elements are sourced almost exclusively from one single country. Despite foregoing rare earth high-performance magnets, this motor delivers identical performance – all within the same dimensions. This is a real advancement, particularly for high-torque lift applications where smooth operation and energy efficiency are critical. A patent application has already been filed.

www.ziehl-abegg.com

New CEO for Fabless GaN Manufacturer

Wise Integration appointed Ghislain Kaiser as Chief Executive Officer. Kaiser succeeds CEO and co-founder, Thierry Bouchet, who will continue to serve as Chief Technology Officer and General Manager, leading the worldwide R&D and driving the technological vision. In 2006, Kaiser cofounded Docea Power, a French EDA startup pioneering full-chip, system-level power and thermal modelling, with the vision of addressing the growing power-consumption and thermal challenges in IC and platform design. As CEO, he led the company to domain leadership and its acquisition by Intel in 2015. He then joined Intel, where for the next decade

he held senior director roles, most recently overseeing system-simulation engineering and worldwide customer-enablement organization. Those programs tackled critical power, thermal, and performance challenges in designing consumer, data-center, and AI systems. Kaiser began his career at STMicroelectronics, where he held technical and leadership positions across test and product engineering, design, and architecture teams. 'Wise Integration spun out from CEA Leti in 2020 using the institute's GaN-on-silicon R&D platform.

www.wise-integration.com

Christian Felgemacher appointed Director Application Engineering

ROHM Semiconductor is pleased to announce the appointment of Dr. Christian Felgemacher as Director Application Engineering. Since October 1st, he has been responsible for both the operational coordination of technical customer support and the strategic direction of ROHM's application engineering activities in Europe. Since joining ROHM in 2017, Dr. Felgemacher has contributed significantly to the establishment of the Application and Technical Solution Center (ATSC) - with the set-up of the company's Power Lab and the development of customer-oriented solutions for ROHM's European customers. In his previous role as Senior Department Manager Application Engineering, he already led the Technical Consulting and Customer Support division with great commitment and promoted conceptual cooperation with important partners from industry and university research. His leadership role was crucial to the expansion of ROHM's activities in the automotive, industrial, and energy sectors - particularly through initiatives related to SiC technologies and inverter development.

www.rohm.com

Global Agreement to Distribute High-Energy Density Capacitors

Quantic™ Evans

Mouser Electronics announces a global distribution agreement with Quantic Evans, a company which is active in high-energy density capacitors for demanding mission-critical applications. Quantic Evans' hybrid capacitors, known as EVANSCAPS, serve diverse markets, including aerospace, energy, and communications, where high-reliability, size, weight, and power (SWaP) are crucial. The Quantic Evans HyCap hybrid capacitors, available to order from Mouser, are designed to provide reliable operation in a wide range of harsh environments, including those with shock and vibration conditions. These devices are available in a capacitance range of 68 µF to 2700 µF with a ±20% tolerance, with a voltage range of 10 V_{DC} to 150 V_{DC}. The HyCap capacitor series' robust construction makes them suitable for energy, industrial, space, and defence applications. They are built with patented hybrid wet tantalum technology, featuring a Tantalum Pentoxide anode and a Ruthenium Oxide cathode.

www.Mouser.com

Groundbreaking for EMC Lab

TDK is building a new EMC laboratory in Regensburg. It will replace the accredited laboratory that has been in existence for more than 60 years at a new location. The facility will offer internal and external customers state-of-the-art capabilities for measuring electro-

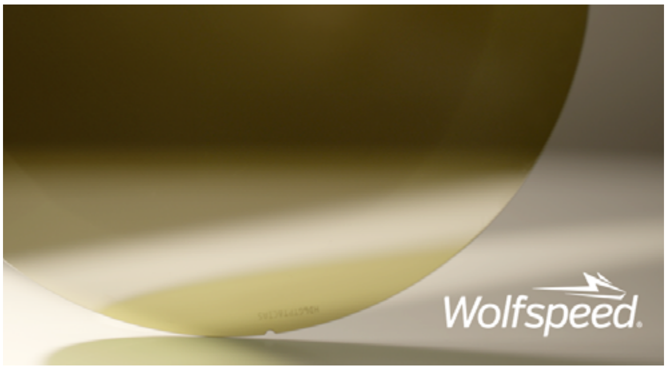
magnetic compatibility (EMC). The groundbreaking ceremony for the new laboratory has now taken place. TDK is investing a double-digit million euro amount in the new building. The new laboratory will have a total area of almost 1,700 square meters, 1,100 square meters of which will be used for the laboratory and measuring stations. A showroom and a large customer area with meeting rooms are also planned. The centerpiece of the laboratory is a new 10-meter semi-anechoic chamber, in which even large vehicles and powerful industrial applications can be measured. It is complemented by a 3-meter full-absorber chamber for RF and radio applications, which is claimed to enable “the fastest measurement methods at the highest frequencies”, as well as a compact chamber for measuring automotive components such as control units or onboard chargers. This chamber is equipped with absorbers that are only ten centimeters deep.

www.tdk-electronics.tdk.com

Commercial Launch of 200 mm SiC Materials Portfolio; ready to Manufacture at Scale

Wolfspeed announced the commercial launch of its 200 mm SiC materials products. Wolfspeed is also offering 200 mm SiC epitaxy for immediate qualification, which, when paired with the company's 200 mm bare wafers, delivers high scalability and improved quality, enabling the next generation of high-performance power devices. The improved parametric specifications of the 200 mm SiC bare wafers at 350 µm thickness and “enhanced doping and thickness uniformity of the 200 mm epitaxy” is claimed to enable “device makers to improve MOSFET yields, accelerate time-to-market, and deliver more competitive solutions across automotive, renewable energy, industrial, and other high-growth applications”.

www.wolfspeed.com



Collaboration on SiC Power Electronics Packages to enhance Flexibility

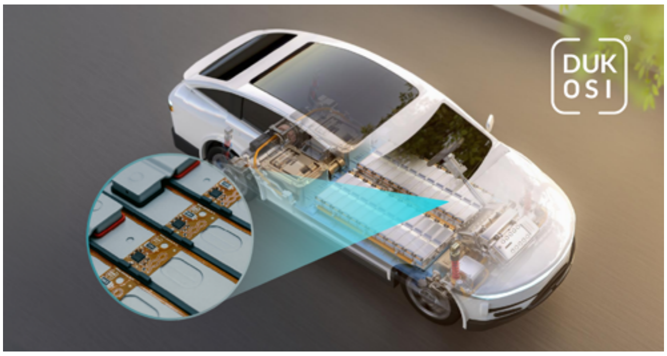
Infineon Technologies and ROHM have signed a Memorandum of Understanding to collaborate on packages for silicon carbide power semiconductors used in applications such as on-board chargers, photovoltaics, energy storage systems and AI data centers. Specifically, the partners aim to enable each other as second sources of selected packages for SiC power devices, a move which will increase design and procurement flexibility for their customers. In the future, customers will be able to source devices with compatible housings from both Infineon and ROHM. The collaboration will ensure seamless compatibility and interchangeability to match specific customer needs. As part of the agreement, ROHM will adopt Infineon's top-side cooling platform for SiC, including TOLT, D-DPAK, Q-DPAK, Q-DPAK dual, and H-DPAK packages. Infineon's top-side cooling platform offers several benefits, including a standardized height of 2.3 mm for all packages. At the same

time, Infineon will take on ROHM's DOT-247 package with SiC half-bridge configuration to develop a compatible package. That will expand Infineon's recently announced Double TO-247 IGBT portfolio to include SiC half-bridge solutions. ROHM's DOT-247 delivers higher power density and reduces assembly effort compared to standard discrete packages. Featuring a unique structure that integrates two TO-247 packages, it enables to reduce thermal resistance by approximately 15 percent and inductance by 50 percent compared to the TO-247. The advantages bring 2.3 times higher power density than the TO-247. Infineon and ROHM plan to expand their collaboration in the future to include other packages with both silicon and wide-bandgap power technologies such as SiC and GaN.

www.infineon.com

ASPICE Capability Level 2 for Next Generation Cell Monitoring System achieved

Dukosi has achieved Automotive SPICE® (ASPICE) Capability Level 2 for development processes related to its next generation cell monitoring system for automotive and electric vehicle (xEV) applications. This important assessment milestone assures compliance with the demanding quality requirements of automotive customers and gives confidence that automotive software and systems are developed with consistent quality, reliability and safety. The intensive assessment was performed by UL Solutions in compliance with ASPICE PAM 4.0 (Process Assessment Model) and in accordance with the ISO/IEC 33002 standard and completed in September 2025. The Automotive Software Process Improvement and Capability Determination (ASPICE) standard, developed by the German Association of the Automotive Industry (VDA), has been established worldwide and is used by leading OEMs and suppliers to evaluate the development processes of software-based systems in and around the vehicle. UL Solutions' rigorous assessment included Dukosi's processes across system development, software development, support and project management, and the scope of this assessment went beyond the scope recommended by VDA. Reinforcing the company's commitment to product safety, Dukosi's development processes are in full alignment with ASPICE PAM 4.0 and ISO 26262.



www.dukosi.com

Manufacturing Partner for Power Devices

iDEAL Semiconductor confirms that its SuperQ™ silicon power devices are now in production at Polar Semiconductor, a foundry specializing in high-voltage, power, and sensor technologies. SuperQ uses a patented asymmetrical RESURF structure; it significantly reduces conduction and switching losses – with up to 2.7x lower resistance compared to legacy silicon and cutting switching losses by up to 2.1x versus competing devices. Polar Semiconductor operates a high-volume 200 mm manufacturing facility in Minnesota and is claimed to be "the only majority U.S.-owned foundry with deep expertise in high-voltage and power semiconductors". With a 50-year heritage in automotive production, Polar is IATF 16949 certified and committed to zero-defect manufacturing. iDEAL's first products – 150 V and 200 V MOSFETs announced in July – are already in production at Polar, with 300 V and 400 V devices to follow. Polar is further expanding to double its manufacturing capacity and invest in next-generation technologies.

www.idealsemi.com

PwrSoC 2025 – Global Experts Discussed Miniaturization of Power Conversion

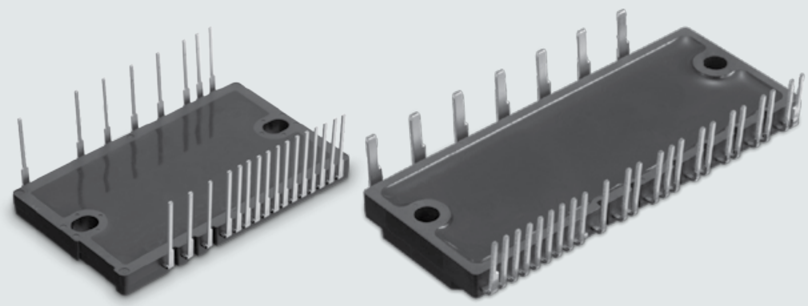
The 9th International Workshop on Power Supply on Chip (PwrSoC) was held from September 24 to 26, 2025, in Seoul, South Korea. This year's workshop marked another significant milestone in the field of integrated power solutions. Over 213 leading researchers and industry professionals from around the world gathered to share insights and advances in the miniaturization and integration of power conversion and power management at the chip, package, and module level. The workshop featured three plenary talks from industry leaders, offering deep insights into the latest developments in miniaturized and integrated power conversion and power management technologies. Following PwrSoC's signature single-track format, the workshop presented high-impact invited presentations and an engaging poster session. The technical program covered a wide range of topics, including Systems & Applications, Integrated Magnetics, Topologies & Control, Wide Bandgap Integration, System-Integrated Packaging & Manufacturing, Integrated Capacitors and Energy Storage, and Granular Power Supply.

www.pwrsocevents.com

Fuji Electric
Innovating Energy Technology

Small-IPM Series

Ideal for Air Conditioners, Inverters, Heat Pumps and Servo Systems



MAIN FEATURES

- **Low-noise and Energy-saving**
  - Low Loss and Low Noise
    Based on 7th Gen. X-IGBT/FWD Technology
- **Improvement of Surge Immunity**
  - Lower Switching dv/dt Characteristics
  - 7th Gen. X-GBT with VCE=650V Guarantee
  - Higher ESD Immunity and Higher Fast-Transient-Burst Immunity.
- **Expansion of Power Density**
  - High Operation Junction Temperature T_{vjop} = 150°C
  - High Accuracy of SC Protection (±25mV)
  - High Accuracy of OH Protection (143±7°C)
- **Built-in Drive ICs & Boot Strap Diodes**
  - Protection Functions: UVLO, SC, Vtemp Output
  - Built-in BSD with Linear Type Series Resistor

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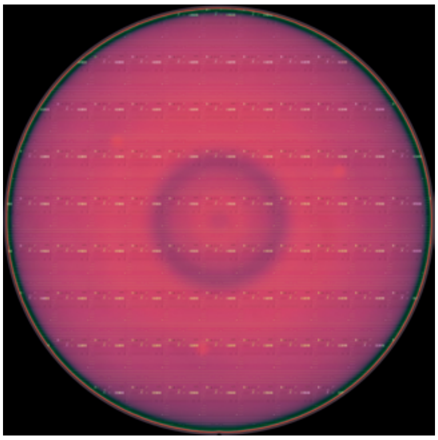
HEAT PUMPS

www.fujielectric-europe.com

300 mm GaN Program launched

Imec welcomes AIXTRON, GlobalFoundries, KLA Corporation, Synopsys, and Veeco as first partners in its 300 mm gallium-nitride open innovation program track for low- and high-voltage power electronics applications. This program track, part of Imec's industrial affiliation program (IIAP) on GaN power electronics, has been set up to develop 300 mm GaN epi growth, and low and high voltage GaN high electron mobility transistor (HEMT) process flows. The use of 300 mm substrates will not only reduce GaN device manufacturing costs, but it will also allow the development of more advanced power electronics devices, such as efficient low-voltage point-of-load converters for CPUs and GPUs. As part of the 300 mm GaN program, a baseline lateral p-GaN HEMT technology platform will first be es-



tablished for low-voltage applications (100 V and beyond), using 300 mm Si(111) as a substrate. For this, process module work centered around p-GaN etch and Ohmic contact formation is ongoing. Later, high-voltage applications are targeted. For 650 V and above, developments will utilize 300 mm semi-spec and CMOS-compatible QST® engineered substrates (a material with poly-crystalline AlN core). During the developments, control over the bow of the 300 mm wafers, and their mechanical strength are prime concerns. Imec expects to have full 300mm capabilities installed in its 300mm cleanroom by the end of 2025.

www.imec-int.com

Passive Components: Plant Opening in China

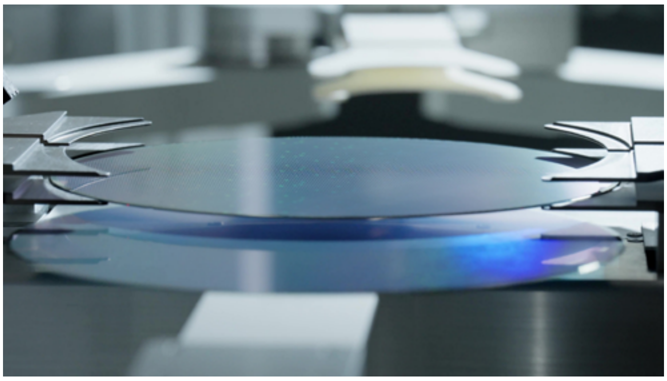
Isabellenhütte Heusler has opened its first plant in China – in Jintan (Changzhou). The company hosted a grand opening ceremony attended by key stakeholders, including customers, suppliers, service providers, local authorities, and political representatives. Dr. Gero

Heusler, member of the advisory board, and the management team – represented by Thilo Gleisberg (CTO) and Dr. Felix Heusler (CFO) – also attended the event and emphasized the strategic importance of the new location for the company's international orientation. With an investment of approximately 18 million Euros and more than 7,000 m² of production space on three levels, the family-owned company is consistently expanding its presence in the world's most important industrial and electronics market. The facility targets LEED Silver certification and will operate entirely on renewable electricity. Isabellenhütte has been known for precision and quality since 1482 - today for its precision and power resistors, current measurement systems, and high-quality alloys. From the outset, the plant has focused on efficient, resource-saving processes and building local expertise. Once in regular operation, over 100 skilled jobs will be created; the first 25 employees have already started work. There are also plans to collaborate with universities and research institutions in the region.

www.isabellenhuette.com

Cleanroom opening at Malaysian Wafer Fab

X-FAB celebrated the grand opening of a manufacturing line at its Sarawak facility. The ceremony was officiated by the Prime Minister of Malaysia, YAB Dato' Seri Anwar Ibrahim, and the Sarawak Premier, YAB Datuk Patinggi Tan Sri Abang Johari Tun Openg.



This major expansion – representing a $600 million investment – added 6,000 square meters of cleanroom space and was completed within two years, from groundbreaking to the first production lots. As a result, the site's monthly wafer start capacity has increased from 30,000 to 40,000, with a key highlight being the more than doubling of capacity for X-FAB's 180 nm BCD-on-SOI technology (XT018). BCD-on-SOI technology is superior in many aspects when compared to conventional bulk BCD technologies. Key advantages include virtual latch-up free circuits, strong EMC performance (due to complete isolation with buried oxide/DTI) and simplified handling of below ground transients. The XT018 platform features a portfolio of voltage options from 10 V to 375 V as well as a full range of automotive Grade-0 qualified Non-Volatile-Memory options. It is specifically designed for next generation automotive, industrial and medical applications operating in extreme temperature ranges from -40 to 175 °C.

www.xfab.com

Headquarter in Italy Opened

RECOM Power Solutions (RPS), part of the RECOM Group, officially celebrated the opening of its new company headquarters in Mareno di Piave, Italy. The event brought together employees from around the world, valued customers, and representatives from politics and business to mark this important milestone.

Among the distinguished guests were Mario Pozza, President of the Chamber of Commerce Treviso-Belluno, Gianangelo Bof, and Andrea Modolo, Mayor of Mareno di Piave. Their speeches and support highlighted the importance of this step for both the region and the continued growth of RECOM Power Solutions.

The celebration embodied the company's core values – teamwork, passion, and a shared vision. In an atmosphere filled with energy and inspiring conversations, the event marked not only the inauguration of the new site but also the beginning of an exciting new chapter in the company's history.

RECOM Power Solutions extends its sincere thanks to everyone who contributed to making this day so special and looks forward with confidence and commitment to a future driven by innovation and excellence in power electronics.

www.recom-power.com

Digital Power Joint Lab to Accelerate High-Efficiency Power Management Deployment

GigaDevice, a semiconductor company specializing in Flash memory, 32-bit microcontrollers (MCUs), sensors, and analog products, has announced the official launch of the Digital Power Joint Lab in collaboration with Navitas Semiconductor. By combining GigaDevice's GD32MCU expertise with Navitas' advantages in high-frequency, high-speed, and highly integrated GaN technologies, and its GeneSiCTM technology leveraging 'trench-assisted planar' technology, the collaboration aims to deliver intelligent and high-efficiency digital power solutions for emerging markets such as AI data centers, photovoltaic inverters, energy storage systems, charging infrastructure, and electric vehicles.

Before its official launch, the lab achieved several important technological milestones, including 4.5kW and 12kW server power supply solutions and a 500W single-stage PV micro-inverter, addressing the industry's demand for high-density, high-efficiency power design and demonstrating the combined innovation strength of both companies. With the establishment of the Digital Power Joint Lab, GigaDevice and Navitas will further expand their collaboration to accelerate innovation in next-generation digital power systems. The lab will focus on developing comprehensive system-level reference designs and application-specific solutions to enable smarter,

greener, and more energy-efficient power systems across data centers, renewable energy, and electric mobility. This partnership marks a significant step toward shaping the future of digital power electronics through technology integration, innovation, and sustainability.

www.navitassemi.com

Planner & Designer Tools for faster Power Sesign

Analog Devices launched ADI Power Studio™, a unified family of power design tools, and introduced two new web-based apps: ADI Power Studio™ Planner (for system-level power tree planning) and ADI Power Studio™ Designer (for IC-level power supply design).

These tools provide engineers with a unified workflow that spans architecture, simulation, configuration and measurement, thereby reducing rework and enabling teams to bring power-dense systems to market more quickly. This is important because modern electronic systems can have dozens or hundreds of interdependent power rails. Power Studio brings ADI's trusted tools into one ecosystem, adds guided workflows, accurate models and automates outputs like BOMs and reports.

www.analog.com

DualPack3 Power Density, Simplified for You

Cost-Efficient Performance in Industry-Standard Packaging

The new DualPack3 modules with IGBT7 technology deliver power density, cost efficiency and robust performance in a compact, proven package. Available in 300–900A ratings at 1200V and 1700V, DualPack3 is built for today's demanding applications.

Key Features

- High power density in a smaller footprint
- Up to 20% reduced losses vs. IGBT4
- Compact 152 × 62 × 20 mm package size
- Higher current output without paralleling modules
- Simplified gate driving with precise dV/dt control
- Reliable operation up to 175°C overload temperature
- Supply chain security with multi-supplier support

Discover how DualPack3 can power your next design.

MICROCHIP

microchip.com/DualPack3

Rapid Control Prototyping System for Power Electronics

The next-generation programmable controller that combines high-performance processing with integrated scoping.

Imperix proudly introduces the B-Box 4, its latest flagship Rapid Control Prototyping (RCP) system. This product is positioned as a flexible, high-performance, and user-friendly digital controller, suitable for the development and testing of virtually any power electronic application.

Engineered with advanced converter control in mind, this 4th-generation controller incorporates cutting-edge peripherals, enabling it to address current demanding needs as well as future challenges.

Simultaneously, the B-Box 4 maintains the ease of use and rapid programming that contributed to its predecessor's success, offering complete support for simulation and automated code generation from within Simulink or PLECS.

Last but not least, users consistently benefit from imperix's software policy, which provides perpetual licenses with complimentary lifetime support and maintenance.

Specialized CPU+FPGA architecture
The B-Box 4 is equipped with a quad-core 1.5GHz CPU, offering direct access to a Kintex-grade FPGA. This architecture, coupled with a highly optimized bare-metal implementation, ensures cutting-edge performance, previously exclusive to custom FPGA implementations. Indeed, control frequencies up to 500kHz are now attainable through CPU-based control, which provides expedited programming, notably via automated code generation from Simulink or PLECS. Consequently, the B-Box 4 is ideally suited for efficiently managing fast-switching applications, particularly those incorporating SiC or GaN semiconductors.

High-speed analog inputs
The B-Box 4 integrates 24 industrial-grade analog inputs offering data acquisition at speeds up to 20 Msps. This unparalleled sampling rate ideally supports high-performance control applications, while also enabling the detailed capture and visualization of complex waveforms – including ripples, harmonics, and transients – similar to a conventional oscilloscope. This unique capability provides engineers with the ability to observe precisely what the control system perceives at no extra cost or effort. This frequently proves invaluable for analyzing the sampling and filtering configuration, evaluating switching harmonics, or for troubleshooting newly deployed applications.

Advanced, high-resolution modulators
The controller integrates advanced modulation capabilities, offering six pre-implemented and thoroughly validated modulator types. These encompass carrier-based modulators equipped with 20-bit counters and an exceptional resolution of 250ps, thereby meeting the rigorous timing demands of fast-switching converters. Furthermore, all PWM signals are accessible for visualization within the monitoring software, enabling precise observation alongside analog signals.

Large, user-editable FPGA
Similar to previous generations, users of the B-Box 4 can program its FPGA completely free of charge with the free version of Vivado or with a third-party tool of their choice. This enables engineers to leverage the device's extensive I/O resources, high-performance capabilities, and robust hardware with utmost flexibility on the software side. Frequently, the optional programming of the FPGA turns out to be the gateway for expanding capabilities in areas such as communication, signal processing, modulation, and various other functionalities.

Instant I/O and performance scalability
Up to 64 units, including 3rd-generation hardware, can be networked via optical fiber, offering plug-and-play I/O expansion capability or enabling distributed control. This is facilitated by 40Gbps networking and imperix's patented RealSync technology, which guarantees low-latency data exchanges and synchronization within ±2ns. In many scenarios, enhanced performance can be achieved by simply stacking multiple devices.

Key Application Areas:
- High-Frequency Converters: Control for isolated DC-DC converters and fast-switching SiC- or GaN-based designs, leveraging high-resolution PWM.
- Multi-Converter Systems: Support for centralized or distributed control for grid-scale systems and large modular converters through enhanced processing and scalability.
- High-Performance Motor Drives: Enabling precise and dynamic control with support for high-precision encoders and sophisticated algorithms.

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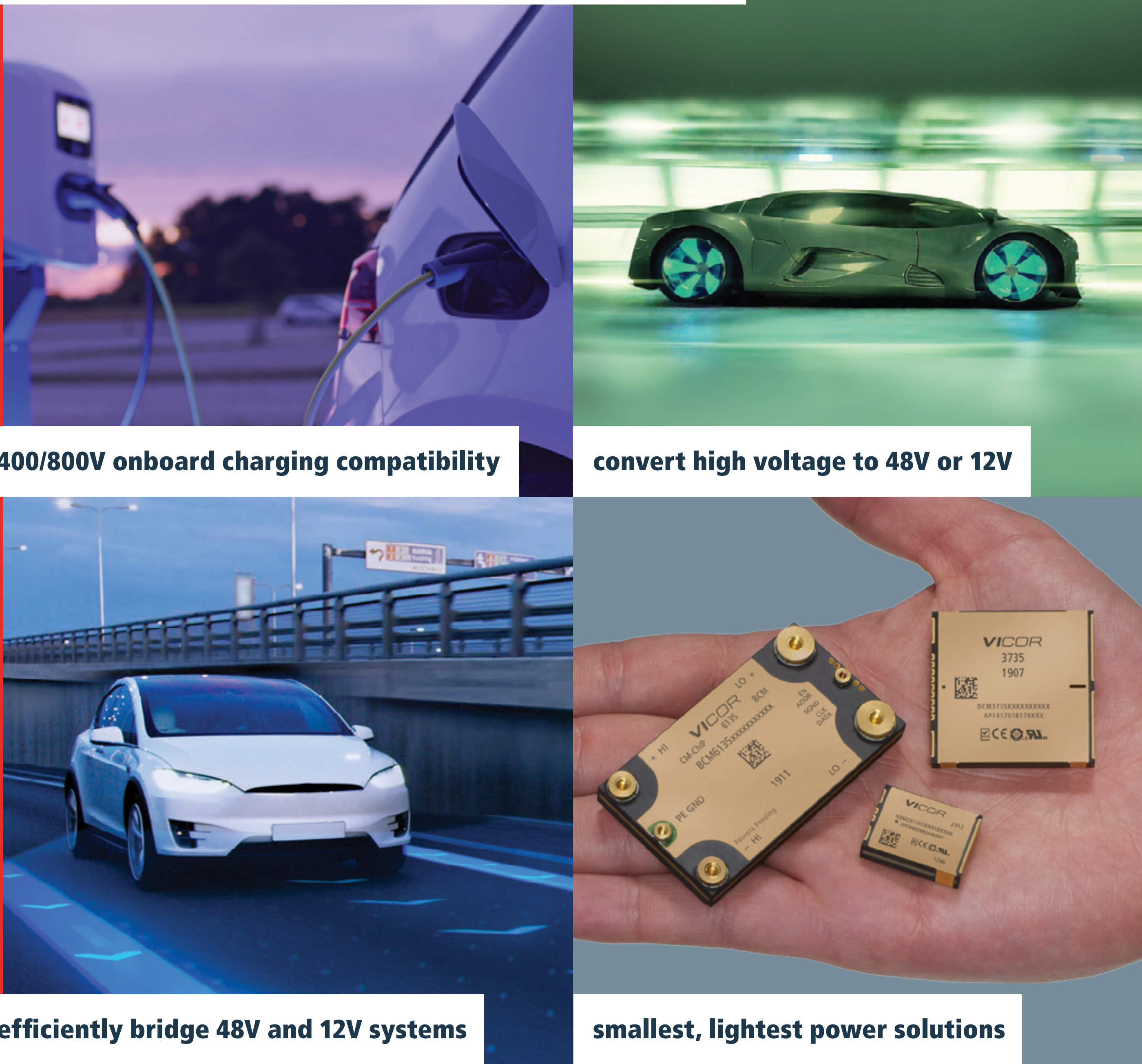

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Advancing Industrial Power Conversion with Silicon Carbide: System-Level Insights and Design Trade-offs

Driven by substantial investments in capacity expansion and improved affordability through cost optimization, Silicon Carbide (SiC) technology is becoming increasingly attractive for a wide range of industrial applications. This article explores the benefits of SiC devices in selected use cases, including HVAC systems, DC fast charging infrastructure, and solar and energy storage systems. Drawing on benchmarked data and practical application insights, it examines key design trade-offs at the topology level, switching behavior, thermal performance, and reliability under real operating conditions. The focus is on system-level implications for engineers designing platforms that demand great efficiency and high power density.

By David Chilachava, Sr. Technical Marketing Manager, Vincotech

Introduction

Silicon carbide (SiC) has emerged as one of the most transformative wide-bandgap (WBG) semiconductor technologies in power electronics. SiC MOSFETs and SiC diodes certainly outperform conventional silicon-based devices. Higher breakdown voltages, faster switching speeds, far greater efficiency under real operating conditions – these properties enable designers to build better power conversion systems that are more compact, thermally robust, and energy-efficient across entire load range.

Industrial applications such as heating, ventilation and air conditioning (HVAC), electric vehicle (EV) DC fast charging systems, photovoltaic (PV) inverters, and energy storage solutions (ESS) are increasingly adopting SiC technology. The driver is not only performance but also regulatory and market demand for higher efficiency, smaller form factors, and reduced lifecycle cost.

SiC in HVAC Systems

HVAC systems are rapidly adopting SiC not only for its performance advantages but also in response to new regulations and growing market demands for greater efficiency, smaller form factors, and lower operational costs.

SiC technology addresses these needs in two critical parts of the system - motor inverters and power factor correction (PFC) stages (see Figure 1)

Motor Inverters

In conventional motor inverters of HVAC systems, silicon IGBTs still dominate. However, their switching losses and limited efficiency at partial loads constrain overall system performance.

Replacing them with SiC MOSFETs results in:

- **Greater efficiency across the load profile:** SiC's lower conduction and switching losses improve efficiency not only at full load but also during partial load conditions, which dominate in typical HVAC mission profile
- **Reduced audible noise:** Operating at higher frequencies in range of 16 to 20 kHz shifts inverter-induced noise out of the audible spectrum
- **Lower operating costs:** Although SiC devices have a higher up-front cost, the energy savings over the system's lifetime deliver a superior cost-performance ratio

SiC MOSFETs offer significant efficiency advantages in motor inverter applications, especially under partial-load conditions. Unlike IGBTs, which maintain a fixed saturation voltage regardless of current, SiC MOSFETs exhibit resistive behavior, allowing conduction losses to scale down proportionally with load current. This makes them inherently more efficient at low operating currents, where the constant voltage drop of IGBTs becomes a dominant loss factor.

These benefits can be further enhanced in embedded drive systems that integrate the inverter and motor into one unit. In such configurations, long motor cables are eliminated, and motor windings are typically designed with insulation rated for higher dv/dt levels. This enables SiC devices to operate at higher dv/dt slew rates using relatively low gate resistor values to further reduce switching losses and improve efficiencies, also at upper load conditions.

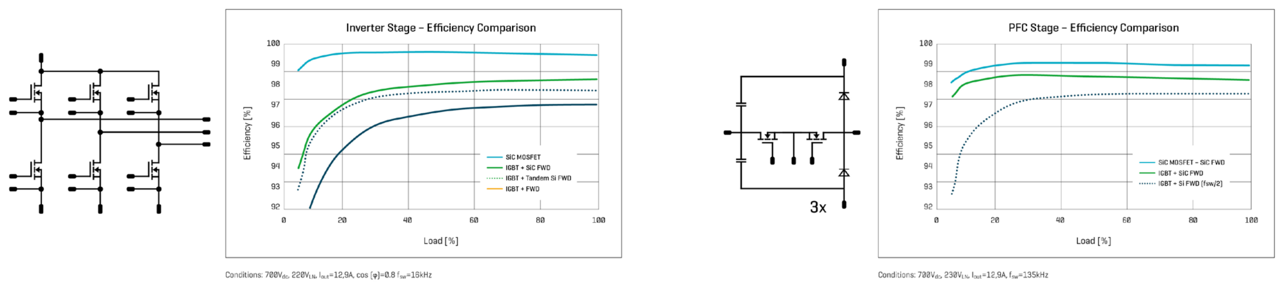

Figure 1: SiC showing clear efficiency advantages, especially under light-load operation in motor inverter (left) and PFC (right) stage


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On the other hand, in standard industrial motor drives the dv/dt slew rates often need to be limited to around 5 kV/µs to protect winding insulation in motors and reduce electromagnetic interference (EMI). To meet this requirement, designers typically choose between two approaches: increasing the gate resistor (Rg) to slow down the dv/dt of SiC MOSFETs, or maintaining relatively low gate resistance and adding an external dv/dt filter.

Using high Rg values restricts the switching performance of SiC devices and leads to increased switching losses, which may require a larger heatsink volume to manage the additional thermal dissipation. In contrast, a dv/dt filter keeps switching losses low, but requires additional filtering components. [1]

PFC Converters

Figure 1 (on left) clearly illustrates how SiC technology outperforms IGBTs in a state-of-the-art neutral boost PFC (NPFC) topology. By using SiC components, the switching frequency is increased to around 135 kHz, close to the conducted EMC level of 150 kHz, where the pure Si solution operates at half that switching frequency. Already the change of FWD by SiC brings efficiency gain from 97,6 to 98,4 % at nominal load. The efficiency can exceed 99 % by replacing IGBTs with SiC MOSFETs.

Opting for SiC components in the PFC stage has multiple benefits:

- **Compact PFC design:** Higher switching frequencies minimize the size of passive components, enabling more compact designs
- **Greater efficiency than Si**, even at higher switching frequencies
- **Lower system costs:** Smaller magnetic components, heat sinks, and enclosures reduce overall system costs
- **SiC diodes as a key enabler:** Their zero reverse recovery loss is essential for achieving both high efficiency and high-power density. IGBTs with SiC diodes is the more cost-effective solution, while a full SiC delivers superior performance.

However, in the PFC stage, topology selection plays a decisive role in determining overall system cost and performance trade-off. The following chart benchmark and compare four topologies under consistent operating conditions.

The Current Synthesizing PFC topology in Figure 3 is based on 3rd harmonic current injection and requires constant power control. The advantages of this topology are that it reduces the SiC content in circuits, calls for just one inductor for 3rd harmonic injection rather than three PFC inductors, and does not need large electrolytic DC link capacitors [3].

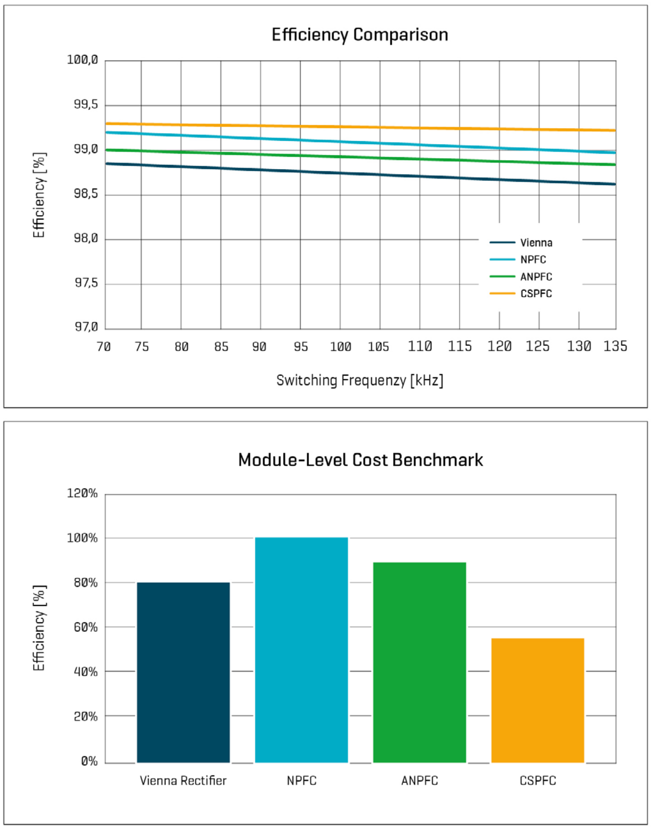

Figure 3: Efficiency and module level cost benchmark of three-phase PFC topologies

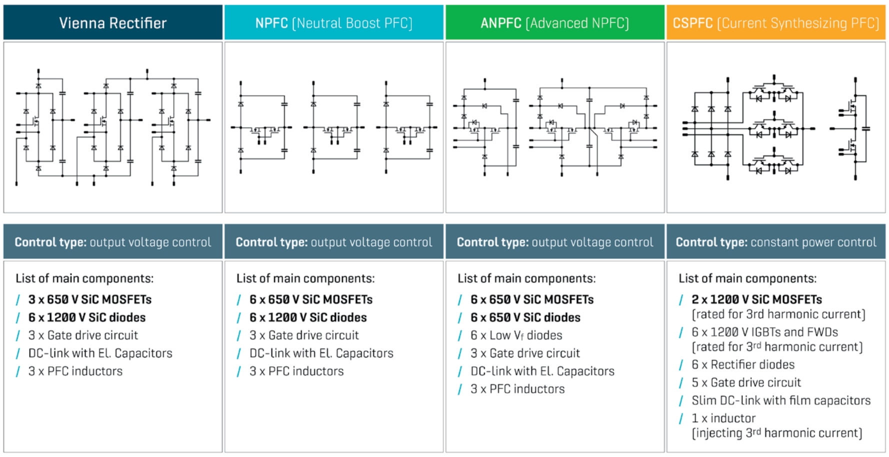

Figure 2: State-off-the-art 3-phase PFC topologies and novel CSPFC topology

An efficiency benchmark reveals that the NPFC topology achieves the highest efficiency among voltage source converters, but also has the highest costs driven by the extensive use of SiC components.

The advanced neutral boost PFC (ANPFC) topology offers a cost reduction of approximately 10 %. This is achieved by lowering the breakdown voltage of the boost diodes from 1200 V to 650 V, allowing the use of more cost-effective components. However, due to the higher voltage drop across two series-connected diodes during freewheeling, the efficiency is approximately 0.2 % lower compared to the NPFC topology.

Further cost savings of around 10 % can be realized with the Vienna rectifier, which uses only one SiC MOSFET per phase. However, due to higher losses in MOSFETs, it also results the lowest efficiency.

The 3rd harmonic injecting CSPFC topology shows highest efficiency. Here the SiC MOSFETs can easily switch at high switching frequencies, as they have only to switch 3rd harmonic current. However, the disadvantage of this topology is the lack of output voltage regulation, which can only be realized by adding an additional DC/DC stage. As the SiC content in this topology is minimal, it also offers the lowest costs.

The first three topologies in *figure 2* are voltage source converters with output voltage control capability. Although they require a similar number of gate drive circuits, PFC inductors, and large electrolytic DC-link capacitors, the Vienna topology uses a single SiC MOSFET per phase, while in NPFC and ANPFC the SiC MOSFETs are in back-to-back configuration.

In the ANPFC topology [2], which is Vincotech's proprietary topology, it is possible to reduce the breakdown voltage of the boost diodes from 1200 V to 650 V, enabling the use of less pricey, lower-voltage SiC FWDs.


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SiC in EV Charging Infrastructure

In the DC fast charging infrastructure, SiC has already established itself as a core technology. Its widespread adoption is driven by the growing demand for faster, more efficient and scalable charging solutions. SiC enables significant improvements in system efficiency - boosting it from typical levels around 95 % to as high as 98 % - while offering better compatibility with higher battery voltages of 800 V and above.

Beyond efficiency gains, SiC contributes to lower operating costs and enabling smaller installation footprints. Both of these benefits are crucial for public charging infrastructure, where space and accessibility are key.

Figure 4 shows several topologies for AC/DC and isolated DC/DC converters. Depending on the output power and battery voltage range, one topology or the other can offer a better cost-performance ratio. However, there are clear trends and narrower choice for bidirectional charging coming from vehicle-to-grid (V2G) use case. In this scenario, electric vehicles not only take power from the grid, but can also feed energy back into it. This capability helps to stabilise the grid, supports the integration of renewable energy, and enables EVs to act as mobile energy storage during the times of peak demand or outages.

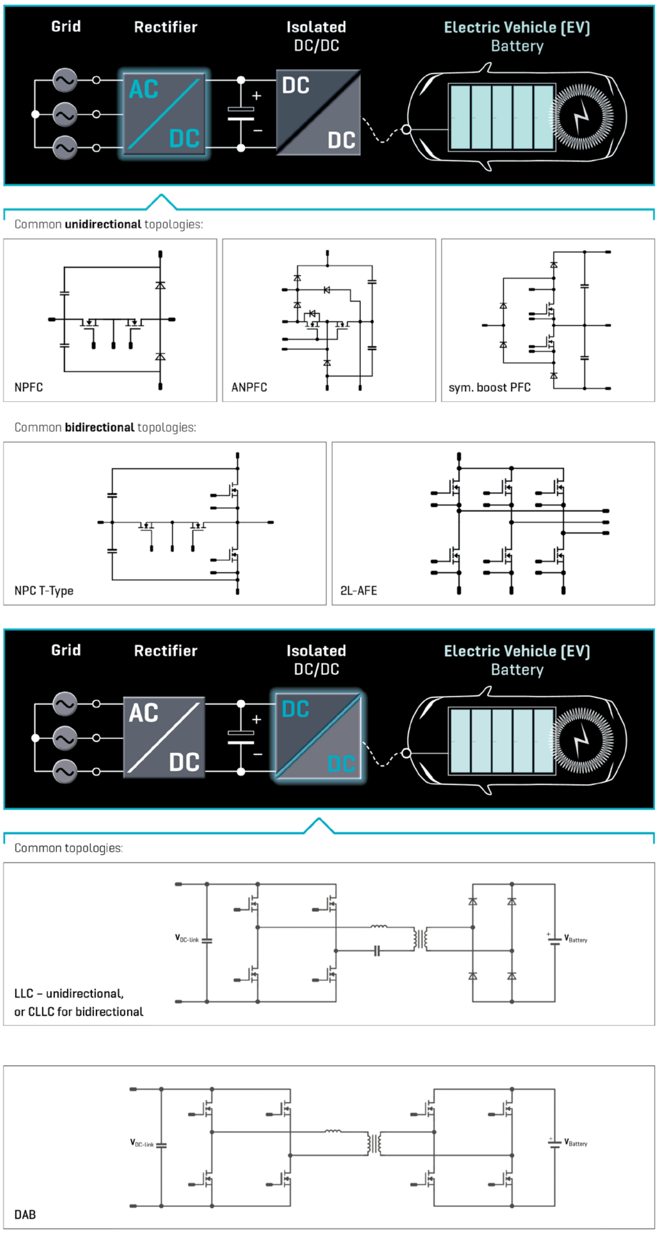

Figure 4: State-of-the-art uni- and bidirectional topologies in DC fast charging for AC/DC and DC/DC power conversion

Towards Megawatt Charging

Megawatt charging systems (MCS) are fast becoming a necessity for long-haul, heavy-duty vehicles such as trucks and buses. These systems can deliver up to 3.75 megawatts. Able to stay on the road longer with fewer pit stops, vehicles operate more efficiently.

Today's MCSs mainly reuse infrastructure for fast charging systems (CCS), achieving higher power levels by stacking multiple subunits, designed for battery voltages up to 920 V. However, the next generation of MCSs is shifting toward 1250 V battery voltages, making integration with 1500 V DC-coupled systems – common in renewable energy and energy storage systems – much simpler. In this architecture, centralized PFC stages or solid-state transformers (SSTs) can connect directly to the medium-voltage grid, followed by modular DC/DC converters. This setup relies heavily on SiC's ability to operate at higher voltages and switching frequencies while maintaining system efficiency. It also requires power modules equipped with the new voltage class of SiC MOSFETs rated for 2 kV or higher.

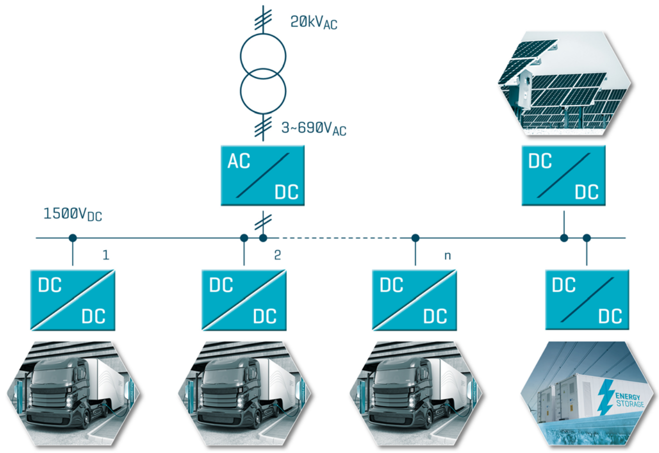

Figure 5: System architecture example of a megawatt charging system

SiC in PV Inverters and ESS

In the residential and commercial PV inverter markets, the use of SiC technology is growing rapidly, especially in hybrid inverters that integrate both solar and battery charging functionalities into a single unit. However, the largest share of SiC deployment is from utility-scale string inverters and energy storage systems. Hybrid topologies combining conventional Si with SiC components are a popular choice for such use cases. These solutions balance cost and performance. For one, they use SiC where its benefits are most impactful, such as in power modules' high-frequency parts. For the other, they retain Si in low-frequency parts where its performance suffices and comes at a lower cost.

Boost stage for PV Inverters

PV inverters typically use two-stage power conversion, where DC/DC boost converters take care of maximum power point tracking (MPPT) and adjust the PV panel output voltage to the required DC-link voltage level. That is the input for DC/AC inverters, which feed solar energy into the public grid. In this input stage two-level and three-level symmetric boost topologies are commonly used, but newer designs are exploring three-level flying capacitor boost architectures [4] for high-power, utility-scale applications.

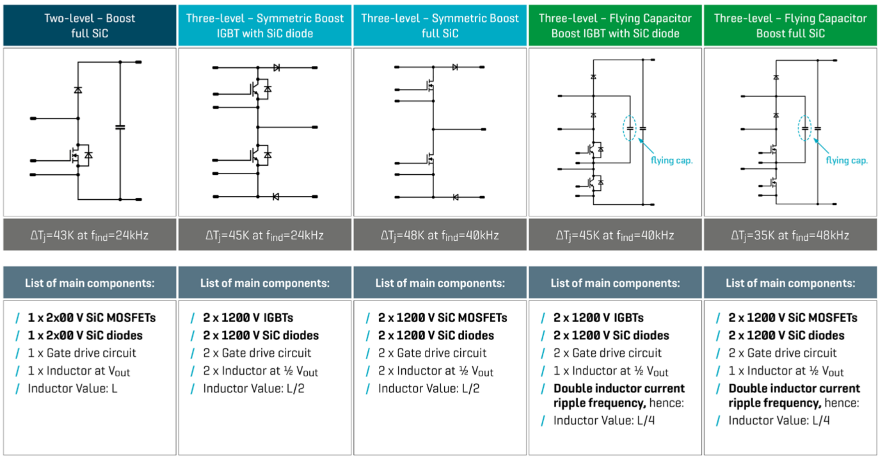

Figure 6: Commonly used boost converter topologies in PV application with the list of main components and main chip junction temperature (T_j) increase at recommended switching frequencies

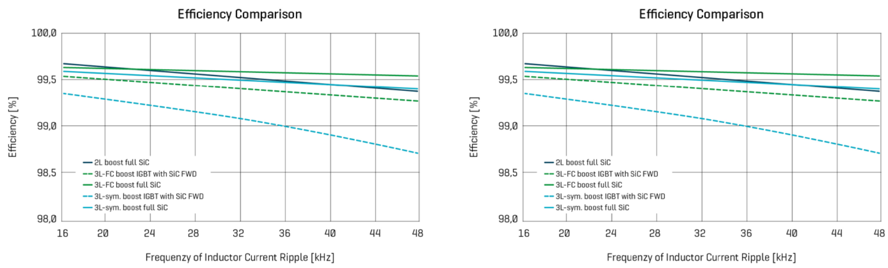

Figure 7: Efficiency and cost benchmark of boost converter topologies under same inductor current ripple frequency

Two-level boost converters are simpler, but they require higher-voltage SiC components of 2kV or more. On one hand to provide sufficient breakdown voltage margin above the 1500 V dc-link and to ensure cosmic ray robustness, and on the other hand to meet the efficiency target. However, these components are significantly more expensive than 1200 V devices used in three-level topologies. Additionally, due to thermal constraints, more chips must be paralleled. As voltage increases, MOSFETs also switch more slowly, so their use is recommended for lower switching frequencies below 24 kHz - resulting in larger and heavier boost inductor needs.

Three-level topologies introduce an additional third voltage level. This reduces the voltage across the boost inductor. Consequently, for a given ripple current, the inductor can be reduced to half its value. This reduces inductor volume, weight, and cost – and that adds up to another big benefit at the system level.

The flying capacitor boost topology differs from the three-level symmetric boost design in that the inductor voltage reverses polarity twice during each switching cycle. This effectively doubles the inductor current ripple. As a result, for the same ripple current, the required inductance is reduced by half compared to a three-level symmetric boost topology - leading to further reductions in the size, weight, and cost of magnetic components. And that improvement comes without changing the specifications for the boost switch and diode, therefore offering the same module price.

Clearly, the flying capacitor topology has best cost-performance ratio compared to both the two-level and three-level symmetric boost topologies. For inductor current frequency of up to 40 kHz, the hybrid three-level flying capacitor topology offers the best system-level cost-performance ratio. Above 40 kHz switching frequencies, full SiC is the solution.

Inverter stage for PV inverters and ESS

In 1500 V PV inverters, hybrid approaches combining Si IGBTs with SiC freewheeling diodes (FWD) based on the three-level NPC I-type topology are well established. These solutions strike a balance between cost and efficiency, offering:

- High efficiency by reducing turn-on losses and thermal stress in IGBTs and eliminating reverse recovery losses in neutral point clamping diodes
- Reduced EMI noise

Active neutral point clamped (ANPC) converters are becoming an increasingly popular option for ESS applications that require full bidirectionality [5]. Featuring SiC MOSFETs in the inner modulation legs, this configuration uses fewer of the expensive SiC switches found in NPC T-type topology to attain excellent efficiency at a very favorable cost-to-performance ratio.

Here, the advantages of SiC MOSFETs compared to a Si IGBT and SiC FWD combination are even more pronounced:

- **High efficiency** due to significant reduction in dynamic losses for both charge and discharge paths, which is critical in battery inverters
- **Improved overload capability**, which is essential for handling transient conditions during grid support or load balancing
- **Reduced cooling efforts**
- **Lower operating costs** (€/kWh)

Figure 9 clearly maps out the design trade-offs engineers can make as they move from Si to SiC technology when designing for PV and ESS applications:

- **Extended life time** by lower thermal stress when switching at Si-level switching frequencies (f_{sw})
- **Smaller, cheaper filter inductors:** up to 2/3 higher switching frequencies (f_{sw}) at comparable junction temperatures (T_j)
- **Higher output power from the same housing footprint** at similar junction temperatures (T_j) and switching frequency (f_{sw})

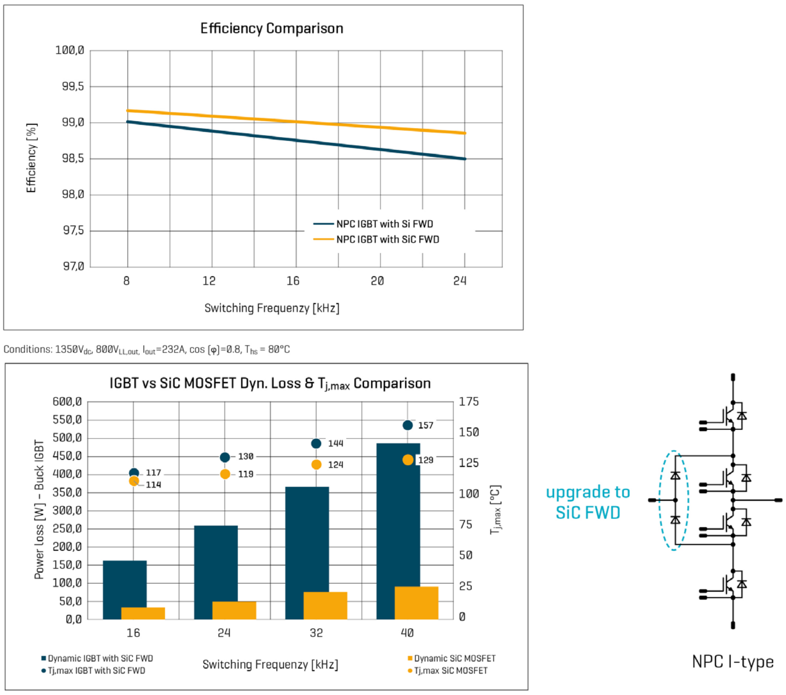

Figure 8: SiC vs Si diode in NPC I-type topology for PV inverters

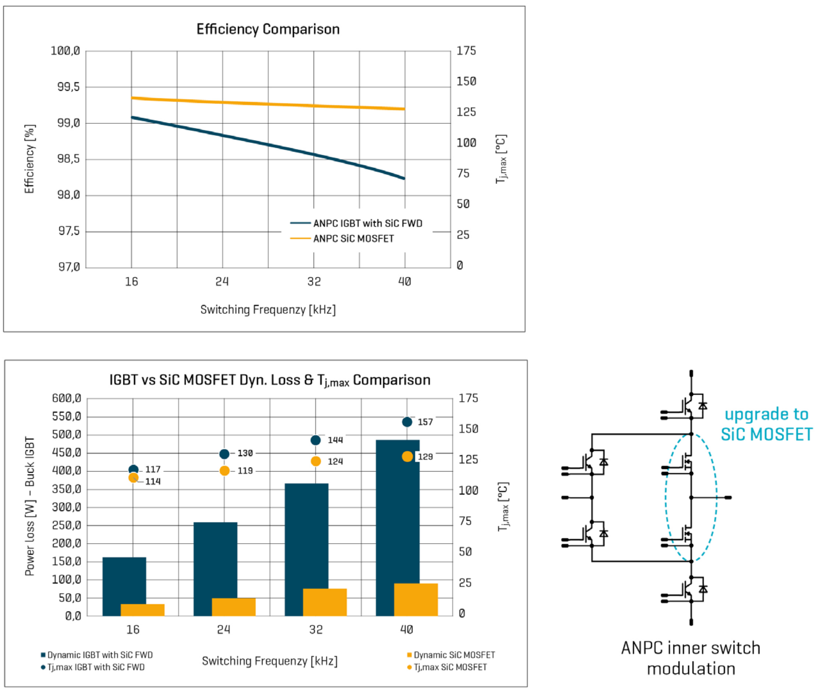

Figure 9: ANPC topology with SiC MOSFETs for ESS

Summary

The adoption of SiC technology is rapidly advancing across industrial sectors due to its superior efficiency, compactness, and reliability. As these devices become more affordable and technologies continues to improve, SiC will increasingly deploy in high-power, high-efficiency applications. In HVAC systems, SiC enables quieter operation and improved energy efficiency, especially under partial load conditions, and helps to meet strict regulatory standards. In EV charging infrastructure, it offers high power density and fast charging up to megawatt-scale, - enhancing accessibility and reducing charging times. SiC is a key enabler in next-generation utility string inverters, sourcing more power from the same physical footprint. In ESS, it delivers the efficient bidirectional performance and robustness for grid support and load balancing. In the visible future, SiC will play a key role in transition for higher PV string voltages beyond 2 kV, helping to further reduce operating costs (€/kWh) and unlock greater system efficiency.

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Achieving Higher Inverter Efficiency by Decoupling Switching Losses and Switching Speeds

Soft-switching power inverters can resolve the traditional trade-off between minimal switching losses and switching speeds. Researchers at FAU Erlangen-Nürnberg, in collaboration with Sanan Semiconductor, have developed a soft-switching inverter that achieves efficiencies exceeding 99.6%. This advancement enables EV manufacturers to improve the driving range and fully utilize the capabilities of wide-bandgap semiconductors.

By Thomas Lehmeier, Yan Zhou, Institute of Power Electronics, Friedrich-Alexander-Universität Erlangen-Nürnberg, and Ajay Poonjal Pai, Head of WBG Semiconductor Innovation, Munich, Sanan Semiconductor

Why aren't we Exploiting the Full Potential of Wide-Bandgap Semiconductor Devices?

High efficiency, low cooling effort, and compact passive components are essential goals for modern power electronics. Wide-bandgap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), present new opportunities to meet these requirements. While the higher switching speeds enabled by SiC and GaN transistors allow for lower losses, and therefore, more compact power electronic systems, they also result in higher dv/dt stresses on the motor windings. To mitigate these effects, practical designs often slow down switching transitions, which consequently increases the switching losses, leaving the full potential of wide-bandgap technologies largely untapped.

The Solution to this Conflict is Soft-Switching

Modern soft-switching converter topologies can significantly reduce these drawbacks, tackling the traditional trade-offs between efficiency and switching speeds. They integrate an auxiliary resonant circuit composed of an inductor and a capacitor, enabling the transistors to switch at zero voltage (ZVS) or zero current (ZCS), which significantly minimizes switching losses. Besides enhancing efficiency and lowering cooling requirements, reduced electromagnetic emissions diminish interference with sensitive devices, allowing for less bulky shielding and filtering. Slower voltage slew-rates also limit voltage spikes, improve system reliability, and reduce bearing currents in electric motors, thus extending their lifespan.

Soft-switching originated in DC/DC converters, where it has already been successfully implemented and commercialized. However, this fundamental principle can also be applied to DC/AC and AC/DC power converters.

Why should you consider the S²I-ARCP Topology?

Various soft-switching inverter topologies are available in literature, primarily distinguished by the placement of the auxiliary circuit. One of the most promising concepts is the Auxiliary Resonant Commutated Pole (ARCP) [1]. This topology consists of a standard B6-bridge and an auxiliary circuit that smoothly switches the transistors of the B6-bridge using ZVS. Researchers at FAU recently evolved this design into a component-reduced variant called the Single Shared Inductor ARCP (S²I-ARCP), where all three phases share a single inductor (see Figure 1) [2]. This topology saves two auxiliary inductors, thereby reducing volume, weight, and cost. The single inductor is now used to commutate all three phases. An intelligent control strategy ensures that only one phase accesses the auxiliary circuit at a time. This can be accomplished by detecting potential collisions between different phases and adjusting the switching edges accordingly.

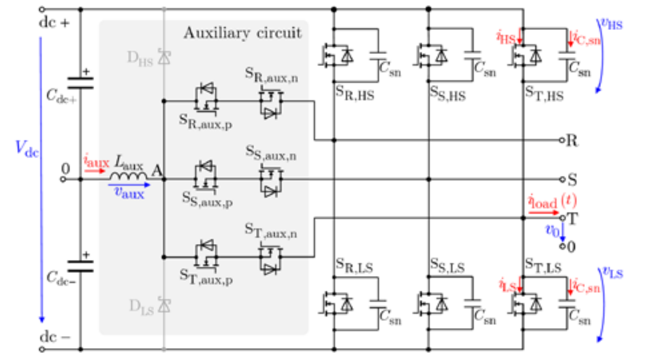

Figure 1: Circuit diagram of the three-phase ARCP with a single shared inductor.

Implementation of the S²I-ARCP Prototype

An 800 V, 15 kW prototype was built to validate this concept. It includes a control board, DC-link voltage measurement, three phase current sensors, a main circuit board containing the B6-bridge and the DC-link at the bottom, and an auxiliary circuit board located at the top that incorporates a toroidal air-coil. To increase the snubber capacitance, NP0 MLCCs are connected in parallel to the output capacitance of the main switches. Sanan 1200 V, 16 mΩ SiC MOSFETs serve as the main switches of the B6-bridge, while Sanan 1200 V, 20 mΩ SiC MOSFETs are used in the auxiliary circuit. The auxiliary switches can be rated for a lower current since current only briefly flows through the auxiliary circuit during commutation. A conventional sinusoidal modulation (other modulation methods are also applicable) generates the gate signals for the main switches. The detailed implementation of the operational strategy for the auxiliary switches, including collision avoidance, is provided in [2].

Figure 2 presents a photograph of the prototype, and Table 1 summarizes the key design parameters and components.

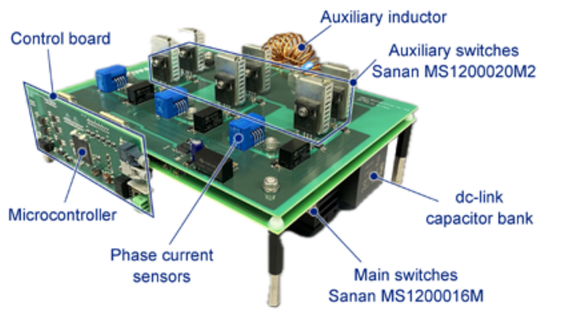

Figure 2: Experimental prototype of the three-phase S²I-ARCP.

Parameter / Component	Value
DC-link voltage V_{DC}	800 V
Rated output power P_{out}	15 kW
Switching frequency f_{sw}	up to 40 kHz
Auxiliary inductor L_{aux}	5.5 µH (air coil)
Snubber capacitance C_{sn}	1 nF (NP0 MLCCs)
Dead-time T_{dead}	185 ns
Main switches	SiC MOSFET Sanan MS1200016M
Auxiliary switches	SiC MOSFET Sanan MS1200020M2
Cooling	Natural convection

Table 1: Main Design Parameters and Components of the Prototype.

dv/dt Limitation and EMI Reduction

Power electronic designers can influence the converter's EMI performance by selecting appropriate parameters and resonant components. The voltage profile can be shaped to comply with the application's specific EMI requirements and *dv/dt* limits. Figure 3 shows that for a low-side (LS) to high-side (HS) transition.

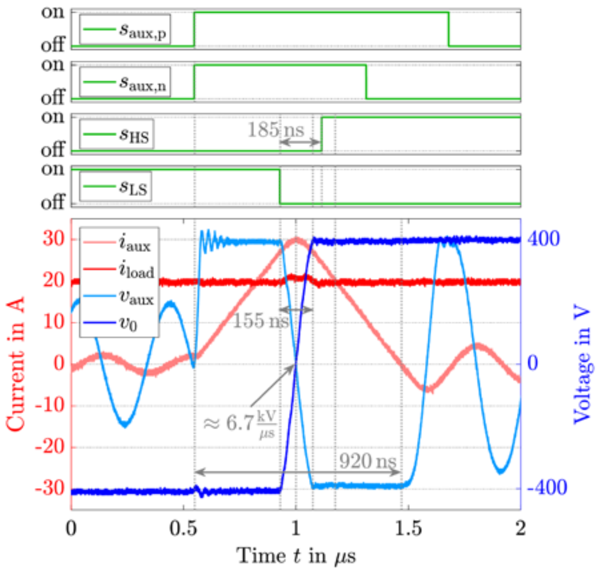

Figure 3: Switching transition waveforms.

Immediately before the switching event determined by the PWM modulation, both auxiliary switches are turned-on at zero current (ZCS), which builds up a current in the auxiliary inductor that drives the resonant transition. Once the low-side switch turns off, L_{aux} resonates with C_{sn}, initiating the charging and discharging of the main switch output capacitances. The voltage across the high-side switch gradually swings down to zero in a slow, smooth, and sinusoidal manner until the conduction condition of the antiparallel diode is met. As soon as the high-side transistor's antiparallel diode conducts, the HS transistor can be turned-on at zero voltage (ZVS), significantly reducing switching losses.

The choice of resonant parameters (L_{aux} and C_{sn}) determines the commutation time, allowing for precise tuning of the maximum *dv/dt* without sacrificing efficiency. The maximum dv/dt for this design is limited to just 6.7 kV/µs, which already meets most common industry requirements.

Efficiency and Power Losses

Figure 4 shows the inverter's measured efficiency plotted against the output power, indicating values that exceed 99.6% across a wide load range - including part-load conditions, where switching losses usually dominate total losses. This level of efficiency allows for the omission of forced air/water cooling within that power range. Further studies [3] have demonstrated a total loss reduction of about 50% compared to a conventional hard-switched B6-bridge, along with the ability to significantly increase the switching frequency under identical cooling conditions.

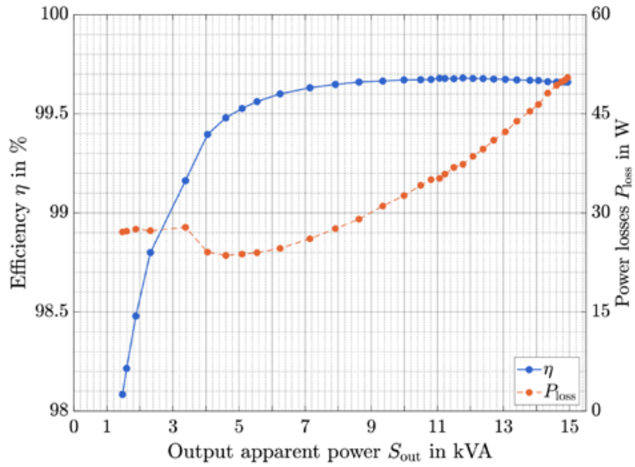

Figure 4: Efficiency and total power losses for different loads.

By raising the switching frequency, the waveform quality of output voltage and current improves, which in turn reduces harmonic losses in a motor powered by the inverter and allows for a smaller capacitor size in the DC-link.

In soft-switching mode with SiC MOSFETs, switching losses can be decreased by up to 90% [3]. The remaining switching losses primarily occur during turn-off, mainly influenced by how quickly the MOS channel closes before the drain-source voltage rises (the V–I overlap). The speed of this turn-off transition depends on the transistor parameters and gate driver characteristics.

Why should you choose Sanan Semiconductor?

Sanan's transistor portfolio is characterized by its exceptionally low internal gate resistance $R_{g,int}$ - down to 0.9 Ω, and carefully optimized input and output capacitances C_{iss}/C_{oss}. This synergy facilitates ultra-fast channel closure and a gentle voltage rise, minimizing the crucial V–I overlap during turn-off. The result is remarkably low switching losses in ZVS operation, providing unmatched efficiency and performance not only in hard-switched but also in soft-switched applications.

What are the Target Applications?

An interesting application for this topology would be the automotive traction inverter. Many automotive manufacturers already employ wide-bandgap semiconductors in their EV drive inverters. However, they often cannot fully utilize their high switching speeds due to system (e.g., motor winding) limitations, resulting in higher power losses and increased cooling requirements. Thanks to soft switching, this topology can decouple switching losses from dv/dt slew rates, thereby reaching up to 90% lower switching losses, under the same switching slew-rate conditions, enabling higher efficiencies, and consequently lower size and volumes.

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Is SPICE Modeling easier the second time around?

After copying the required curve data into the Model Generator, click "Done" and it performs the calculations and produces a finished QSPICE® model for the component. However, getting SPICE models right for power circuit simulation, it appears, is not as simple as it seems.

By Siddharth Mohan, senior design engineer at Qorvo

The task of creating models presents numerous challenges for both discrete components and ICs, particularly when working with legacy SPICE software. With discrete components, SPICE doesn't have built-in device equations for many common discrete components. For ICs, most current modeling methods are cumbersome and time consuming. The issue is that SPICE was originally intended for IC design and didn't plan specifically for using discrete components in circuit simulations.

Discrete Component Modeling

When conceiving and writing Qorvo's QSPICE®, Mike Engelhardt, who also wrote LTspice®, made multiple improvements with respect to simulating discrete components such as MOSFETs, JFETs and diodes. One of his central goals in creating QSPICE was to devise new device equations for these parts that match their performance much more precisely than those in other SPICE software. He also extended the built-in device equations in QSPICE for wide bandgap GaN and SiC MOSFETs and JFETs.

Since SPICE, as originally developed didn't include accurate device equations for these parts, modeling challenges emerged. "For example, consider the normal power MOSFET," Mike Engelhardt noted. "The channel is very short – less than a micron, just like in an IC, but the width of the channel can be a meter wide in order to handle the potentially many amps of current of a power converter."

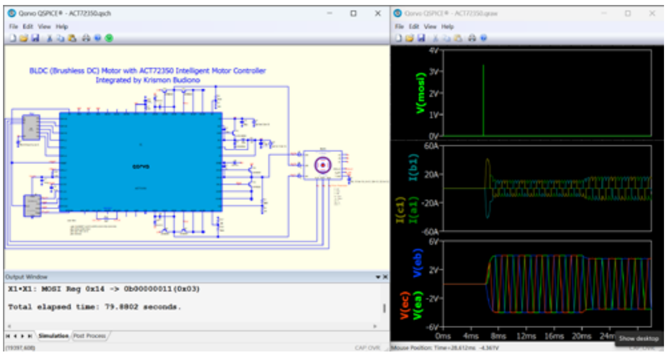

Figure 1: This simulation illustrates the ability of QSPICE users to create models for complex parts in C++ to enable the simulation of highly complex circuits, such as this brushless DC motor (BLDC) example.

That's still a small area that fits on a typical die size. The device equations of the channel are well described by the normal SPICE MOSFET device equations for the monolithic MOSFETs of ICs, but the capacitance between the gate and drain behaves very differently than a monolithic MOSFET. In the monolithic MOSFET, the gate and drain are adjacent.

With MOSFETs in ICs, the channel is beneath the gate and doesn't have a strong impact on the gate-drain capacitance. But the conventional discrete power MOSFET is a vertical device – the gate and drain are opposite each other and form a parallel plate capacitor with the channel between the plates, Mike Engelhardt explained. "For discrete MOSFETs, the channel's conductivity has a strong impact on the gate-drain capacitance. It's common for a power MOSFET's gate-drain capacitance to vary by a factor of five depending on whether the channel is conducting or not. Since this gate-drain capacitance is the Miller capacitance, you can't present the switching behavior of a normal power MOSFET in SPICE with the built-in device equations. That's the problem."

In principle, there would be two ways of solving this problem, he said. One way would be to use the behavioral modeling capability of SPICE to implement new device equations, but this results in wildly complicated models that go on for pages. "The dark side of me finds these models amusing, the mature side of me finds them sad," Mike Engelhardt continued. "It's like someone has an axe to grind because they were rejected from Mensa and wanted to make MOSFET models so complicated no one else can understand or use them." Such models often crash a SPICE program. "Whereas SPICE can solve a circuit with very many thousands of transistors, it can have trouble trying to solve a circuit with a single such MOSFET modeled in this method. Promoting such a model shows a fairly perfect ignorance of circuit simulation."

The other way to solve this problem, according to Engelhardt, is to extend the device equations in SPICE itself to manage this non-linear capacitance. "That's what we've done in QSPICE, which natively handles this non-linear charge. The advantage is that it al-

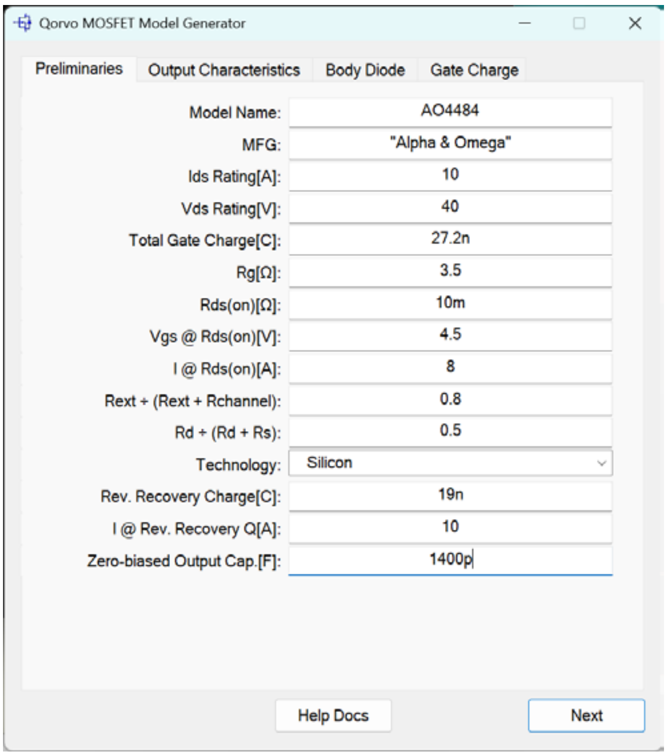

Figure 2: The first step to use the QSPICE Model Generator to create a SPICE model is to plug in basic parameter information from the part's datasheet.

lows accurate simulation of common power MOSFETs with the robustness required to simulate as many as you want in the same simulation." The way SPICE has implemented diode modeling has also been flawed. "For example, consider diode reverse recovery due to charge storage of diffusion capacitance. The standard SPICE equations are for a snap diode. A snap diode is a very useful thing. Given a forward current, there is an amount of charge you have to pull out before the diode turns off. This charge to pull out is proportional to the forward current."

"Since time multiplied by current is charge, the constant of proportionality has the units of time. This constant of proportionality is the diode model parameter TT, the transient time," Engelhardt said. "Anyway, a snap diode abruptly goes from conducting to non-conducting in reverse recovery. With an inductance, you can create an extremely short pulse, like going from zero to a few volts and back in maybe 100 picoseconds. It's used in particle beam blanking." But a major SPICE issue for diodes is that most of them aren't snap diodes, even though every diode in SPICE is a snap diode. "So again, you have to modify the device equations in SPICE to get a diode in simulation to behave as it does in reality."

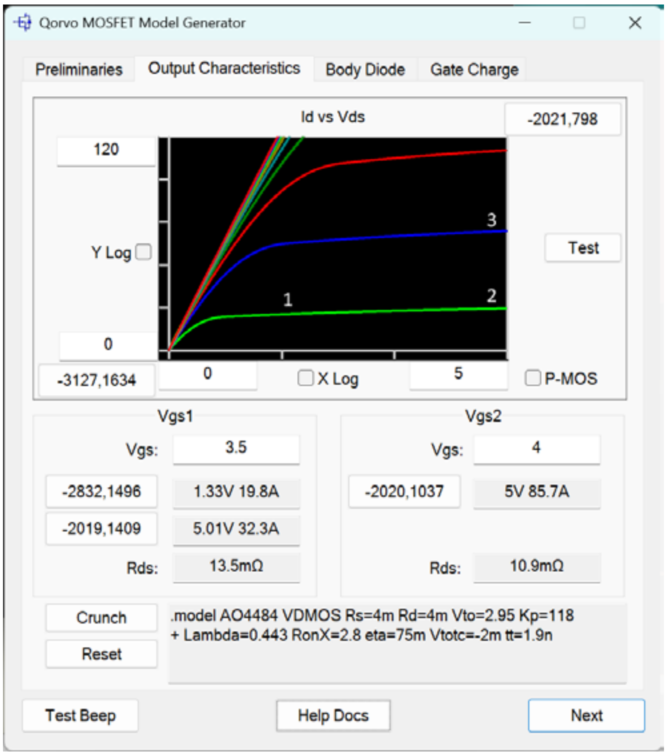

Figure 3: The next step to use the Model Generator is to digitize datasheet curves, in this example starting with the I_d vs V_{DS} curves.

JFETs, the red-headed stepchildren of the electronic components world, have always had SPICE issues. "JFETs were never really properly implemented in SPICE," Engelhardt observed. "In reality, they have a very pronounced quasi-saturation region. Some JFETs go into saturation with a drain source voltage that does not depend on the gate source voltage."

Historically, no one seemed to care because the production scatter is accepted to be so large, the models for JFETs didn't make much difference in designs, Engelhardt noted. But QSPICE contains much-improved JFET device equations, and the tool for making discrete JFET models describes much more accurately the performance of these parts in circuits.

The key to improving the model-making process is having a fundamental understanding of the capabilities and limitations of SPICE. Though components such as MOSFETs and JFETs were included in SPICE from the beginning, it was from the perspective of them being within an IC, not as discrete parts. "SPICE has built-in device equations for the devices one can print on an IC," Mike Engelhardt said. "These are abstract, parameterized, equations. SPICE modeling comes down to supplying values for these parameters for a specific instance of a device, and this system works very well for IC design, even for circuits with many thousands of transistors."

When re-thinking his approach to SPICE while writing QSPICE, Engelhardt started from scratch and addressed some limitations he found while making models for Linear Technology parts. "People know I also wrote LTspice, but what people usually don't know is I had also made the majority of the IC models in LTspice." Based on his work creating thousands of LTspice models, Engelhardt made it a priority in QSPICE for designers to be able to build models faster and easier: "Making those mixed signal simulation models was non-trivial. With QSPICE, I solved that problem. One can make detailed models of mixed-signal ICs with minimal effort."

IC Model Making

The QSPICE embedded library contains a range of model examples useful for creating both simple and complex power ICs. Figure 1 shows a highly complex power management part, the Qorvo ACT72350, modeled in QSPICE using C++.

The C++ used in these examples is fully accessible, which helps designers understand how to create their own models. One example is called PracticalSMPS, in the QSPICE release under File=>Open Demo...=>PracticalSMPS. "It was inspired by an MPS (Monolithic Power Systems) constant on time product," Engelhardt said. "It only takes a day to make a model like that, and all the behavior is there, including all fault handling. There are also a couple classic Unitrode parts in the release in their up-to-date form from TI." These models are implemented as hierarchical designs so users can look inside and see the proper way to create such models. "You'll also see some Qorvo devices, and these are literal models of their respective products. Even the SPI and I²C registers are implemented." He added that if designers want to include SPI or I²C in their own models, it's quite easy. "There are APIs for both," he said. "It only takes a few lines of C++ to add them."

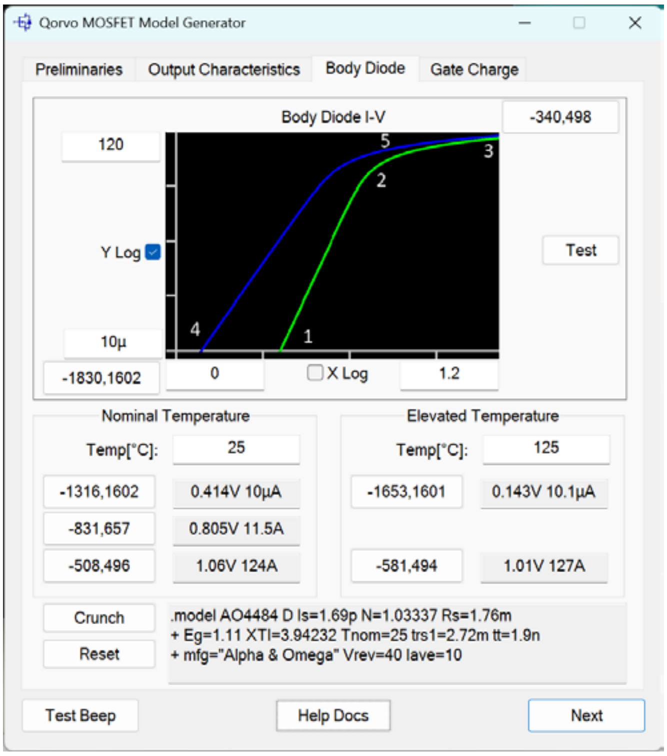

Figure 4: Users can add the curve data using cursor click technique shown in the "Learn How to Create QSPICE Models in Minutes" video referenced in the article.

Using the Model Generator

A key part of QSPICE's model-friendly environment is a tool Engelhardt developed that enables users to make their own discrete component models using information typically found on datasheets. This tool is found in QSPICE under File=>Model Generator… =>Diode or JFET or MOSFET. The Model Generator automates the process of using complex mathematics to transform this data into a SPICE model, cutting the time to make a model from potentially a dozen hours to perhaps a dozen minutes. For more information on modeling discrete MOSFETs, JFETs and diodes in QSPICE, please visit: https://www.qorvo.com/design-hub/videos/learn-how-to-create-qspice-models-in-minutes

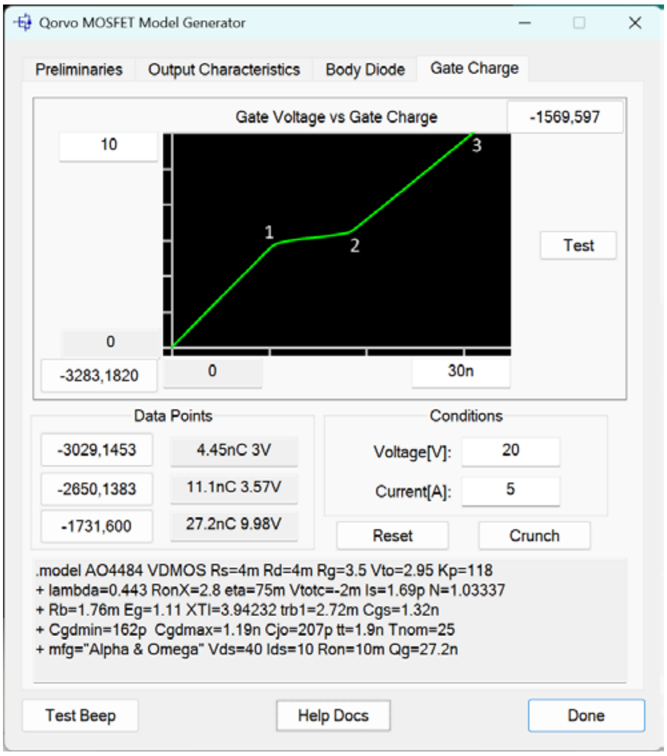

Figure 5: After copying the required curve data into the Model Generator, click "Done" and it performs the calculations and produces a finished QSPICE model for the component

Creating discrete component SPICE models previously required in-depth knowledge of the physics of electrical component design and the ability to derive parameters using complex mathematical equations. Bob Cordell, a well-regarded circuit design expert, devotes over 30 equation-filled pages to basic SPICE model creation in his recent book, "Designing Audio Circuits and Systems." An experienced SPICE model engineer might spend a dozen or more hours creating a single model, in addition to time spent collecting data.

In this example, the QSPICE generator is creating for the model for the Alpha & Omega Semiconductor AO4484. Users would put basic datasheet information into fields, as shown in Figure 2, to start the model generation process for a particular part. They would then copy curves on the datasheet, Figures 3, 4 and 5, into the QSPICE model generator. The Model Generator performs the calculations and produces a finished QSPICE model for the component:

```
.model AO4484 VDMOS Rs=4m Rd=4m Rg=3.5 Vto=2.95 Kp=118
+ lambda=0.443 RonX=2.8 eta=75m Vtotc=-2m Is=1.69p N=1.03337
+ Rb=1.76m Eg=1.11 XTI=3.94232 trb1=2.72m Cgs=1.32n
+ Cgdmin=162p  Cgdmax=1.19n Cjo=207p tt=1.9n Tnom=25
+ mfg="Alpha & Omega" Vds=40 Ids=10 Ron=10m Qg=27.2n
```

Conclusion:

QSPICE has features that simplify the creation of SPICE models for discrete components and ICs while emulating the performance of the parts in circuits more accurately. Fundamental issues with Berkley SPICE and discrete devices are solved in QSPICE through the use of improved device equations. Modeling of complex ICs is made significantly easier through the use of an advanced C++ process. And the addition of a discrete component model generation tool makes the creation of MOSFET, JFET and diode models vastly easier than with other SPICE software.

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Experience the Future of Power Conversion in Home Appliances with Hybrid SiC SLIMDIP and Full SiC SLIMDIP

Increasing environmental concerns as well as cost of energy make reduction of power consumption a critical challenge. Consequently, demand for high-efficiency power semiconductor devices in consumer applications is rising rapidly. To meet these requirements, Mitsubishi Electric has developed two new SLIMDIP IPM one of which is Hybrid SiC SLIMDIP and the other being Full SiC SLIMDIP.

By Keisuke Kawamoto and Dr. Mustafa Cem Ozkilic, Mitsubishi Electric Europe B.V., Germany and Akiko Goto, Mitsubishi Electric Corporation, Japan

Introduction

Mitsubishi Electric DIPIPM concept, that integrates power semiconductors (3 phase inverter stage with IGBT and FWD), LVIC and HVIC gate drivers with protection logic circuits for cost-effective inverter application, was first introduced to the market back in 1997 [1]. Several different type of Mitsubishi Electric DIPIPM Families with 600V and 1200V rating for various output current ratings and additional topologies have been introduced since then [2]. Among these DIPIPM Families, SLIMDIP with 600V RC-IGBT technology, which was released in 2015, has become a sought after DIPIPM for home appliances and low power industrial drives applications [3,4].

Power consumption reduction has become an important topic in recent years, hence energy-efficient solutions are increasingly required in consumer applications. To address the demand for higher efficiency Mitsubishi Electric has developed two new types of SLIMDIP Series, one of which contains Hybrid structure with SiC MOSFET and RC-IGBT whereas the other contains Full SiC MOSFET structure, both in SLIMDIP Package with 15A/600V ratings.

Concept of Full SiC SLIMDIP and Hybrid SiC SLIMDIP

Full SiC SLIMDIP (PSF15SG1G6) contains the latest state-of-the-art Mitsubishi Electric SiC MOSFET chip technology whereas Hybrid SiC SLIMDIP (PSH15SG1G6) consists of Mitsubishi Electric RC-IGBT chips (IGBTs and FWDs on a single chip) and the latest state-of-the-art Mitsubishi Electric SiC MOSFET chips placed in parallel at each switch position which are driven by state-of-the-art driver ICs having been implemented with protection functions in a transfer molded structure [5-7].

Within Hybrid SiC SLIMDIP, a small MOSFET chip is placed in parallel with each RC-IGBT chip so that SiC MOSFET could enhance the conduction loss performance by reducing the on-state voltage drop at each switch position. By optimizing the SiC MOSFET size and the gate drive for each device, the MOSFET area is minimized, enabling integration into a package 30% smaller than that of a conventional Si SJ-MOSFET and Si IGBT solutions. Moreover, the low on-state voltage of the SiC MOSFET allows the use of the Si RC-IGBT with reduced switching losses (Figure 1).

Drive and package compatibility of Full SiC SLIMDIP and Hybrid SiC SLIMDIP, with conventional SLIMDIP consisting of RC-IGBT chips only, have been achieved by: i. adjusting the VGS(Vth) of the SiC MOSFET chips suitable to be driven by single 15 V control power supply, ii. adapting same pin arrangement and protection functions in SLIMDIP package.

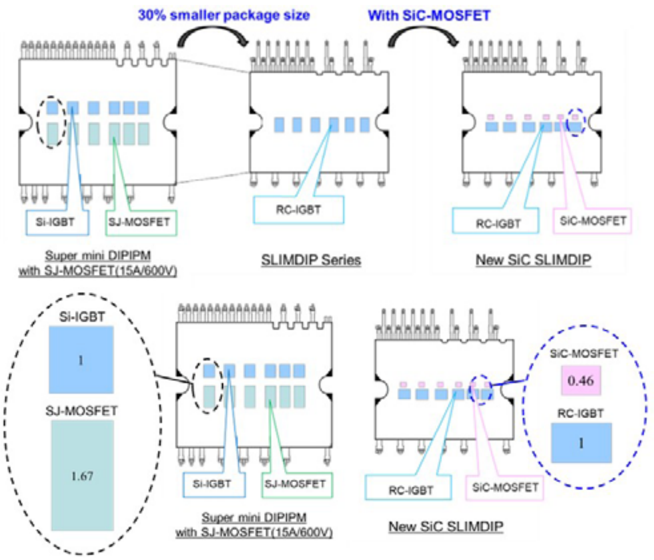

Figure 1: Package comparison of Super Mini DIPIPM with SJ-MOSFET, conventional SLIMDIP, and Hybrid SiC SLIMDIP

New Gate Drive with Delay Control for Hybrid SiC SLIMDIP

When driving parallel-connected SiC MOSFET chips and RC-IGBT chips using conventional drive circuits, there are concerns about hard switching and current concentration on the SiC MOSFET, as the SiC MOSFET chips may turn on before the RC-IGBT chips. Therefore, a new state-of the-art drive IC was developed for Hybrid SiC SLIMDIP adapting sequential control of the gate drive signals by implementing a time delay between the gate drive pulses which are applied to each of the RC-IGBT chip and the SiC MOSFET chip (Figure 2).

The delay control avoids any hard switching operations of the SiC MOSFET chip during turn-on and turn-off states so that the switching losses of the SiC MOSFET chip is prevented, leading to soft switching. Hence, SiC MOSFET chip generates only DC loss and are allowed to be minimized down to the required size.

Static Characteristics of Hybrid SiC SLIMDIP

The Static characteristic of a power stage, impacting the DC losses, can be significantly enhanced by operating an RC-IGBT chip and a SiC MOSFET chip in parallel. As shown in Figure 3., Hybrid SiC SLIMDIP static characteristic in low current region below the built-in

potential of the RC-IGBT is dominated by SiC MOSFET chip portion whereas in the current region above the built-in potential of the RC-IGBT is dominated by combination of static characteristic of both the RC-IGBT chip and the SiC MOSFET chip. Inverters for consumer and pump applications often operate at steady low-load operation for extended periods hence the new enhanced static characteristic across the entire current region of Hybrid SiC SLIMDIP can meet the market demand, providing higher efficiency particularly at steady low-load operation.

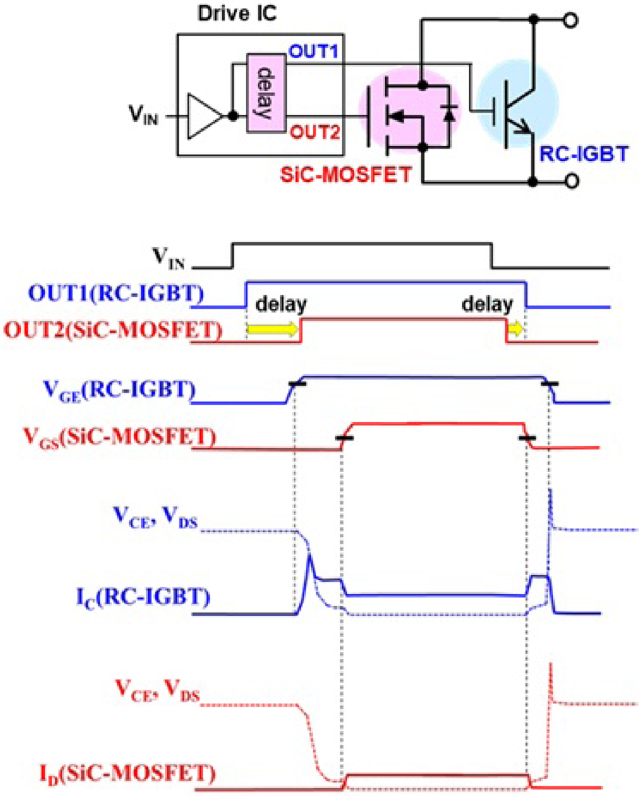

Figure 2: Developed drive circuit and timing chart

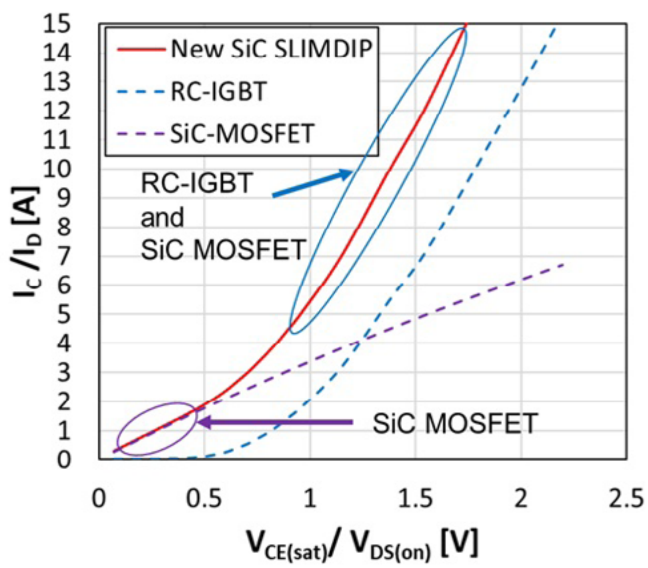

Figure 3: Static characteristics of Hybrid SiC SLIMDIP (Condition: V_D=15 V, T_j=125°C)

Static Characteristics and Switching Characteristics of Full SiC SLIMDIP

Static Characteristics

In Figure 4a forward and in Figure 4b reverse conduction characteristics of 15A/600V Full SiC SLIMDIP and 15A/600V RC-IGBT utilized conventional SLIMDIP are shown. As can be seen, static characteristics of Full SiC SLIMDIP are improved over the entire current range compared with that of RC-IGBT utilized conventional SLIMDIP Series.

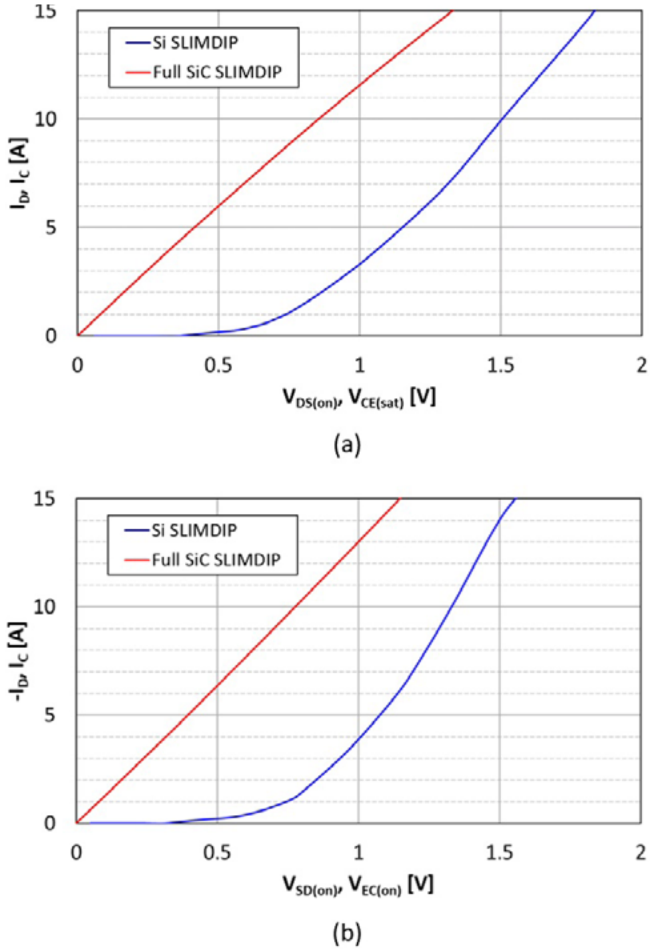

Figure 4: a) Forward static characteristic, b) Reverse static characteristic of Full SiC SLIMDIP and RC-IGBT SLIMDIP (Condition: V_D=15 V, T_{ch}/T_j=125°C, Si SLIMDIP: SLIMDIP-L)

Full SiC SLIMDIP and RC-IGBT SLIMDIP turn-on and turn-off waveforms are shown in Figure 5a, Figure 5b, and Figure 5c respectively. As expected, Full SiC SLIMDIP has lower recovery and turn-on losses compared with that of RC-IGBT SLIMDIP. On the other hand, since SiC MOSFET has the minority carrier structure, no tail current occurs during turn-off so that turn-off losses could be improved as well. As illustrated in Figure 4c, improvement of switching characteristic of Full SiC SLIMDIP can be seen in the entire current region compared with that of RC-IGBT SLIMDIP.

Power Loss Comparison of SLIMDIP Series

Carrier Frequency vs. Allowable Output Current

Figure 6 shows the characteristics of the effective output current of I_o vs. the carrier frequency under the condition that the average operating junction temperature T_j of the power chips remain below 125°C for safe operation whilst the heat sink temperature T_f is at 100°C.

The applications, where DIPIPM are used could vary widely, thus the applied carrier frequencies during operation could range from several kHz up to 20 kHz. As shown in Figure 6, Full SiC SLIMDIP, with overall reduced power losses, does not only allow larger out-


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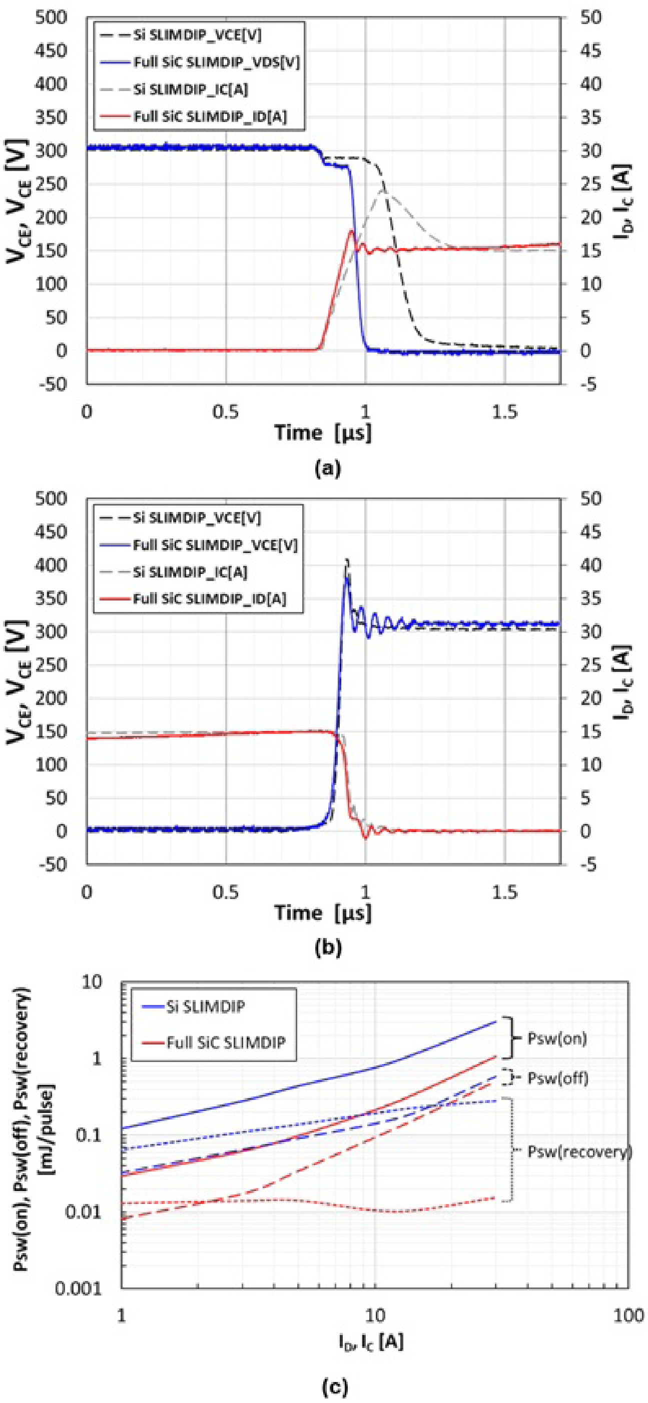
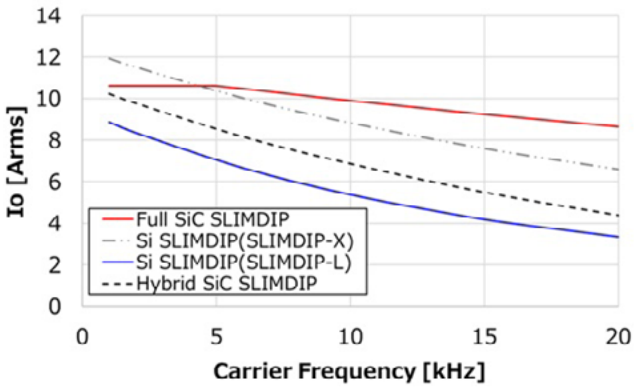


Figure 5: a) Turn-on switching waveforms, b) Turn-off switching wave-forms, c) Switching Characteristics of Full SiC SLIMDIP and RC-IGBT SLIMDIP (Condition: V_{DD}/V_{CC}=300 V, V_D=15 V, V_{IN}=0↔5 V, Inductive Load, T_{ch}/T_j=125°C, Si SLIMDIP: SLIMDIP-L)



put current for the full range of carrier frequencies compared with that of SLIMDIP-L (Si SLIMDIP) but also allow larger output current at high carrier frequencies compared with that of SLIMDIP-X (Si SLIMDIP) (600V / 20A), having equipped with a higher rated current Si RC-IGBT.

Hybrid SiC SLIMDIP

Figure 7 demonstrates the loss comparison between conventional RC-IGBT based SLIMDIP types, namely SLIMDIP-L and SLIMDIP-W, with Hybrid SiC SLIMDIP at steady low-load operation. Based on these results, utilization of Hybrid SiC SLIMDIP has reduced total losses by 47% and 40% compared with that of SLIMDIP-L and SLIM-DIP-W respectively.

Since Hybrid SiC SLIMDIP shares DC losses between the RC-IGBT chip and the SiC MOSFET chip the losses generated within the RC-IGBT chip as well as the junction temperature could be reduced compared with those of conventional SLIMDIP. Hence, Hybrid SiC SLIMDIP can increase the output current capability of an inverter stage further or have lower junction temperature levels at the same output current level compared with those of conventional SLIMDIP. As illustrated in Figure 8 the junction to case temperature difference ($\Delta T_{j\text{-}c}$) of Hybrid SiC SLIMDIP can be reduced by 34 % (approximately 8 K) at an inverter output current (I_O) of 7.5 A_{rms}.

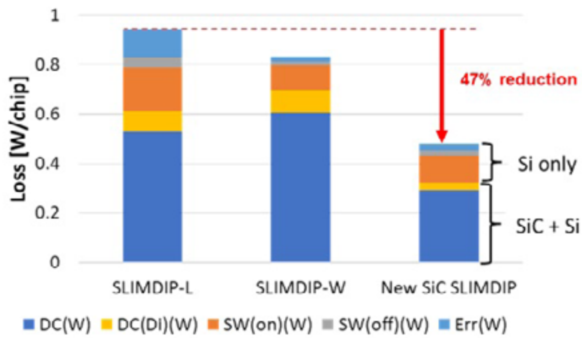


Figure 7: Loss simulation result comparison (Conditions: 2 phase modulation, VCC=300 V, I_O=1.5 Arms, VD=15 V, fc=5 kHz, PF=0.8, M=1.1547)

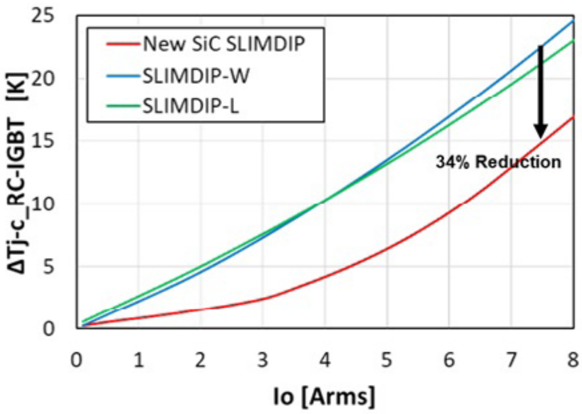


Figure 8: Junction temperature rise comparison between SLIMDIP-L, SLIMDIP-W and Hybrid SiC SLIMDIP (Conditions: 2 phase modulation, V_{CC}=300 V, I_O=7.5 Arms, V_D=15 V, f_c=5 kHz, P_F=0.8, M=1.1547)

Figure 6: Effective Current vs. Carrier Frequency Characteristics (Conditions: Sinusoidal PWM, V_{DD}/V_{CC}=300 V, V_D=15 V, M = 1, PF=0.8, T_{ch}/T_j=125°C, T_f=100°C, $R_{th(c\text{-}f)}$=0.3K/W(1/6 module), $R_{th(j\text{-}c)}$=Max value(1/6 module)

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Full SiC SLIMDIP

Full SiC SLIMDIP has the efficiency advantage over both steady low-load and full load range. To illustrate this efficiency advantage and loss reduction, two distinct applications focusing on distinct operating conditions have been considered and related loss calculations have been.

The first application focused on is the air conditioner example where low output current and low switching frequency are the dominant operation characteristics for the entire operation life of the power module. As can be seen in Figure 9, Hybrid SiC SLIMDIP provides up to 40% of loss reduction whereas Full SiC SLIMDIP provides up to 82% of loss reduction compared with the overall losses of RC-IGBT SLIMDIP.

The second application focused on is the washing machine example in which high output current and high switching frequency are the dominant operation characteristics for the entire operation life of the power module. As can be seen in Figure 10, Hybrid SiC SLIMDIP provides up to 25% of loss reduction whereas Full SiC SLIMDIP provides up to 65% of loss reduction compared with the overall losses of RC-IGBT SLIMDIP.

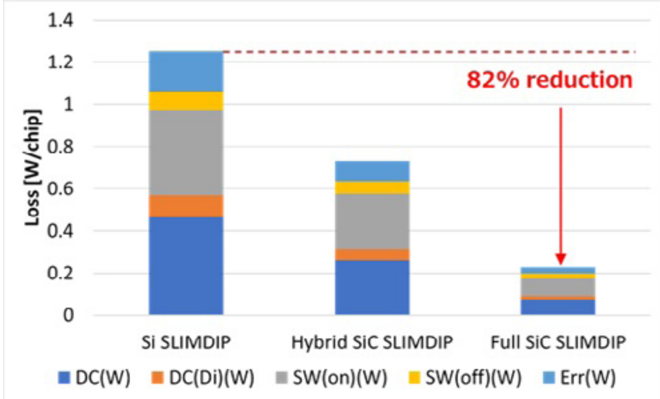

Figure 9: Loss Simulation Result for Air Conditioner (Conditions: Sinusoidal, V_{DD}/V_{CC}=300 V, I_O=1.5 Arms, V_D=15 V, f_c=5 kHz, P_F=0.8, M=1, T_{ch}/T_j=125°C, Si SLIMDIP: SLIMDIP-L)

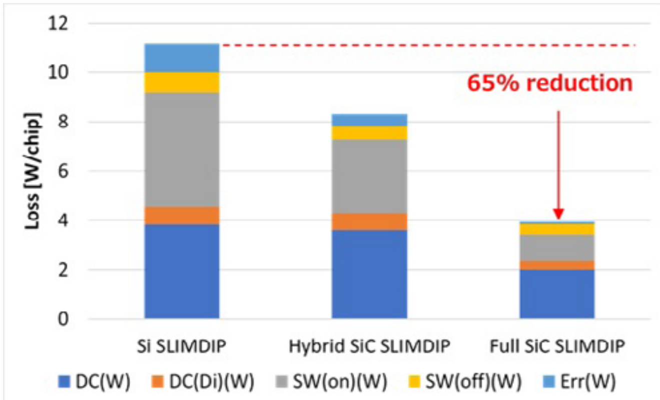

Figure 10: Loss Simulation Result for Washing Machine (Conditions: Sinusoidal, V_{DD}/V_{CC}=300 V, I_O=7.5 Arms, V_D=15 V, f_c=15 kHz, P_F=0.8, M=1, T_{ch}/T_j=125°C, Si SLIMDIP: SLIMDIP-L)

Conclusion

SLIMDIP with 600V RC-IGBT technology has become a sought after DIPIPM for whitegoods and low power industrial drives applications. Mitsubishi Electric has developed Hybrid SiC SLIMDIP, especially for steady low-load efficiency, and Full SiC SLIMDIP, steady low-load and full load efficiency, to address increasing efficiency requirements in home appliances and industrial drive applications.

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Formic Acid Soldering – Enabling the Next Generation of Power Devices (Part 1)

Reflow soldering traditionally meant using flux, and subsequently, dealing with flux residues post-reflow. By employing a fluxless reflow process using formic acid vapor, flux residues are eliminated, processes are streamlined, and device performance is optimized, making this a viable reflow strategy for the next generation of power devices.

By Joseph Hertline, Product Manager for Engineered Solder Materials, Indium Corporation

As power devices evolve for applications in electric vehicles, renewable energy, AI servers, and advanced industrial systems, packaging material selection is a critical factor to achieve design targets for performance and reliability. Soldering remains the most widely used interconnect method for die attach, top-side die connections, and large-area joints such as substrate-to-baseplate. A broad range of alloys and configurations makes soldering versatile, but the reflow method can significantly impact feasibility, cost of ownership, and performance.

Why Formic Acid Soldering?

The fundamental objective of soldering in power device packaging is to form a thermomechanical bond between metallized assembly components, which is achieved by wetting the solder alloy to the base metals. Traditional soldering relies on flux – delivered with a solder paste, pre-applied on a preform, or separately dispensed – to reduce surface oxides and promote wetting. While traditional soldering is effective, the use of flux can create challenges, such as flux residue causing electromigration, especially considering power device design trends toward high voltage. While cleaning can mitigate risk, it increases process steps, equipment needs, and consumables in production.

Formic acid (HCOOH) soldering is a technique that introduces formic acid vapor in to the reflow oven/chamber, creating a reducing atmosphere that effectively removes surface oxides and promotes good solder wettability without a flux. When activated in nitrogen-rich atmospheres at about 180–250°C, formic acid decomposes into reactive species that reduce surface oxides, leaving behind metal surfaces. Byproducts such as CO_2 and H_2O are easily removed via vacuum. The result is an oxide-free, clean joint that requires no post-reflow cleaning.

Reaction Mechanism:

a) *2HCOOH + Metal Oxide (MeO) → Me(COOH)$_2$ + H$_2$O*

b) *Me(COOH)$_2$ → "Clean" Metal + 2CO$_2$ + H$_2$*

Figure 1: Reaction mechanism when using formic acid.

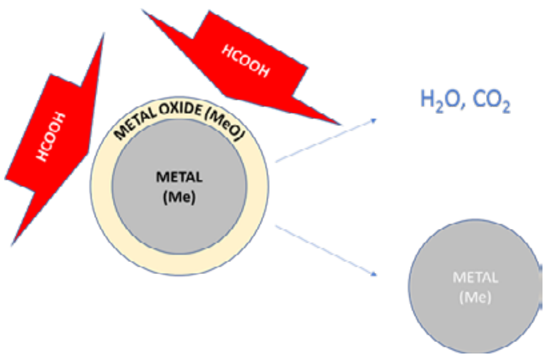

Figure 2: Formic acid (HCOOH) reaction with metal oxide.

Formic acid soldering has seen growing adoption in power electronics applications where reliability, thermal efficiency, and high yields are critical. There are multiple advantages to eliminating flux in the material and process flow:

- **Improved cleanliness:** Eliminate residues that compromise reliability in high-voltage designs or interact poorly with encapsulants.
- **Reduced voiding:** With vacuum, <1% voiding is achieved—an order of magnitude lower than flux-based soldering—delivering superior thermal conductivity and lower resistance.
- **Streamlined process:** Removes the need for cleaning, reducing cycle time, equipment, and factory footprint.
- **Environmental benefit:** Cuts energy and waste associated with solvent cleaning.

For Design Engineers, this means fewer trade-offs: robust joint integrity, solid thermal performance, high reliability, and simplified process flow to scale and meet next generation power device requirements.

Adoption Across Industries

Formic acid soldering has already moved beyond the lab and into high-volume production in industries like semiconductor packaging, LED manufacturing, power electronics, and high-performance computing. Semiconductor packaging like wafer bumping, flip-chip, and SiC/GaN modules remains a stronghold due to cleanliness and fine-pitch requirements. LED manufacturing benefits from void-free bonds for efficient thermal dissipation, which is critical in high-power lighting. In power electronics and power modules, leading players in the industry employ formic acid soldering for substrate-baseplate attach today, while adoption is growing for die-level and package-cooler applications. High-performance computing and AI systems are emerging adopters, leveraging ultra-low voiding and cleanliness to improve thermal management in advanced packaging.

It's clear that formic acid reflow is a mainstream soldering technique, and with continued adoption comes a growing knowledge base of best practices for materials selection and process design.

Key Design Considerations

On the materials side, fluxless solder preforms are the standard. Solder preforms are engineered parts consisting of a solder alloy and can be fabricated in a wide variety of sizes and shapes through precision manufacturing for consistent solder volume. While a formic acid atmosphere is highly effective at removing surface oxidation to promote wetting, it does not react with organics or other potential impurities that can inhibit solderability. Therefore, residue-free materials, a high degree of surface cleanliness, and high-purity alloy compositions are must-haves for design engineers when adopting a solder preform approach.

Additional materials technologies are emerging, including tacking agents and solder pastes designed specifically for formic acid reflow processes. In this case, application of the material is done via stencil printing or dispensing, therefore material rheology and application suitability are critical attributes. The elimination of post-reflow residues is the key innovation driving the design of these materials, where the typical residue-forming components in fluxes such as rosins, activators, and other additives are replaced by solvents that evaporate during reflow. Metrics such as thermogravimetric analysis confirm that these emerging materials technologies leave virtually zero residue after reflow, giving engineers confidence in downstream processes like wire bonding and encapsulation.

Reflow Process Considerations

Not all reflow systems are capable of soldering with formic acid. Conventional convection ovens may be retrofitted in limited cases, but purpose-built formic acid/vacuum systems are the norm.

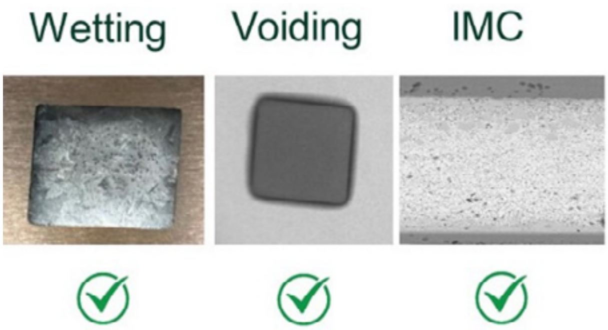

Figure 3: Typical solder joint quality with formic acid/vacuum soldering.

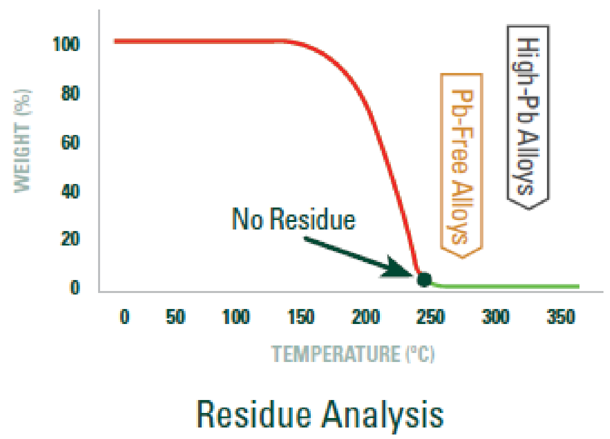

Figure 4: Thermogravimetric analysis (TGA) for fluxless tacking agent.

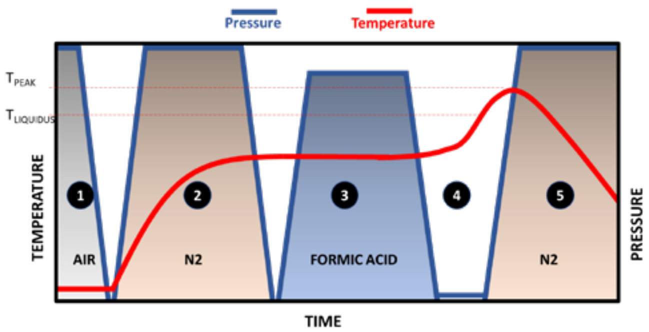

Figure 5: Typical formic acid soldering profile: temperature, gas-exchange, and vacuum.
Phase 1: oxygen removal. Phase 2: preheat under low oxygen.
Phase 3: soak under formic acid for oxide removal at 180-250°C.
Phase 4: reflow and vacuum for void removal.
Phase 5: cooling/solidification.

Vendors such as PINK, budatec, Heller Industries, Centrotherm, ATV Technology, STT Vacuum Reflow Systems (Palomar® Technologies), 3S Silicon Tech, HVT, and others, provide formic acid-capable systems. Heating methods vary between conduction, convection, induction, or IR. Oven designs can be set up for batch processing or in-line processing, therefore equipment capabilities and throughput requirements are key considerations.

While basic parameters including temperature, ramp, and time above liquidus are still relevant with formic acid soldering, precision control over the reducing environment is important for success. Parameters such as formic acid concentration (typically 3–15 % in nitrogen), flow rate, soak temperature, and exposure time must be optimized. Key phases in a typical process are shown in figure 5; these key phases include oxygen removal, preheating under low oxygen, soaking under formic acid for oxide removal (180-250°C), reflow and vacuum for void removal, and cooling/solidification.

Materials compatibility must also be considered: Cu, Ni, Ag-plated, and ceramic substrates each behave differently and may require adjustments to the formic acid soak parameters. However, a balance is important - excessive formic acid exposure can lead to other side effects, such as "tin steaming," a cosmetic surface phenomenon seen with heavily oxidized parts.

While precise process design is essential, the performance and cost-of-ownership advantages of eliminating flux make formic acid soldering highly compelling. In Part 2 of this article, we will explore case studies showing how material innovations expand process windows and enable its use in next-generation power device designs.

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Unlocking the Potential of Multilevel Power Conversion Topologies

Multilevel power conversion topologies have long been a subject of research, offering distinct advantages over traditional power conversion methods. These advanced systems are particularly attractive in applications such as datacenter AC/DC power supplies, where optimizing power efficiency while achieving cutting-edge power density is essential.

By Tom Spohrer, Sr. Technical Staff Engineer-Product Marketing, Microchip Technology's dsPIC Business Unit

Multi-level AC/DC converters can be more compact for a given power level because the ripple frequency will be higher, requiring smaller inductors and smaller input filters than other topologies need. Historically, the widespread adoption of multilevel topologies has been hindered by the complexities and costs associated with their control. However, recent advancements in digital signal controller (DSC) technology and sophisticated control strategies are paving the way for broader implementation, unlocking the full potential of multilevel converters, making them viable solutions in environments with stringent power demands.

This article explores the design challenges of a Flying Capacitor Multilevel (FCML) Totem-Pole Power Factor Correction (PFC) circuit. These converters employ multiple voltage levels to reduce voltage stress on each switch and enhance the quality of the output waveform. This is achieved through the use of capacitors that "fly" between different voltage levels, creating intermediate voltage steps. These capacitors play a crucial role in balancing voltage across switches and minimizing overall harmonic distortion, which can also lead to reduced electromagnetic interference (EMI). The intermediate voltage levels also allow for the use of lower voltage components, improving overall efficiency.

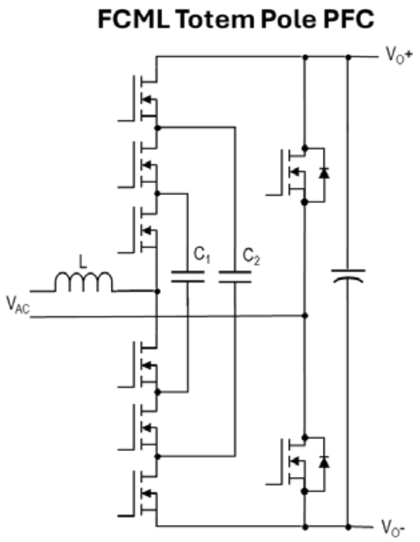

Figure 1: Switching states cause voltage drift across capacitors, demanding precise control algorithms.

As the FCML circuits operate, the various flying capacitors are charged and discharged based on the switching states at that point in time. Not all capacitors are involved equally in every switching transition, leading to unequal charge/discharge cycles and natural voltage drift that must be compensated for by the controller.

Implementing the FCML topology requires sophisticated control algorithms to manage the multiple switches, flying capacitors and

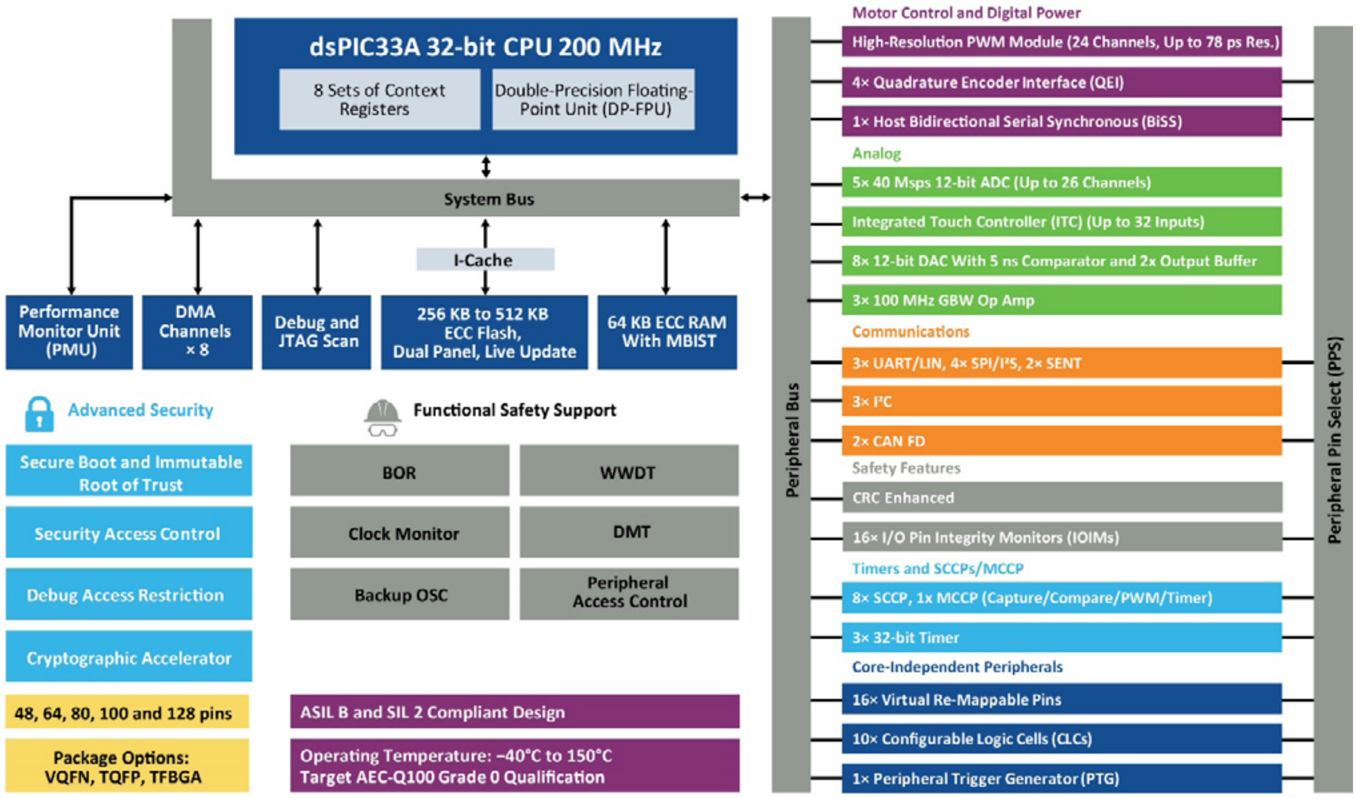

Figure 2: The dsPIC hardware and tools ecosystem streamlines FCML control algorithm development and deployment.

totem-pole configuration. These algorithms ensure proper voltage balancing, minimize harmonic distortion and maintain system stability. Advanced DSCs0), such as Microchip's dsPIC33A family, are particularly well-suited for this application. In an FCML PFC topology, the controller must accurately sample the voltages on the flying capacitors, which is crucial for maintaining voltage balance, supply stability and overall power efficiency. Imbalances can compromise performance, reduce efficiency and even damage components.

Multilevel converter topologies demand advanced control strategies to coordinate the growing number of switches and voltage levels. A key challenge is maintaining voltage balance across each flying capacitor; any imbalance can result in overvoltage conditions and potential damage to components. In an ideal (n)-level FCML circuit, the average voltage across each flying capacitor is defined by (V_c = V_{dc}/(n - 1)).

Increasing the number of levels in an FCML enhances harmonic performance by lowering total harmonic distortion (THD) and producing an output waveform that more closely resembles a pure sine wave. While efficiency can also benefit from additional levels, there is a threshold beyond which further increases introduce greater losses and system complexity, potentially diminishing overall efficiency. These losses stem from both switching events and capacitor-related factors such as leakage currents and equivalent series resistance (ESR).

As the system's complexity grows, so does the challenge of maintaining stability, particularly due to the interactions among multiple control loops. Additionally, the higher number of switches in multilevel topologies makes the management of switching losses more demanding. Effective control of these switches is therefore essential to achieving and sustaining high power efficiency in FCML systems.

Over the years, many control strategies have been developed to address these issues. Traditional methods, feedback control or redundant switching state selection, typically operate based on instantaneous measurements or simple rules. While these approaches can be effective, they may struggle to maintain precise capacitor voltage balance under rapidly changing load conditions, disturbances or in systems with significant delays and nonlinearities. They often rely on local information and do not account for the future impact of current control actions, which can lead to slower response times and less optimal performance, especially in complex multilevel topologies.

Overall, while multilevel topologies can offer many benefits such as higher power density, improved efficiency and reduced harmonic distortion, they also introduce significant challenges in control. For instance, the frequency of the system's poles based on current operating conditions often varies more with multilevel topologies than they do with traditional topologies. Implementing adaptive control strategies that adjust controller parameters in real-time based on system dynamics can help compensate for pole movement, ensuring that the system remains stable and performs as desired under all conditions.

Feed-forward control is often used in conjunction with feedback control to improve the performance and stability of FCML topologies. Feed-forward control anticipates the effect of known disturbances, such as changes in the input voltage or load conditions, and compensates for them before they affect the system output. This can improve the dynamic response of the system and it helps in maintaining stable operation and reducing transient deviations. By providing a proactive adjustment based on the input conditions, feed-forward control can enhance the overall stability of the PFC circuit. By adjusting the control signals in advance, it reduces the burden on the feedback loop and minimizes the impact of these disturbances on the output. Feed-forward control can help in achieving a near-unity power factor by adjusting the duty cycle of the switches based on the input voltage, ensuring that the input current remains in phase with the input voltage.

Another control strategy that is often used in FCML designs is redundant switching state selection. These designs inherently offer multiple switching combinations—known as redundant states—that can produce the same output voltage while affecting different capacitors. By intelligently selecting among these states, the controller can actively charge or discharge specific capacitors, thereby maintaining their voltages within the desired range. This approach is highly effective and leverages the natural redundancy of the FCML topology.

Predictive and model-based control techniques, such as Model Predictive Control (MPC) or Finite Control Set MPC (FCS-MPC), have also gained traction. These methods use mathematical models of the converter to predict future capacitor voltages and optimize switching actions accordingly, rather than simply reacting to present or past errors. By minimizing a cost function that includes capacitor voltage deviation, predictive control can deliver excellent performance, especially under dynamic operating conditions.

In contrast, MPC uses a mathematical model of the FCML to predict the evolution of capacitor voltages and other system states over a defined future time horizon. At each control step, MPC evaluates multiple possible switching sequences and selects the one that minimizes a cost function—typically incorporating capacitor voltage deviations, switching losses and output quality. This predictive approach enables the controller to proactively manage capacitor voltages, ensuring they remain balanced even in the presence of disturbances or dynamic operating conditions.

The dsPIC® family of DSCs has emerged as a leading platform for implementing Flying Capacitor Multilevel (FCML) Totem-Pole Power Factor Correction (PFC) topologies, owing to its combination of high-performance processing, advanced analog integration and flexible control peripherals. Notably, the dsPIC33A series features high-speed, low-latency analog-to-digital converters (ADCs) that enable precise, real-time sampling of flying capacitor voltages. This is an essential requirement for maintaining voltage balance, supply stability and optimal power efficiency in FCML systems. With 12-bit ADCs capable of 40 million samples per second throughput, these controllers provide the rapid, accurate measurements necessary for advanced control algorithms.

The dsPIC33A's powerful digital signal processing core supports the execution of complex feedback and feed-forward control strategies with minimal latency, ensuring fast transient response and high efficiency. Dual 72-bit accumulators enable both 32-bit and 16-bit fixed-point digital signal processing (DSP) operations, delivering exceptional precision for demanding control applications.

Integrated high-resolution pulse-width modulation (PWM) peripherals offer granular control over multiple switches and voltage levels which is an essential feature for multilevel converter topologies. With Fine Edge Placement (FEP) PWM resolution as fine as 78 picoseconds, the dsPIC DSC facilitates precise switching, which helps minimize losses and maximize system efficiency. Additionally, a robust interrupt system and versatile timers further enhance the controller's ability to implement adaptive, real-time control strategies, ensuring reliable performance even under rapidly changing operating conditions.

Complementing its hardware capabilities, the dsPIC ecosystem includes comprehensive software and development tools that streamline design, prototyping and debugging. This synergy of advanced hardware features and robust software support empowers engineers to efficiently develop, test and refine control algorithms, making the dsPIC DSC an ideal solution for unlocking the full potential of FCML power conversion topologies in modern, high-efficiency power systems. As technology continues to advance, the potential for multilevel power conversion topologies to revolutionize power electronics becomes increasingly apparent, promising a future of more efficient and more compact power solutions.

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Optimizing DC/DC Converter Stability: AC and Transient Analysis in Simulations of Source Impedance Effects

This article investigates the optimization of DC/DC converter stability through AC analysis in the frequency-domain and transient analysis in the time-domain. While frequency-domain methods like the Middlebrook criterion effectively assess impedance interactions, they fall short of capturing nonlinear dynamics and constant-power load instabilities under transient conditions. Time-domain transient analysis bridges this gap by simulating real-world performance during transients, aiding in the selection of filter component values. By using both AC analysis in the frequency-domain and transient analysis in the time-domain simulation strategies, engineers will have the tools to minimize design iterations and enhance stability in their designs.

By Joe Ares, Senior Principal Engineer, Vicor Corporation

Source impedance plays a critical role in determining system stability and performance when designing with DC/DC converters. Variations in source impedance arising from input filters, cabling or power distribution networks can interact with the converter's input dynamics, potentially leading to instability, oscillations or degraded transient response. Understanding and mitigating these effects is essential for ensuring reliable operation in applications ranging from aerospace to consumer electronics.

Frequency-domain AC analysis provides valuable insight into stability margins and steady-state behavior via small-signal models like Bode plots and impedance overlap techniques. However, these methods rely on linearized approximations, which may overlook nonlinear dynamics or transient events prevalent in real-world operation. Another approach is needed to complete the picture: time-domain analysis, particularly transient analysis, captures large-signal behavior, transient responses and nonlinear interactions under varying conditions. Engineers can therefore achieve a comprehensive understanding of stability by using simulation tools to conduct AC and transient analysis, ensuring robust designs that perform reliably in a wide range of likely real-world scenarios. This white paper examines the impact of source impedance on DC/DC converter stability, contrasts frequency-domain and time-domain methodologies and highlights the benefits of transient analysis for optimizing performance.

AC vs transient analysis

AC analysis simulations of source impedance focus on evaluating the interaction between the DC/DC converter's input impedance and the source impedance, using frequency-domain techniques like Bode plots. The Middlebrook stability criterion, which assesses stability by ensuring the ratio of source impedance to converter input impedance remains below unity, provides a critical framework to prevent oscillations. This approach identifies instability risks at frequencies where source and converter impedances are closely matched.

In transient analysis, a constant-power load (CPL) closely mimics the behavior of a downstream DC/DC converter, as both exhibit negative incremental impedance characteristics. A CPL maintains constant power by decreasing its input current as input voltage increases (and vice versa), mirroring the input dynamics of a tightly regulated DC/DC converter, which adjusts its current draw to maintain constant output power. Both CPLs and DC/DC converters can destabilize the power system due to their negative impedance, potentially causing oscillations or instability.

However, CPLs oversimplify the complex behavior of actual converters, which include nonlinear control loops, switching harmonics and mode-dependent impedance variations (e.g., continuous vs. discontinuous conduction). These simplifications may lead to inaccuracies in predicting transients during start-up or fault conditions, where the converter's behavior deviates from a perfect CPL. Moreover, CPLs fail to capture beat frequencies arising from parallel converters with unsynchronized switching frequencies, as noted in the Vicor DCM Design Guide's discussion of parallel operation.

Despite these drawbacks, a CPL is often sufficient for time-domain transient analysis, as it captures the dominant destabilizing effect—negative impedance—while remaining computationally efficient. It allows engineers to analyze worst-case stability scenarios such as load steps or voltage transients and design robust input filters or control strategies without needing a detailed model of the downstream converter. For many applications, especially in early design stages or system-level analysis, the CPL's simplicity and ability to replicate primary dynamic interactions make it a practical and effective tool, balancing accuracy with simulation speed and ease of implementation.

AC analysis

In MIL-STD-461 EMI testing, the Line Impedance Stabilization Network (LISN) shown in Figure 1 introduces a standardized impedance, typically 50 µH in series with 5Ω for specific frequency ranges, ensuring repeatable EMI measurements. This impedance interacts with the DC/DC converter's input filter and control loop, potentially altering conducted emissions and stability margins or inducing oscillations if the impedances overlap at certain frequencies, as analyzed in frequency-domain AC analysis. Unlike the variable source impedance encountered in real-world systems, such as batteries or power buses, the LISN's fixed impedance may mask or exaggerate issues that manifest in actual operation. While LISN-based testing verifies compliance with EMI standards, these interactions necessitate additional AC analysis or transient analysis to ensure converter performance and stability in practical applications, particularly when transitioning from test conditions to real-world environments.

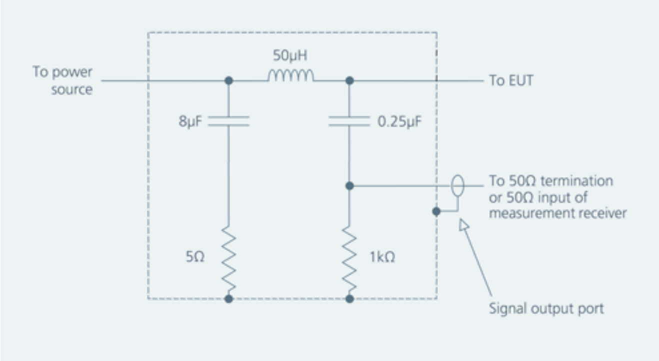

Figure 1: The standard LISN indicated by MIL-STD-461 for EMI testing shown above provides a fixed impedance, which may either mask or exaggerate stability issues. Additional AC and transient analysis is therefore needed to get a more accurate understanding of system stability with variable source impedance.

The Middlebrook stability criterion requires that the source impedance, including the converter's internal capacitance, remain significantly lower than the converter input impedance in frequency-domain AC analysis. A common design target is a source impedance at least ten times lower (20 dB separation), but for low-voltage, high-power designs, this can necessitate impractically large capacitors. In these cases, a minimum of two times lower (6 dB separation) may suffice, balancing stability with practical component sizing. To verify the stability of the DC/DC converter DCM3623T50M31C2M00 in the presence of a LISN, the AC analysis schematic shown in figures 4, 5 and 6 as well as the impedance plots shown in Figure 7 illustrate three scenarios:

(1) No external input capacitor, severe impedance overlap.
(2) 700 µF external capacitor with 250 mΩ damping resistor, no impedance separation.
(3) 1.7 mF external capacitor with 250 mΩ damping resistor, 6 dB impedance separation.

The simulations also incorporate the LISN impedance, the converter's internal input capacitance and the converter input impedance, calculated using the formula provided in the Vicor DCM Design Guide shown in figure 2.

$$Z_{IN\text{-}DCM} = -\frac{V_I^2}{P_I} \quad or \; -\frac{\Delta V_I}{\Delta I_I} \quad for\ all\ F\ [0 : 20kHz]$$

$Z_{IN\text{-}DCM}$ = Negative incremental impedance of the DCM
V_I = Input voltage to the DCM
I_I = Input current of the DCM
P_I = Input power of the DCM
ΔV_I = Change in the input voltage of the DCM
ΔI_I = Change in the input current of the DCM
F = Control loop bandwidth of the DCM

Figure 2: Formula to simulate the input impedance of the DCM.

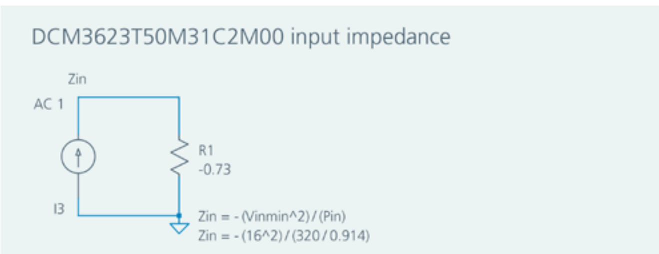

Figure 3: Simulation schematics for the input impedance.

The simulation schematics for AC analysis of a Vicor DCM3623T-50M31C2M00 with LISN enable comparison of different source impedance scenarios. Figures 4, 5 and 6 show the simulation schematics for the input impedance with no external input capacitor (figure 4), with a 700 µF external capacitor with 250 mΩ damping resistor and no impedance separation (figure 5) and with 250 mΩ damping resistor and 6 dB impedance separation (figure 6).

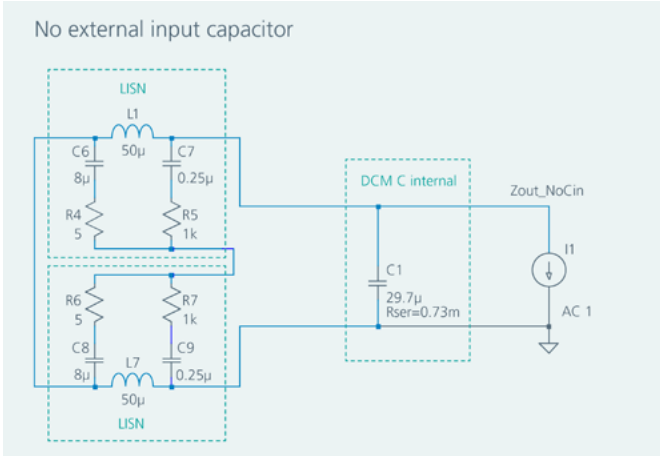

Figure 4: Simulation schematics for the input impedance with no external input capacitor at all.

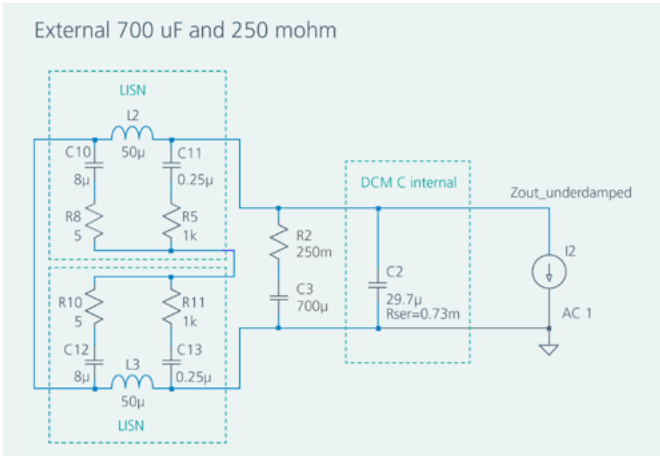

Figure 5: Simulation schematics for the input impedance with a 700 µF external capacitor with 250 mΩ damping resistor and no impedance separation.

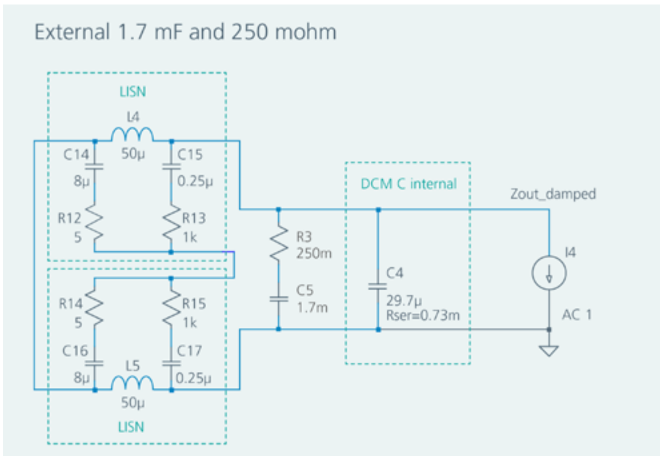

Figure 6: Simulation schematics for the input impedance with a 1.7 mF external input capacitor with 250 mΩ damping resistor and 6 dB impedance separation.

The AC analysis of each of the three scenarios presented in Figures 3, 4, 5 and 6 illustrate how the use of different input capacitance values impact source impedance overlap effects in the frequency domain. Figure 7 clearly shows that when there is no external input capacitance at all (scenario 1), the overlap is severe and will cause serious stability issues for the system.

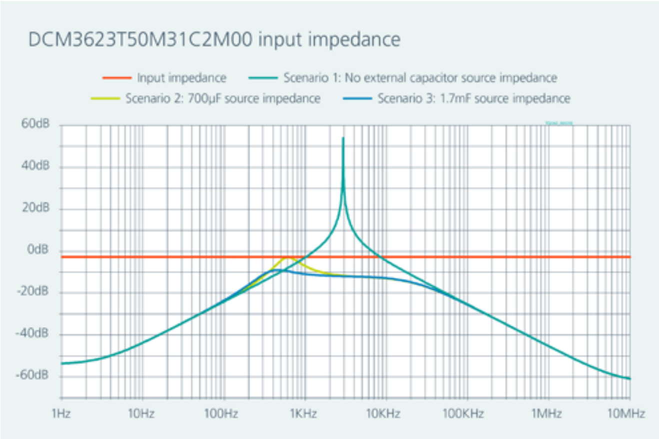

Figure 7: When there is no external input capacitance at all (scenario 1), the overlap is severe and will cause serious stability issues for the system.

Transient analysis with CPLs

A CPL can be implemented in time-domain transient analysis using a behavioral current source, defined by the expression I = Power / (Voltage across the terminals) in LTspice®. To model dynamic loads, a voltage source can replace the fixed power value, dynamically adjusting the power and changing the expression to I = V(POWER) / (voltage across the terminals). Additionally, undervoltage can be incorporated using an "if" statement, setting the current to zero when the terminal voltage drops below a specified threshold. This enhances the simulation's realism by mimicking converter behavior during low-voltage events. Figure 8 is an LTspice simulation schematic of CPLs B1 (without undervoltage) and B2 (with undervoltage). Voltage source V1 pulses from 0 VDC to 100 VDC for 50 ms and represents power in the expressions for CPLs B1 and B2.

For time-domain transient analysis, a CPL simulates transient behavior with the input voltage set to 16 VDC, the minimum operating voltage of the DCM3623T50M31C2M00. The simulation schematic shown in Figure 9 and plots shown in Figure 10 use the same scenarios as the frequency-domain AC analysis simulations in Figure 7. The first scenario (no external capacitor) experiences oscillations with a 5 W load, demonstrating instability. Scenarios 2 and 3 (external capacitors of 700 µF and 1.7 mF) are subjected to 320 W loads applied for 30 ms with 1 ms rise and fall times and demonstrate different levels of transient attenuation. Faster rise and fall times, which are realistic in practical applications, may necessitate increased capacitance or adjusted damping resistance to minimize undershoot or overshoot, ensuring robust transient response and stability under dynamic conditions.

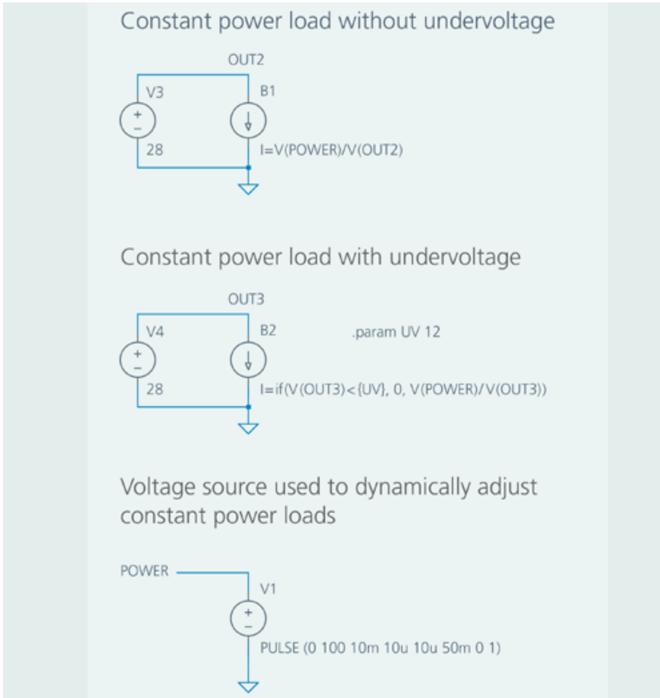

Figure 8: CPLs using behavioral current sources B1 (without undervoltage) and B2 (with undervoltage) realistically simulate a DC/DC converter's response to transient events.

Voltage transients and damping resistors
Simulating overvoltage and undervoltage is crucial to ensure DC/DC converters can endure transient events such as load dumps, input surges and power interruptions. Time-domain transient analysis models these conditions by applying step voltage changes or transient pulses, replicating scenarios like power bus fluctuations or battery sags. In contrast, frequency-domain AC analysis, with its focus on steady-state small-signal behavior, is inadequate for these large-signal transients. Incorporating accurate parasitic models and worst-case component tolerances is thus essential to prevent overly optimistic behavioral predictions, particularly when evaluating thermal effects and interactions between the input filter and converter, ensuring compliance with standards like MIL-STD-704 or MIL-STD-461.

Choosing the correct value of damping resistors in input filters is vital for managing transients and maintaining stability, particularly in systems with DC/DC converters or high source impedance. These resistors mitigate resonant peaks that can amplify transients, causing instability or excessive overshoot and undershoot. In time-domain transient analysis, resistor values are iteratively adjusted to achieve critical damping, optimizing settling time and transient response while preserving filter efficiency. Frequency-domain AC analysis ensures the filter's output impedance remains sufficiently lower than the converter's input impedance, avoiding destabiliz-

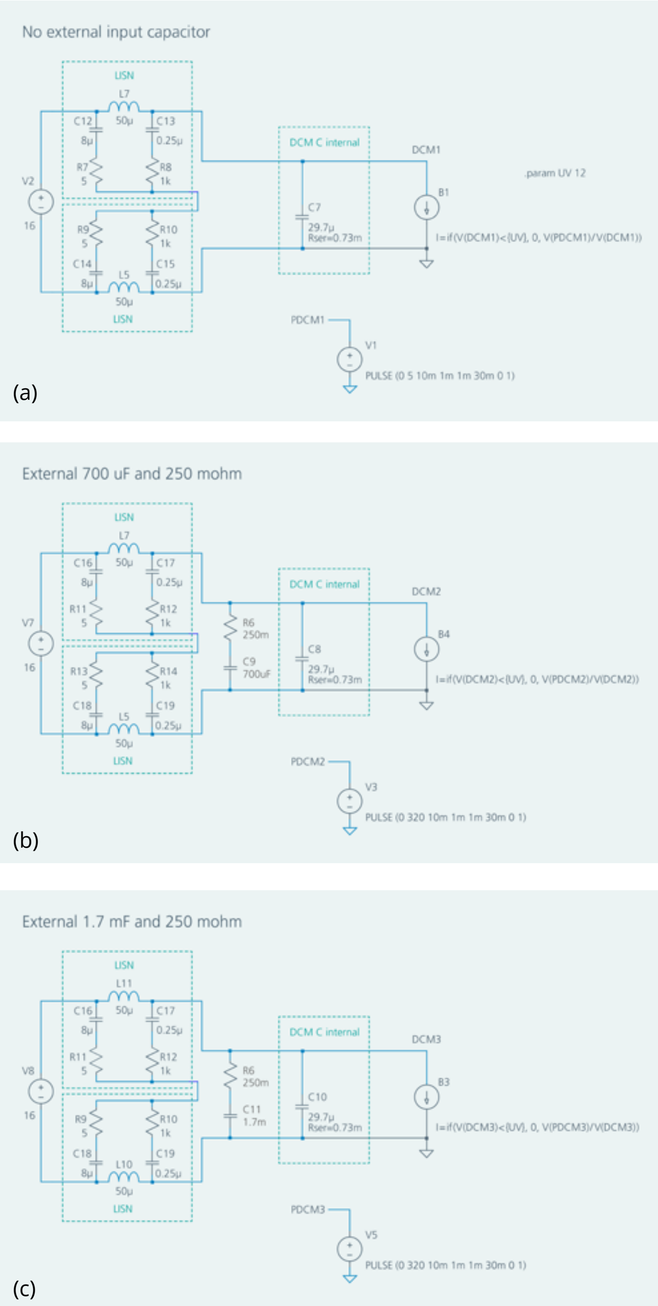

Figure 9: Schematics with LISN, internal and external input capacitance and CPL simulate response to a transient for the three scenarios presented in Figure 7.

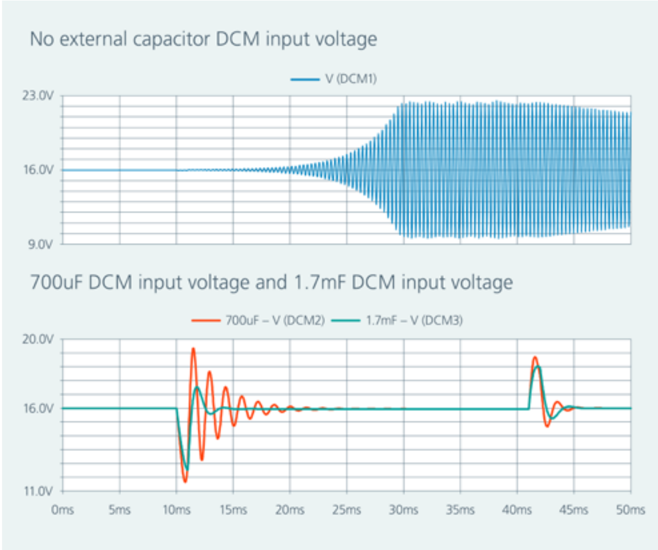

Figure 10: Transient response in each of the three schematics shown in Figure 9 shows how different input capacitance choices can impact system stability with CPL.

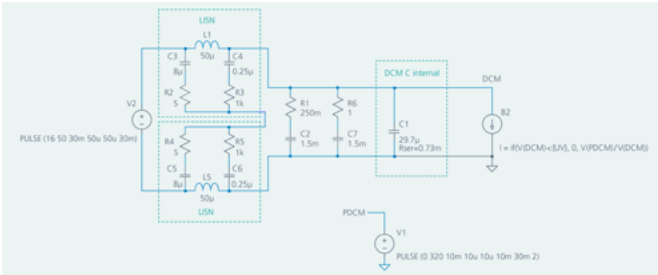

Figure 11: Transient analysis schematic of minimum and maximum input voltage steps with load transient employs higher input capacitance and pulse-withstanding damping resistors to model DC/DC converter stability when confronted with power bus fluctuation

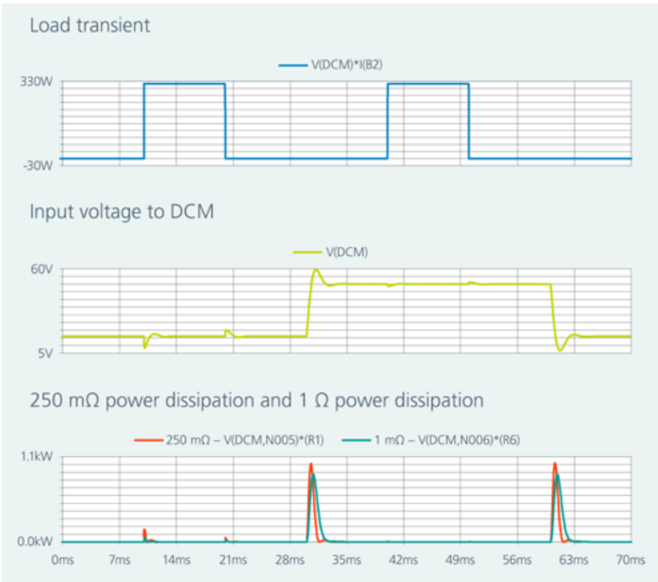

Figure 12: Simulated transient performance of voltage step, load step and damping resistor power dissipation using the schematics in Figure 11 allows the system designer to balance system stability, efficiency and power dissipation when choosing appropriate damping resistors.

ing overlap, but time-domain transient analysis offers a more comprehensive view by capturing nonlinear dynamics and large-signal effects. High power dissipation in damping resistors, driven by voltage ripple from the source or pulsed loads near the source impedance's resonant frequencies, necessitates careful resistor sizing, often requiring pulse-withstanding resistors to handle sustained or transient power demands.

To address a 16 to 50 V transient, the external input capacitance is increased beyond 1.7 mF, and damping resistors are adjusted to reduce overshoot and undershoot, with a 320 W CPL applied at both voltage levels. The transient analysis schematic shown in Figure 11 and plots shown in Figure 12 illustrate the transient response and power dissipation, guiding the selection of appropriately rated pulse-withstanding resistors. This ensures the filter design balances stability, efficiency and thermal performance for reliable operation under diverse transient conditions while adhering to practical component constraints.

Solid solutions

Vicor DC/DC converters leverage zero-voltage switching (ZVS), zero-current switching (ZCS) and high-frequency operation to enhance filter design efficiency. These technologies minimize switching losses and electromagnetic interference (EMI), enabling the use of smaller, more compact input and output filters compared to traditional pulse-width modulation (PWM)-based converters. The high switching frequency, typically in the megahertz range, reduces the size of filter components like capacitors and inductors needed to meet EMI requirements. This results in a more space-efficient power delivery network, which is particularly advantageous in aerospace applications where size and weight are critical constraints.

The analysis of source impedance effects on DC/DC converter stability highlights the importance of integrating frequency-domain AC analysis and time-domain transient analysis to deliver robust, reliable performance across demanding operating conditions. By combining AC analysis, which leverages the Middlebrook stability criterion to ensure impedance separation, with transient analysis, which captures nonlinear dynamics of constant power loads and transient events, engineers can comprehensively address stability challenges posed by source impedance, input filters and real-world power distribution networks. Strategic optimization of the filter components mitigates resonant peaks and transient-induced oscillations, balancing stability, efficiency and thermal performance.

This dual-domain approach empowers engineers to design DC/DC converters with filters that exceed stringent standards, such as MIL-STD-461 and MIL-STD-704, preventing catastrophic failures in mission-critical applications from high-power aerospace systems to compact consumer electronics. By adopting this methodology, designers can minimize costly iterations, enhance system reliability and confidently meet the evolving demands of modern power electronics.

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Multilevel Topology for AI System Efficiency: Foundations for the Future

ICERGi's Patented Multilevel Topology, Digital Control and Gate Drive Solutions for Powering AI, Industrial, and EV Charging Applications

By Rytis Beinarys and Garry Tomlins, ICERGi

A standout advancement in the power system space is the Multi-Level (ML) topology. The ML topology delivers two paramount advantages – highest power density and industry-leading efficiency. ICERGi's leadership in this ML space is underpinned by a patent-backed product ecosystem covering advanced isolated gate drive technology, digital control solutions designed specifically for multilevel applications and ownership of the principal patent for the ML topology itself (Figure 1).

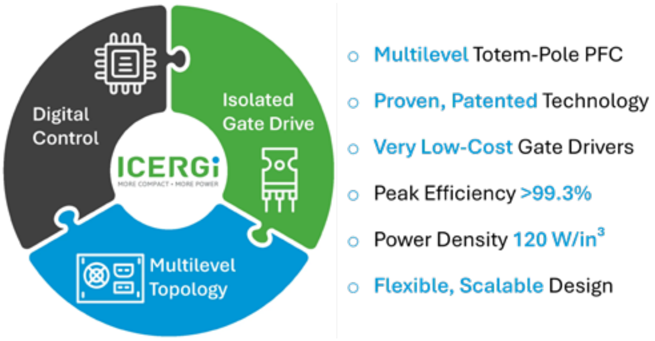

Figure 1: ICERGi Multi-Level Ecosystem – Products & IP

ICERGi's patent portfolio is a fundamental ecosystem for multilevel power conversion systems with its associated gate drive silicon, designed for all switching devices such as Si, SiC, GaN and IGBT. Furthermore, this patent portfolio includes control techniques in multilevel converters which can be embedded in any digital controller format [1]. By integrating ICERGi's patented Flying-Capacitor Multilevel (FCML) topology with its patented isolated gate driver and digital control technologies, manufacturers can unlock new levels of efficiency, power density and cost-effectiveness which are all essential for scaling AI-driven computing, powering next-generation industrial systems, and meeting the rigorous requirements of modern electric vehicles. ICERGi's innovations thus form the backbone of tomorrow's intelligent, sustainable power infrastructure.

The Three-Level Flying-Capacitor Bridgeless Totem-Pole PFC (3L-FC-BTP-PFC) has become an attractive solution for the latest generation of power supplies, where both high efficiency and compliance with emerging standards are critical. By combining the benefits of the bridgeless totem-pole structure with multilevel operation, this topology reduces voltage stress across each device which enables lower switching losses and higher effective operating frequencies (Figure 2). The result is improved efficiency at high load while also maintaining superior performance at light load, both of which are essential for meeting the demanding requirements of ORv3 as well as the 80 PLUS Titanium and Ruby certification levels [2], [3].

Recent industry developments highlight the increasing adoption of multilevel architectures in high-performance power systems. Infineon Technologies, for instance, has released several application notes and reference designs highlighting 3-level bridgeless totem-pole PFC implementations [4], [5]. A notable example is the *REF_3K3W_3LFC_PSU* reference design – a 3.3 kW high-frequency, high-density PSU for server and data center applications that employs a 3-level flying-capacitor totem-pole PFC front end. Such work demonstrates the broader industry recognition of multilevel PFC topologies as an effective means to enhance efficiency and improve overall power density in next-generation server and data center systems.

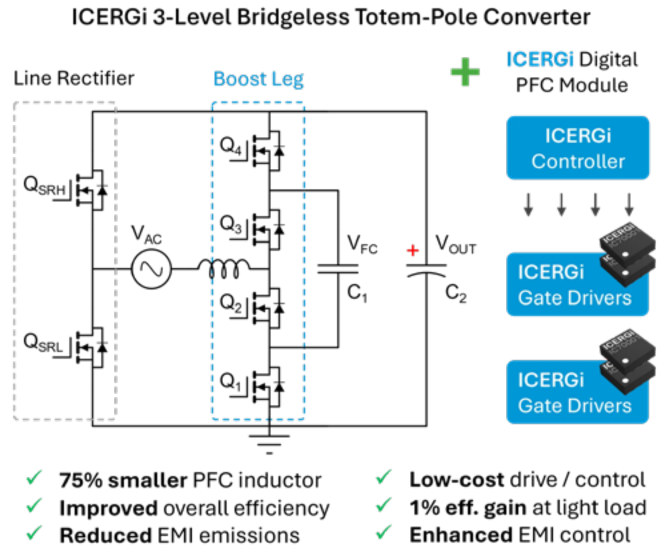

Figure 2: 3-Level Flying Capacitor Bridgeless Totem-Pole PFC enabled by ICERGi's Control and Drive Solutions

Isolated Gate Driver Overview for Multilevel Power Converters

ICERGi's isolated gate drivers provide floating, isolated drive for each multilevel switch at extremely low cost per driver. The IC70-001 is designed for Si MOSFETs, while the IC70-002 is optimized for SiC devices, with GaN and IGBT drivers currently in development [6].

At the core of ICERGi's gate driver are two small transformers (Figure 3). These convert input pulse edges (rising and falling) into isolated drive signals. This method allows precise pulse-width modulation (PWM) to drive power switches. The structure ensures interlocked operation by design, which means that if no input pulses are present, the output will safely revert to a low state.

ICERGi's isolated gate drive technology offers the following key features and advantages:

- Compatible with all switch types (GaN, SiC, Si, and IGBT)
- Extremely low cost per gate driver
- Galvanically isolated up to 5 kV
- Low quiescent current consumption <700 μA
- Fast, precise switching with typical propagation delay <15 ns
- Supports both planar and standalone transformer designs
- Optimized for lowest switching losses and drive power

ICERGi's gate drivers are versatile and can drive low-side and high-side switches, as well as any floating power MOSFETs used in multi-level converters. They are equally suited for complementary switch pairs and support both traditional PWM and ICERGi's pulse-drive methods (Figure 4). These drivers are ideal for switching applications that require level-shifting, high-side, or floating operation. They can be used with controllers for PFC, LLC, or asymmetric half-bridge designs, and are compatible with Si and SiC MOSFETs across a wide range of voltages.

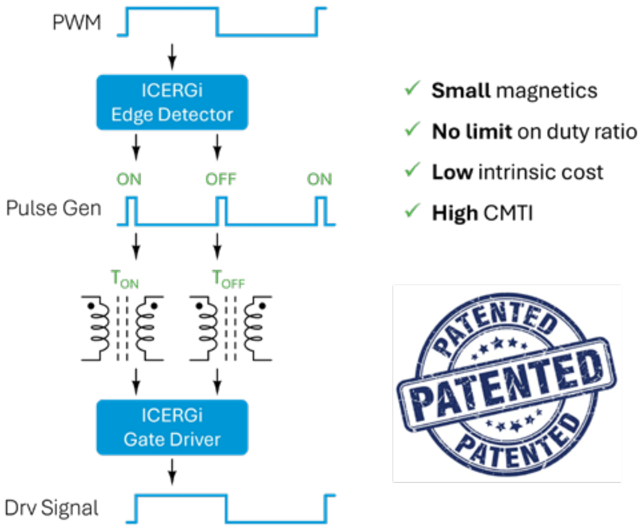

Figure 3: ICERGi's Isolated Gate Driver Functional Overview

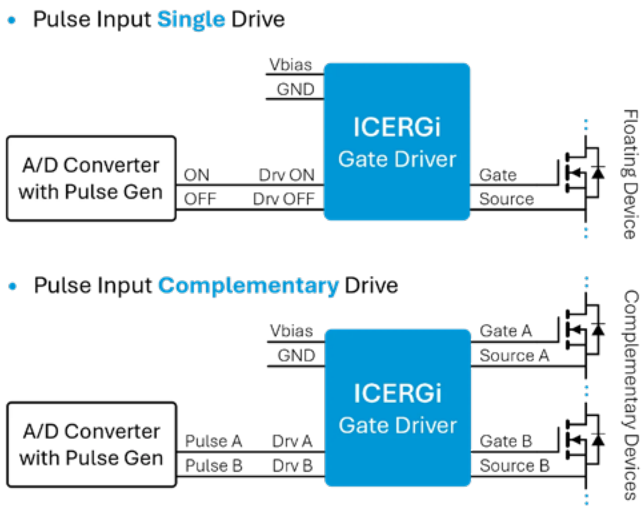

Figure 4: ICERGi Gate Driver Implementation Examples

Digital Control for Multilevel Converters

ICERGi specializes in advanced digital control of PFC converters, leveraging high-performance, cost-effective ARM® Cortex™-M0+ microcontrollers with rich peripheral sets and a mature development ecosystem. This platform provides a robust and efficient foundation for implementing precise, real-time control of PFC systems. Combined with ICERGi's proprietary control algorithms and scalable, low-cost hardware architecture, it enables compact, reliable, and high-efficiency power conversion across a wide range of applications.

Built on the proven ARM® Cortex™-M0+ processor, our solutions are typically implemented on compact, plug-and-play digital control daughter cards. These cards feature integrated gate drivers and auxiliary circuitry, forming a complete control and drive suite for power conversion systems. Designed for seamless integration, they support applications up to 5 kW and beyond. Proven in the field and backed by a robust development framework, ICERGi's controllers deliver exceptional efficiency, flexibility, and scalability across various PFC power levels.

- Enables 99.3% efficiency (*including EMI filter and bias supply*)
- Proven active and passive control techniques protect flying capacitor voltage under steady-state and transient conditions
- Proprietary fast and sophisticated protection for flying capacitor voltage during abrupt events, such as input surge
- Advanced predictive current control with intra-line-cycle compensation to enhance dynamic response and power quality across different operating conditions
- Implemented on the widely popular, low-cost Cortex M0+ processor, with seamless integration and upgrade options to more advanced MCU architectures (ARMv7-M, ARMv7E-M)

ICERGi Multilevel and its Advantages

Multilevel PFC improves power conversion by using multiple voltage levels to achieve lower total harmonic distortion (THD), reduced switching losses and improved electromagnetic interference (EMI). Compared to conventional two-level PFC, flying capacitor multilevel PFC distributes voltage stress more evenly across semiconductor

Feature / PFC	Conventional	Interleaved	Multilevel
Circuit Complexity	Low	Medium	Higher[1]
Efficiency	Moderate	High	Very High
Input Current Ripple	High	Low	Very Low
EMI	Moderate	Improved	Excellent
Thermal Distribution	Single Path	Spread	Distributed
Component Stress	High	Reduced	Much Lower
Control Complexity	Low	Medium	Higher[1]
Scalability	Limited	Good	Excellent
Size / Weight	Moderate	Larger	Compact

Table 1: PFC Topology Comparison

[1] *Higher circuit/control complexity is managed by ICERGi's turnkey control and gate drive technology which enables practical adoption of multilevel PFC*

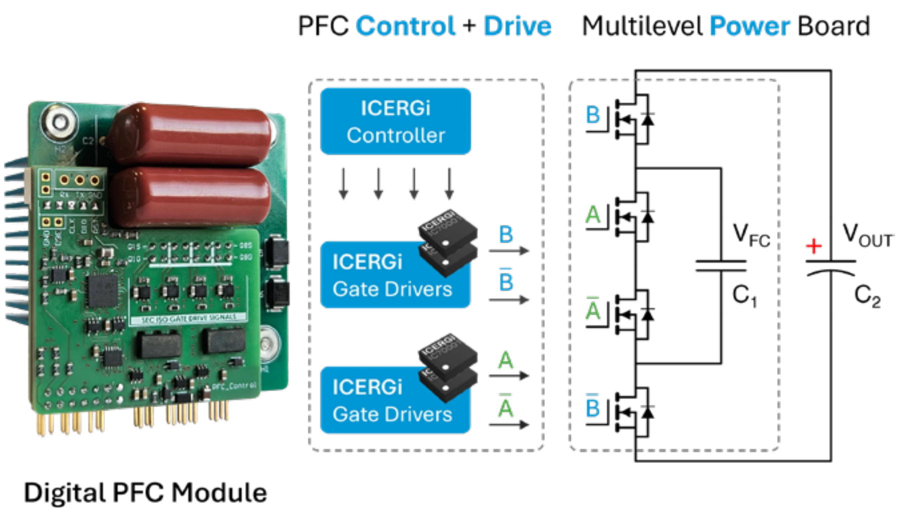

Figure 5: ICERGi's Digital PFC Module (Control + Drive + Power)

devices, enabling the use of lower voltage-rated components and boosting overall efficiency. Moreover, by supporting higher effective switching frequencies and improved waveform shaping, multilevel PFC can shrink passive components such as PFC main inductor and EMI filter stage leading to a more compact and thermally optimized power stage. For a more detailed comparison of PFC topologies, please see Table 1 below.

ICERGi has created a multilevel boost converter architecture that separates power and control functions for design flexibility. The solution uses a two-board layout: MOSFETs are located on the power board, while the gate driver array and digital microcontroller ecosystem sit on a daughter control board (Figure 5). This modular design simplifies integration, optimizes thermal performance, and allows for a compact layout. Supported by proprietary IP, ICERGi's multilevel approach is compatible with a wide range of Si and SiC switching devices. It enables broader adoption of multilevel power technologies and unlocking new value opportunities for high-efficiency, high-power AC/DC converter designers.

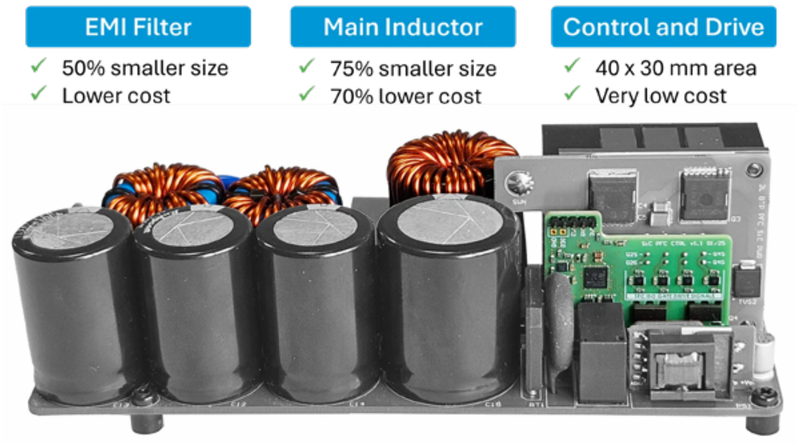

Figure 6: 3.3 kW 3L-FC-BTP-PFC Evaluation Board with 400 V SiC

Advancing Multilevel PFC with 400V CoolSiC™ MOSFETs
With the push for higher efficiency and power density in modern power electronics being driven by AI edge computing, advanced industrial loads, and next-generation applications there is growing demand for innovative solutions. At the forefront of this evolution, Infineon Technologies has launched CoolSiC™ Gen2 400V MOSFETs devices which are specifically optimized for multilevel PFC topologies. These new switching devices enable designers to achieve superior performance in power conversion systems, addressing the challenges of efficiency, thermal management, and reliability [7].

Building on this advancement, Infineon has also introduced multilevel PFC reference designs featuring their 400V CoolSiC devices. These designs leverage ICERGi's patented multilevel technology, combining Infineon's advanced semiconductor capabilities with ICERGi's expertise in high-performance AC/DC converters. ICERGi further highlighted these breakthroughs at APEC 2025 by introducing its own reference design (Figure 6, Figure 7) and sharing technical insights into performance and scalability [8].

- **Higher efficiency:** reduced switching and conduction losses
- **Lower system complexity:** simplified gate driver circuitry
- **Enhanced robustness:** higher blocking voltage capability
- **Higher power density:** more compact and scalable design

Key improvements compared to 150V stacked Si MOSFET variant

Conclusion

ICERGi has established a robust position in intellectual property and product ownership within the realm of multilevel power conversion which delivers unparalleled efficiency and cost-effectiveness for AI, industrial power, and EV charging applications. The recent introduction of advanced 400V SiC components by Infineon, combined with the adoption of ICERGi's patented technology in new power module developments by leading industry players, demonstrates the pivotal significance and future opportunity of ICERGi's IP and product ecosystem. These advancements not only validate ICERGi's approach but also highlight the transformative impact of achieving the highest efficiency at the lowest cost in power systems.

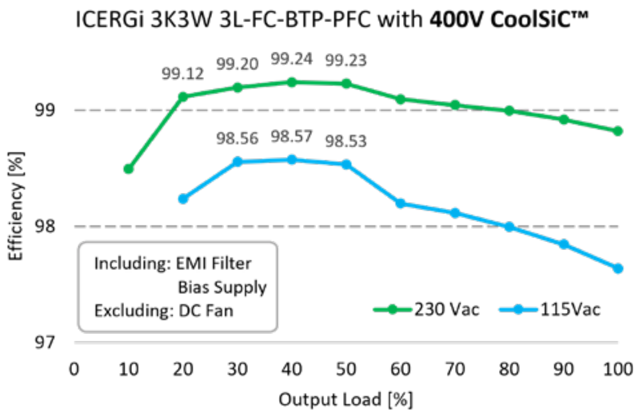

Figure 7: 3.3 kW Bridgeless Totem-Pole PFC Efficiency Data

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Solving Military-Avionics DC/DC Power Challenges with Modularity (Part 1)

While power electronics designers are skilled at designing power supplies, they often lack the knowledge necessary to meet military or aerospace standards. This series of four articles provides guidance to help designers understand standard parameters and presents best practices for the effective design of aerospace and military-grade power supplies. This first part provides a comprehensive list of key stress limits, which will serve as an essential technical reference.

By Christian Jonglas, Technical Support Manager, GAIA Converter

Military and avionics applications demand more powerful power supplies. This is mainly due to two factors: first, many functions that were in the past performed using mechanical or hydraulic methods are now fully electric; and second, emerging technologies such as high-power processing like mission critical computer, software defined radars directed-energy weapons (DEW) or any AI based electronic device require significantly more energy. This increase in demand for electrical energy is illustrated by the following examples: the Dassault Mirage F1 was equipped with 2 15 kVA electrical generators [1.1], whereas the new Dassault Rafale is equipped with a 80 kVA generator [1.2]. In another example, the F16 Fighting Falcon uses a 40 /60 KVA [1.3] generator, while the latest F35 Lightning II is equipped with a system that can generate up to 160 kVA [1.4]. Military vehicles are also keeping pace, with hybridization leading to increasingly powerful electric power sources.

Given these figures, it is not surprising that electronic design engineers are required to produce new projects following the SWaP (Size Weight and Power) trend for lower size, lower weight and higher power. The challenge of developing modern applications is also exacerbated by the fact that power supplies must comply with stringent standards. In most cases, leveraging a modular power architecture based on COTS (Commercial Off-The-Shelf) components remains the simplest and most effective approach. This article will provide a comprehensive review of standards to design power supplies for military and avionic, and suggest some examples of functions designed with discrete components, and their counterpart using COTS-based modular power supplies such as those proposed by GAIA Converter.

Domain	Standard	Country/Org	Primary Focus	Rev(2025)
Military Aircraft	MIL-STD-704	USA (DoD)	Voltage stability, transients, power quality	F
Civil Avionics	DO-160	RTCA (Global)	Environmental/electrical testing	G
Civil Avionics	ABD100.1.8 (A380) ABD100.1.8.1 (A350)	Airbus	Airbus-specific DO-160 enhancements	-
Military Vehicles	MIL-STD-1275	USA (DoD)	28V DC systems, transients, reverse polarity	F
EMC	MIL-STD-461	USA (DoD)	EMC emissions and immunity	G
Military Vehicles	DefStan 61-5 Part 6	UK (MoD)	UK equivalent to MIL-STD-1275	Issue 7
EMC	DefStan 59-411 Part 3	UK (MoD)	Electromagnetic Compatibility	Issue 3
Military Vehicles	VG 96916-5	Germany	Electrical system for land vehicle	2023-06
EMC	VG 95373-20	Germany	EMC emissions and immunity testing	2021-5
Military Equipment	MIL-STD-810	USA (DoD)	Environmental specifications	H

Table 1: The main standards relevant to the design of military or aerospace power supplies are listed in this table with their main purpose and latest revision for 2025.

Standard	**Steady state (Vdc)**				**Transient (Vdc)**			**Spike (Vdc)**
Military and Civil Avionic								
	Nominal	Normal	Abnormal	Emergency	Low normal	Low abnormal	High Abnormal	
MIL-STD-704F	28	22 – 29	20 – 31.5	16-29	18/15ms	0,Up to 7s	50/50ms	-
	270	250-280	240-290	-	200/10ms	0,Up to 7s	350//50ms	-
DO-160G (section 16)	28	22-30.3	20.5-32.2	18-30.3	10/35s	0,Up to 1s	80/100ms	600V /10µs/50Ω
	270	285-235	220-320	235	140/7s	0,Up to 1s	425/50ms	
ABD100	28	27-30.3	18.5-46	25.5-32	20/1s	0,Up to 5s	46/100ms	600V /10µs/50Ω

Table 2: The voltage specifications for military and civil avionics power supply buses are defined in the three main standards above, with voltage ranges under different conditions, as well as transient voltages.

Military and avionic standards

The following standards specify the key electrical and environmental requirements for designing military and avionics power supplies:

- **MIL-STD-704:** *Aircrafts Electrical power characteristics,* which defines requirement for DC and AC electrical busses in military aircrafts. This document can be used in conjunction with the MIL-Hdbk-704 handbook providing guidance for the test procedure.
- **RTCA DO160:** *Environmental Conditions and Test Procedures for Airborne Equipment.* Dedicated to civilian avionic, this standard describes both the electrical and environmental conditions for civilian avionics. The avionic bus voltage limits along with conducted and radiated electrical noise and susceptibility are also described.
- **ABD100:** Counterpart of DO160, this standard is dedicated to Airbus aircrafts exclusively.
- **MIL-STD-1275:** *Characteristics of 28 V_{DC} input power to utilization equipment in military vehicles.* Applicable to all electronic devices onboard of military vehicles. This standard defines limits for 14 and 28 VDC bus voltage.
- **Mil-STD-461:** *requirement for the control of electromagnetic interference characteristics of subsystems and equipment.* This standard defines the EMC rules for military equipment.
- **Defstand 61-5 part 6:** *28 V_{DC} Electrical Systems in Military Vehicles,* similar to MIL-STD-1275, released by the British ministry of defense.
- **Defstand 59-411 part 03:** *Electromagnetic Compatibility Test Methods and Limits for Equipment and sub systems.* Released by the British ministry of defense, similar to MIL-STD-461.
- **VG 96916-5** *Electrical system for land vehicle, DC networks, technical specification requirements for electrical systems and compliance test on system and component level.* Also similar to MIL-STD -1275, this standard is released by the German institute of standards for Germany.

- **The VG 95373** *Electromagnetic compatibility (EMC).* It defines the limit for conducted emission, while (**VG 95373-20**) covers conducted susceptibility, and VG 95373-24 deals with the limit for conducted emissions (current).
- **MIL-STD-810** *Environmental engineering considerations and laboratory test* that defines mechanicals and cycling test procedures and specifications.

Standard	Steady state (Vdc)	IES(1) (Vdc)	Cranking Surge (Vdc)	Injected surge (Vdc)	Injected spike (Vdc)	RPP(2)
Military Vehicle						
MIL-STD-1275 F(3)	20-**28**-33	12/1s	16/30s	100/50ms	+/-250/70µs/0.2J	Required
DefStan 61-5 Part 6 12V dc system	12.5-**12**-15	3V/15ms	4/10s	20/50ms 115V/400ms	-150/0.1µs (50Ω) +150/0.1µs (50Ω)	Required
DefStan 61-5 Part 6 24V dc system	(18)25-**24**-30(32)	8V/5ms	14/20s	40/50ms 198V/350ms	-200/0.1µs (50Ω) +200/0.1µs (50Ω)	Required
VG 96916-5	16-**24**-32 8-**12**-16	10V/50ms 5V/50ms	See ISO16750-2	151/200ms(1Ω) 79/200ms(0.5Ω)	70/2ms/(100A)	-

(1) Initial Engagement Surge
(2) Reverse Polarity Protection
(3) Values divided by 2 for 14V nominal

Table 3: The standards applicable to military vehicle equipment define the voltage range, surges, and other disturbances.

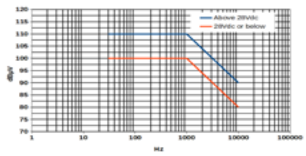
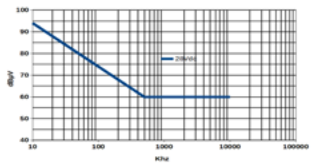
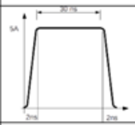
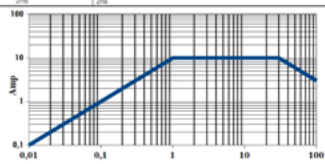
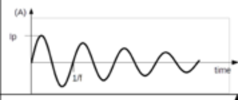
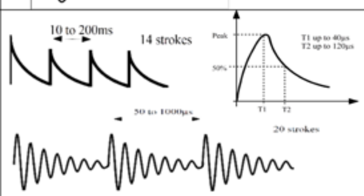
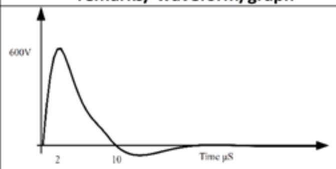
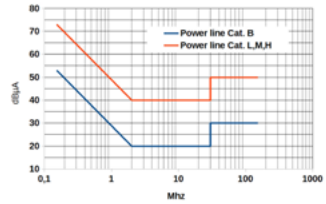
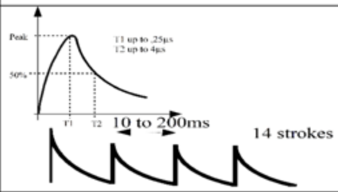
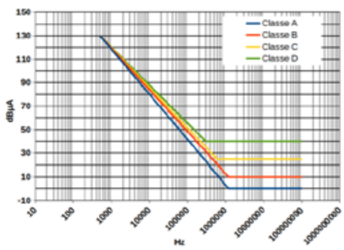
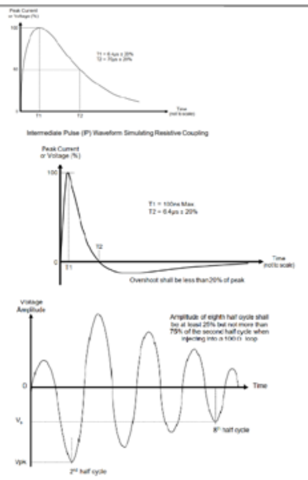
EMC STANDARDS : MIL-STD-461G			
section	**name**	**values**	**remarks/ waveform/graph**
CE101	Conducted emissions EMI	30Hz to 10Khz 76dBµA min 60Hz to 10Khz 80dBµA min	
CE102	Conducted emissions EMI	10kHz to 10Mhz 60dBµV min	With limit relaxation for other than 28V dc 
CS101	Conducted Susceptibility, Power Leads	From 30Hz to 10Khz up to 136dBµA	
CS109	Conducted Susceptibility, Structure Current	60 to 100khz up to 120dBµA	
CS114	conducted susceptibility, bulk cable injection	4khz to 200Mhz up to 120 dBµA	
CS115	conducted susceptibility, bulk cable injection, impulse excitation	5A 30ns (30Hz repetition)	
CS116	conducted susceptibility, damped sinusoidal transients, cables and power leads	10kHz to 100Mhz, 10Amax	 
CS117	conducted susceptibility, lightning induced transients, cables and power leads	Multiples wave forms spikes injection from 75 to 200V, and from 75A to 2000A	

Table 4: The Mil-STD-461 defines multiples electromagnetic interference disturbances that are defined according to multiple waveforms and levels.

EMC STANDARD : DO-160G			
section	**name**	**values**	**remarks/ waveform/graph**
Section 17	Voltage spike	600 V 10µs 50Ω	
Section 18	Audio frequency Conducted Susceptibility	10Hz to 15Khz, up to 4Vpp injections	
Section 19	Induce signal Susceptibility	Not detailed here (Applicable to system)	
Section 20	Radio frequency Susceptibility	Conducted: 10Hz to 400Mhz up to 0.3A	
Section 21	Emission of Radio frequency Energy Conducted	150KHz to 152mhz, 20dBµA min. 9dBµA (2 to 30Mhz) Cat. P	
Section 21	Emission of Radio frequency Energy (Radiated)	Not detailed here (Applicable to system)	
Section 22	Lightening induced transient susceptibility	Multiples wave forms spikes injection from 100 to 3200V, and from 4A to 5000A	
Section 23	Lightening direct effect	Not detailed here (Applicable to system)	

EMC STANDARD : DEFSTAN 59-411 Part 3			
section	**name**	**values**	**remarks/ waveform/graph**
DCE01.B DCE02.B	Conducted Emissions, Primary Power Lines	20Hz to 150MHz **0dBµA** min.	
DRE01.B DRE02.B	Radiated emissions	Not detailed here (Applicable to system)	
DCS01.B	Conducted Susceptibility	20Hz-50KHz **3Vrms max**	
DCS02.B	Conducted Susceptibility	50Khz -400Mhz up to **115 dBµA**	
DCS04.B, DCS05.B, DCS06.B, DCS08.B DCS09.B,DCS10.B, DCS12.B		Multiples wave forms and levels generator source impedance : 5Ω and 0.2Ω Ipk : 320A to 10KA Vpk (open loop) 1.6 to 5 KV	

One challenge in military power supply design is efficiently locating relevant parameters within extensive standards documents. Tables 2 to 6 provide a concise overview of the main parameters that DC/DC power supply designers must consider in relevant standards. Although, these tables are not exhaustive, some requirements like limited inrush current, isolation voltage, or load dump are voluntary not described. Section markers and waveform diagrams for EMC standards help identify parameters and serve as preliminary guides before consulting the full standard. It is essential to consult the complete standard document before beginning the design for several reasons:

- Older revisions of a standard may have different limit values.
- Many parameters cannot be fully described by numbers alone; they require curves and detailed explanations for proper context.
- Standards often include descriptions of test fixtures and setup diagrams, which are crucial for understanding how parameters are measured and applied.

Table 5: The EMC requirements for civil avionic equipment is covered by the section 17 to 23 of DO-160G.

Table 6: The UK Ministry of Defense has published a document named DEFTSAND 59-411 Part 3, which defines the disturbance limits for electromagnetic compatibility of equipment and subsystems.

By referring directly to the full standard, designers ensure they account for the most current requirements and fully understand the test conditions associated with each parameter.

Table 4 and 5 describe EMC requirements from the most well-known reference documents, MIL-STD-461 and DO-160. However, standards released by European countries, such as the UK's DEFSTAN 59-411 and Germany's VG 95373-20 series, are also worth considering. For some equipment categories, these standards feature more aggressive specifications than their MIL-STD counterparts. This is particularly the case for conducted EMI on primary power lines, where limits for Class A equipment extend down to 0 dBμA, as shown in Table 6. The parameters of VG 95373-20 are not described in this article and follow a similar philosophy to DEFSTAN 59-411. Readers are invited to consult directly the VG 95373-20 document for further details.

The parameter values in standards like DO-160 and VG 96916-5 can seem daunting, such as a 600 V spike or a 151 V surge on a 28 V supply. However, these extreme transients can be clamped with straightforward circuits. Using GAIA Converter commercial off-the-shelf (COTS) transient limiters simplifies this further.

Clamping, EMI and examples

Subsequent articles will demonstrate these clamping methods (Part 2), dive into EMI containment (Part 3), and conclude by presenting examples from GAIA Converter's modular power architecture designed for full compliance with these aggressive standards (Part 4).

[1.1] https://www.globalsecurity.org/military/world/europe/mirage-f1-variants.htm

[1.2] https://web.safran-group.com/safran-on-board/en/rafale.html

[1.3] https://goallclear.com/wp-content/uploads/2024/02/AC_OEM_Collins_F16_EPS.pdf
[1.4] NEXT GENERATION AIRPLANE ELECTRICAL POWER SYSTEMS Nguyen Viet Nguyen B.S., University of Washington, Seattle, 2002.

www.gaia-converter.com

Figure 1: This 40 W power supply complies with Mil-STD-704,Mil-STD-461, Mil-STD-1275, and DO 160 standards thanks to its FLHG60, the latest integrated input front-end from GAIA Converter.

Industrial Power Supply Series now also with 600 W and 1000 W Models

TDK-Lambda has expanded its GUS series of single-output general-purpose power supplies with 600 W and 1000 W models. Designed for applications such as light industrial equipment, factory automation, semiconductor fabrication, ATE test systems, LED lighting, and broadcast, the new models provide output voltages of 12, 24, 36, and 48 V, achieving efficiencies of up to 95 % with a load of 30 to 100 %. Both units feature an internal cooling fan with an acoustic noise,

which is typically less than 45 dBA. The GUS600 model measures 101.6 x 41 x 152.4 mm^3 (W x H x D), while the GUS1000 has a compact package size of 101.6 x 41 x 177.8 mm^3. The models feature an operating temperature range of -20 to +70 °C and the output voltage can be adjusted for non-standard system voltages while output remote on/off is available as an option. Safety certifications include IEC/EN/UL/CSA62368-1 (compliant to IEC61010-1) and carry the CE and UKCA marking for the Low Voltage, EMC and RoHS Directives. The units also comply with EN 55011-B and EN 55032-B conducted and radiated emissions standards and meet EN 61000-3-2 harmonics and IEC 61000-4 immunity standards. The GUS series also meets IEC 62477-1 (OVC III) and has an input-to-output isolation of 2,000 V_{AC}, input-to-ground of 3,000 V_{AC}, and an output-to-ground of 500 V_{AC}. The nominal input voltage is 100 – 240 V.

www.jp.lambda.tdk.com

DualPack 3 IGBT7 Modules deliver High Power Density and simplify System Integration

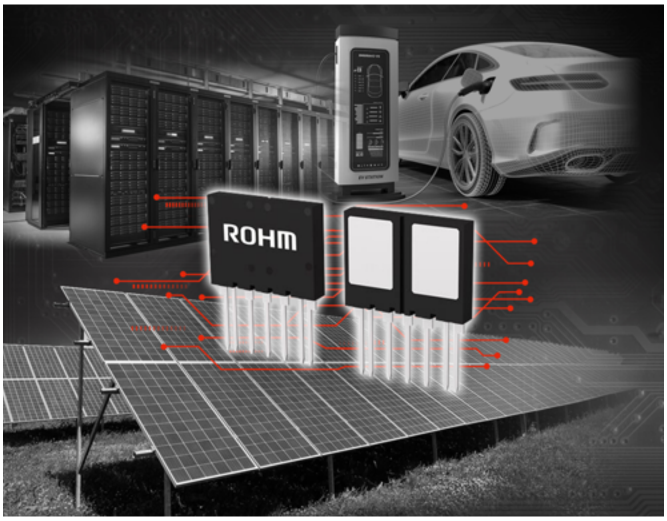
Microchip Technology announced a family of DualPack 3 (DP3) power modules featuring advanced IGBT7 technology available in six variants at 1200 V and 1700 V with high-current ranging from 300 – 900 A. The DP3 power modules are designed to address the

growing demand for compact, cost-effective and simplified power converter solutions. These modules use the latest IGBT7 technology, engineered to reduce power losses by up to 15 – 20 % compared to IGBT4 devices and operate reliably at higher temperatures up to 175 °C during overload. DP3 modules enhance protection and control during high-voltage switching, making them suitable for industrial drives, renewables, traction, energy storage and agricultural vehicles. Available in a phase-leg configuration, the DP3 power modules in a footprint of approximately 152 mm × 62 mm × 20 mm, enable a frame size jump for increased power output. This type of power packaging eliminates the need for paralleling multiple modules and helps reduce system complexity and Bill of Materials (BOM) costs. Additionally, DP3 modules provide a second-source option to industry-standard EconoDUAL™ packages for greater flexibility and supply chain security for customers.

www.microchip.com

2-in-1 SiC Molded Module

ROHM has developed the "DOT-247," a 2-in-1 SiC molded module (SCZ40xxDTx, SCZ40xxKTx), suited for industrial applications such as PV inverters, UPS systems, and semiconductor relays. The module retains the versatility of the "TO-247" package while achieving design flexibility and power density. The DOT-247 features a combined structure consisting of two TO-247 packages. This design enables the use of large chips, which were structurally difficult to accommodate in the TO-247 package. Additionally, through optimized package structure, thermal resistance has been reduced by approximately 15 % and inductance by approximately 50 % compared to the TO-247. This enables a power density 2.3 times higher than the TO-247 in a half-bridge configuration – achieving the same power conversion circuit in approximately half the volume. These products featuring the DOT-247 package are available in two topologies: half-bridge and common-source. Currently, two-level inverters are the mainstream in PV inverters, but there is growing demand for multi-level circuits such as three-level NPC, three-level T-NPC, and five-level ANPC to meet the need for higher voltages. In the switching sections of these circuits, topologies such as half-bridge and common-source are mixed – making custom products necessary in many cases when using conventional SiC modules.

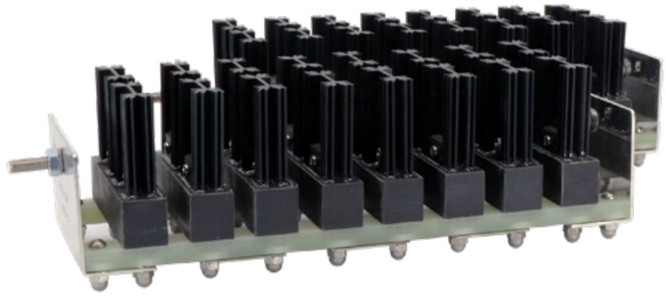


Therefore, ROHM has developed each of these two topologies into a 2-in-1 module to support various configurations such as NPC circuits and DC/DC converters. Evaluation boards will also be made available.

www.rohm.com

Fast Recovery Power Rectifier Assemblies

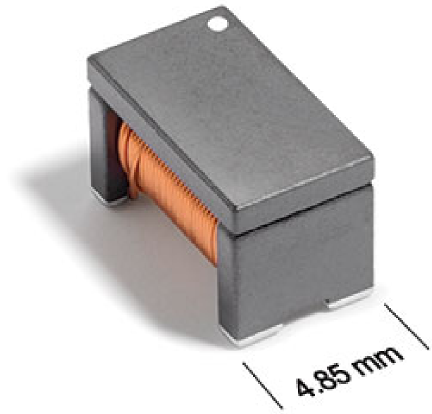
Dean Technology (DTI) extended their their power rectifier assembly line, the HRFS5 Series. They join the HRS5 series and HRS10 series of standard recovery power assemblies. The HRFS5 series follows the open frame concept found in the legacy HRS5 and HRS10 products, allowing for better thermal conductivity and are intended for ambient air applications but can also be used in submerged oil environments. It offers a reverse recovery time (TRR) of 75 ns maximum, which is good for switching applications. HRFS5 units offer a maximum repetitive reverse voltage range from 14.4 to 28.8 kV and 5.7 A of average forward current. All products in the HRFS5 series line are capacitor compensated and modular based.



www.deantechnology.com

LLC Half-Bridge Transformers for isolated Gate Driver Bias Supply

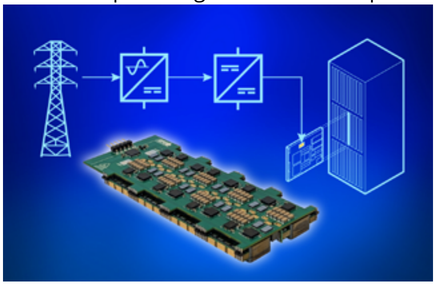
The HTX8045C Series transformers from Coilcraft build on the proven chip-style construction of the HTX family – an improvement over conventional core and bobbin designs. This surface-mount configuration reduces component size and enhances manufacturing efficiency. With higher isolation voltage compared to the HTX7045C and an interwinding capacitance as low as 0.55 pF, the HTX8045C is particularly well-suited for use in isolated gate driver bias supplies employing the open-loop LLC topology to achieve low EMI noise and high CMTI (Common Mode Transient Immunity). These characteristics make it especially beneficial for high-frequency switches including SiC, GaN and IGBT technologies. The HTX8045C is AEC-Q200-qualified, making it suited for automotive traction inverters and motor controls, automotive on-board chargers (OBC), EV charging stations, battery management systems (BMS), automotive DC/DC converters as well as other automotive and industrial applications.



www.coilcraft.com

800 V_{DC} Power Architecture for AI Data Centers

EPC develops innovative power converter to accelerate the adoption of 800 V_{DC} distribution systems for the next generation of AI data centers. Future AI factory data centers will require megawatt-scale rack power delivery systems. To address this challenge, EPC has developed a low-cost, low-profile GaN-based, 6 kW 800 V-to-12.5 V converter based on an Input Series Output Parallel (ISOP) topology.



Benefits of a GaN-based Solution include higher power density as it only occupies under 5,000 mm² and only 8 mm in height, making it ideal for space-constrained AI boards. And also high efficiency and reduced losses, as it efficiently converts 800 V_{DC} to 12.5 V_{DC} close to the load, reducing bussing losses and improving system-level efficiency.

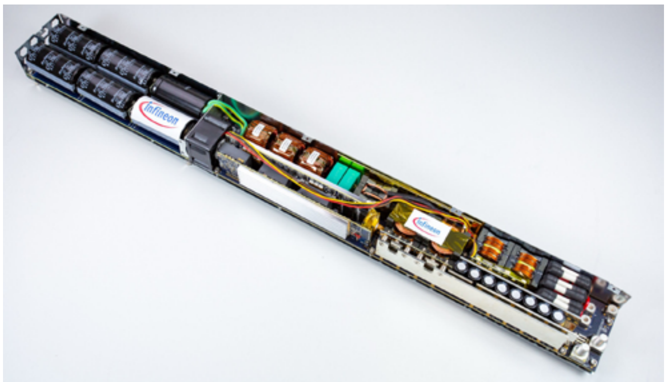
By moving from AC directly to 800 V_{DC} at the rack level, and then stepping down to 12.5 V at the board, EPC's GaN-based solution eliminates unnecessary conversion stages and enables the scalability, simplicity, and energy optimization demanded by tomorrow's AI data centers.

"GaN is an essential technology for the 800 V_{DC} ecosystem," said Alex Lidow, CEO of EPC. "Our collaboration with NVIDIA is to develop compact, efficient, cost-effective board-level conversion to power future AI factories at gigawatt scale."

www.epc-co.com

Power Supply Unit Reference Design for AI Data Centers and Servers

Infineon Technologies has introduced a 12 kW reference design for high-performance power supply units (PSUs), specifically designed for AI data centers and server applications. The reference design offers high efficiency and high-power density, and leverages all relevant semiconductor materials silicon, silicon carbide and gallium nitride. It is aimed at research and development engineers, hardware designers, and developers of power electronics systems.

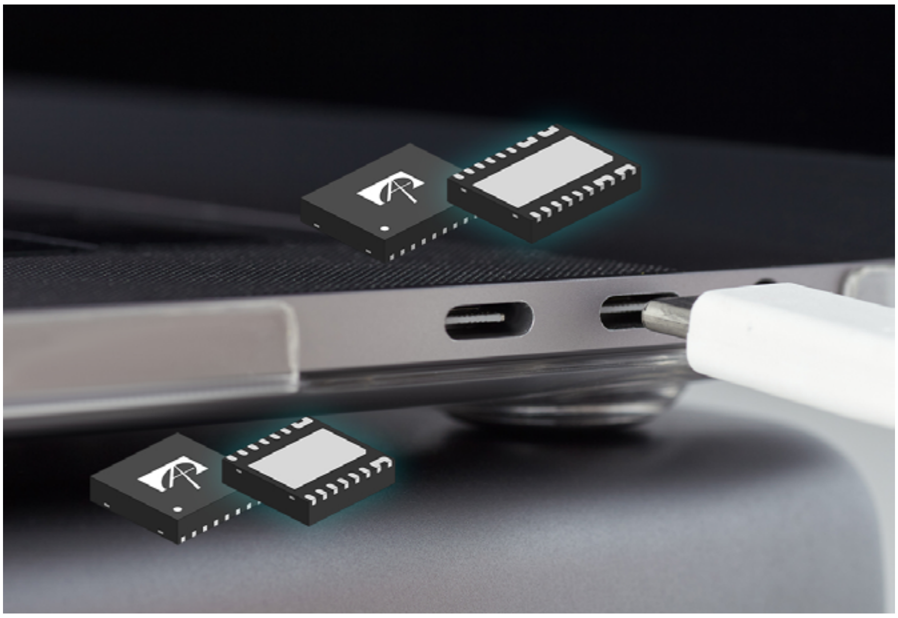


To achieve high-performance levels, the design leverages advanced power conversion topologies in both the AC/DC and DC/DC power stages. The front-end AC/DC converter features a 3-level flying capacitor interleaved power factor correction topology, delivering peak efficiency above 99.0 percent while reducing magnetic component volume. This is achieved by Infineon's CoolSiC™ technology. The isolated DC/DC converter features a full-bridge LLC resonant converter and offers peak efficiency above 98.5 percent, enabled by using two planar high-frequency transformer and Infineon's CoolGaN™ technology. These architectures, combined with the company's latest wide-bandgap technologies, achieve a power density of up to 113 W/in³. Another key feature of the 12 kW PSU reference design is the bidirectional energy buffer, which is integrated into the overall power supply topology. This converter enables compliance with hold-up time requirements while significantly reducing capacitance requirements. Furthermore, the energy buffer provides a grid-shaping function, improving system reliability and limiting both fluctuations and the rate of change of power drawn from the grid during transient events.

www.infineon.com

Duo of Protection Switches that support Type-C EPR 3.1 extended Power Levels

Alpha and Omega Semiconductor announced two Type-C sink and source protection switches to increase the power delivery capability of USB Type-C ports to 240 W, paving the way for Type-C extended power range (EPR) implementations. The AOZ13058DI offers overvoltage/overcurrent protection features suited for 48 V Type-C sinking applications, while the AOZ15953DI provides the additional protection features needed for Type-C sourcing applications. These switches help designers safeguard 48 V Type-C EPR capabilities to enhance reliability and functionality in high-performance and gaming laptops, personal computers, monitors, docking, and other higher-power connected portable devices. The AOZ13058DI features a 20 milliohm resistance and provides a set of features including programmable soft-start, overvoltage, ideal diode reverse-current, short-circuit, overcurrent, overtemperature, and ESD protection. These features also help isolate and protect downstream components from abnormal VBUS voltage and potentially harmful current conditions. Ideal diode fast reverse current protection allows multiple power paths to be connected in parallel without interference. The switch's integrated positive and negative transient voltage suppression at VIN enhances immunity to voltage spikes meeting IEC safety standards (IEC61000-4-2: ±8 kV contact, ±15 kV contact; IEC61000-4-5: 20 A (8/20 µs) on VIN and VOUT). The AOZ13058DI also features a programmable current limit function, permitting its application as a sourcing switch in an EPR 3.1 docking system.



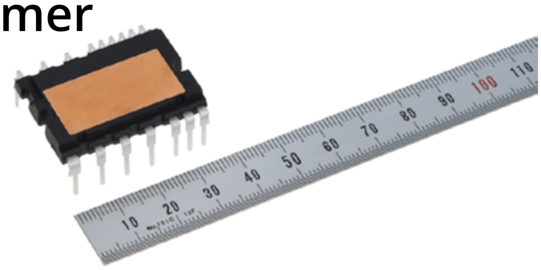
www.aosmd.com

DC Power Analyzer

The IT2705 DC Power Analyzer is a highly integrated modular DC power analyzer designed for dynamic power consumption measurement, battery simulation, and power characterization. It combines DC power, electronic loads and arbitrary waveform generator with an intuitive GUI, supports Oscilloscope Sampling and Data Logging function, allowing for the creation of complex testing without the need for secondary development. The IT2705 is an 8-slot modular power analyzer, supporting DC power supplies, regenerative electronic loads, bidirectional DC power supplies, and SMU source meters (4 categories, 20 models, covering 20 W to 500 W per module). Modules of the same type can be paralleled in master-slave mode to expand power, maximizing equipment utilization and broadening the test range. Four current ranges with seamless auto-ranging enable accurate analysis of transient current changes from low-power sleep mode to active operation. Oscilloscope sampling rate up to 200 kHz ensures precise capture of microsecond-level parameter variations.

www.itechate.com

Compact Power Modules for Consumer and Industrial Equipment



Mitsubishi Electric has developed a compact version of its DIPIPM power semiconductor modules specifically for use in consumer and industrial equipment such as packaged air conditioners and heat pump heating and hot water systems. The Compact DIPIPM series comprises the PSS30SF1F6 (30 A / 600V) and the PSS50SF1F6 (50 A / 600 V). By utilizing reverse-conducting IGBTs (RC-IGBTs), the module's footprint has been reduced to almost 53 % of that of the company's conventional Mini DIPIPM Ver.7, enabling more compact inverter substrates in packaged air conditioners and other applications. In 1997 Mitsubishi Electric commercialized the DIPIPM intelligent power semiconductor module with a transfer mold structure; this integrated switching elements and the control ICs that drove and protected them. Despite the smaller product size, the use of high-heat dissipation insulating sheet material suppresses temperature rise at the junction, achieving a current rating of 50 A. An additional interlock function contributes to the simplification of inverter substrate design, but it also simplifies the short-circuit protection design of inverter substrates. By maintaining the same insulation distance between terminals and the heat sink as that of conventional products, replacement of those products is facilitated. Furthermore, the lower limit of the continuous operating temperature is now extended to -40 °C.

www.mitsubishielectric.com

100 V N-Channel Power MOSFET

Toshiba Electronics has launched the TPH2R70AR5, a 100 V-rated N-channel power MOSFET fabricated in the company's U-MOS11-H process. The MOSFET will be primarily used in switched-mode power supply (SMPS) applications, particularly high-efficiency DC/DC converters. Key application sectors will be within data centres, communications base stations, and other high-end industrial equipment. The TPH2R70AR5 offers significant performance advantages over devices manufactured with the existing U-MOSX-H process. For example, compared to the earlier TPH3R10AQM, the drain-source on-resistance ($R_{DS(ON)}$) has reduced by around 8 % to 2.7 mΩ (max.) while the total gate charge (Q_g) is now 37 % lower at 52 nC (typ.). The $R_{DS(ON)}$ x Q_g figure-of-merit (FoM) is therefore improved by 42 %. Housed in the SOP (N) package measuring 5.15 mm x 6.1 mm, the TPH2R70AR5 is rated for a maximum drain current (I_D) of 190 A at an ambient temperature of 25 °C. The device is capable of operating with a channel temperature (T_{ch}) up to 175 °C, thereby reducing the need for cooling measures.

Toshiba also offers circuit design support tools: the G0 SPICE model, which verifies circuit function in a short time, and highly accurate G2 SPICE models that accurately reproduce transient characteristics.

www.toshiba.semicon-storage.com

500 W integrated Power Supplies for High-Rel Applications

GAIA Converter has launched the GRD-50A-M series of scalable 500 W integrated power supplies for high-reliability markets such as military and aerospace. This family of commercial-off-the-shelf board power supplies, designed for 24 V_{DC} and 28 V_{DC} input, complies with major military standards, including MIL-STD-1275, MIL-STD-704, and MIL-STD-461. Key specifications and features include a 16-38 V_{DC} permanent input voltage with transient voltage protection of up to 100 V_{DC}, as well as reverse polarity

and overload protection. The power supplies offer a total output power of 500 W with 12 V_{DC}, 15 V_{DC}, 24 V_{DC} or 28 V_{DC} output voltage. The GRD-50A-M series features an overall efficiency of 89 %, with full protection for output short circuit (hiccup mode), overvoltage, and overtemperature. The series features 1500 V_{DC} primary-secondary isolation and 500 V_{DC} chassis ground isolation. Overall board dimensions are 255 x 70 x 24.25 mm³ and operating temperatures extend from -40 °C to +85 °C base-plate. Furthermore, the GRD-50A-M comes in a range of different configuration options, including board only (/B), coated (/V), and parallel (/P).

www.gaia-converter.com

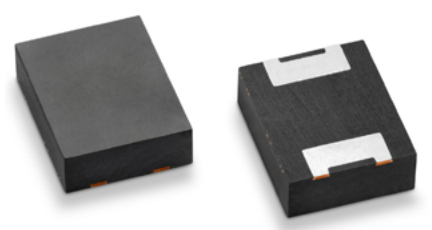
40 W DC/DC Converters for demanding space-constrained Applications

XP Power launched the BCT40T series of 40 W DC/DC converters, housed in a 1” x 1” (25.4 mm x 25.4 mm) package designed for PCB mounting. This series is suited for industrial technology, ITE, and communications applications where space is a critical constraint; it is specifically engineered for sectors such as test & measurement, robotics, process control, analytical instruments, and communications equipment. It features a 4:1 input voltage range and operates with an efficiency of up to 89 %. Models are available with nominal 24 V_{DC} inputs (ranging from 9.0 V to 36.0 V_{DC}) and 48 V_{DC} inputs (ranging from 18.0 V to 75.0 V_{DC}). The BCT40T offers single regulated outputs ranging from 3.3 V to 24 V_{DC}, as well as dual regulated outputs at ±12 V_{DC} and ±15 V_{DC}. Furthermore, the single-output models offer the flexibility of ±10% output voltage adjustment via an external trim resistor, enabling specific voltage requirements. Protection features include 2kV_{DC} isolation between input and output, continuous short-circuit protection with auto-recovery, and overload protection typically set between 130 % and 180 %. It also incorporates overtemperature protection (at 115 °C case temperature), under-voltage lockout (UVLO), and overvoltage protection via a Zener diode clamp. The series holds worldwide safety approvals, meeting IEC/UL/EN62368-1 standards, as well as applicable CE and UKCA directives. It also complies with EN55032 Class A/B for conducted and radiated emissions, and EN61000-4-x for immunity. With a 3-year warranty, the BCT40T series stands as a reliable and high-performance solution for power delivery.

www.xppower.com

3 kA TVS Diode in Compact Surface Mount Package

Littelfuse launched the DFNAK3 Series of High-Power TVS Diodes. These surface mount devices deliver 3 kA (8/20 µs) surge current protection - claimed to be the highest available in such a small footprint - making them suited for safeguarding DC-powered systems and Power over Ethernet (PoE) applications in demanding environments. Unlike traditional high-surge TVS diodes that come in bulky axial-leaded or large surface mount packages, the DFNAK3 Series uses a compact DFN package -

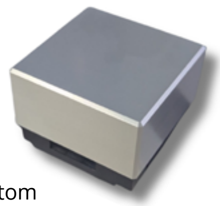


“making it the smallest 3 kA-rated TVS diode on the market today”. It offers a 70 % smaller footprint than overcoated alternatives and is also 70 % lower in height than standard SMD-type coated packages. This enables space-constrained, high-density PCB designs without compromising surge performance or system robustness. Engineered to meet IEC 61000-4-5 Level 4 requirements, the DFNAK3 Series provides an alternative to standard TVS diodes, MOVs, and GDTs. The surface mount configuration also supports cost-effective, automated PCB assembly, reducing overall production complexity.

www.littelfuse.com

High-Efficiency Power Chokes

ITG Electronics highlights its portfolio of power factor correction (PFC) chokes: the PFC282820 Series, purpose-built for 800 – 5000 W continuous conduction mode PFC boost converter applications in high-wattage industrial and automotive systems. Featuring a 27.5 mm x 20 mm footprint with a height of 28.5 mm, the PFC282820 Series helps design engineers to meet demanding power density requirements without sacrificing efficiency. A wider configuration (27.5 mm x 28.5 mm) is also available to support higher current handling needs, all within the same 5,000 W power ceiling. Part of ITG’s Cubic Design PFC Choke lineup, the PFC282820 Series utilizes flat wire and a square core to deliver enhanced power density and thermal performance compared to traditional toroidal alternatives. The series is engineered to support the evolving requirements of AC to DC power conversion in next-generation industrial and automotive electronics. The PFC282820 Series supports inductance ranges from 33 – 330 µH, with custom values available upon request.



High-current output options can handle up to 46 A, with approximately 50 % roll off for superior performance under load.

www.itg-electronics.com

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