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Bodo´s Power Systems®

Electronics in Motion and Conversion

May 2026

PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the

- **Differential inductance** $L_{diff}(i)$ and $L_{diff}(\int Udt)$
- **Amplitude inductance** $L_{amp}(i)$ and $L_{amp}(\int Udt)$
- **Flux linkage** $\psi(i)$
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** $B(i)$
- **DC resistance**

Also suitable for 3-phase inductors

APPLICATIONS

Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**

- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

AVAILABLE MODELS

Model	max. test current	max. pulse energy
DPG10-100B	0.1 to 100A	1350J
DPG10-1000B	1 to 1000A	1350J
DPG10-2000B	2 to 2000A	1350J new model
DPG10-2000B/E	2 to 2000A	2750J new model
DPG10-3000B/E	3 to 3000A	2750J
DPG10-4000B/F	4 to 4000A	8000J
DPG20-10000B/G	10 to 10000A	15000J

Technological leader in pulsed inductance measurement for 20 years

www.ed-k.de

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Supporters & Friends

A Media
Katzbek 17a
24235 Laboe, Germany
Phone: +49 4343 42 17 90
Fax: +49 4343 42 17 89
info@bodospower.com
www.bodospower.com

Founder
Bodo Arlt, Dipl.-Ing.
bodo@bodospower.com

Editor in Chief
Alfred Vollmer, Dipl.-Ing.
alfred@bodospower.com

Correspondent Editor Bavaria
Roland R. Ackermann, Dipl.-Ing.
roland@bodospower.com

Editor China
Min Xu – xumin@i2imedia.net

US Support
Rusty Dodge
rusty@eetech.com

Creative Direction & Production
Bianka Gehlert
b.gehlert@t-online.de

Publisher
Holger Moscheik
holger@bodospower.com

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Where it all began

May is usually the month when the power electronics community meets in Nuremberg for PCIM, but not this year. Every now and then, the event needs to move to June, presumably for availability reasons with the convention center. This year, this is actually pretty awesome, because for Bodo's Power Systems a circle will also close next month. It was at this exact event, back in May 2006, when Bodo, at the show, ended his cooperation with a former publication, and made the decision to start his own magazine, as a one-man-show, immediately. Actually, my family and I were all there during this memorable event. Today, we are all working for the magazine.

As the circle closes, we will start to celebrate the 20th anniversary this year, at the very location where it all began. Bodo returned to his hometown back then, and within a few days he found someone for the layout-design, and also someone who designed his website and e-newsletter. The rest is history! Well, the gentleman who helped with the website is still around today, and also the daughter of the layout-designer. Rumour has it, she was already heavily involved in the design at the beginning of the magazine. That's great proof of Bodo's commitment to continuity, and as I am now taking over more and more responsibility, I am very grateful for still having them on our team!

Please visit us at our booth at PCIM, you can find us in hall 4, booth 423, and celebrate this very special occasion with us. We'll bring the whole team to Nuremberg, and Bodo will be incredibly happy to share memories and have a chat about the last 20 years and all that has happened in our industry during the lifetime of the magazine. Unfortunately, although we will have time for many stories and celebrations, the trip will also be a "work trip".

The editorial team will, of course, be available for meetings, and as always we will host a panel on Wide Bandgap at the technology stage, which you can also find in hall 4. We will cover SiC in two sessions on Wednesday, and host one GaN session on Thursday. A great appetizer for "Bodo's Wide Bandgap Event 2026", which will take place December 1 and 2 at the Hilton Munich Airport again.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive, of every issue of the magazine, is available for free at our website bodospower.com.

My Green Tip of the Month:
The current skyrocketing prices for fuel make this an easy one. Any opportunity to leave the car standing makes it beneficial in two ways now: for the environment AND your wallet. Use public transportation whenever you can!

Holger

Events

SEMICON Southeast Asia 2026
Kuala Lumpur, Malaysia May 5 – 7
https://expo.semi.org/southeastasia2026

CWIEME Berlin 2026
Berlin, Germany May 19 – 21
https://berlin.cwiemeevents.com

ISPSD 2026
Las Vegas, NV, USA May 24 – 28
www.ispsd2026.com

EnerHarv 2026
Madrid, Spain May 27 – 29
www.enerharv.com

ECCE Asia 2026
Nagasaki, Japan May 31 – June 4
https://ipec2026.org

GaN Marathon 2026
Florence, Italy June 7 – 10
https://ganmarathon.com

PCIM Expo & Conference 2026
Nuremberg, Germany June 9 – 11
https://pcim.mesago.com/nuernberg

Sensor+Test 2026
Nuremberg, Germany June 9 – 11
www.sensor-test.de

EV Tech Expo Europe 2026
Stuttgart, Germany June 9 – 11
www.evtechexpo.eu

Bodo's Wide Bandgap
EVENT 2026

December 1 - 2
Hilton Munich Airport
Mark your Calendar!

"Meet
the TOP EXPERTS
for SiC and GaN!"

December 1
Opening Roundtable
& Come Together

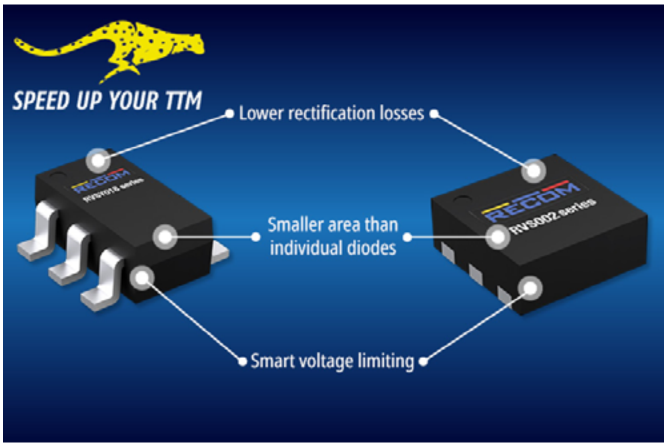
December 2
Conference
& Tabletop Exhibition

bodoswbg.com

Bodo´s Power Systems®

Entering the World of Discrete Power

RECOM is rolling out a range of rectifier ICs to allow engineers to build their own discrete DC/DC isolated power supplies. The range includes a fully integrated full-bridge rectifier with smart output-voltage limiting, that occupies less board space than 4 diodes, and a rectification controller IC for use with an external FET, suitable for either high-side or low-side rectification. The RVS002 integrates two N-channel MOSFETs and two Schottky diodes in a DFN2*2 package to create a low-loss full bridge rectifier capable of handling up to 3 W. A built-in intelligent voltage limiter prevents the output voltage from rising excessively under no load conditions, which increases voltage stability. When the power supply is under load, the limiter remains inactive and does not draw current. The RVSY018 synchronous rectification controller operates at up to 700 kHz, with a 30 ns turn on and 10 ns turn off characteristic, making it suitable for high-frequency power conversion applications. The rectification IC is self-powered from a single AC input allowing either high side or low side rectification. The controller supports both CCM and DCM operation and is compatible with both QR and active clamp flyback topologies. Both rectifier solutions operate over a -40 °C to +125 °C temperature range and are reflow oven solderable.



www.recom-power.com

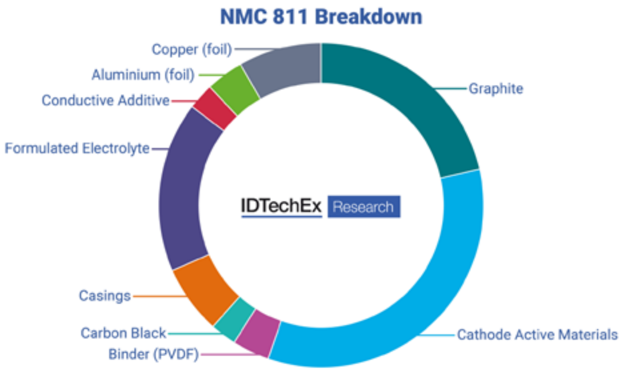
PCIM Europe 2026 puts AI in the Spotlight

From 9 to 11 June 2026, the PCIM Expo & Conference will once again take place in Nuremberg/Germany. With over 650 exhibitors and more than 500 presentations, this power electronics event will offer a comprehensive program for trade visitors. With the new AI & Data Centers Stage, this year's trade fair and conference program will focus on the topic of artificial intelligence and data centers for the first time. The escalating energy needs of modern data centers are driving demand for high-performance, energy-efficient, and sustainable solutions. With the AI & Data Centers Stage, the PCIM Expo 2026 places a distinct emphasis on two of the most important future trends in power electronics. This stage brings together expert presentations and best practices addressing the growing influence of artificial intelligence and the escalating energy demands of modern data centers. PCIM will cover the entire power electronics value chain, ranging from power semiconductors, test and measurement technologies, and automation solutions to materials for different fields of application, including the aviation industry. Last year the event welcomed 685 exhibiting companies, 16,500 visitors, and more than 800 conference participants from the realms of science and industry.

https://pcim.mesago.com

Materials Trends for EV Li-ion Cells: Market and Technology

IDTechEx's market report "Materials for Electric Vehicle Battery Cells and Packs 2026-2036: Technologies, Markets, Forecasts" explores the materials that act as the foundation for the EV battery cell market and predicts that the overall cell material market for electric vehicles will reach US$154 billion by 2036. What will be the next steps? Higher percentage silicon anodes are being developed that would significantly improve cell energy density. IDTechEx predicts a shift towards silicon over graphite in premium vehicle anodes towards the end of the next decade. There is significant development of semi-solid and solid-state electrolytes to replace liquid electrolytes and enable use of higher energy density anode materials. This would require polymer, ceramic or oxide-based materials. This is expected to be limited, however, due to challenges with scaling manufacturing. Furthermore, development of LMFP, LMO and LNMO is approaching commercialization, shifting the cathode materials market away from cobalt and towards low-cost manganese. Lithium anodes enable extremely high energy density, but increases battery degradation and reduces cycle life. A small proportion of the market may shift to lithium by the end of the next decade, reducing graphite demand, especially in an anode-less cell design. Lithium anodes can also be paired with low-cost sulfur cathodes to develop high gravimetric energy density cells. This would entail a reduction in other cathode material intensities, though market share is expected to be very limited in the EV sector.



www.idtechex.com

ROHM
SEMICONDUCTOR

EcoSiC

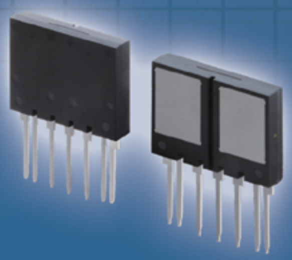
Meeting your needs. Portfolio expansion.

SiC Power Modules

HSDIP20

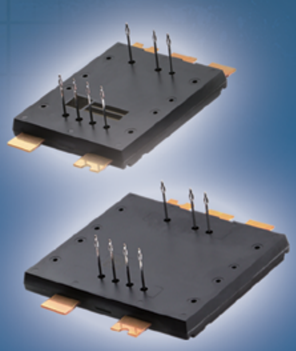
- Compact 4-in-1/6-in-1
- Circuit-oriented element layout (4-in-1, 2-in-1, etc.)
- Improved heat dissipation characteristics

DOT-247



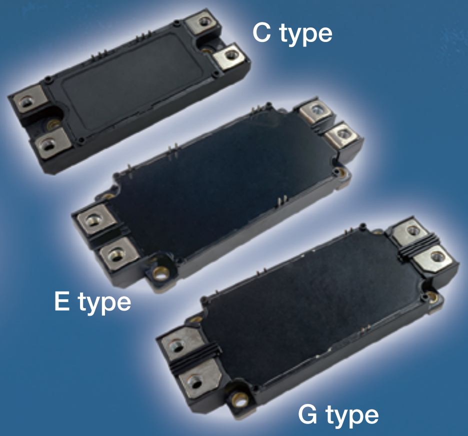
- 2-in-1 TO-247-4L
- Improved heat dissipation performance
- Half-bridge/source common

TRCDRIVE pack™



- Parallel multi-chip configuration provides high current capability
- Low Ls improves switching performance
- Reduced size through improved heat dissipation performance

Case type



- Parallel multi-chip configuration provides high current capability
- Gel encapsulation in case

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www.rohm.com

New Date for PCIM India

The PCIM Asia New Delhi Conference has been postponed by one day and will now take place from 10 to 11 December 2026 at the Yashobhoomi Exhibition and Convention Centre (IICC) in New Delhi. This adjustment was made due to organizational conditions and enables the conference to be executed even better. Following its debut last year, the event is returning to India and inviting scientists, industry experts and emerging talent from industry and research to submit abstracts on current topics in power electronics. The call for papers is open until 21 May 2026.

www.pcim.in

Global Distribution Agreement for Silicon Power MOSFETs

iDEAL Semiconductor has signed a global distribution agreement with DigiKey, who will stock the semiconductor manufacturer's products. Under the agreement, DigiKey will distribute iDEAL's portfolio of silicon MOSFETs. The collaboration provides customers with immediate online access to inventory through DigiKey's global e-commerce platform. iDEAL Semiconductor's SuperQ™ technology is designed to enable improved energy efficiency and power density while maintaining the reliability, manufacturability, and cost structure of standard silicon processes. The devices are suited for applications including battery management systems (BMS), motor drives, fast charging, data center power architectures, and other high-performance power conversion systems.

www.idealsemi.com

AI-ready UPS Systems Validation

Unlike traditional workloads with slow and predictable power variations, modern AI creates "pulsed loads", where processors switch rapidly between idle and full capacity. Power demand can swing from 0 % to 100 % and back in milliseconds, creating erratic "on-off" cycles that place power infrastructure under severe stress. Uninterruptible power supply (UPS) systems must now also function as a dynamic power conditioner capable of reacting to these variable load swings in real time. If it cannot manage these pulses effectively, they can be reflected back to the grid or backup generators, threatening overall system stability or even breakdown. Vertiv provides critical infrastructure technologies, including large power converters. Its Power Center in Bologna/Italy needed to validate new Input Power Smoothing algorithms for its Vertiv™ Trinergy™ UPS systems. These intelligently draw energy from the UPS batteries during peak pulses, shielding the upstream generator from the erratic behavior of an AI load. Veritiv created a fully integrated measurement ecosystem from Yokogawa, anchored by the WT5000 Precision Power Analyzer, DL950 ScopeCorder, GM10 Data Acquisition System, and tied together by the IS8000 software platform. This configuration allows measuring currents of up to 5000 A, where the WT5000 Precision Power Analyzer provides primary power analysis. The DL950 ScopeCorder captures the transient behavior of the "pulsed loads" using its 16 channels. Connecting these domains is Yokogawa's IS8000 software, which synchronizes the instruments using the IEEE 1588 Precision Time Protocol (PTP).

www.yokogawa.com

Positive Trade Show Echo

Around 36,000 visitors went to Nuremberg/Germany in order to attend the trade show "embedded world 2026", which took place from 10 to 12 March, 2026. This is a growth of more than 13 percent compared to the previous year. With its range of topics and technical exchanges, the embedded world Conference once again sent a signal about the industry's strength in 2026. Technical presentations, scientific insights and dialogue between experts were an integral part of the embedded world conference, which is targeted to the developer community. Of course, all these embedded systems need power supplies, and that's why major power companies showed their solutions in Nuremberg. The next embedded world in Nuremberg will take place from 16 to 18 March 2027.

www.embedded-world.de

TOSHIBA

High Power SiC MOSFET Modules

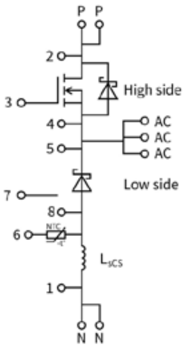
Package highlights

- High reliability by using silver sintering technology
- Equipped with current sensing terminal & built in thermistor
- High channel temperature (Tch, max=175°C)
- Low stray inductance
- Low thermal resistance

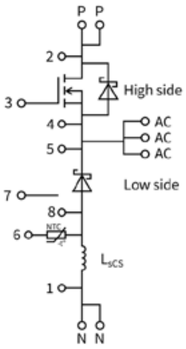
Featured products

•	3300V	800A - MG800FXF2YMS3
•	3300V	500A - IX500FXF2YMS4
•	2200V	1500A - IX1500YD2YMS4

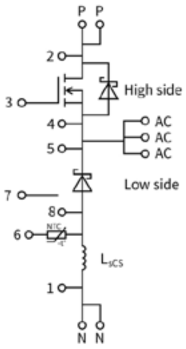
Internal circuit options



Half bridge



Chopper low



Chopper high

Valid for MG800FXF2YMS3 only

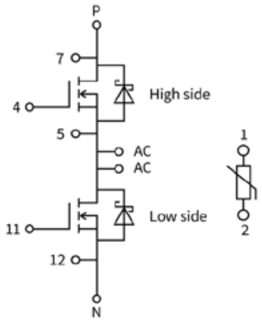
Package highlights

- High mounting compatibility with Si IGBT module
- Lower loss characteristics than Si IGBT module
- High channel temperature (Tch, max=150°C)
- Low stray inductance
- Low thermal resistance

Featured products

•	1200V	400A - MG400Q2YMS3
		600A - MG600Q2YMS3
•	1700V	250A - MG250V2YMS3
		400A - MG400V2YMS3
•	2200V	250A - MG250YD2YMS3

Internal circuit options



Half bridge

Excellence in Power

Visit us at PCIM 2026 -Hall 4A-227

toshiba.semicon-storage.com

Production Site in Singapore

Wevo is expanding its presence in the Asia-Pacific region with a production site in Singapore. Located in the Tuas industrial area, the facility will serve as a key hub for supplying customers with locally manufactured polyurethane systems that offer proven solutions across a wide range of industries. This facility will feature identical production processes and quality standards to those of the company's headquarters in southern Germany. In addition to a fully integrated production line, the building in the Tuas industrial area also offers ample storage and packaging capacity. The start of production is scheduled for the third quarter of 2026. The initial focus will be on the polyurethane portfolio, including polyurethane potting compounds, adhesives and sealants for electronics manufacturing – for instance through dispensing under atmospheric pressure or vacuum. Wevo products protect sensitive components against chemicals, vibration, foreign matter, dust, humidity and high temperatures.

www.wevo-chemie.com

Partnership for SiC-based Solid-State Transformers

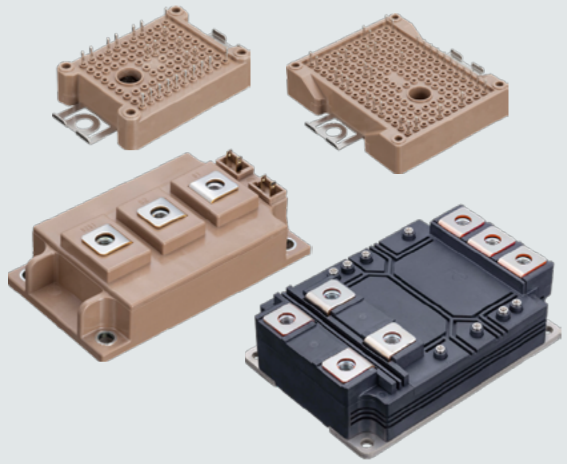
Infineon Technologies and DG Matrix, an expert in Solid-State Transformer (SST) solutions, are partnering to enhance the efficiency of power conversion required to connect AI data centers and industrial power applications to the public grid.

As part of the collaboration, DG Matrix will source latest-generation silicon carbide (SiC) technology from Infineon for use in its Interport™ multi-port solid-state transformer platform. A solid-state transformer replaces conventional copper and iron-based transformers. It features higher efficiency, significantly greater power density (smaller size and lower weight) and improved scalability. Compared to conventional transformers, SSTs are up to 14 times smaller and 40 times lighter. SSTs enable direct power conversion from the medium-voltage levels supplied by the grid to the low voltages required by applications such as AI data centers, electric vehicle (EV) charging infrastructure, renewable energy systems and industrial microgrids. Infineon expects that the global semiconductor market volume for SSTs could reach up to one billion US dollars in the next five years.

www.infineon.com

Fuji Electric
Innovating Energy Technology

All-SiC Trench gate MOSFET – 3rd Generation

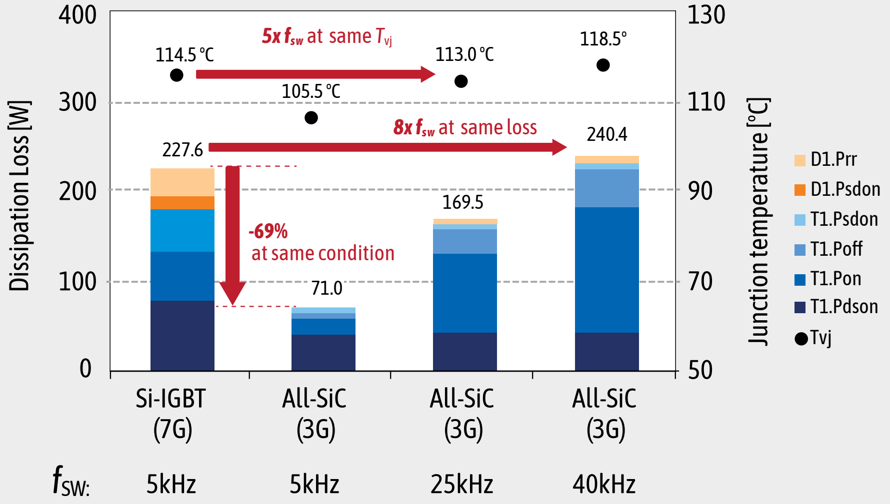


MAIN FEATURES

- Reduced $R_{on}A$ at low and high temperature
- SBDs are no longer required. 3rd generation modules provide increased area for the MOSFET's active region.
- High reliability – stable $V_{GS(th),}$ no bipolar degradation
- Good trade-off between $R_{on}A$ and $V_{GS(th)}$
- Simplified production process for cost effectiveness, improved yield rate

WELDING
TRAIN
SOLAR
MV-INV
SERVO
UPS
WIND

Module: 1200V / 600A 62 mm module
Condition: $f_O = 50Hz$, $V_{DD} = 600V$, $\cos\varphi = 0.9$, $m=1$, $T_{vj} = 150°C$,
$V_{GE} = +15V/-15V$(Si-IGBT), $V_{GS} = +15V/-3V$(All Sic),



www.fujielectric-europe.com

Report on GaN Semiconductor Reliability and Robustness

Efficient Power Conversion (EPC) has released its Phase 18 Reliability Report, providing insights into eGaN™ device reliability. The report builds on previous work by closing the gap between lab-generated reliability testing and real-world device performance across mission profiles. It introduces additional methodologies to better predict device lifetime under application-specific stress conditions, shaped through close collaboration with customers and supported by peer-reviewed research and international conference publications. The report emphasizes the significance of comprehending the fundamental wear-out mechanisms in GaN HEMTs and presents a quantitative methodology for estimating the overall device lifetime based on the predominant stress conditions experienced during operation. The methodology allows for more accurate lifetime predictions across a wide range of applications by combining different stress factors, like voltage, current, temperature, and duty cycles. Phase 18 is similar to earlier reports, but it goes much deeper into the main wear-out mechanisms. These include the reliability of gates in pGaN structures, the ability to handle stress and overvoltage (robustness), the maximum current density, and the wear-out of thermomechanical devices in both chip-scale and QFN-packaged formats. The report also looks at reliability in dynamic switching conditions and high-frequency operation, which gives us a better idea of how things work in real life. In addition, the report introduces mission-specific reliability evaluations, including motor drive applications characterized by rapid current transients and varying load conditions. A customized testing methodology is presented to emulate these application-specific stress profiles, demonstrating the robustness of EPC's GaN technology under such conditions.

www.epc-co.com

Distributor and Semiconductor Manufacturer cooperate on holistic Design Suite

DigiKey announces the availability of an enhanced eDesignSuite experience, developed through a collaboration with STMicroelectronics (ST) and Ultra Librarian. The tool environment allows engineers to design, simulate, refine and confidently validate their projects using ST components and to purchase their entire bill of materials (BOM) directly from DigiKey in a few steps. The eDesignSuite, developed by ST, is a free, publicly accessible, no-license-required online design platform that provides a unified workflow for power management, signal conditioning, NFC/RFID applications and other design domains. The collaboration with DigiKey and Ultra Librarian expands the platform's capabilities by tightly integrating component models, simulation flows, BOM management and multi-CAD exports.

The eDesignSuite experience now also provides e.g. the following capabilities: Integrated thermal and electrical simulation support through SIMPLIS/SIMetrix, enabling deeper performance verification and design confidence. Real-time BOM refinement with live impact analysis, allowing engineers to immediately see how parameter changes affect design choices and performance. Seamless export of schematics and BOMs to multiple CAD environments, including OrCAD, Altium and Eagle. Application-specific design support, including power management design, thermal-electrical simulation, signal conditioning and NFC/RFID calculators.

www.digikey.com

Strategic Agreement for Critical Metals Recovery

INDIUM CORPORATION®

Indium Corporation® has executed a long-term offtake framework agreement with Flash Metals USA Inc., a wholly owned subsidiary of Metallium Limited (MTM), for the supply of critical metals recovered using Metallium's Flash Joule Heating technology. Under the agreement, Indium Corporation will purchase metals recovered from secondary raw materials and electronic scrap through Flash Metals USA's recycling operations, including gallium, germanium, copper, tin, gold, and indium. The agreement, with an initial term of 10 years with automatic five-year renewal options, establishes a robust and diversified supply chain for U.S.-based recovery of strategic metals. Indium Corporation operates its own metals and compounds reclaim and recycle program that provides specialized recycling services for the electronics, semiconductor, display, battery, and other specialty material industries.

www.indium.com

Integrated Power Module Family adds Silicon Carbide 3-Phase Module

Apex Microtechnology recently announced the release of the MSA303, the latest member to its family of Integrated Power Modules. The module utilizes Silicon Carbide MOSFET technology to improve efficiency over other devices in its class. Three fully independent half-bridges provide 40A of continuous current, with 600V supply. The MSA303 is built on a thermally conductive, but electrically isolated substrate to provide versatility and ease in heatsinking.

“This device represents a significant step forward in power density for high-voltage motor drive applications,” said Jens Eltze, Director of Business Development at Apex Microtechnology. “By combining Silicon Carbide MOSFETs, integrated gate drive, and comprehensive protection features into a single module, we enable engineers to reduce design risk, improve efficiency, and accelerate time to market. This product reflects our continued commitment to delivering high-performance power analog solutions for demanding applications.”

By integrating three half-bridges, gate drive circuitry, and protection features into a single module, the MSA303 supports system designs where size, weight, and power (SWaP) are critical considerations. Its compact architecture enables high power delivery within a small footprint, helping engineers optimize space in demanding application environments.

The MSA303 protection features include under-voltage lockout (UVLO) and active Miller clamping to improve reliability. Silicon Carbide Schottky Barrier free-wheeling diodes are included in parallel with the body diode of each MOSFET, eliminating the need for external output protection diodes. The integrated gate drivers provide isolation between the inputs and high-voltage outputs, and by integrating the gate drive with the output MOSFETs, parasitics that impact switching behavior are kept at a minimum, improving switching characteristics while reducing potential oscillations.

The MSA303 targets high-power applications such as motor drive systems, variable frequency drives (VFDs), DC/AC converters, power inverters, and test equipment. Its integrated architecture and use of Silicon Carbide MOSFETs enable high-efficiency switching, reduced parasitics, and improved thermal performance, making it well suited for designs requiring high power density, fast switching, and reliable operation under demanding conditions.

Apex Microtechnology specializes in high-performance power operational amplifiers, pulse width modulation (PWM) amplifiers, integrated power modules, precision ICs and precision voltage references (VRE). Product form factors include monolithic ICs, board-level “open frame” modules, and traditional hybrid designs capable of delivering up to 40 A of continuous output current and voltage supply ranges from 5 V to 2500 V. Target applications focus on high power precision control of current, voltage and speed for the industrial, test and measurement, aerospace & defense, and medical markets.

www.apexanalog.com

Applied Power Electronics Conference and Exposition – APEC 2026

APEC, a leading yearly event in applied power electronics, provides a meeting site to facilitate worldwide power electronics personnel in sharing their latest technological learnings, insights, and product developments.

By Don Gerstle, US-Correspondent, Bodo's Power Systems

The 2026 Applied Power Electronics Conference and Exposition (APEC) was held in San Antonio, Texas, USA from Sunday, March 22 through Thursday March 26, with preliminary PSMA & PELS Magnetics and Capacitor workshops on Saturday March 21. These workshops are traditionally held just before APEC starts.

APEC 2026 was sponsored by the Power Sources Manufacturers Association (PSMA), the IEEE Power Electronics Society (PELS), and the IEEE Industry Applications Society (IAS). APEC covers the practical, applied, and theoretical facets of power electronics, from low to high voltage and low power to high power applications, across many fields aimed at students, engineers, and all other personnel involved in the design, application, and utilization of power electronics.

APEC 2026 was held at the Henry B. González Convention Center, with 57,300 sq. ft. of exhibit space, over 70 meeting rooms, and two large ballrooms, where Plenary sessions were held in one ballroom. The Convention Center is in downtown San Antonio beside the picturesque River Walk.

Just before APEC started, PSMA and PELS held two full day parallel workshops. One was on Magnetics, on better ways to model, characterize, and improve core design, coil design, winding, and improvements in materials and design processes.

There was a record level attendance at the Magnetics workshop, with a full calendar of events. During breakfast, lunch, and at the end of the meeting, there was networking with the other attendees, along with poster presentations and technology demonstrations run by academia and industry SMEs from across the world on magnetics products, applications, and test equipment. After breakfast, for the rest of the morning there were back to back presentations, kicked off with Peter Zacharius from the University of Kassel presenting "Physics Based Model Approaches to Develop Analytical Calculations and Simulations of Magnetics Losses in Ferrites". The rest of these presentations focused on other comprehensive discussions on modeling magnetics. Each presentation was followed by Q&A, where there were excellent discussions between industry SMEs and the SME speakers on problems, next steps, and potential solutions to magnetics challenges they faced. This was followed by a panel discussion with the speakers answering and discussing more questions from the attendees. After lunch there was another set of presentations focused on applying design basics/AI to achieve design automation for the design of magnetic components, with a panel session at the end to answer further questions from the audience.

The other parallel workshop was on Capacitors, which had the latest updates in research and practical applications, with technical presentations from academic and industry SMEs. There were multiple interactive technology demonstrations. This workshop targeted power electronics designers, researchers, end users, and supply chain personnel.

APEC 2026 had a huge turnout, with 5,100+ attendees registered, from 56 countries and regions. APEC activities included 18 Professional Education Seminars with over 1,200 attendees registered, 4 Plenary Sessions, over 570 Technical Sessions, over 170 Industry Sessions, 2 Debate Sessions, multiple Exhibitor Presentations, and an exhibition floor with 322 company exhibitors. This year featured the Student Demonstration Competition for the first time at APEC. All submittals were pre-reviewed and screened to select the best material and ensure compliance with the conference's standards. There were 750+ paper reviewers.

The migration of the data centers to 800VDC distribution for future AI and other data centers, coupled with dramatically increased AI current levels/density, along with the associated power conversion and product changes from the power grid to the AI GPUs, was an underlying theme on a lot of the technical sessions. These changes will impact power devices from the power grid through power at the device level. This will evolve as the industry develops and refines the power conversion stages with the 800VDC architecture. Multiple companies, including Microchip, TI, and Toshiba, covered approaches to this architecture in their exhibits.

There were many sessions on WBG devices, both GaN and SiC, including design improvements in different parameters, drivers, power stages, increased density and integration, vertical power, modeling, measurement techniques, reliability, efficiency, EMI mitigation, along with applications in many areas including AI, data center power, EVs, and associated charging. There were also sessions on improvements on conventional technology.

The Professional Education Seminars were held on Sunday March 22 and Monday morning March 22. These were a combination of theory and practical applications. There were six tracks, including

1. Devices
2. Convertors
3. Control
4. Applications
5. Magnetics & EMI/EMV & Grid (1)
6. Magnetics & EMI/EMV & Grid (2)

Each of the speakers presented a substantial amount of comprehensive material geared towards the power electronics audience.

Monday afternoon there were four Plenary Sessions, with industry/academic leaders discussing current key energy issues and potential future impacts, challenges faced by industry and academia, and potential ways to address these. These were well done and inspirational, with each receiving a strong round of applause. These included

1. HVDC Distribution for Future AI Data Centers
2. Enabling Copernicus: Power Electronics at the Heart of Earth's Health Monitoring
3. Why Now is the Time to Address Power Semiconductor Sustainability
4. MagNet Challenge: The Serendipity when Power Magnetics meet AI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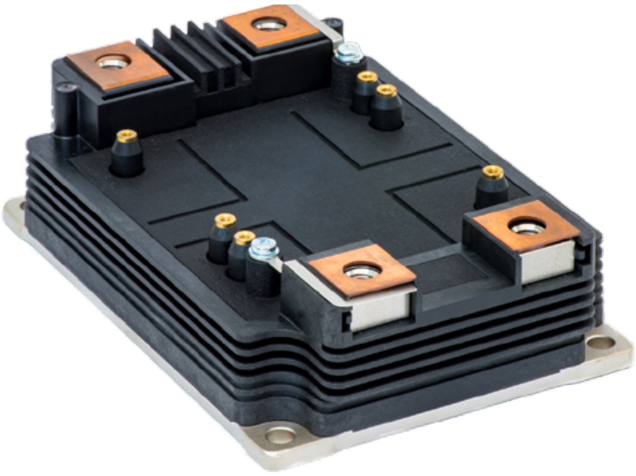

Monday evening there were three social/networking events; the APEC 2026 Welcome Reception, the MicroMouse Contest, and the Young Professionals Networking Reception. The APEC 2026 Welcome Reception launched the opening of the Exhibition Floor after the end of the Plenary Session.

There were 322 exhibits for conference attendees to see the latest components, products, and services across a comprehensive range of power aspects and applications. These included design materials, active and passive devices, design tools, power supplies, test equipment, applications geared towards the new 800V power architecture, software, and multiple services. The Exhibit Hall was open again all day Tuesday, and Wednesday morning through early afternoon.

In the Exhibit Hall OnSemi discussed their new vertical GaN with its performance benefits versus lateral GaN devices. Tektronix released their new oscilloscope probe with a high bandwidth and wide temperature range to facilitate measurements in harsh environments, including GaN and SiC applications.

At the Street Level there was a Micro Mouse Contest to see which robotic mice that the entrants had designed and made got through the maze the fastest. The Young Professionals (YPs) Networking Reception gave the YPs a chance to network with other YPs, along with Industry and Academia professionals.

Tuesday through Thursday APEC had parallel Technical and Industry sessions. There were over 570 Technical Sessions from academic institutions, industry, and government agencies, that covered a wide range of topics on power, including modeling, simulation, fabrication, design, and application, ranging from component to module to circuit to systems level, from low voltage to high voltage, and from low power to high power. Some technology areas that were covered in the range of topics included the latest GaN and SiC, with more integration of drivers and WBG power devices, with some focus on the new 800VDC architecture applications.

The Industry session presenters discussed their latest updates in all aspects of power electronics.

Tuesday there was a Spouse and Guest Lunch as a follow-up to the Monday Spouse and Guest Breakfast. Tuesday afternoon there was a Student Job Fair that provided students a great means to meet with power electronics companies to discuss job opportunities.

Following the Student Job Fair, there were two Debate Sessions, where a Chair led a team of SMEs, who gave their opinions on critical power issues faced by the power community, then had Q&A with the audience. There were two topics this year:

1. Bidirectional Devices: Will emerging bi-directional devices have wide adoption or not?
2. In Power Electronics, Should the future rely more on Generative AI for Design or Predictive AI for Optimization?

Tuesday evening there was a PELS Mentorship Round Table for ready access to academic and industry leaders for students and engineers to discuss their career and next steps.

Tuesday afternoon and Wednesday afternoon there were Student Demonstrations, where student teams from universities worldwide showcased their innovative research in power electronics and related fields. Teams were encouraged to present prototypes, along with posters, slides, or videos on their project. Each project was judged by SMEs from industry and academia on multiple aspects, with first through third place projects receiving certificates and cash awards.

The Expo Theaters (1–4) in Hall 4 had exhibitor sessions focused on GaN technology, data center power, and EMI/EMC, with more information than was available at their booth on their respective components, products and services, on Tuesday afternoon, with additional sessions on Wednesday.

Wednesday morning there was a PELS Women in Engineering (WIE) Breakfast with a presentation, “From Doubt to Drive: Career Confidence for a Fast-Changing World” by Seema Bakshi, followed by a Networking Session.

Wednesday evening there was a Social Event at The Espee, a boutique amphitheater and events venue near the Convention Center. Buses were set up to take people to The Espee from the convention center and back again.

Thursday morning the remainder of the Technical Sessions were completed, along with the rest of the Industry Sessions. AmberSemi chaired an Industry Session titled “Vertical Power for AI Data Centers.” Despite this being the last day of APEC, there was a standing room only crowd there in a 250 person room. This included speakers from AMD, Nvidia, Global Foundries, and AmberSemi, exploring upcoming power architectures for future AI infrastructure, and the many challenges and work underway to address multiple limiting / interactive issues including dramatically increasing current/current density/power needed, reduced ASIC voltages, reliability, magnetics, and 3D space challenges even with vertical power, particularly as server heights are being reduced to pack more processing in each rack. AI systems are becoming power limited before becoming compute limited.

Thursday afternoon there were Dialog Sessions on 31 different topics, from AC-DC Converters through Power Electronics Applications. Papers selected for the Dialog Sessions were picked for topics of interest to smaller groups of APEC attendees. They were presented in poster format, to facilitate more direct interactions between the presenters and the attendees.

Next year APEC will be at the Ernest N. Morial Convention Center, in New Orleans, LA from March 7-11, 2027.

About the Author

Don Gerstle has been in the electronics industry over 50 years, in design, development, test, manufacturing, quality, and reliability, in aerospace, commercial, industrial, and data center hardware, in individual contributor roles as well as management roles. He retired from Google in early March 2026 after 13 years there, leading a team responsible for the quality of some of the new data center hardware, and previously was at Murata Power Solutions and C&D Technologies Power Electronics Division, responsible for the quality and reliability of some of the DC-DC converters and AC-DC power supplies. Don is a member of the IEEE. Don is on the IPC 9-82 committee responsible for the IPC-9592 Requirements for Power Conversion Devices for the Computer and Telecom Industries, for the Draft, A, and B revisions, and the revision C currently underway. He has a BS degree with an EE major from the University of Louisville, and an MSEE from the University of Southern California on a Hughes Aircraft Master Fellowship.
don.gerstle@gmail.com

www.apec-conf.org

Solution-based Manufacturing Platform for Advanced WBG Technologies

Wide bandgap (WBG) semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are driving a new wave of innovation in power electronics. SiC, with a bandgap roughly three times larger than conventional silicon (Si), enables nearly ten times higher critical electric field strength.

By Dr. Ajay Poonjal Pai, Head of Innovation,
and Dr. Wesley Chih-Wei Hsu, Head of Research and Development, Sanan Semiconductor

This allows SiC unipolar devices - such as Schottky diodes and MOSFETs - to operate efficiently in the several-kilovolt (kV) range, a regime traditionally challenging for silicon-based technologies. In addition, these devices offer lower conduction losses under partial-load conditions and significantly reduced switching losses, making SiC highly attractive for demanding applications such as automotive traction inverters, data centers, and photovoltaic (PV) systems. Gallium Nitride (GaN), by contrast, excels in high-frequency and lower-to-mid voltage applications due to its superior electron mobility and lower capacitances. These properties enable extremely fast switching and high power density, making GaN particularly well suited for compact power supplies, server architectures, and fast chargers. As efficiency and miniaturization become increasingly important, GaN is gaining strong traction in consumer electronics and data center power conversion stages.

Driven by electrification trends and the rapid growth of renewable energy systems, WBG-based devices have already achieved significant market penetration. At the same time, the expansion of hyperscale data centers – fueled by cloud computing and artificial intelligence workloads – is further accelerating demand for high-efficiency WBG power semiconductors. These developments are also reshaping power semiconductor supply chains. Product development cycles are shortening, and traditional roles are evolving, particularly in the automotive sector, where OEMs and Tier-1 suppliers are increasingly participating in power module and chip development. However, the high capital investment and specialized expertise required for WBG manufacturing remain major barriers to entry.

This is where Sanan Semiconductor plays a pivotal role as a specialized semiconductor foundry, providing scalable manufacturing platforms that allow fabless companies and system innovators to access advanced SiC and GaN technologies without large upfront investments. In addition to manufacturing capacity, Sanan supports faster time-to-market through mature process design kits (PDKs), standardized platforms, and high-volume production capabilities. With its vertically integrated WBG manufacturing platform, Sanan offers customers the expertise, scale and flexibility needed to manufacture WBG semiconductors across the entire value chain - from crystal growth and substrates to epitaxy, device fabrication, packaging, and final testing. Serving multiple customers and markets further enables economies of scale, helping to reduce overall costs and expand access to WBG technologies.

Vertically Integrated State-of-the-art WBG Mega Factory Leveraging 20+ years of Compound Semiconductor Expertise

In 2020, Sanan established a state-of-the-art vertically integrated WBG mega factory (Figure 1), spanning more than 165 acres and designed with a planned annual capacity of approximately half a million wafers. Built with an investment exceeding $2 billion, the facility supports SiC production from substrates to packaged products across 150 mm, 200 mm, and 300 mm platforms, GaN production from epitaxial wafers to packaged devices. This broad capability enables Sanan to serve customers at multiple stages of the value chain. Vertical integration allows tight control over supply, quality, and cost, creating significant advantages in manufacturing consistency and scalability. These strengths are supported by more than 20 years of experience in compound semiconductor technologies, including GaAs, GaN, InP, lithium niobate (LN), and lithium tantalate (LT), serving applications across optoelectronics, RF systems, optical devices, and power electronics.

Figure 1: Bird's-eye view of Sanan's Vertically Integrated State-of-the-art WBG Mega Factory

Mastering the Material, a Key to Success in WBG Semiconductors!

Manufacturing WBG materials differs significantly from conventional silicon processing. Taking SiC as an example, monocrystals are typically grown using sublimation, unlike silicon crystals, which are grown from a melt. In addition, SiC wafer processing is inherently more challenging due to the material's high hardness and brittle nature, as well as the elevated temperatures required during processing. These factors not only increase production costs but also lead to higher defect densities compared to silicon technologies. As a result, deep understanding of the base material – and the way defects originate and propagate through the manufacturing chain – is critical to achieving high device yield. Recognizing this, Sanan initiated dedicated SiC material research and development in 2017, leveraging its extensive experience in compound semiconductors. This effort led to the in-house production of high-purity SiC powder using proprietary processes, achieving a purity level of 99.9999% (6N). Such purity is essential for producing low-defect substrates capable of supporting high-yield device fabrication. Furthermore, the vertically integrated structure of the manufacturing chain - from powder synthesis to final packaging - enables strong process correlation across all stages, supporting improved quality and yield. Building on several years of successful 150 mm substrate production, Sanan released 200 mm SiC substrates for mass pro-

Lukas Philipp, Daniel Rückert, Thomas Schulze und Steffen Knapp, GVA experts for development

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duction in 2025. These substrates achieve industry-leading specifications in warp, bow, and surface quality, and have been validated for production by major global customers. Figure 2 shows a 200 mm SiC boule (left) and substrate (right) released for mass production in 2025.

The 200 mm SiC substrates were further characterized using X-ray topography (XRT) at Fraunhofer IISB in Erlangen, Germany. Figure 3 presents the characterization result, the XRT topogram of the 11-20 plane, shown in (a), reveals minimal visible dislocations. This observation is further supported by the quantitative defect density measurements shown in (b) and (c), which indicate very low densities of threading screw dislocations (TSD) and basal plane dislocations (BPD) respectively. Specifically, the measured TSD density is approximately 110 cm^{-2}, while the BPD density is approximately 35 cm^{-2}, demonstrating the high crystalline quality required for reliable high-performance SiC device fabrication.

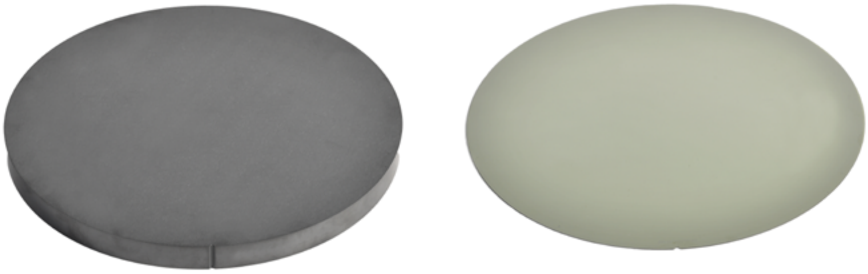


Figure 2: 200mm SiC Boule (left) and Substrate (right) released for mass production

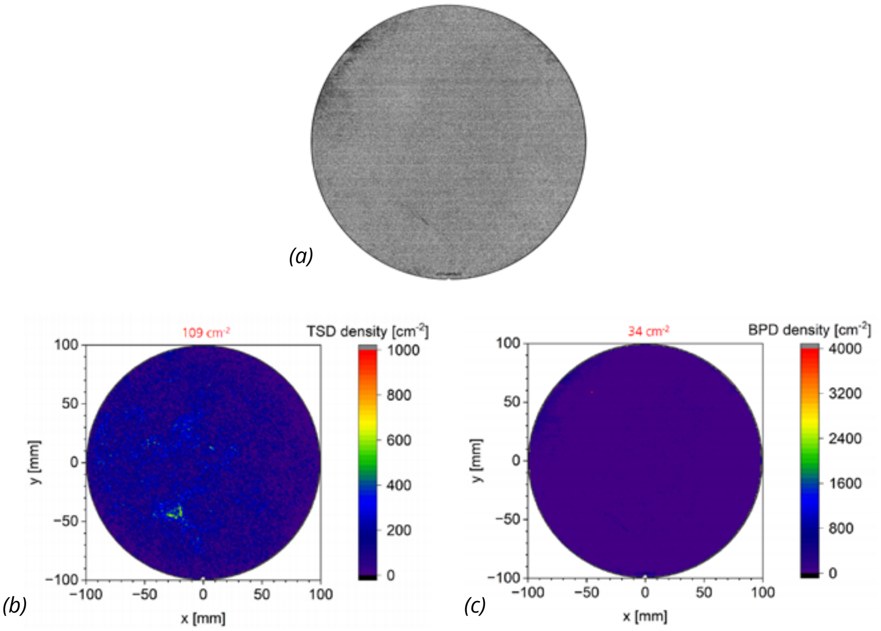


Figure 3: 200mm SiC Substrate currently in mass production: (a) XRT Topogram of the 11-20 plane showing minimal dislocations visible; XRT Imaging showing very low TSD (b) and BPD (c) densities. The test was performed at Fraunhofer IISB, Erlangen, Germany.

300mm SiC Substrates Production Ramping Up

An emerging application area for SiC substrates is Augmented Reality (AR) and Virtual Reality (VR), where large-diameter 300 mm substrates are increasingly preferred. The market for SiC substrates in these applications is projected to grow rapidly, with an estimated compound annual growth rate (CAGR) approaching 200% between 2025 and 2030. Beyond AR/VR, SiC's excellent voltage-blocking capability, combined with its high thermal conductivity, makes it an attractive material for thermal management solutions in AI-driven systems. In particular, SiC substrates are well suited as heat spreaders and interposers in advanced packaging architectures, where efficient heat dissipation and electrical isolation are critical. Together, these emerging applications are driving strong demand for large-diameter 300 mm SiC substrates. In response to this growing market demand, Sanan has initiated the development of 300 mm SiC substrates, which have already been sampled to customers worldwide. Figure 4 illustrates the portfolio of 150 mm, 200 mm substrates, and 300 mm SiC substrates, currently ramping up, for applications such as interposers, heat spreaders, and AR/VR systems. The transition toward volume production of 300 mm substrates represents an important step in supporting next-generation packaging and high-performance computing applications.

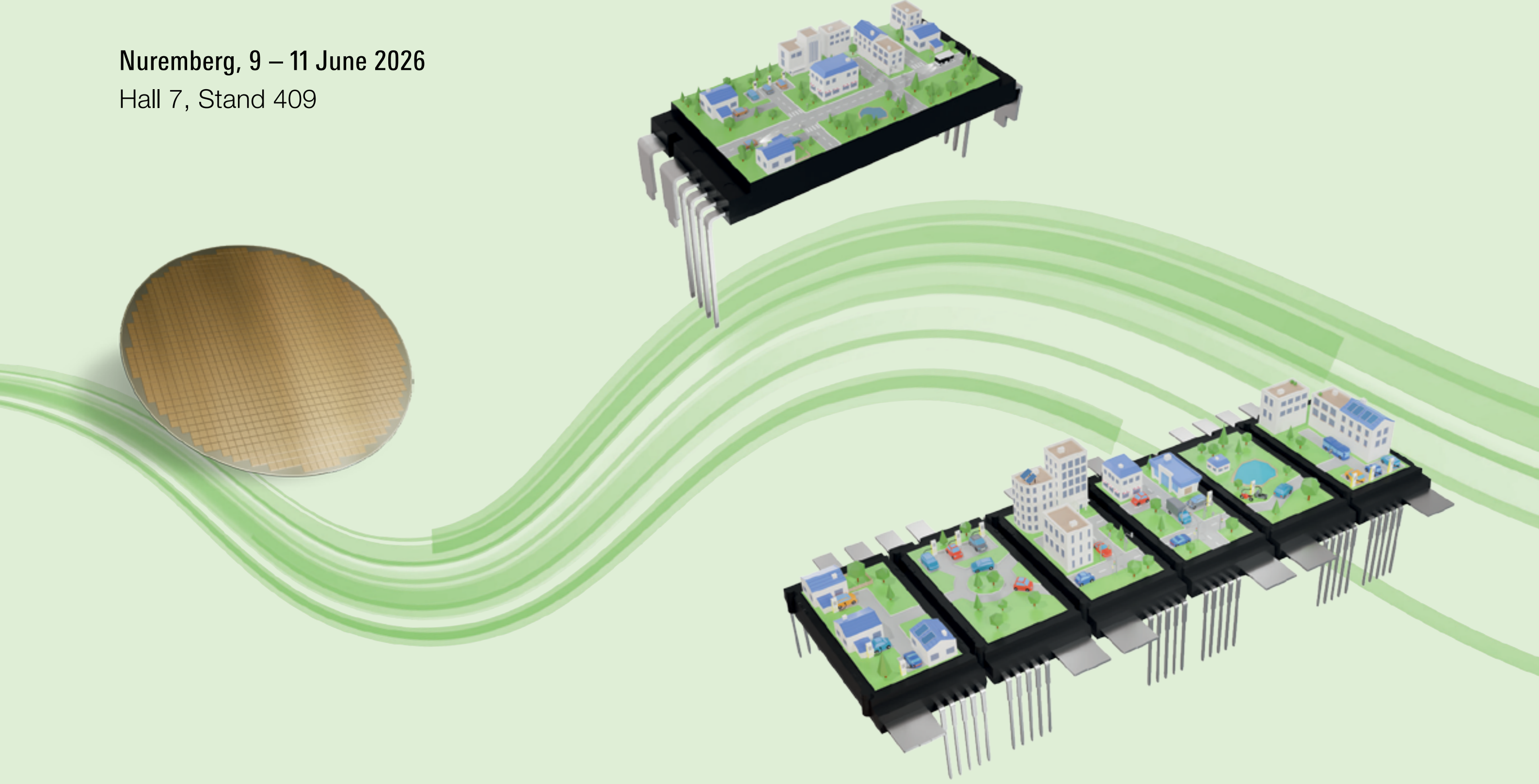
Figure 4: 150mm, 200mm and 300mm SiC Substrates currently ramping up for interposer/ heat spreader/ AR applications

SiC/GaN Epitaxial Wafers

SiC devices are typically fabricated on an epitaxial layer grown on a substrate, where the epitaxial layer serves as the device's drift region. A well-controlled epitaxial process is essential not only to prevent the formation of new defects in the drift layer, but also to suppress the propagation of residual killer defects originating from the substrate. As a result, high-quality epitaxy is a key enabler for achieving both high device performance and high-volume manufacturing yield. Sanan has established mass production of SiC epitaxial wafers on both 150 mm and 200 mm substrates. The company offers epitaxial thicknesses ranging from a few micrometers for low-voltage applications in automotive, consumer, and renewable energy systems, up to thicknesses of 150 µm to support emerging ultra-high-voltage applications, as discussed in the following section. In addition, multilayer epitaxial structures are available, enabling advanced device architectures such as super-junction SiC MOSFETs - widely regarded as the next major step in SiC device evolution. GaN-on-Si epitaxial wafers are also supported, with thickness ranges from 1.5µm to 7 µm.

Thick-film SiC Epitaxy for 10-20 kV Devices

SiC devices are increasingly being explored for ultra-high-voltage grid applications, which require MOSFET and IGBT structures capable of breakdown voltages in the 10–20 kV range. Achieving such voltage ratings demands significantly thicker epitaxial layers - often exceeding 100 µm - approximately ten times thicker than those commonly used in today's SiC devices. In addition, these structures



require extremely low doping concentrations, introducing further complexity in process control. Together, these requirements create new manufacturing challenges, including increased formation of triangle, downfall, and linear defects, which tend to grow with epitaxial thickness. Maintaining tight control over doping uniformity, wafer bow, and warp also becomes increasingly critical. Overcoming these challenges requires deep process expertise and careful optimization, not only in epitaxial growth but also in crystal growth and subsequent polishing steps. Through continuous process refinement and material optimization, Sanan has successfully demonstrated SiC epitaxial layers with thicknesses of up to 150 µm. These advances provide a foundation for enabling next-generation ultra-high-voltage SiC MOSFET and IGBT technologies for future grid infrastructure.

Solution-based Manufacturing Platform for Advanced WBG Technologies

To help customers scale innovative concepts into high-volume products with short turnaround times, Sanan offers a comprehensive Chip Design Platform. This platform includes a reference process flow, TCAD and SPICE modeling capabilities, a Design Rule Manual (DRM) defining layout rules, a Process Design Kit (PDK) that provides the complete design toolkit for the specific technology node, and Process Control Monitors (PCM) to verify and maintain process integrity.

Building on this platform, Sanan has released three generations of SiC MOSFET technologies (Figure 5), covering Rdson classes from 10 mΩ to 1000 mΩ and voltage classes ranging from 650 V to 2000 V. These industrial- and automotive-qualified devices are available as bare dies as well as in standard discrete packages such as TO-247 and D2PAK, including top-side-cooled and customer-specific packages [1]. To date, more than 300 million SiC devices have been shipped globally across a wide range of applications, demonstrating the maturity and scalability of the technology platform.

Sanan's deep technical expertise, combined with large-scale manufacturing capabilities, enables a solution-based approach in which the company acts either as a developer, manufacturer, or both. The flexible process and manufacturing platform allows customers to scale their own technologies into mass production while tailoring device characteristics to specific application needs. This integrated approach accelerates both initial prototyping and production ramp-up, enabling faster time-to-market and earlier revenue generation.

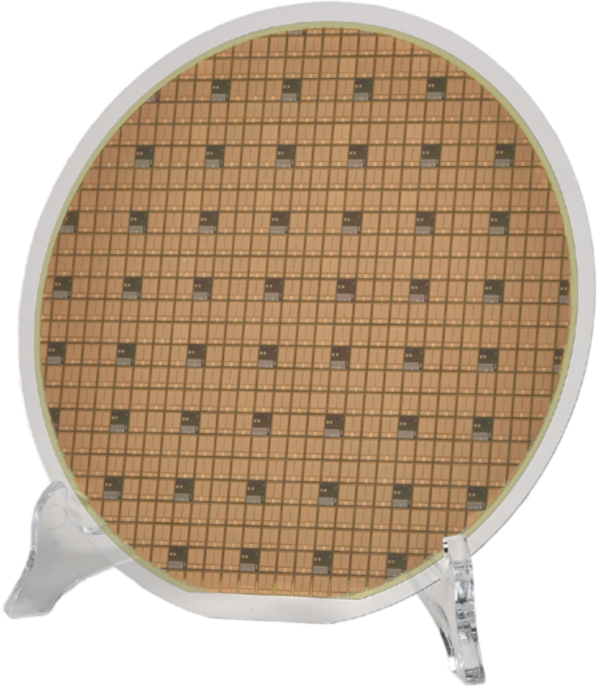


Figure 5: Automotive SiC Planar Mosfet Technology bare-die wafer

As an example of solution-driven optimization, one technology platform was specifically tuned for high-frequency soft-switching applications. Key device parameters - including internal gate resistance as well as input and output capacitances - were carefully optimized to achieve soft-switching behavior with very low switching losses. The resulting technology was benchmarked against nine competing devices available on the market. A calorimetric method was used to evaluate temperature rise, which serves as an indirect indicator of switching losses. The optimized platform demonstrated lower temperature rise compared to most competing technologies, as can be seen from Figure 6. Further details of this benchmarking study are available in [2].

Advanced Applications Demand Advanced MOSFET Technologies

For cost-sensitive applications, a mature SiC planar MOSFET platform based on standard aluminum front-side metallization (FSM) provides a well-balanced cost-to-performance solution. For more demanding environments, nickel–palladium–gold (NiPdAu) FSM can be offered to enhance robustness and performance, while copper-based FSM is available for applications requiring the highest levels of reliability. For applications targeting very low specific on-resistance, i.e., Rds*A figure of merit (FOM), a trench MOSFET-based platform (see Figure 7) is being introduced with cell pitch

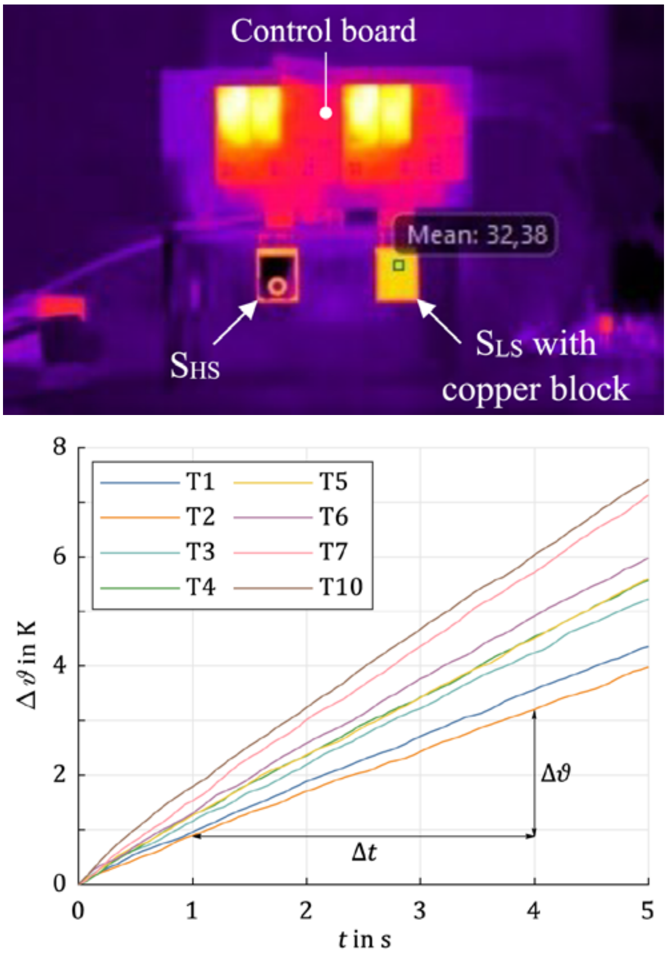


Figure 6: (Top) Thermal Image of Calorimetric Setup used to characterize the switching losses under soft-switching conditions. (Bottom) Measured temperature rise of the copper block. Temperature rise is directly proportional to the switching losses. (Lower deltaT → lower switching losses). T1:Sanan SiC Mosfet, T2-T10: Competitor SiC Mosfets, T8-T9: Excluded from this test due to voltage slew rates exceeding the test setup. [2]

below 2µm to deliver Rds*A (25°C) below 1.6 mΩ*cm2, for a 1200V device. Furthermore, the development of super-junction MOSFET technology platform (see Figure 8), to be released later this year, is expected to further improve device FOM, enabling significant performance gains and bringing SiC devices closer to silicon in terms of overall cost-performance competitiveness.

Delivering Quality in Quantity

In addition to scale, Sanan places a strong emphasis on robust quality management and continuous improvement to achieve consistently high yields. Its mega-fab is certified to multiple international standards - including ISO 9001, IATF 16949, QC 080000, ISO 14001, ISO 45001, ISO 27001, ISO 22301, ANSI/ESD S20.20, AEO, SA8000, and C-TPAT - reflecting a comprehensive commitment to quality, safety, sustainability, security, and supply chain excellence. Hazardous substance process management (HSPM) is implemented in accordance with QC 080000, while environmental management practices aligned with ISO 14001 support the reduction of the facility's environmental footprint.

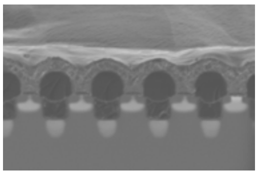


*Figure 7: SEM image of Sanan's Trench Mosfet (platform in development) reaching below 1.6 mΩ*cm2 for a 1200V device*

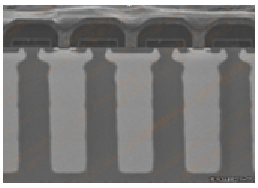


*Figure 8: SEM image of Sanan's Superjunction Mosfet (platform in development) reaching below 1.5 mΩ*cm2 for a 1200V device*

To further enhance manufacturing consistency and yield, automation technologies such as SMIF (Standard Mechanical Interface) and OHT (Overhead Hoist Transport) have been deployed in the fully automated 8-inch production line, in line with global best practices to minimize particle contamination. Sanan's reliability laboratories are CNAS-certified, enabling not only internal qualification testing but also automotive-grade product certification for customers. In addition, the manufacturing flow includes wafer-level burn-in (WLBI) and known-good-die (KGD) capability, while a comprehensive failure analysis (FA) laboratory supports rapid root-cause identification and short troubleshooting cycles.

Chip Capabilities Complemented by a Strong Packaging Ecosystem

To fully realize the superior performance of WBG devices, advanced packaging technologies are essential. These technologies enable lower parasitic inductances, improved thermal management, and optimized layouts that support reliable current sharing - all while maintaining an attractive price-to-performance ratio. As a vertically integrated manufacturer, Sanan offers in-house capabilities for several state-of-the-art packaging solutions. In addition, the company has established a strong global ecosystem of carefully selected OSAT partners and design houses. This collaborative network enables the rapid definition, development, and production of customer-specific packaging solutions, ensuring short turnaround times for our customers and supporting faster deployment of high-performance WBG products.

For the curious minds: Our Chief Process Officer, Dr. Tzu Kun Ku, will offer deeper insights into our manufacturing platform during his presentation on the exhibitor stage at PCIM 2026 in Nuremberg.

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[2] T. Lehmeier, Y. Zhou, M. März, and A. P. Pai, "Influence of SiC MOSFET Device Parameters on Zero-Voltage Switching Losses," in Proc. PCIM Europe, Nuremberg, Germany, 2025, pp. 1928–1934.

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GaN Motor Drive Evaluation Boards: EPC9186HC2/HC3 and EPC91202

Engineers need practical tools for evaluating GaN motor inverter architectures. The boards described in this article, EPC9186HC2/HC3 and EPC91202 integrate the power stage, sensing circuitry, and protection functions, which means that these platforms help engineers to prototype and assess GaN-based motor drive solutions under realistic operating conditions.

By Marco Palma, Director, Motor Drives Systems and Applications, and Maurizio Di Paolo Emilio, Marcom Director, Efficient Power Conversion (EPC)

Gallium nitride (GaN) power devices are enabling a new generation of high-efficiency, high-power-density motor drive systems. Compared with conventional silicon MOSFETs, GaN transistors offer significantly lower gate charge, reduced output capacitance, and very low on-resistance, allowing power converters to operate at much higher switching speeds. As a result, motor inverters based on GaN technology can achieve switching frequencies well above 100 kHz while reducing both conduction and switching losses. These characteristics enable smaller passive components, improved efficiency, and more compact system designs.

In addition to improving efficiency, the fast switching speed of GaN devices enables higher-bandwidth motor control and better dynamic performance. But the rapid changes in voltage that occur when GaN switches on and off pose new design challenges. High dv/dt switching edges can affect measurement circuits, control electronics, and electromagnetic behavior. This means that system-level design and layout must be done very carefully [1].

In practical motor drive systems, engineers must evaluate current-sensing accuracy, protection response time, control-loop stability, electromagnetic behavior, and thermal performance under realistic operating conditions. These aspects are essential for ensuring reliable operation when adopting GaN technology in motor inverter applications.

To support this development process, dedicated evaluation platforms are often used. In this work, two evaluation boards based on 100 V 750 µΩ EPC2361, developed by Efficient Power Conversion (EPC) for three-phase motor inverter applications, are considered: the EPC91202 and the EPC9186HC2/HC3. The EPC91202 platform enables evaluation of the EPC2361 in a relatively straightforward inverter configuration, making it suitable for analyzing the device›s intrinsic switching and conduction performance. In contrast, the EPC9186HCx platform serves as a reference design that enables the paralleling of multiple devices per switch position, allowing the investigation of higher current operation and the design considerations associated with device paralleling in GaN-based motor drive architectures.

GaN Motor Drive Evaluation Platforms

Wide bandgap devices, such as GaN transistors, significantly influence the behavior of modern motor inverter systems. Thanks to their high electron mobility and low parasitic capacitance, GaN FETs enable faster switching transitions than conventional silicon MOSFETs. These characteristics allow motor inverters to operate at higher switching frequencies while maintaining high efficiency.

The switching power loss of a device can be approximated by

$$P_{sw} \approx 0.5 \cdot V_{DS} \cdot I_D \cdot (t_r + t_f) \cdot f_{sw}$$

where V_{DS} is the device voltage, I_D is the current, t_r and t_f are the voltage rise and fall times, and fsw is the switching frequency.

Because GaN devices significantly reduce t_r and t_f, switching losses remain manageable even as switching frequency increases. This enables operation in the 100–150 kHz range for motor drives, reducing current ripple, shrinking passive component sizes, and enabling faster control loops.

Evaluation platforms such as the EPC9186 and EPC91202 boards provide useful reference implementations of GaN-based three-phase motor inverter systems. Both platforms integrate the key elements of a complete inverter stage, including gate drivers, sensing circuits, and protection features, enabling investigation of GaN device behavior under realistic motor-drive operating conditions. While both boards implement a full three-phase inverter topology, they target different operating regimes in terms of current capability and switching frequency, making them suitable for exploring different design approaches in GaN-based motor drive architectures.

EPC9186HC2/HC3 High-Current Evaluation Platform

The EPC9186HC2/HC3 is a three-phase BLDC inverter evaluation board designed to demonstrate the performance of 100-V enhancement-mode GaN (eGaN) FETs for motor-drive applications. The board integrates the complete power stage required for a three-phase inverter and enables rapid evaluation of GaN devices in motor control systems. The inverter stage is implemented using EPC2361 eGaN FETs, arranged in a three-phase bridge configuration. Multiple devices are paralleled at each switch position to support high current capability while maintaining a very low effective on-resistance. The board includes the key functional blocks required for motor inverter evaluation: integrated gate drivers, phase current sensing, voltage monitoring, housekeeping, power

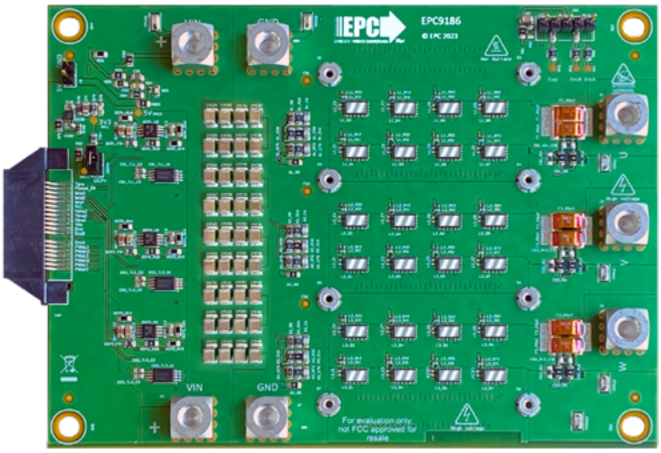
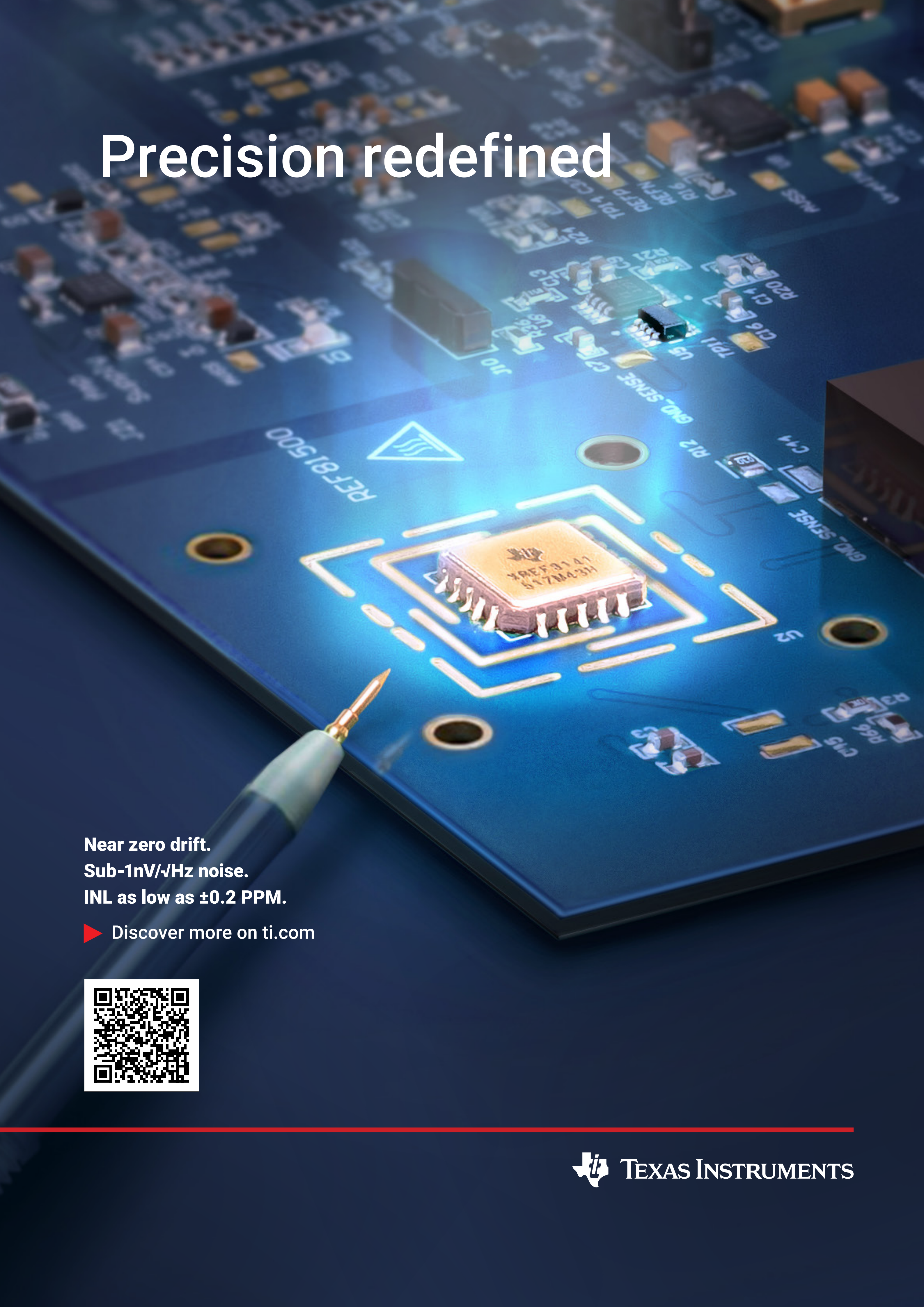


Figure 1: EPC9186HC2/HC3 evaluation board.



supplies, and protection circuitry. These functions allow the EPC9186HC2/HC3 platform to operate as a standalone inverter stage when connected to an external controller. Phase current sensing enables the implementation of advanced control techniques such as field-oriented control (FOC). Because of its high current capability and integrated sensing features, the EPC9186HC2/HC3 board provides a platform for evaluating GaN-based motor drive architectures, including efficiency, current measurement behavior, and protection response [3].

EPC91202 High-Frequency Optimization Platform

The EPC91202 evaluation board is a three-phase motor drive inverter designed for applications requiring high switching frequency and high power density. The board demonstrates the capabilities of EPC eGaN FET technology in motor drive systems operating from low-voltage DC bus supplies.

The power stage is implemented using EPC2361 eGaN FETs, configured in a three-phase bridge topology. The design supports DC bus voltages up to approximately 76 V and output currents up to approximately 50 A_{RMS}, depending on cooling conditions.

The EPC91202 integrates several key subsystems required for motor drive evaluation:

- gate driver circuitry for the GaN power devices
- current sensing for phase current measurement
- voltage monitoring and fault detection
- housekeeping power supplies

The board is intended to operate with an external motor controller, enabling rapid prototyping of GaN-based motor drive systems. The high switching speed achievable with the GaN devices allows operation at switching frequencies significantly higher than those typically used in silicon-based motor drives.

As a result, the EPC91202 platform provides a useful tool for evaluating high-frequency motor inverter operation and investigating the system-level behavior of GaN-based motor drive architectures [4].

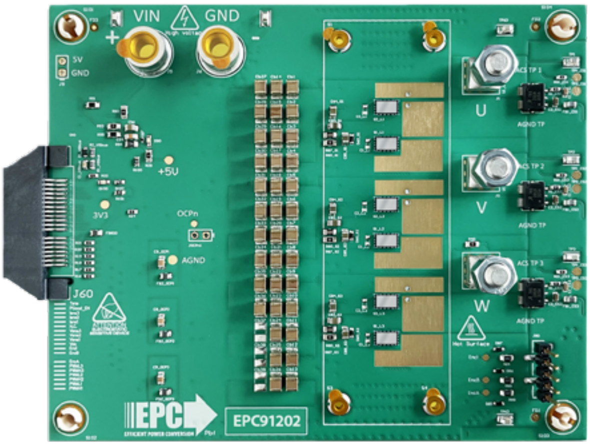


Figure 2: EPC91202 evaluation board

Current Measurement and Protection Strategy

Accurate current measurement is essential for implementing modern motor control algorithms, particularly in field-oriented control (FOC)- based systems. Reliable phase current information is required to regulate torque production, maintain control loop stability, and detect abnormal operating conditions.

Both evaluation platforms have built-in current-sensing circuitry, which lets you monitor the inverter phase currents. You can connect these measurements to an external motor controller to use closed-loop control algorithms. The sensing circuitry is designed to have sufficient bandwidth and accuracy to handle switching frequencies much higher than those used in standard silicon-based motor drives.

Both reference designs include protection systems to keep the power stage safe. When there is a fault, the inverter stage needs fast protection systems that can detect abnormal current levels and shut down the power stage when needed. The protection functions include overcurrent detection, which ensures that the inverter can be safely tested during development and system integration.

Feature	**EPC9186HC2/HC3**	**EPC91202**
Application focus	High-current motor drive evaluation	High-frequency motor drive evaluation
GaN device	EPC2361 eGaN FET [5]	
Topology	Three-phase inverter	
DC bus voltage	Up to ~76 V	
Output current capability	up to 150 A_{RMS} (multiple GaN devices in parallel)	Up to ~50 A_{RMS}
Switching frequency capability	Up to 100 kHz	Up to ~150 kHz
Integrated functions	Gate drivers, current sensing, voltage monitoring, protection	
Target applications	Robotics, high-current motor drives, industrial actuators	Compact high-frequency motor drives, battery-powered systems

Table 1: Comparison of the EPC9186HC2/HC3 and EPC91202 GaN motor inverter evaluation boards.

Thermal Performance

Thermal management plays a critical role in high-performance motor inverter designs, particularly when exploiting the high switching speeds enabled by GaN devices. Although GaN transistors typically exhibit lower switching losses compared with silicon MOSFETs, the high power density achievable with these devices requires careful thermal evaluation at the system level.

The thermal performance of the EPC9186HC2/HC3 motor drive inverter platform has been characterized under realistic motor drive operating conditions. Measurements were performed on a motor bench using a 48 V DC bus, with PWM switching frequencies of 20 kHz, 50 kHz, and 100 kHz, and a dead time of 75 ns. The tests were conducted at an ambient temperature of 25.5 °C, with both natural convection and forced-air cooling.

Under natural convection conditions, the EPC9186HC2/HC3 board can deliver approximately 40 A_{RMS} per phase without a heatsink, while 70 A_{RMS} per phase can be achieved with a heatsink, with a temperature rise from the eGaN FET case to ambient below 50 °C. When forced airflow of approximately 400 LFM (Linear Feet per Minute) is applied, the board can deliver currents up to 150 A_{RMS} per phase under steady-state conditions.

The measured temperature rise of the GaN devices as a function of switching frequency and cooling configuration is illustrated in Figures 3 and 4, based on thermal characterization results for the EPC9186HC2/HC3 evaluation board.

A similar thermal characterization is reported for the EPC91202 three-phase inverter evaluation platform, as illustrated in Figure 5. The thermal performance summary of the EPC91202 board shows that, when operated on a motor bench at an ambient temperature of 24 °C, with a 48 V DC supply, 100 kHz PWM switching frequency, and natural convection cooling, the inverter can deliver approximately 25 A_{RMS} per phase without a heatsink and up to 32.5 A_{RMS} per phase with a natural-convection heatsink attached, while maintaining a temperature rise below 50 °C from the eGaN FET case to ambient. The temperature measurements were recorded under steady-state conditions.

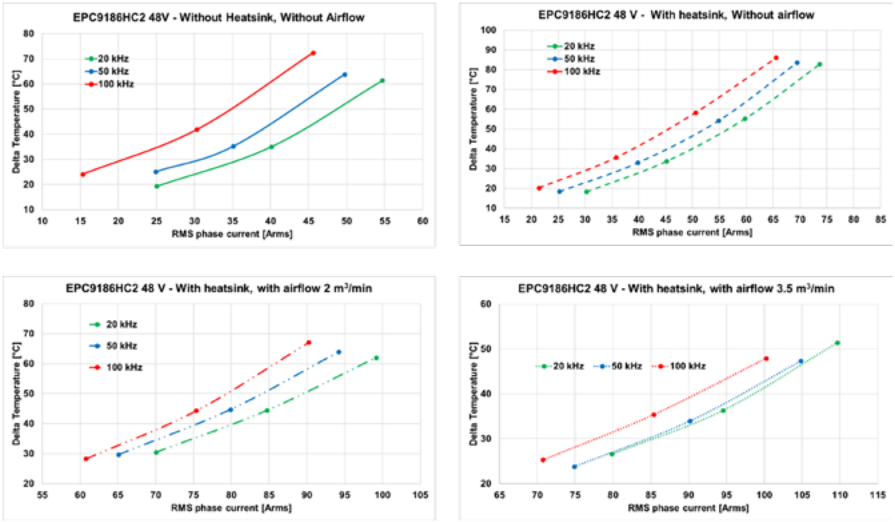


Figure 3: Temperature profile of the EPC9186HC2 under different conditions.

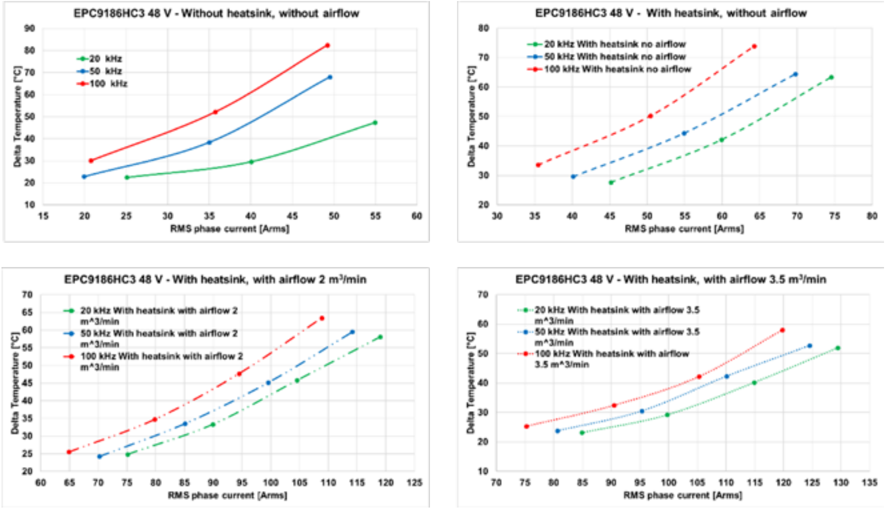


Figure 4: Temperature profile of the EPC9186HC3 under different conditions.

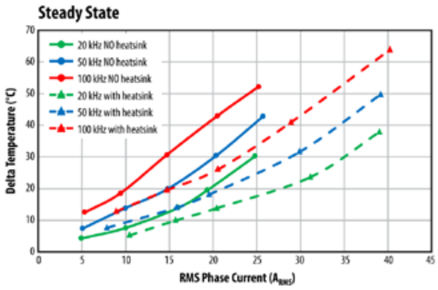


Figure 5: EPC91202 GaN FET temperature rise versus ambient temperature under steady-state conditions at different PWM switching frequencies.

Conclusion

GaN power devices enable significant improvements in switching speed, efficiency, and power density compared with conventional silicon-based solutions. These characteristics make GaN technology particularly attractive for modern motor drive systems, including robotics, industrial automation, and battery-powered applications.

The EPC9186HC2/HC3 and EPC91202 boards provide practical tools for evaluating GaN motor inverter architectures. By integrating the power stage, sensing circuitry, and protection functions, these platforms allow engineers to rapidly prototype and assess GaN-based motor drive solutions under realistic operating conditions.

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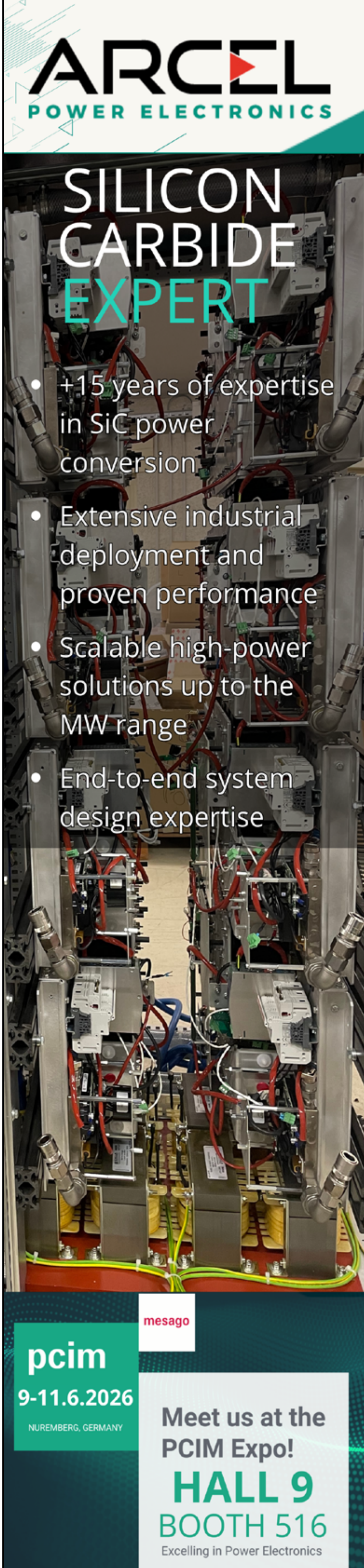


An enhanced TO-247 Package Significantly Lowers SiC MOSFET Temperature

ISOMOS™ from Analog Power Conversion, LLC, (APC-E)/Luminus [1] improves on the thermal performance of the popular TO-247 package used in many SiC based designs enhancing reliability and simplifying assembly without resorting to expensive modules.

By Lawrence Mazer, FAE Manager and Martin Held, Senior Engineer;
Analog Power Conversion, (APC-E) / Luminus

The ubiquitous TO-247 package remains a cornerstone in power electronics for high-reliability applications due to its superior high voltage power handling ability relative to other discrete packages. Despite the growing share of SMT and Top-side cooled packages it retains a dominant market share [2] for discrete power devices, and it will continue to grow along with the growth in applications such as traction inverters, chargers, energy storage, solar/wind inverters, datacenter power supplies and industrial motor drives. Standard TO-247 variants require external electrical isolation materials for safe heatsink mounting. These isolating materials introduce significant thermal penalties. This report evaluates the thermal performance of an advanced TO-247 package with an internal Direct Bonded Copper (DBC)[3] ceramic isolating element, specifically, an Aluminum Nitride (AlN) substrate providing 2.5 kV isolation, against the standard non-isolated TO-247 with external thermal/ electrical isolation interface materials. Thermal modeling and experimental measurements demonstrate a reduction of junction-to-sink thermal resistance of approximately 60% compared with standard TO-247 devices using isolation pads. This improvement results in a 41% lower junction temperature and enables significant system-level benefits including increased power density, reduced heatsink requirements, and simplified assembly.

ISOMOS™ – TO-247 with High Performance Integrated Ceramic DBC Element

The motivation to employ wide bandgap devices like SiC MOSFETs is to achieve greater power efficiency and increase power density for more compact systems. Conventional TO-247 packages pose challenges in this regard with sub-optimal thermal performance. The standard TO-247 package has an electrically conductive tab typically at the MOSFET Drain potential for mounting to a cold-plate/heatsink. For purposes of electrical safety, i.e., reduced shock hazards, and improved noise margin, it is desirable to electrically isolate the mounting tab from the heatsink especially in cases where multiple devices operate at different potentials. This is typically accomplished using thermally conductive but electrically isolating ceramic, mica or similar Thermal Interface Materials (TIM). These elements often complicate assembly and increase thermal resistance from the package to heatsink impacting thermal performance. Alternatively, the ISOMOS package from APC Electronics (APC-E) [1] moves the thermal-electrical isolation layer inside the package. The DBC utilizes a highly thermally conductive ceramic, Aluminum Nitride (AIN), with copper bonded to both sides of the ceramic substrate via a high-temperature oxidation process. This creates a much shorter and more efficient thermal path from the silicon die to the heatsink compared to external thermal interface materials (TIMs) for isolation.

AIN has amongst the highest thermal conductivity, approximately 200W/m-k, of ceramic insulating materials. Its thermal conductivity is ~6x higher than Alumina and ~2.5x higher than Silicon Nitride, which are also popular ceramic materials used for isolation. Additionally, ISOMOS offers a guaranteed and tested 2.5kV RMS isolation voltage compliant to UL 1557[4]. While the ISOMOS and the standard TO-247 share identical external dimensions their internal construction is quite different. Referring to Figure 1, the standard TO-247 requires external electrical isolating foil whereas the ISOMOS requires nothing more than the application of a thin layer of thermal grease to fill in any microscopic voids between the heatsink and backside tab. The elimination of external isolation pads simplifies assembly and enables more consistent automated manufacturing as an engineered solution rather than manually assembled. As opposed to ISOMOS the standard TO-247 requires manual application of foil and related materials introducing errors caused by misalignment and/or uneven pressure of the isolated pads.

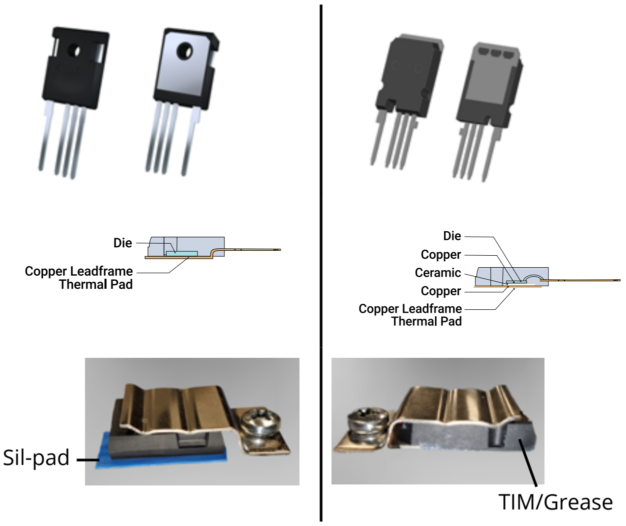


Figure 1: Comparison between the standard TO-247 and ISOMOS™ with integrated DBC.

The Performance and Quality Advantage of ISOMOS

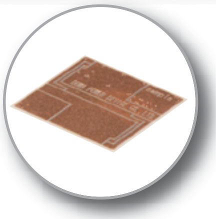
In summary we find the following benefits offered by ISOMOS:

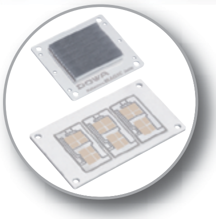
Lower Thermal Impedance → Better Thermal Performance

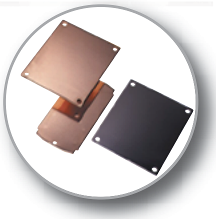
- Internal DBC provides a solid, highly conductive copper-ceramic path from die/package base to heatsink allowing SiC MOSFETs to run cooler. Also note thermal isolation pads/foil vary widely in terms of performance and long-term stability.

Improved Reliability and Long-Term Stability

- Reduced thermal stress can increase device lifetime or allow higher current/power per device. Lower die temperatures (e.g., 20–30°C cooler in DBC vs. TIM) means enhanced reliability; A commonly used reliability rule of thumb is that failure rate halves for each 10°C reduction in junction temperature (Arrhenius acceleration model).







- Excellent Coefficient of Thermal Expansion (CTE) matching. – The Aluminum Nitride (AlN) ceramic in the isolated ISOMOS package is engineered for minimal Coefficient of Thermal Expansion (CTE) mismatch with the Silicon Carbide (SiC) die.

Simplified Assembly & Lower Recurring Labor Over Time

- No need to cut/align pads, apply grease, inspect pad placement/ flatness - simpler assembly flow. Saves labor per device once implemented and associated costs. Reduced assembly steps reduce chances of human error (misalignment, improper torque, grease smear/uniformity issues), which improves yield and reduces rework.

System-Level Benefits

- Because of better thermal efficiency, the number of devices can be reduced (higher current per device). Additionally, the heatsink size, cooling system, or derating margin shrinks - reducing overall system cost/size/complexity resulting in Improved power density.
- Reduced parasitic drain-to-heatsink capacitance due to common heatsink improves switching performance and reduces EMI
- For rugged applications (automotive, industrial), improved thermal and isolation reliability adds to product lifetime - important for warranty, maintenance, brand reputation.
- Overall efficiency of the system will be improved based on the simple fact that ON Resistance of the SiC MOSFET will be lower at lower junction temperatures.

Cost Advantages at Scale

- Even with a modest package adder, for multidevice systems the integrated DBC approach becomes cheaper than pad + grease + labor once you include recurring assembly costs and pad/grease materials. Many systems employ over 48 MOSFETs which further increases system complexity and cost.

System Thermal Performance Comparison – ISOMOS™ vs Standard TO-247

To demonstrate the thermal advantage of ISOMOS a comparison between ISOMOS and a standard non-isolated TO-247 along with a popular TIM was made. A material with thermal conductivity equal to 1.8W/m-k was selected as the TIM used with the non-isolated 1200V, 13mW, TO-247 package and compared to one of the similar rated devices in the ISOMOS family. Please refer to Table 1 where measured and calculated thermal impedances were compared.

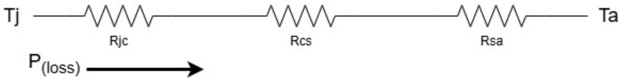


Figure 2: Basic Thermal Stack

For reference let us recall the basic thermal ohms law per Figure 2.

Thermal Ohms Law: T_j-T_a = $P_{(loss)}$ * (R_{jc} + R_{cs} + R_{sa}) where,
T_j = Junction temperature. Source of heat.
T_a = Ambient Temperature
$P_{(loss)}$ = MOSFET Power loss
R_{jc} = Junction-Case thermal Resistance of the TO-247 package
R_{cs} = Typically some form of TIM and/or Grease
R_{sa} = Sink-Ambient thermal resistance of heat sink

T_j-T_a represents the total thermal budget for a system. Thermal resistances add up reducing the available budget which designers work to minimize. The thermal resistance of ISOMOS, being significantly less than standard TO-247 using external isolation materials, provides more headroom for increased power density or keeping the same power density but at lower system cost and lower junction temperature of the SiC switch.

We will use a standard method used to compare the thermal impedance, $R_{\theta(pad)}$, of Thermal Interface Materials (TIMs) such as the sil pad used here.

$R_{\theta(pad)}$ = Z_θ/A where Z_θ is the thermal impedance specification and A = thermal pad contact area of a TO-247 package.

For the sil pad, from the datasheet, Z_θ = 0.28 (°C-in^2/W) @ 25psi.

For the TO-247, we assume the contact area A=0.33in^2.

$R_{\theta(pad)}$ = Z_θ/A = 0.28 (°C-in^2/W)/0.33in^2 = 0.85°C/W.

We add the junction-case thermal resistance from Figure 3 package to $R_{\theta(pad)}$ for the total thermal stack, junction - sink, $R_{\theta(js)}$.

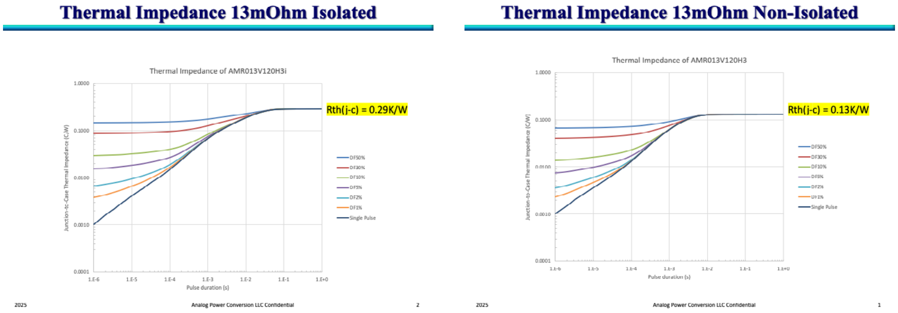


Figure 3: Thermal Impedance Curves for both Standard TO-247 AMR013V120H3 and ISOMOS AMR013V120H3i

$R_{\theta(js)}$ = $R_{\theta(jc)}$ + $R_{\theta(pad)}$ = 0.13°C/W + 0.85°C/W = 0.98°C/W

which correlates to the 1.06°C/W measured value. A heating current of 1.5A was applied at 50V drain voltage increasing the MOSFET P_{diss} to 75W. Thermocouples were placed on the heatsink and die junctions to accurately measure temperature per Figure 4.

Device and Isolation Type	Rth °[C/W]	Measured Temperature
TO-247 with 1.8W/m-K isolation pad	1.06 measured vs 0.98 calculated	111°C
ISOMOS – 1200V, 13mΩ, Isolated TO-247 package	0.42, per Figure 3, measured incl grease (grease adds ~ 0.2)	79°C

Table 1: Thermal Impedance Comparison

The results as shown in Table 1 demonstrate the thermal advantage of ISOMOS. A significant 41% lower junction temperature using just a thin layer of Aavid Ther-o-Link thermal grease for proper mounting to the heatsink. At 111 °C the maximum operating temperature is close to exceeding recommended operating conditions. Beyond this temperature system reliability may be impaired. ISOMOS keeps the temperature at 79°C, well within normal operating conditions.

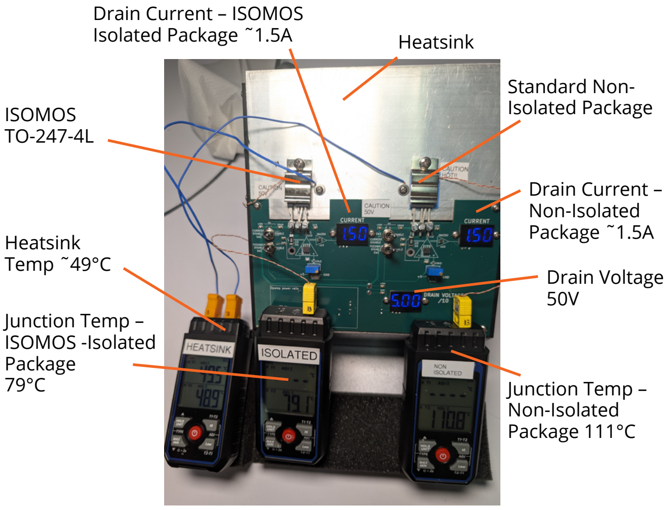


Figure 4: Thermal Measurement

Additionally, the 46°C delta consumes less of the thermal budget as discussed previously and increases the thermal headroom that can be used in the design stage for increasing the output power for the same system without additional cost. Alternatively, consideration may be used to reduce system size including the heatsink, sized for smaller power losses, or increasing switching frequency for smaller inductors and capacitors.

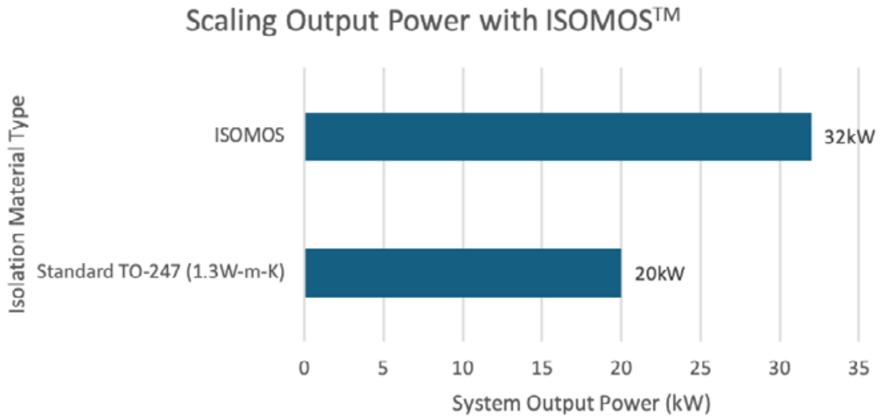


Figure 5: Estimated Output Power Comparison

Increasing Output Power with ISOMOS

In scaling output power to 20kW for example the advantages of ISOMOS become more apparent. Using the measured values of thermal resistance above a model was created to estimate power losses. At 20kW output level there will be 300W power loss at 98.5% efficiency. From our thermal ohms law in Figure 2 we can estimate that using the same 1200V, 13mΩ MOSFETs but with the integrated ceramic DBC the system output can increase to over 30kW as shown in Figure 5 in the same enclosure. The extra thermal headroom in such a system may also be utilized to reduce the number of parallel MOSFETs per switch position and significantly reduce system cost and size.

Summary and Conclusions

Addressing the needs of increasing power levels offered by Wide Bandgap (WBG) semiconductors like SiC MOSFETs require engineers to carefully consider advanced packaging to increase power density. ISOMOS from APC-E with its integrated high-thermal-conductivity Direct Bonded Copper (DBC) ceramic element has been shown here to help designers address these issues without the necessity of moving toward expensive modules. Compared to a standard non-isolated TO-247, ISOMOS has been shown to significantly reduce the junction-to-heatsink thermal resistance compared to that of a standard TO-247, resulting in a 32°C lower junction temperature at 75W. When scaling this advantage to higher power levels such as 20kW we see the DBC-integrated ISOMOS delivers ~60% more power in the same footprint. Capitalizing on the extra thermal headroom the designer can now choose higher $R_{ds(on)}$ MOSFETs at lower cost for a given output power or a reduction of heatsink size with lower losses and increasing power density.

Beyond upfront cost, the ISOMOS delivers measurable reliability and thermal advantages that reduce lifetime cost. The integrated ceramic DBC provides a stable, low impedance thermal path with excellent CTE matching to SiC die, avoiding silicon pad creep, grease pumpout, and torque dependent thermal degradation over time. This results in lower and more stable junction temperatures, improved thermal cycling robustness, and reduced maintenance or field failure risk. Essentially ISOMOS from APC-E helps extend the legacy of the very popular high power TO-247 package into the future.

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800 V SiC Power Module with Integrated Current Measurement

Take an integrated PCB-based power module and combine it with coreless current sensing. This story describes how it can deliver a compact, efficient, and thermally robust solution for next-generation EV traction inverters.

By Patrick Salcher, Research Engineer, Silicon Austria Labs; Thomas Langbauer, Team Leader Architectures & Topologies, Silicon Austria Labs; Taiga Kyosaki, Technical expert of Current Sensors, Asahi Kasei Microdevices Corporation; Takahisa Shikama, Strategy & Business Leader of Magnetic Sensor Products, Asahi Kasei Microdevices Corporation; Takaya Higa, Field Application Engineer, Asahi Kasei Microdevices Europe GmbH

The electrification of vehicles is accelerating the demand for traction inverters that are not only compact and lightweight but also highly efficient. To meet these requirements, the industry is moving towards 800 V architecture and SiC (Silicon Carbide) power devices, which enable faster switching speeds, improved thermal performance and higher efficiency. However, these advancements introduce new challenges in structural design, requiring a holistic approach that integrates electrical performance, thermal management, and sensing capabilities into a single platform. Miniaturization is a key driver for next-generation inverter designs. Reducing size and weight without compromising reliability demands innovation in packaging and component integration. Among these, coreless current sensing has emerged as a critical technology, enabling smaller footprints while maintaining high accuracy and bandwidth

Challenges for Current Sensing in Next-Generation Inverters

Current sensing is essential for closed-loop control in traction inverters, ensuring precise motor operation and system safety. However, next-generation systems impose challenging design constraints. SiC devices operating at 800 V generate extremely steep voltage slopes, requiring sensors with high dv/dt immunity. The rapid switching characteristics of SiC also demand sensors that can track fast current transients without delay, while maintaining accuracy under low torque conditions typical of city driving.

Conventional cored sensors provide high signal-to-noise ratio (SNR) and robustness but add bulk and weight, limiting design flexibility. To overcome these limitations, coreless current sensors are increasingly favored for compact inverter designs. For this proof of concept, AKM's EZ232L was selected because it meets all critical requirements:

- High resolution (approximately 1 A_{RMS}) across a wide current range
- Wide bandwidth and fast response for SiC switching
- Robust immunity against high dv/dt noise

In addition to integration benefits, the choice of sensing technology plays a critical role in system performance. Compared to Si-based Hall sensors, which suffer from low sensitivity and typically require a magnetic core, compound Hall technology (InAs) used in AKM's EZ232L provides high sensitivity without the need for a core, enabling miniaturization and flexibility. While TMR sensors also offer high sensitivity, they face inherent reliability challenges: large surge currents or transient signals can disturb the magnetic balance, reduce accuracy and introduce hysteresis. Hall-based sensors, on the other hand, are well-established and highly robust, maintaining stable performance even under strong magnetic fields and harsh operating conditions, outlined in Table 1. These characteristics make compound Hall sensors an ideal choice for next-generation traction inverters, where precision, reliability, and compact design are essential.

Feature	Compound Hall (AKM)	Si Hall	TMR
SNR	*High*	*Low*	*High*
Robustness against strong magnetic field	*Excellent*	*Excellent*	*Limited*

Table 1: Comparison of magnetic sensors

Proof of Concept: Compact and Efficient Power Module

The proposed power module shown in figure 1 demonstrates a new approach to miniaturization and efficiency. It offers an all-in-one solution, integrating aluminum oxide direct copper bonded (DCB) substrates atop SiC power semiconductors, gate driver circuits, and current sensing capabilities. By leveraging standard PCB technology and off-the-shelf components, the design achieves both flexibility and cost advantages for small-to-medium production volumes. This integration concept addresses the growing need for compact, scalable solutions in EV power electronics.

The EZ232L Hall-effect IC enables coreless current sensing with high accuracy and resolution, supporting improved inverter efficiency over a wide operating range. Mounting the sensor directly on the PCB under the busbars ensures robust current measurement and wide bandwidth without adding extra bulk.

Several innovations make this power module suitable for high-power EV applications. First, the use of top-side-cooled QDPAK Infineon semiconductor devices, combined with a PCB substrate and close-by added DC link bypass capacitors, achieve an exceptionally low loop inductance of approximately 5 nH, which is critical for stable high-speed switching while maintaining low voltage overshoots. A two-sided cooling approach enables a compact footprint even with integrated gate drivers and sensors, while maintaining adequate thermal performance. This is made possible by effective heat spreading through the QDPAK heat slugs and the integrated isolation for each discrete device.

Additionally, the cooling concept resolves typical planarity issues associated with top-side cooling, as the assembly is clamped between two cooling plates. By integrating control and gate electronics in close proximity to the power devices, the PCB-based design supports robust and reliable commutation—even at very high current levels. This layout minimizes parasitic inductance and ensures clean commutation, which is essential for SiC-based systems operating at high voltages.

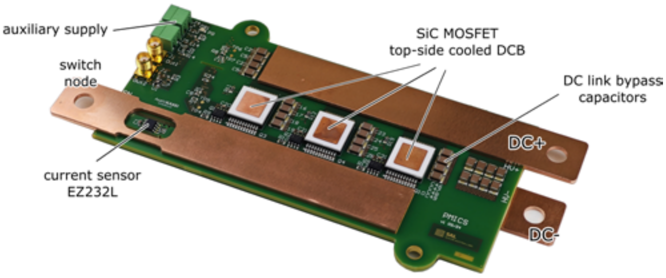

Figure 1: Proof of Concept board of current sensor integrated power module.

Measurement Result

Figure 2 shows the schematic of the test setup. The current sensor EZ232L was used for the following tests. Three SiC half bridged are utilized in parallel and 15 V DCDC converters are used as an isolated power supply for the gate drivers.

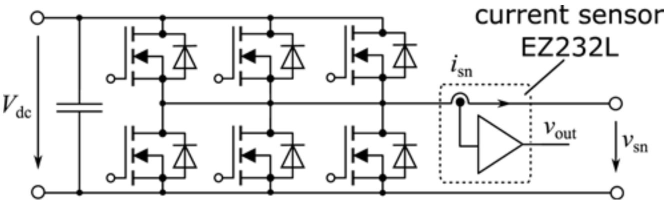

Figure 2: Schematic of the test setup.

An external 420 μF film capacitor with a 2.6 mΩ ESR is used to stabilize the DC link supply.

Figure 3 illustrates the actual measurement of a pulse current. The pink trace represents the reference signal i_{sn} captured by a Rogowski coil, while the yellow trace shows the output from the EZ232L sensor v_{out}. The measured response time $t_{response}$ for the EZ232L (at 150 A, half load current) was 808 ns, demonstrating its ability to follow rapid current changes with minimal delay.

Figure 4 presents the measurement results for dv/dt performance. To evaluate the influence of voltage slew rates on the sensor output, the half-bridge was operated without load at 800 V, producing voltage slopes of 98 V/ns. The EZ232L sensor output v_{out} was monitored at the BNC connector, which corresponds to the yellow trace, the pink trace represents the current probe i_{sn}, and the light blue is the DC link voltage V_{dc} and the green traces show the switch node voltage v_{sn}. These results confirm the sensor's robustness under extreme dv/dt conditions.

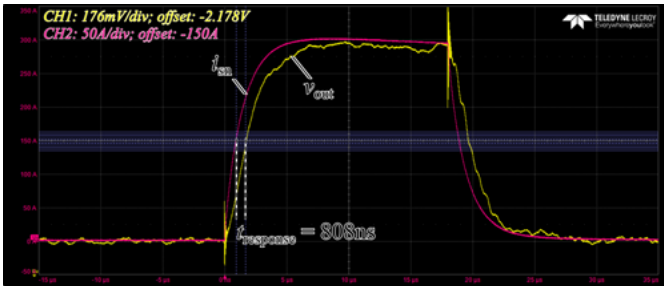

Figure 3: Response time measurement.

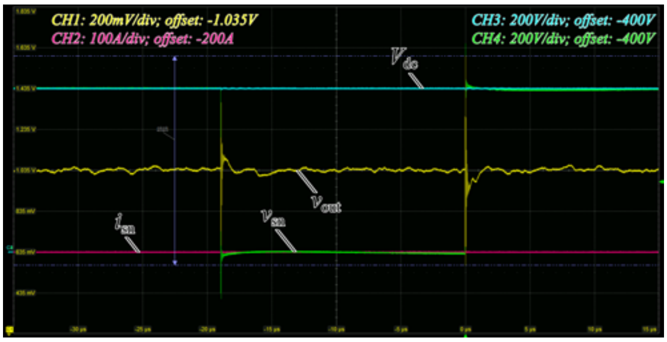

Figure 4: dv/dt measurement.

Conclusion

This proof of concept illustrates how PCB-based power module integration, combined with coreless current sensing can deliver a compact, efficient, and thermally robust solution for next-generation EV traction inverters. By merging electrical performance, thermal reliability, and sensing accuracy into a single platform, this approach sets the stage for standardized, cost-effective designs that meet the demands of future high-voltage EV architectures. The EZ232L offers several benefits for automotive traction inverter applications and is well positioned to support future requirements.

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Reverse Recovery Charge Is Not a Constant

Why Q_{RR} Depends on Time and Why That Matters in Modern Power MOSFETs

Reverse recovery charge, Q_{RR}, is one of those parameters most power engineers know well. It appears prominently in MOSFET datasheets, it finds its way into switching-loss equations, and it is often used to compare devices when efficiency matters. The problem is not that Q_{RR} is unimportant; it is that it is commonly misunderstood.

By David Jauregui, Co-Founder and Chief Technology Officer, iDEAL Semiconductor

In modern power converters, particularly high-frequency, hard-switched designs, Q_{RR} does not behave like a fixed device constant. Instead, it depends strongly on how long the MOSFET's body diode conducts current before the device is reverse-biased. In systems where dead time is aggressively minimized, the actual reverse recovery charge involved in switching can be far lower than the datasheet value. This effect becomes increasingly pronounced in MOSFETs rated above 100V.

These trends are consistently reflected in analytical modeling, device-level simulations, and controlled laboratory measurements spanning multiple voltage classes. Recognizing Q_{RR} as a time-dependent quantity rather than a static number allows designers to model losses more accurately, optimize dead time with confidence, and recover efficiency that is often left unrealized.

Where reverse recovery really comes from

The source of reverse recovery is the intrinsic body diode present in most vertical silicon power MOSFETs. In half-bridge and synchronous converter topologies, this diode conducts current during the brief interval when both MOSFETs are off. That interval is typically set by the system's dead time.

While the diode is forward-biased, minority carriers are injected into the MOSFET's drift region. When the complementary MOSFET turns on, and a reverse voltage is applied, the stored carriers must be removed before the diode can block. They are eliminated either through recombination within the silicon or by being swept out as a reverse current spike. This transient process is what is referred to as reverse recovery.

Reverse recovery behavior is commonly summarized using three parameters: reverse recovery charge, Q_{RR}; peak reverse recovery current, IRM; and reverse recovery time, trr. Of these, Q_{RR} is most often used as a proxy for switching loss. However, the way Q_{RR} is typically measured and reported obscures its behavior in real-world applications.

Why datasheet Q_{RR} often misrepresents reality

Industry standards measure Q_{RR} after the body diode has been conducting long enough to reach steady-state forward conduction. At that point, minority-carrier storage has fully saturated, yielding a worst-case value for comparison.

The difficulty is that modern converters rarely operate under these conditions. In high-performance systems, dead times are routinely pushed into the tens of nanoseconds. High-frequency SMPS designs often operate with dead times between 20ns and 100ns, Class-D audio amplifiers reduce dead time to tens of nanoseconds to minimize distortion, and many motor drives are similarly optimized for efficiency.

At these time scales, the body diode never reaches steady-state conduction. The amount of stored charge is therefore much lower than the datasheet Q_{RR} value, sometimes by a wide margin. Using steady-state Q_{RR} to estimate switching losses in these systems can significantly overstate the real loss contribution.

Stored charge accumulates over time, not instantly

The reason Q_{RR} is not constant is due to the physics of minority-carrier storage. When the body diode begins conducting, the stored charge does not appear instantaneously. Instead, it builds up gradually, following an exponential curve governed by the device's minority-carrier lifetime.

For very short body diode conduction times, only a small amount of charge is injected into the drift region. As conduction time increases, stored charge rises exponentially until it approaches a saturation level. That saturation level corresponds to the steady-state Q_{RR} reported in datasheets. When the conduction interval is short relative to the minority carrier lifetime, only a fraction of that charge is present.

This behavior means that Q_{RR} is fundamentally a function of body diode conduction time. Treating it as a single fixed number ignores the operating regime in which many modern converters actually run.

Why voltage rating amplifies the effect

The time dependence of Q_{RR} becomes more pronounced as the MOSFET voltage rating increases. Higher-voltage devices require longer drift regions to support their breakdown voltage. The larger silicon volume takes longer to fill with injected carriers during diode conduction.

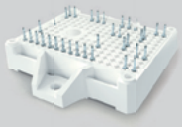
As a result, higher-voltage MOSFETs require longer conduction intervals to reach full-charge saturation, even if their intrinsic carrier lifetime is similar to that of lower-voltage devices. In practice, this means that short dead times reduce effective Q_{RR} far more dramatically in 150V, 200V, and higher-voltage MOSFETs than in lower-voltage parts.

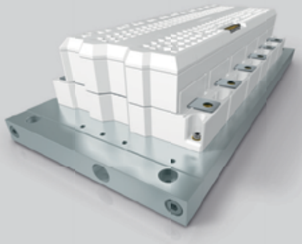
This explains why designers working with higher-voltage silicon often see a disconnect between datasheet Q_{RR} values and observed switching behavior when dead time is minimized.

What simulation shows about Q_{RR} versus time

To better understand how this time dependence manifests across voltage classes, device-level simulations were used to examine reverse recovery behavior under controlled conditions. To explore this behavior in detail, charge-balanced silicon MOSFETs rated at 150V, 200V, and 650V were evaluated using mixed-mode TCAD simulations, representing modern low-loss device architectures commonly used in high-performance power converters, including


1500VDC





designs such as iDEAL Semiconductor's SuperQ™ technology. The simulation data for various voltage class MOSFETs is shown in Figure 1. For each voltage case, the body diode conduction time was swept from tens of nanoseconds to several hundred nanoseconds, and the resulting reverse recovery charge was extracted.

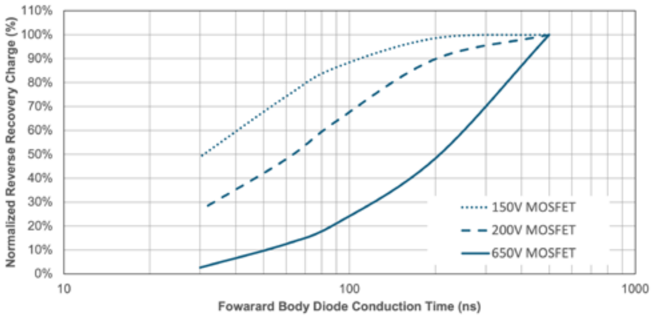


Figure 1: TCAD simulation data of Q_{RR} vs Ton

The results reveal a clear and consistent trend. Q_{RR} increases exponentially with body diode conduction time, and the time required to approach saturation increases with voltage rating. At a conduction time of approximately 30ns, the effective Q_{RR} was reduced by roughly 30 percent in the 150V device and by about 60 percent in the 200V device. In the 650V device, Q_{RR} decreased by more than 90% relative to its long-conduction value. Even at 500ns, the highest-voltage device had not yet fully reached steady-state saturation.

For systems operating with dead times below 100ns, these differences are not subtle; they fundamentally change how reverse recovery should be modeled.

Measurement confirms the trend

Simulation alone is not sufficient. To validate the results, a 200V MOSFET was tested using a platform that allowed independent control of forward conduction current, switching slew rate, and body diode conduction time.

When the diode was allowed to conduct for a long interval, the measured Q_{RR} closely matched the datasheet value, confirming that the test conditions reproduced conventional characterization conditions. As the conduction time was reduced towards 30ns, the measured Q_{RR} decreased steadily, following the same exponential trend predicted by simulation.

The strong agreement between simulation and measurement confirms that the reverse recovery charge is inherently transient and strongly dependent on conduction time, rather than a fixed property of the device.

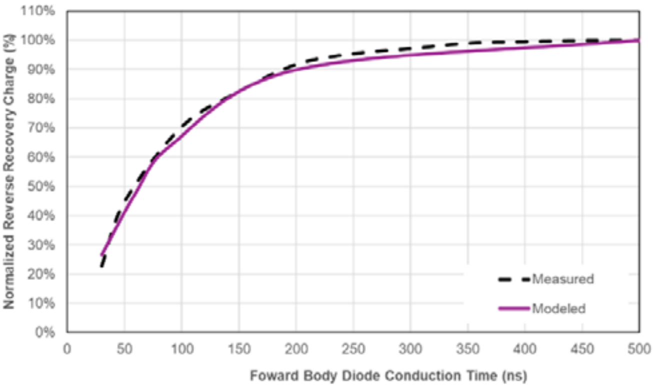


Figure 2: Measured and Modeled MOSFET Q_{RR} versus t_{BDC}

Dead time versus body diode conduction time

One source of persistent confusion in system design is the difference between programmed dead time and actual body diode conduction time. Dead time is defined digitally by the PWM controller, but the interval during which the body diode actually conducts depends on a combination of analog effects. These include driver propagation delays, external and internal gate resistance, MOSFET capacitances, and threshold voltage variation.

In practice, the body diode conduction interval is often significantly shorter than the programmed dead time. As a result, many systems already operate in a regime where effective Q_{RR} is well below the datasheet value, even if designers are not explicitly accounting for it. Understanding this distinction is essential for optimizing dead time and improving efficiency.

When Q_{RR} causes loss and when it does not

Another important nuance is that Q_{RR} does not create loss in the MOSFET that stores the charge. The loss occurs when the reverse recovery current is forced through a switching device during its turn-on transition. In synchronous buck converters, this mechanism can significantly increase switching loss in the control MOSFET. In other topologies, such as phase-shifted full-bridge converters, reverse recovery may occur without incurring a comparable switching loss penalty.

This makes the impact of Q_{RR} highly application-dependent and reinforces the need to evaluate reverse recovery behavior in the context of the specific topology and operating mode.

Why excessive dead time is often unnecessary

To ensure shoot-through immunity, many designs use dead times on the order of hundreds of nanoseconds or more. However, timing analysis via Monte Carlo analysis shows that the actual variation caused by component tolerances is often far smaller than assumed. Reducing dead time shortens body diode conduction, lowers diode conduction loss, and significantly reduces effective Q_{RR}, provided the system remains outside the shoot-through region.

System-level measurements, as shown in Figure 3, typically show a clear minimum in total loss as dead time is reduced. Operating near this minimum allows designers to capture efficiency gains that are otherwise masked by conservative assumptions.

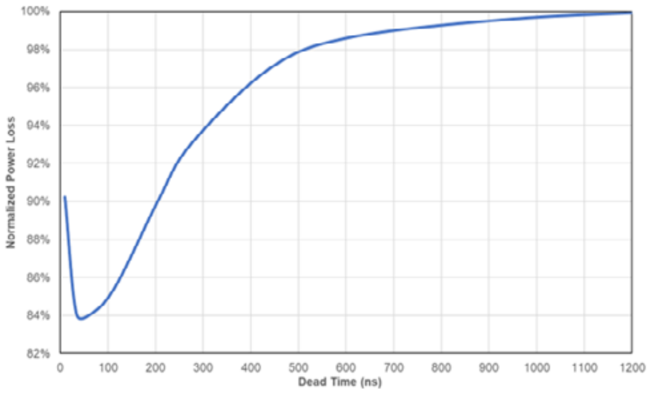


Figure 3: Normalized Power Loss versus Dead Time

Time to rethink how Q_{RR} is specified

Treating Q_{RR} as a single worst-case number made sense when switching speeds were slower and dead times were longer. In modern converters, it no longer reflects real operating conditions. Presenting Q_{RR} as a function of body diode conduction time would enable more accurate loss prediction, better dead-time optimization, clearer device comparison, and higher overall system efficiency.

A practical implication of this behavior is that a single datasheet Q_{RR} value may be insufficient. A more useful approach would be to present Q_{RR} as a function of body diode conduction time, or to specify Q_{RR} at multiple defined conduction intervals. This would allow designers to accurately model losses and optimize dead time based on real operating conditions rather than worst-case assumptions.

Conclusion

Reverse recovery charge in power MOSFETs is not a static parameter. It is a time-dependent quantity governed by minority carrier lifetime, device geometry, and the duration of body diode conduction. Both simulation and measurement show that in fast-switching systems, effective Q_{RR} can be far lower than datasheet values, particularly in higher-voltage devices.

Recognizing this behavior allows designers to move beyond overly conservative loss estimates and unlock the efficiency gains already present in their systems. As switching speeds continue to increase and dead times shrink, understanding the time-dependent nature of reverse recovery becomes essential for accurately interpreting device behavior in modern power system design. In this context, both Q_{RR} characterization and designers' thinking about it must evolve as well.

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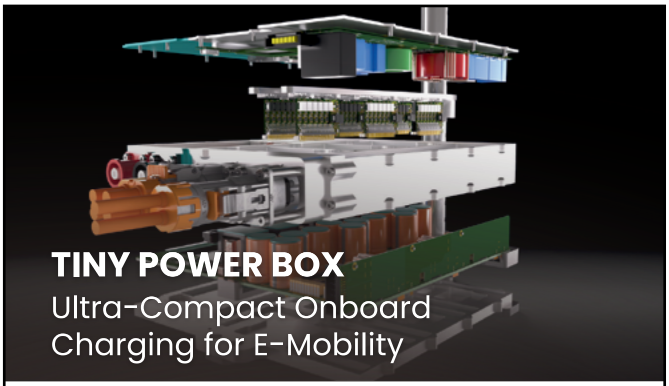

Data Centers evolve to meet AI's massive Power Needs

In this article, I'll examine the derivation and delivery of data center power to the server functions doing the computing, why the power distribution architecture needs to change to meet rapidly evolving AI computing and power requirements, and how to make this possible.

By Brent McDonald, Systems and Applications Engineer, Texas Instruments

Figure 1 shows the IT server rack-level power requirements needed as a function of time. Figure 1 projects that by 2028, an IT rack will need 1.5MW of power, which is 10 times more power than what server racks are using today.

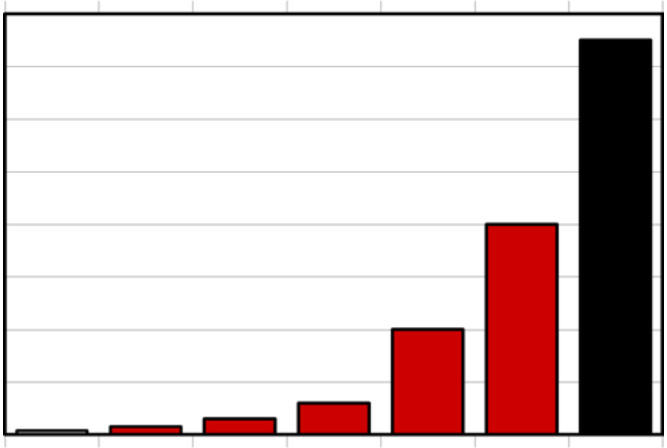

Figure 1: Rack-level power requirements

A brief history

In order to appreciate the magnitude of the changes occurring in the power delivery network inside data centers and servers, let's briefly review the current architecture. Figure 2 shows the first-generation power distribution architecture, which has dominated servers and data centers since the 1990s to today. The top-left area of Figure 2 shows three-phase AC power coming from the AC power grid. This power is transformed from a "medium-voltage" of approximately 13kV to an AC line-to-line voltage of 480V. An uninterruptable power supply (UPS) buffers this voltage.

When the AC grid loses power, the UPS uses local batteries and an inverter function to keep the data center servers running long enough for the backup generators to take over, using either an automatic transfer switch (ATS) or a static transfer switch (STS). The 480V line-to-line AC voltage is equivalent to a 277V$_{AC}$ line-to-neutral voltage.

After delivery of the three phases of the 277V$_{AC}$ to the IT server rack, a power-supply unit (PSU) performs power factor correction (PFC) and generates a regulated 12V output for distribution to the server IT trays. This 12V distribution voltage for first-generation architectures powers various loads, voltage regulators and other point-of-load regulators (PoL), creating voltages to power the processors, memory and communication integrated circuits used throughout the server trays. This architecture worked well when the total rack power was around 10kW to 20kW. As demand for more computing power has increased, however, so has the power required to handle these computing functions.

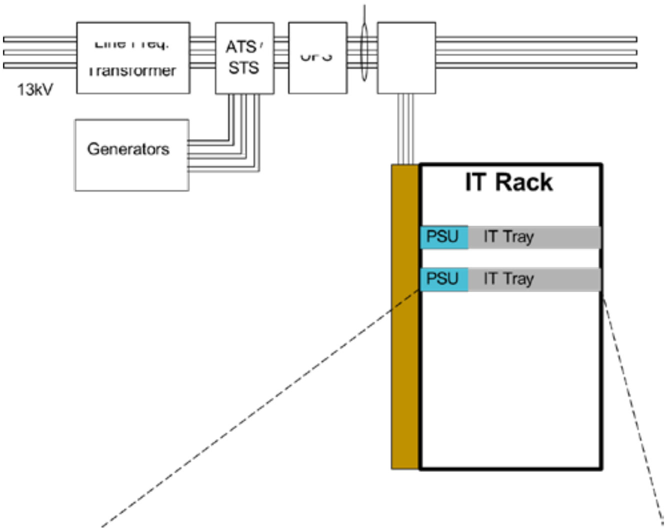

Figure 2: First-generation traditional rack servers

Figure 3 shows the next evolution in the data center power distribution architecture. Starting from the upper- left area of Figure 3, this architecture begins with the same medium-voltage input power source. Like the first-generation architecture, transformers convert from three-phase 13kV to a $480V_{AC}$ line-to-line voltage. This architecture does not use a UPS but instead sends the equivalent $277V_{AC}$ line-to-neutral voltage directly to local PSUs inside the IT rack. These PSUs are no longer dedicated to each server tray but rather combined in a single power shelf. In this context a power shelf is simply a shelf of power supplies with their outputs sharing the common load demands from the IT equipment.

There are typically six PSUs in each power shelf in a N+1 configuration to achieve redundancy. Adding power shelves achieves the total required power for the IT rack. The output of these power shelves is a $50V_{DC}$ bus that is distributed to each IT tray through a high-current busbar running along the back of the server rack. While some second-generation installations retain the UPS function, others will remove it (as shown in Figure 3) and replace it with a local battery backup unit (BBU) that keeps the $50V_{DC}$ bus active until power is restored or the backup generators can take over. In some cases, a capacitor shelf or capacitor backup unit (CBU) can help eliminate excessive voltage transients, current transients associated with any power disruptions. The 50V bus inside each IT tray goes to a local intermediate bus converter creates the 12V needed to power the system loads in the IT trays.

The second-generation architecture allows the IT rack to power loads beyond what the first generation can do. Realistic loads for the second generation are in the 100kW range. Once the total power required starts to hit around 200kW, the distribution losses become significant and make further power increases impractical.

AI data center power delivery

Data center racks responsible for running advanced AI models are now expected to eclipse 1MW of power in the 2028 time frame. Distributing this amount of power in a second-generation architecture would result in 20,000A of current, assuming a 50V busbar. The busbar required to deliver this much current is heavy, costly and very impractical. As a result, a higher-voltage $800V_{DC}$ or $\pm 400V_{DC}$ bus for power distribution in new AI IT server racks will reduce the high-current busbar requirements from 20kA to 1.25kA. This order-of-magnitude reduction in current will help keep the overall power delivery efficiency high and enable the use of a lower-volume and lower-density copper busbar. Figure 4 shows this architecture.

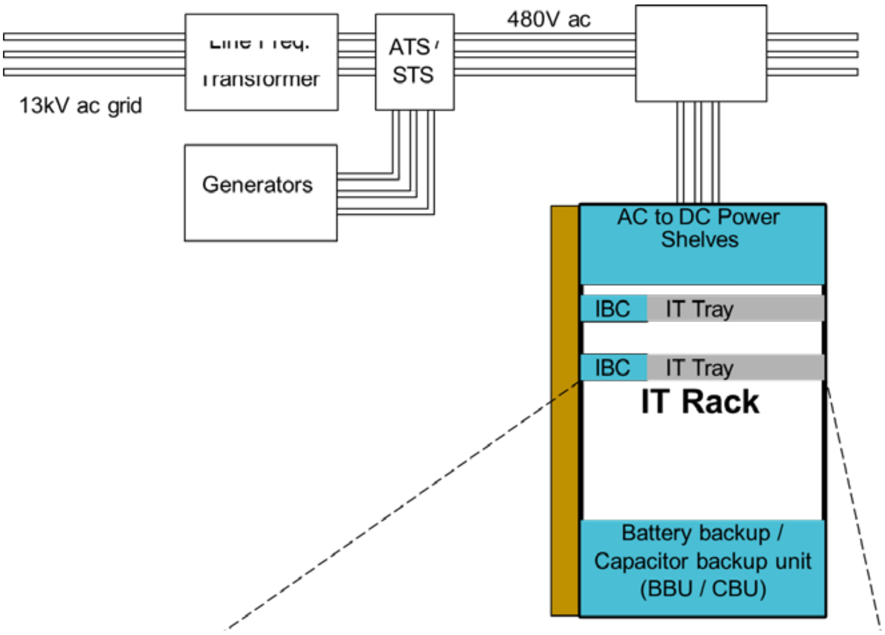

Figure 3: Second generation – cloud and AI computing

The power shelf from the second-generation architecture is replaced with a sidecar, which takes the three-phase 480V_{AC} grid voltage as its input. The sidecar converts this to the 800V_{DC} or ±400V_{DC} bus and distributes it to one or more IT server racks. The sidecar also now houses the BBU. In addition to improving the power distribution efficiency, the third-generation architecture also makes more room in the IT rack for computing functions.

In some sense, increasing the computational density of the IT server rack is even more critical than the power distribution problem. AI-based IT racks use hundreds of processors to rapidly process the volume of computations necessary for AI to function at its best. These processors need to be able to communicate with each other in a high-density footprint. Removing a significant portion of the power conversion from the IT rack makes it possible to fit more processors in a smaller space. Now each IT tray in the rack takes as its input this 800V_{DC} or ±400V_{DC} bus voltage. The intermediate bus converter in the tray then converts that voltage for distribution on the IT tray. The distribution voltage could be 48V, 12V or even 6V depending on the chosen architecture.

What comes next?
While the third-generation architecture does a great job of improving the power distribution efficiency and significantly increasing the computation density inside the IT rack, it does so at the expense of taking up more space on the IT floor of the data center. As a result, the next step in the data center evolution is moving the sidecar AC/DC power conversion functions from the IT floor into a utility room.

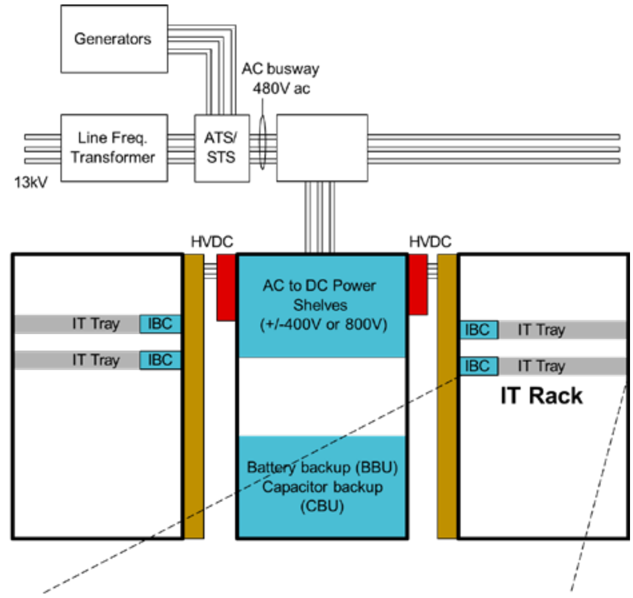

Figure 4: Third generation – AI computing DC distribution sidecar

Figure 5 illustrates a proposal for a fourth-generation architecture. In this architecture, the sidecar houses the BBU functions and the AC/DC function has been moved into a solid-state transformer (SST).

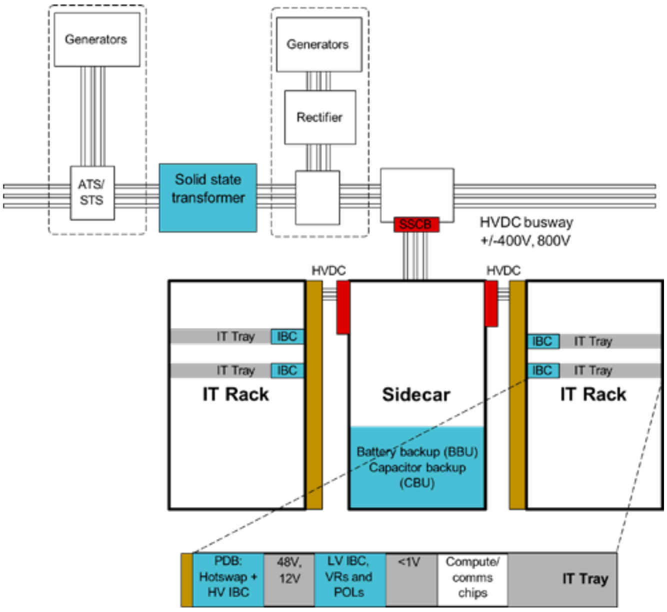

Figure 5: Fourth generation – AI computing SST and DC distribution

In the first-, second- and third-generation architectures, the input voltage is the 13kV medium-voltage provided by the grid. It gets transformed into the three-phase 480V_{AC} distribution bus that then gets converted to the DC distribution bus voltage. The SST replaces both the 13kV transformers and the 480V_{DC} to 800V_{DC} or ±400V_{DC} power conversion. The SST achieves the PFC function, the voltage step-down and the conversion to DC in a single power conversion stage. The backup generators now need to connect at the medium-voltage node or at the output of the SST through an AC/DC converter. The net result is a higher-efficiency power distribution network and more space on the IT floor for computing.

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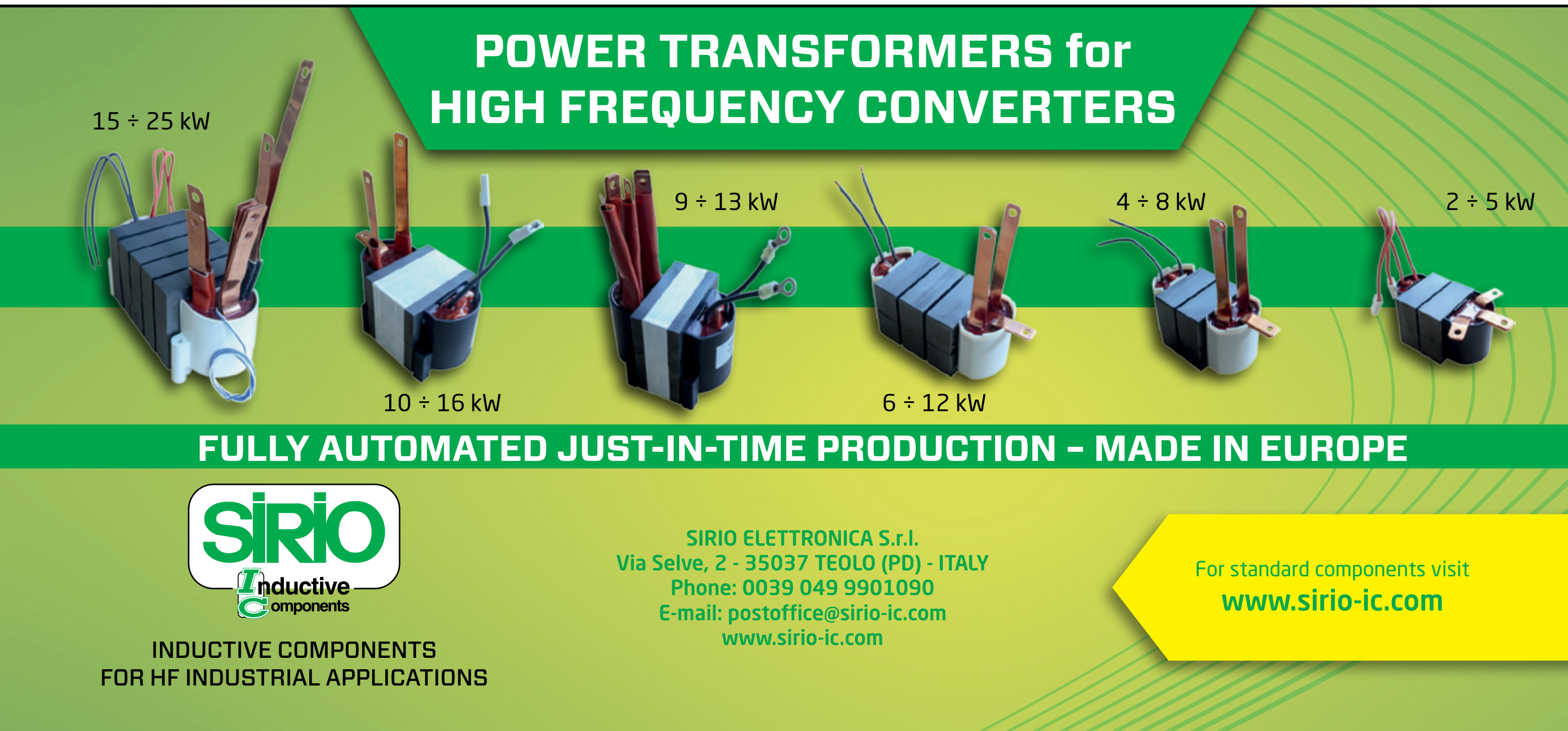


How to bring ultra precise Current Measurement to all Use Cases – not just DC

What are the challenges in power measurement and efficiency calculation? DCCT current transducers are hundreds of times more accurate than standard Hall-effect transducers commonly used for current control in frequency converters. Unfortunately, they are also significantly more complex in design. This story looks at the applications and provides a look at using DCCTs in test benches.

By Horst Bezold, CEO, Signaltec
and Jörn Burk, Head of Industrial Sales for DACH and Eastern Europe, LEM

Broadband precision power meters digitize voltage and current signals. The sampled values u (t) and i (t) are multiplied together. The arithmetic mean of the resulting power curve p (t), averaged over one or more fundamental periods, yields the active power P. The accuracy of power measurement depends on the amplitude accuracy of the voltage and current samples, the time delay between these samples, and the precision of the measurement interval or zero-crossings used to determine the period length.

The first frequency converters appeared in the late 1960s. It took over 20 years before measurement devices were available that could handle the extremely steep voltage edges and distorted current signals of converters. One example is the LEM NORMA Power Analyzer D 6000 from the early 1990s. At that time, current measurement was done using very broadband coaxial shunts and the so-called GUARD technique, which minimized common-mode interference. Common-mode currents from the measurement channel to the device housing are generated by measuring very steep voltage edges at high potential, resulting in amplitude and phase angle errors.

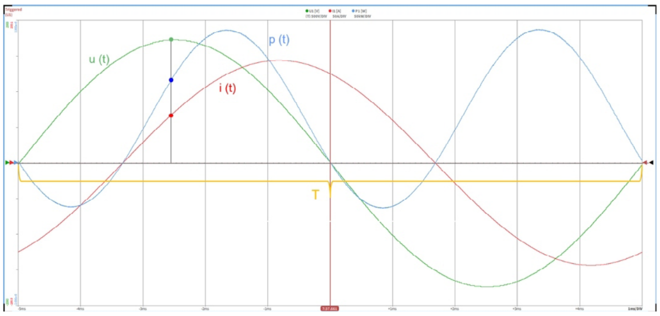


Figure 1: Active power calculation. The two signals u(t) and i(t) must be sampled and multiplied absolutely simultaneously. The accuracy of the active power depends on the amplitude accuracy of the sampled values, the time delay between voltage and current sampling (phase error) as well as on the errors in determining the averaging interval T.

Losses cannot be measured directly

Another challenge in measuring losses in frequency converters and electric motors is their high efficiency and the fact that losses cannot be measured directly. Loss calculation for these drive components is always based on input and output power. For an inverter, this means electrical DC power at the input and electrical AC power at the output. For an electric motor, it's electrical input power and mechanical output power. While individual active power values can be measured with reasonably high accuracy, the uncertainty in loss measurement must consider that errors in input and output power measurements may go in opposite directions – e.g., input power measured too high and output power too low. Thus, the uncertainty in loss measurement is highly dependent on the component's efficiency. It's easy to see that for inverters with nearly 99 % efficiency, measurement errors can result in more than 100 % deviation in actual losses. Therefore, power meters and sensors of the highest accuracy must be used for loss calculations in drive components.

As already mentioned, external coaxial shunts used to be quite suitable for these measurements in terms of amplitude accuracy and phase fidelity. However, measuring the small voltage drop at the shunt output on a high and very distorted voltage signal was highly problematic. The connected measuring device had to have exceptionally high common-mode rejection. In addition, external high-current coaxial resistors were very expensive.

For many years now, ultra-precise DCCT current transducers – galvanically isolated from the measurement signal – have been used to extend the measurement range of power meters. This technology was originally developed to regulate linear DC high-current sources in particle accelerators. One early application in medical technology was magnetic field measurement in MRI scanners.

High DC accuracy alone is not sufficient to precisely calculate losses in an inverter. The transducers must maintain amplitude accuracy across a wide frequency range up to several hundred kHz and must not introduce additional phase shifts between the actual voltage and current signals. Such shifts would alter the power factor and lead to errors in active power and loss calculations.

Comparison of Old and New Transducer Generations

The first mass-produced DCCT transducers were not yet optimized for measuring higher-frequency AC currents. This may be one reason it took so long for these sensors to gain traction in extending the measurement range of power meters. Additionally, the older generation of transducers had relatively high sensitivity to external AC fields. Today, however, they have become standard. Specialized transducers now cover frequency ranges from DC up to several MHz. These are typically only needed for very high-frequency applications, such as signal analysis of new, fast semiconductor switches. In these cases, switching frequencies can approach 100 kHz, and with very low-inductance loads, the harmonics of the switching frequency can theoretically extend into the MHz range.

For typical power and loss measurements, such a wide frequency range is not necessary. The impedance in the measurement circuit significantly attenuates most high-frequency components in the current. And if there are no frequency components in the current, there will be no active power components at that frequency either, because only signal components of voltage and current at the same frequency generate active power or losses.

DCCT current transducers are hundreds of times more accurate than standard Hall-effect transducers commonly used for current control in frequency converters. Unfortunately, they are also significantly more complex in design. In the past, two identical inductors were required to measure the DC component of the current. The second inductor was used solely to compensate for disturbances caused by the first inductor in the main core. These inductors had to be manufactured with extreme precision and uniformity. This report does not delve into the exact workings of the old analog technology.

In developing the latest generation of DCCT transducers, LEM used its expertise in microprocessor-controlled error compensation from other current measurement technologies. In the new IN series, the second inductor for noise suppression has been eliminated.

Figure 2: LEM high precision IN range.

Disturbances caused by the inductor used for DC measurement are learned during the production process, digitized, stored in the processor, and then compensated via a D/A converter, an analog amplifier, and a compensation winding in the main core. Hardly any error-prone analog components are needed in the transducer anymore. Even offset adjustment is stored in the FPGA. The typical DC accuracy of the latest transducers is in the low single-digit ppm range. LEM has patented this new technology.

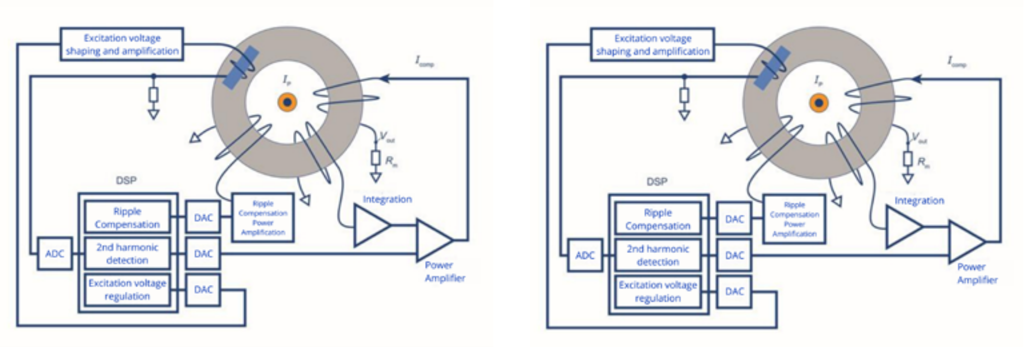


Figure 3: Conventional analog DCCT and new technology with FPGA compensation.

Transducers are now also developed with AC optimization in mind. Here too, LEM uses its knowledge of DC/AC current transducers suitable for converter applications. In the AC circuit, DCCT transducers differ only slightly from standard current-compensated Hall-effect transducers.

Simplifying the use of transducers in test benches

Testing high-voltage batteries in production environments has historically been complex. To simplify the use of transducers in test benches, a dedicated transducer power supply is required. This should ensure stable operation as well as high-precision signal integrity of the connected transducers and burdens. To meet these challenges, SIGNALTEC, who is specialized in broadband power measurement technology, developed its Single- and Multi-Channel Transducer Systems (MCTS), both featuring galvanically isolated power supply channels. SIGNALTEC has established a well-equipped measurement and testing lab where development-stage amplitude and phase accuracy measurements can be performed across a wide frequency range. Extensive accessories allow the transducer output signals to be adapted to all types of current or voltage inputs on measuring devices.

Integrating transducers into automation systems often requires specialized signal digitization, particularly in end-of-line battery manufacturing test setups. High-precision and fast EtherCAT converters can provide this functionality in real time. These converters have evolved significantly from the first models. The first so-called EtherCAT converter could only measure current and provided an EtherCAT protocol at the output. The latest systems, such as Powerlens from REDCUR, developed in collaboration with SIGNALTEC, now offer complete current and voltage measurements, EtherCAT output, and additionally support a CAN protocol.

DCCT transducers have become the standard for extending the measurement range of wideband power analyzers, with digitally compensated DCCT transducers which are aimed to deliver ever more accurate results in both DC and AC current measurement.

Together with its partners, SIGNALTEC and REDCUR, LEM has committed to the field of ultra-precise DCCT current sensors. SIGNALTEC provides AC-optimized CT transducers along with the accessories needed for easy integration into test benches, while REDCUR delivers complete measurement systems for testing high-voltage batteries in production environments.

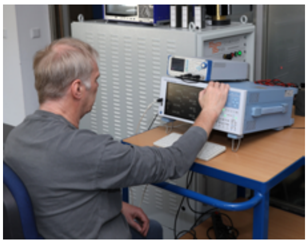


Figure 4 Testing high-voltage batteries. At the high-frequency test bench, amplitude and phase deviations of the transducers can be measured up to a frequency of 500 kHz. Reference standards are coaxial shunts and pulse current transformers.

Figure 5: Using a 1000 A pulse current source, the time delay through the transducer is measured.

Figure 7: Adjustment of the Powerlens measurement system.

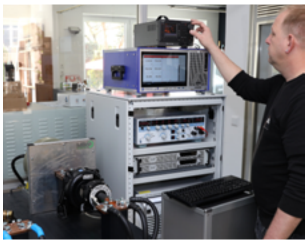


Figure 6: At the high-power test bench, DC power and AC low-frequency power with variable power factor can be simulated up to 1200 V and 2000 A.

www.lem.com

Isolated DC/DC Power Supplies: Module or Discrete Design?

When is a fully integrated module the better option, and when does a discrete design offer the greater advantage? This story discusses the major factors and trade-offs; it helps design engineers to make the best-fitting decision for their individual design.

By the engineering team of RECOM Power

In the development of isolated DC/DC converters, that decision often arises at an early project stage. Some applications benefit from the speed and simplicity of a ready-made module, while others justify a more customised power stage assembled from individual components. Both approaches can be technically valid, but they differ significantly in terms of flexibility, engineering effort, manufacturability and total system cost.

DC/DC Components of the shelf

Finished DC/DC modules are often the preferred route where development schedules are tight and design risk must be contained. They simplify integration, reduce the effort required to qualify individual components and provide a predictable solution in terms of performance, isolation and compliance. In low-volume projects or early design phases, this can make modules the more practical choice.

Discrete DC/DC implementation

A discrete implementation, by contrast, gives engineers more control over the converter architecture. Topology, thermal behaviour, mechanical integration and PCB placement can all be tailored more closely to the application. This added freedom can be particularly valuable where board space is constrained, where unusual form factors are required, or where electrical specifications do not align neatly with the footprint of a standard module.

The key decision-making factors

In practice, the choice is rarely determined by component cost alone. Engineering resources, availability of suitable magnetic components, validation effort, production methods and in-house power design expertise all play a role. An isolated DC/DC converter is not simply a controller paired with a transformer; it is a tightly balanced subsystem in which switching behaviour, isolation, regulation, EMI performance and thermal constraints interact continuously.

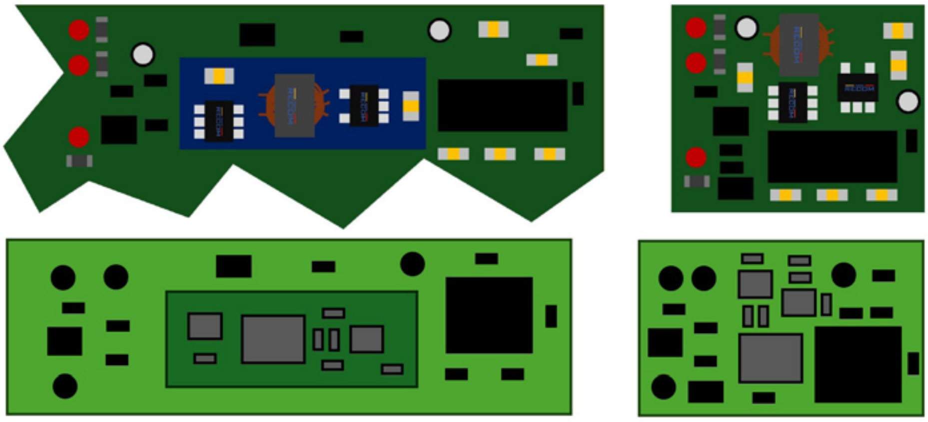


Figure 1. DC/DC supply modules (left) require a fixed space, while a discrete approach (right) can better accommodate space-constrained PCB layouts.

Transformer

The isolation transformer remains one of the key elements in that equation. In many designs, it is the component that most strongly influences feasibility, efficiency, mechanical size and output-voltage configuration. If no suitable standard transformer is available, the effort associated with a discrete solution can rise quickly. On the other hand, an application-specific magnetic design may unlock optimisations that a standard module cannot easily deliver.

What about the layout?

PCB layout is another important consideration. A power module occupies a clearly defined area on the board and can simplify placement. A discrete design, however, can often be distributed more flexibly within the available space. That can be advantageous in compact assemblies, irregular board geometries or densely integrated systems where every square millimetre matters. In some cases, discrete solutions may also fit better into established manufacturing flows by avoiding secondary assembly steps associated with larger module packages.

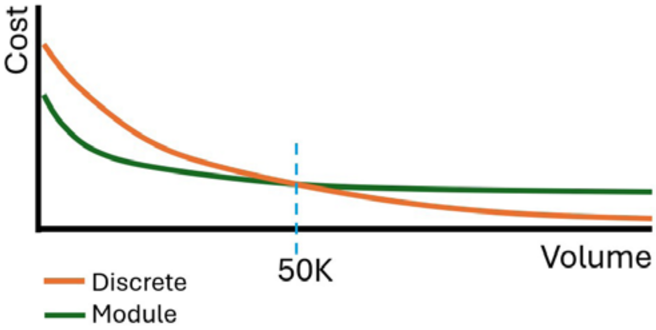


Figure 2. Discrete designs have a higher initial cost, but they become the more cost-effective approach (based on TCO) after approximately 50,000 annual units.

The cost picture typically follows a familiar pattern. Modules tend to offer an economic advantage at lower production volumes because they reduce development overhead and shorten implementation time. Discrete approaches may become more attractive as annual quantities rise and the design can be optimised more precisely around material cost and manufacturing efficiency. The exact crossover point depends on the application, however, and should be evaluated case by case rather than assumed in advance.

For development teams, the central question is therefore not simply 'module or discrete?', but which approach offers the best balance of risk, effort, flexibility and total cost for the specific project. A structured assessment at the start of development—covering board space, target cost, time-to-market, certification requirements and available design expertise—can prevent expensive redesigns later in the process.

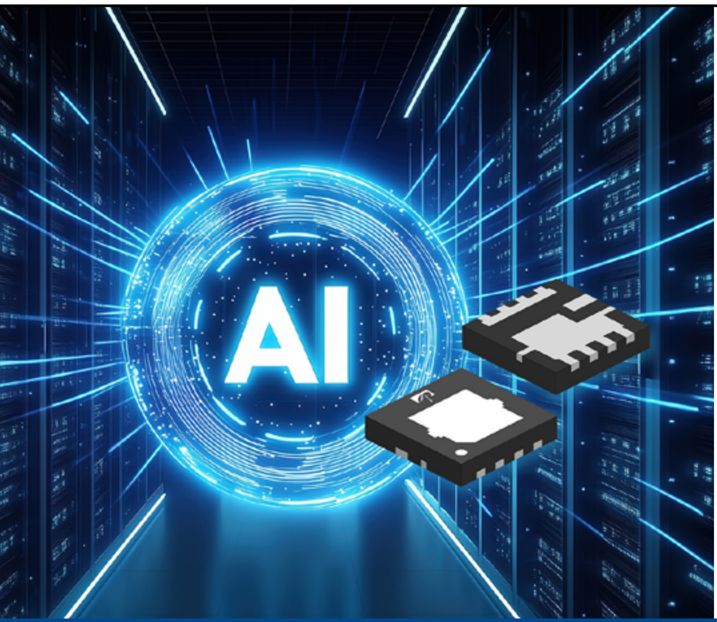
The market is increasingly moving toward greater design freedom. In addition to complete power modules, suppliers are beginning to offer matched core components for discrete isolated DC/DC solutions, allowing engineers to combine a more customised implementation with a reduced level of design risk. For the industry, this widens the spectrum between standardisation and full custom development. RECOM is among the suppliers addressing this shift by supporting both prequalified module solutions and the relevant core components for discrete converter design.

Time-to-market

To reduce development effort and support shorter time-to-market targets, RECOM also provides matched IC and transformer combinations for discrete converter designs. These combinations are selected to provide the appropriate driver topology for the intended application and to ensure magnetic and electrical compatibility between the components. They also take into account power-transfer requirements, input and output voltages, isolation requirements and height constraints, and they are pre-tested and verified as matching building blocks within the converter concept.

This approach is also relevant from a sourcing perspective. RECOM is the only single source company providing both the IC and the transformer. For design teams, this means that two of the central functional elements of an isolated DC/DC converter can be obtained from one supplier, rather than being specified and sourced separately.

www.recom-power.com



Designing Power Supplies for Industrial Functional Safety – Part 2: Creating a Safe Power Design

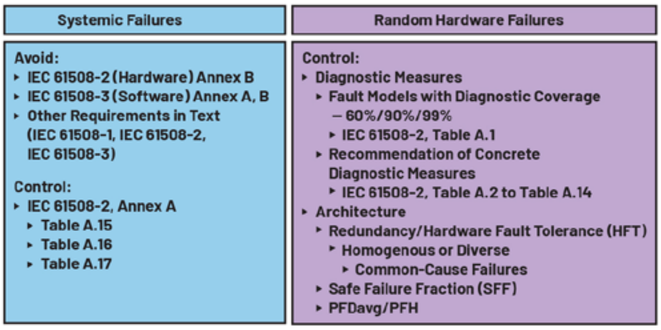
While Part 1 of this series showed what the IEC 61508 requires from power supplies to achieve functional safety, Part 2 provides insights into applying the basic functional safety standard's principles about eliminating systematic failures and controlling random hardware failures to ensure safe power supply design.

By Bryan Angelo Borres, Senior Functional Safety Engineer, Analog Devices

This Part 2 of this series details the critical distinction between systematic and random failures that can impede a safety-related system from achieving a safe state, emphasizing the necessity of a safe power supply design adhering to standards like IEC 61508. Systematic failures, which are deterministic and include both hardware and software faults, must be eliminated through proactive design modifications, such as implementing component derating, robust overvoltage protection, and proper power supply monitoring. Conversely, random hardware failures that result from component degradation mechanisms are controlled using diagnostic measures and architectural design, primarily quantified through failure modes, effects, and diagnostics analysis (FMEDA). Effective management of both failure types—eliminating systematic weaknesses and controlling random hardware failures—is essential to meet the required safety integrity level (SIL).

IEC 61508: A Recall

Aside from knowing what the functional safety standard requires, it's important to know the types of failures that can hinder safety-related systems from achieving the safe state when starting a safety-related system, thus, safe power supply design. A safety function can either carry out positive actions to avoid hazardous situations or prevent actions from being taken to maintain a safe state. In terms of failures, a safety function can either have a systematic failure or a random one as shown in Figure 1. Systematic failures include both hardware and software. These failures occur in a deterministic way due to a certain cause and can be eliminated by modification of the design and other measures. For instance, IEC 61508 provides normative techniques and measures so systematic failures can be avoided and controlled. More details can be found in part of this story which was published in Bodo's Power Systems 8/2025.



Systemic Failures

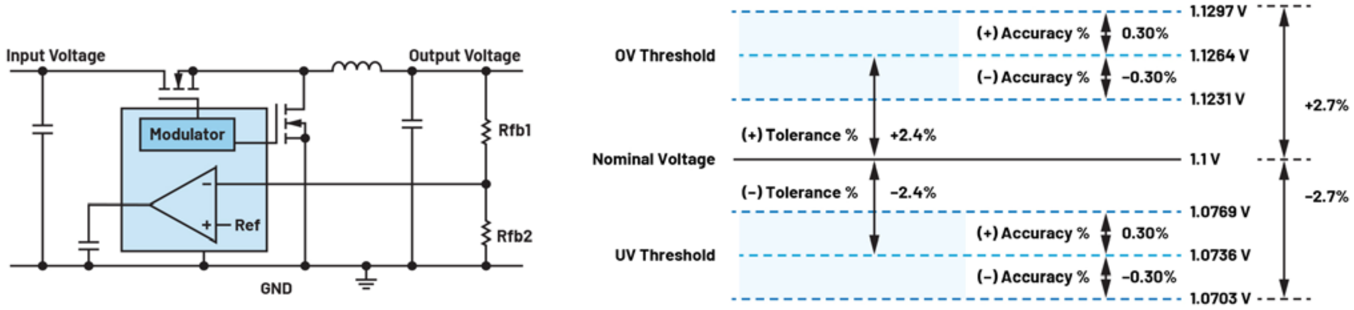
Avoid:
- IEC 61508-2 (Hardware) Annex B
- IEC 61508-3 (Software) Annex A, B
- Other Requirements in Text (IEC 61508-1, IEC 61508-2, IEC 61508-3)

Control:
- IEC 61508-2, Annex A
  - Table A.15
  - Table A.16
  - Table A.17

Random Hardware Failures

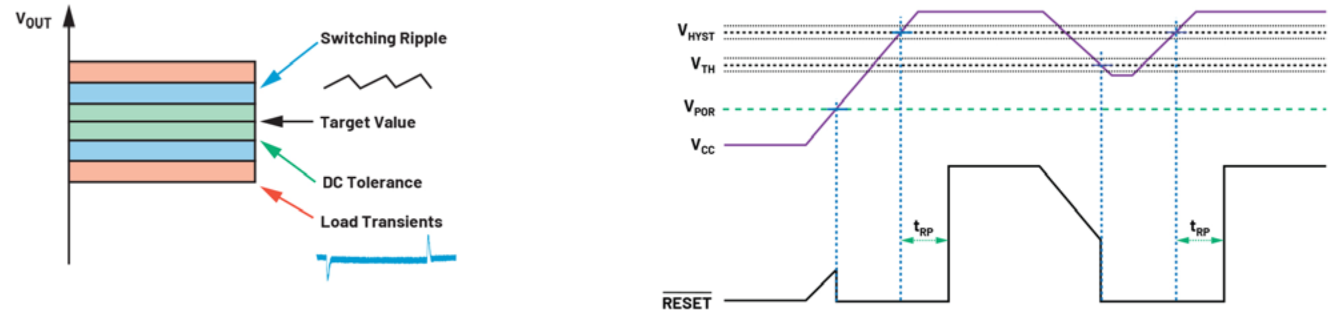
Control:
- Diagnostic Measures
  - Fault Models with Diagnostic Coverage – 60%/90%/99%
    - IEC 61508-2, Table A.1
  - Recommendation of Concrete Diagnostic Measures
    - IEC 61508-2, Table A.2 to Table A.14
- Architecture
  - Redundancy/Hardware Fault Tolerance (HFT)
    - Homogenous or Diverse
      - Common-Cause Failures
  - Safe Failure Fraction (SFF)
  - PFDavg/PFH

Figure 1: IEC 61508: systematic failures vs. random hardware failures.



(a) Switch-Mode Power Supply Circuit Example

(c) Power Supply Monitor Accuracy and Tolerance Example



(b) Factors Affecting the Accuracy of Power Supply Output

(d) A Timing Diagram of a Monitored Voltage V_{CC} and Reset Output Signal of a Voltage Supervisor

Figure 2: Power supply monitoring considerations.[1,2,3]

On the other hand, random failures can only occur in hardware. These types of failures result from one or more of the possible degradation mechanisms in the hardware happening at a random time. Thus, random hardware failures can only be controlled through diagnostic measures and the proper design of architecture.

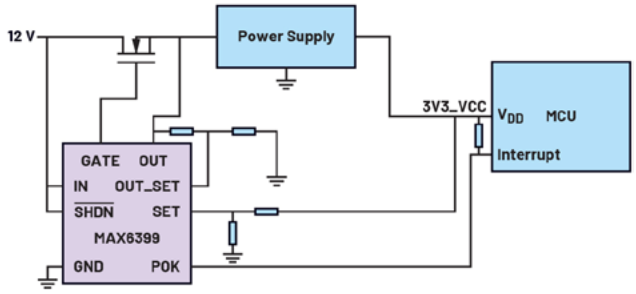
Controlling Systematic Failures

Regardless of safety integrity level (SIL), measures against voltage breakdowns, and other power supply-related dangerous failures, are mandatory to control systematic failures. This can be in the form of passive measures such as employing passive protections (such as fuses and Zener diodes), implementing proper derating of components, and allotting sufficient operating margins. In terms of active measures, this can be in the form of power supply diagnostic measures such as adding overvoltage protections, windowed power supply monitoring, secondary voltage control, current limiting, and other active protection circuitries. These measures to control systematic failures are important to implement in a power supply design aiming for compliance with a certain SIL.

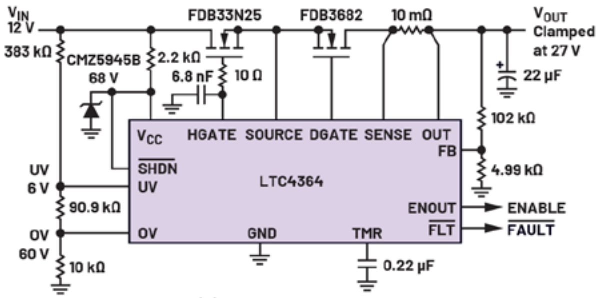
Aside from complying with the required performance requirements scoping electrical, thermal, mechanical, electromagnetic compatibility, product safety, and other related standards, some questions to ponder are as follows.

Are all voltages properly monitored to enable proper power sequence? Consider different factors affecting a power supply's output accuracy when setting the power supply monitor's overvoltage (OV) and undervoltage (UV) thresholds to enable seamless sequencing and diagnostics. This can be seen in Figure 2.

Are sufficient protections, for example, surge protections, etc., or other measures employed to improve electromagnetic immunity? Consider protection measures such as OV/UV protection as in the MAX6399, surge stoppers as in the LTC4364, reverse-input protection, reverse-current, and current-limiting, as shown in Figure 3.



(a) OV/UV Protection



(b) Surge Stopper with Ideal Diode

Figure 3: Employing protections to improve system reliability.[2]

Are well-tried components used according to their specifications with sufficient derating, such as 67 % of loading condition?4 Sufficient derating involves ensuring components operate in their safe operating area as well as employing additional operating margins as shown in Figure 4. For instance, a 125 °C-rated part provides sufficient derating when used to operate at 55 °C ambient operating temperature with junction temperature rising to 85 °C.[4,5,6]

Further questions of interest are: What other systematic failure modes need to be addressed? What about Back EMF (electromotive force) that can damage input circuitries[7]? Are there any timing/pulse-width issues that can cause cross-conduction? Furthermore, it is important to check for hot spot issues that can cause thermal runaways as shown in Figure 5.

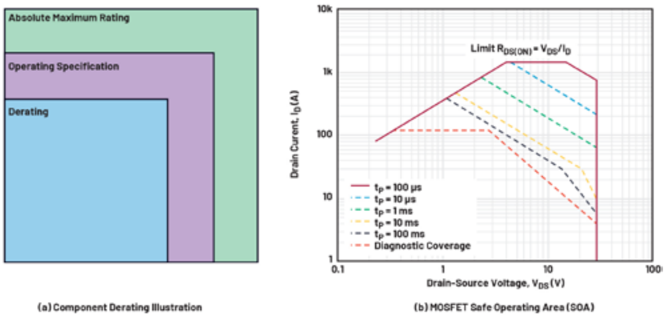


Figure 4: Employing protections to improve electromagnetic immunity.[6]

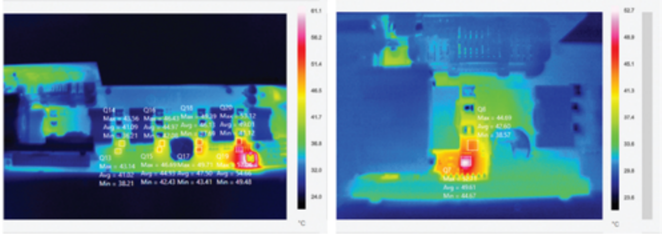


Figure 5: Hot spot comparison of a board running at full load during discharge (left) and charge (right) modes of operation, respectively.[8]

Controlling Random Hardware Failures

A failure modes, effects, and diagnostics analysis (FMEDA) document is used to analyze and quantify the impact of random hardware failures on the performance of safety-related systems. Its input includes failure rate, application, and hardware design information. Meanwhile, its output shows block failure modes and effects, failure rates λSD, λSU, λDD, and λDU, diagnostic coverage for each failure mode, and the SIL metrics. These are shown in Figure 6.

Analyzing a product with an FMEDA includes other requirements. The first requirement is analyzing the failure modes of components used to implement the safety function. The second requirement is employing additional safety (diagnostic) measures/built-in self-tests (BISTs) against dangerous undetected failures to improve SIL

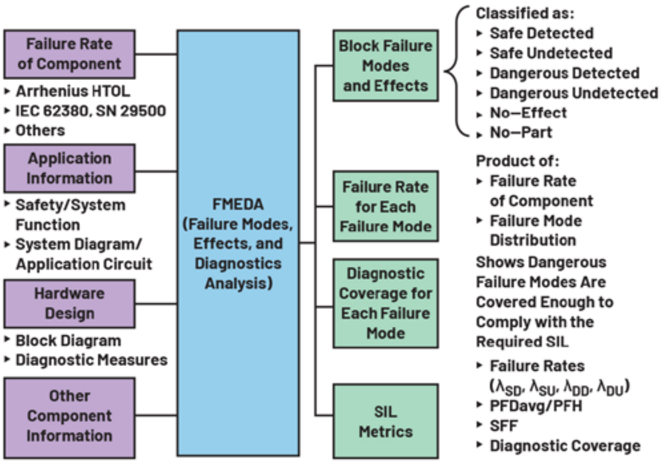


Figure 6: FMEDA composition.

metrics accordingly. Doing iterations until the required safe failure fraction (SFF) and probability of dangerous failure (PFH/PFDavg) metrics are met is the third requirement. These three are complemented by other considerations; they include using functional safety compliant components,[9] which offer several benefits, or using Analog Devices' FS-enabled parts, which provide safety application notes10 to show an IC's failure rate information, failure mode distribution (FMD), and pin failure modes and effects analysis (FMEA) information to help speed up the system FMEDA.

Conclusion

In summary, the foundation of a robust and safe power supply design lies in a rigorous approach to failure management as prescribed by IEC 61508. Addressing systematic failures is paramount; these deterministic faults must be eliminated through proactive design choices, such as implementing windowed voltage monitoring, employing sufficient component derating, and integrating surge protection. By adopting both passive and active measures early in the development cycle, engineers can mitigate risks like thermal runaway and voltage breakdowns, ensuring the power system remains within its defined safe operating area even under stress.

Furthermore, the design must account for the unpredictable nature of random hardware failures. While these cannot be eliminated through design alone, they are effectively managed by quantifying risks via FMEDA. By meticulously analyzing failure rates and incorporating diagnostic coverage like BISTs, designers can control hardware degradation impacts to meet stringent SIL requirements. Ultimately, the synergy between eliminating systematic weaknesses and controlling random hardware failures ensures that the power supply functions not just as a power source, but as a reliable backbone for functional safety systems.

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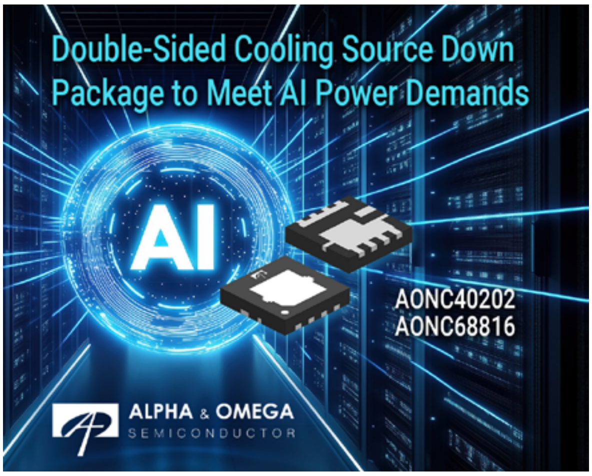
www.analog.com

200 V MOSFETs in Multiple Standard Power Packages

iDEAL Semiconductor expanded its SuperQ™ 200 V MOSFET portfolio with the iS20M5R5S1T, which is available in the industry-standard TOLL package, and the iS20M6R3S1P, available in the TO-220 package. The iS20M5R5S1T achieves a maximum $R_{DS(on)}$ of 5.5 mΩ, while the iS20M6R3S1P delivers a maximum $R_{DS(on)}$ of 6.3 mΩ. Versions in D2PAK-7L (iS20M5R5S1H) and TOLT (iS20M5R5S1TC) are also planned. Typical applications are e.g. in next-generation power systems and motor-drive applications as well as switched-mode power supplies (SMPS), secondary-side synchronous rectification, and high-current industrial and battery-powered systems. The $V_{GS(th)}$ is specified with +/- 0.5V.

www.idealsemi.com



25 V and 80 V MOSFETs meeting AI Server Power Demands

Alpha and Omega Semiconductor (AOS) introduced its AONC40202 25 V MOSFET and AONC68816 80 V MOSFET that are available in DFN 3.3 x 3.3 double-sided cooling source-down packaging. The devices are designed to support intermediate bus converter (IBC) DC/DC applications in AI Servers. AONC40202 and AONC68816 feature a top-clip design for the exposed drain contact. The packaging technology used in the AONC40402 25 V and AONC68816 80 V MOSFETs features a large top clip, which enables a thermal resistance rate value of $R_{thc\text{-}top(max)}$ to be 0.9 °C/W. The AONC40202 has a continuous current capability of up to 405 A, with a maximum junction temperature of 175 ° C.

www.aosmd.com

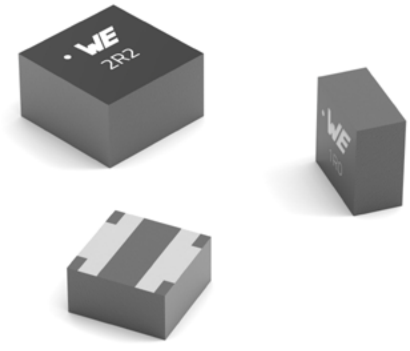
Power Modules designed for harsh Environments

Microchip Technology announced its BZPACK mSiC® power modules, designed to meet HV-H3TRB (High Humidity High Voltage High Temperature Reverse Bias) standards. Available in topologies including half-bridge, full-bridge, three-phase and PIM/CIB configurations, they are suited for deployments in industrial and renewable energy applications. BZPACK modules feature a baseplate-less design with Press-Fit, solderless terminals and optional pre-applied Thermal Interface Material (TIM). The MB and MC families of mSiC MOSFETs are targeted towards both industrial and automotive applications, with AEC-Q101 qualified options available. These devices support common gate-source voltages $V_{GS} \geq 15$ V and are available in TO-247-4 Notch and die form (waffle pack).

www.microchip.com

Power Inductors for Automotive Electronics

With the WE-MXGA inductors Würth Elektronik presents AEC-Q200-certified components qualified for automotive applications. The inductors are well suited for use in lighting, infotainment systems, DC/DC converters (48 V/12 V), battery-management systems, ADAS modules, and LED headlights. The magnetically shielded SMT storage inductor WE-MXGA is particularly targeted towards high-frequency switch-mode power supplies, especially for switching regulators based on the latest GaN and SiC transistor technologies. These power inductors, which are made from pressed nanocrystalline powder core material, are available in two versions, in form factor 4020 with inductances of 0.16 to 4.7 µH and in form factor 5030 with inductances of 0.22 to 15 µH. With a current capability of up to 28 A and an operating voltage up to 80 VDC, the inductor has an operating temperature range from -40 °C up to 125 °C.



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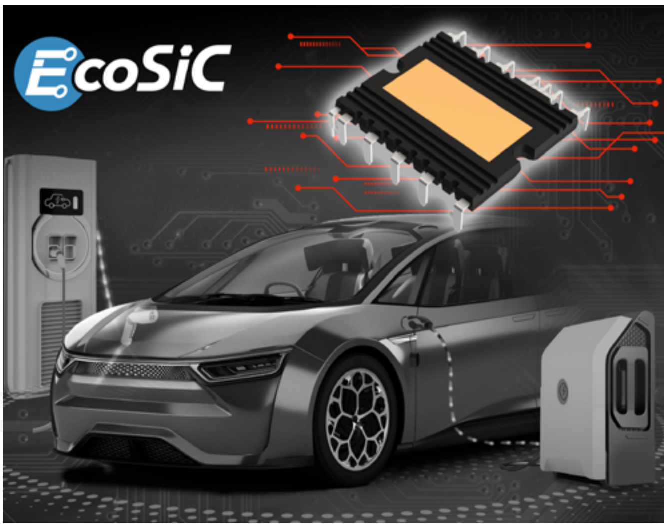
Reference Designs for Three-Phase Inverters based on SiC Power Modules



ROHM has released reference designs named "REF68005", "REF68006", and "REF68004" for three-phase inverter circuits featuring EcoSiC™ brand SiC molded modules "HSDIP20", "DOT-247", and "TRCDRIVE pack™ " on ROHM's website. Designers can use the data provided in these reference designs to create the drive circuit boards. When combined with ROHM's SiC modules, these designs help reduce the person-hours required for device evaluation. The designs support output power levels up to the 300 kW class. Three types of SiC modules compatible with these reference designs are already available for purchase through online distributors such as DigiKey and Farnell. Several support resources, including simulation and thermal design support, are available to facilitate quick evaluation and implementation of the products. ROHM's comprehensive solutions can provide valuable assistance in component selection.

www.rohm.com

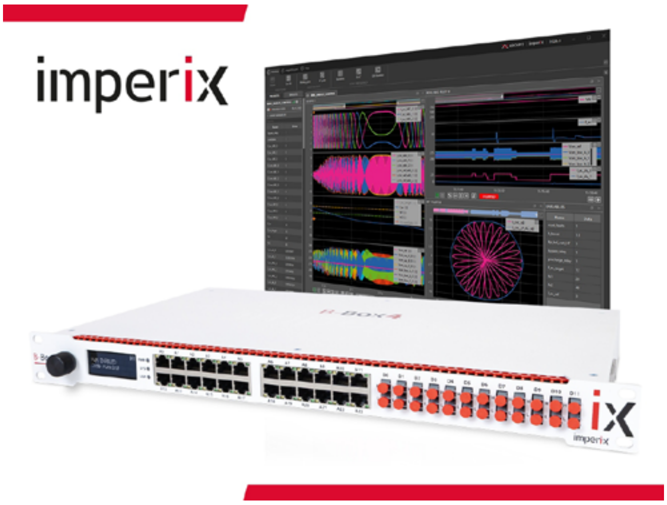
2000 V / 40 A 4-Phase Boost Module

Inventchip Technology (IVCT) introduced the IV3B20023BA2, 2000 V 4-phase boosts in a 3B module package. Each phase consists of a 2000 V 23 mΩ SiC MOSFET and a 40 A diode connected in a boost converter topology. The product is aiming 1500 V solar photovoltaic (PV) system applications. The four boost phases are divided into two electrically isolated groups. Each group has two boosts with a common power ground and a separate boost output, plus an NTC for DBC temperature sensing. With such a topology arrangement, the module maximizes the flexibility of the circuit configuration for PV systems with a single, two or four DC inputs. The 3B module has the same dimensions as the standard Easy-3B and provides a minimum 10 mm creepage from terminals to terminals and terminals to heatsink. The difference is that the 3B uses a metal base instead of a bare DBC. The metal base allows the module to be screwed on a heatsink with a stable fixing force and avoids the module's plastic case aging issue which could lead to the reduction or loss of the fixing force during temperature cycling tests or real applications. This 2000 V MOSFET is based on Inventchip's second generation SiC technology. The co-packed 2000 V SiC diode was designed to carry a surge current over 5 times of its rated DC current. Compared to the flying-cap topology currently used in 1500 V PV systems, the 2000 V boost converter simplifies PV MPPT circuit design e. g. by eliminating external capacitors.

www.inventchip.com.cn

Prototyping Controller for Wide-Bandgap Power Converters

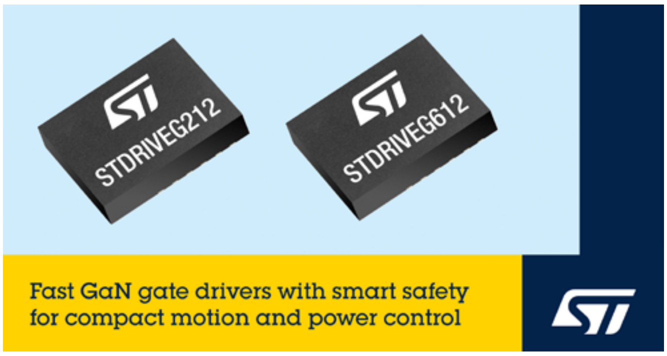
Imperix introduced the B-Box 4, a Rapid Control Prototyping (RCP) system for power electronics. Featuring a proprietary architecture optimized for low-latency operation, the controller delivers advanced control loop speeds and signal fidelity. The device aims to accelerate experimental prototyping activities in both industrial and academic research environments. The B-Box 4 enables 20 MSamples/s synchronous sampling at all analog inputs simultaneously. This captures the full high-frequency content of current ripple or medium-frequency waveforms, and it permits the direct visualization of waveforms without extra instrumentation. Using oversampling, the B-Box 4 is not only a control system but also a monitoring and debugging tool, usable directly from the readily available measurements. It provides a PWM resolution of 250 ps, which is useful for ultra-fast switching applications, especially for techniques relying on phase shift control such as within medium-frequency converters. B-Box 4 can execute the control loop of simple systems in under 2 µs, directly from the CPU. The device is fully integrated into an ecosystem of products designed to accelerate prototyping in power electronics.



www.imperix.ch

GaN Half-Bridge Drivers provide smart Protection

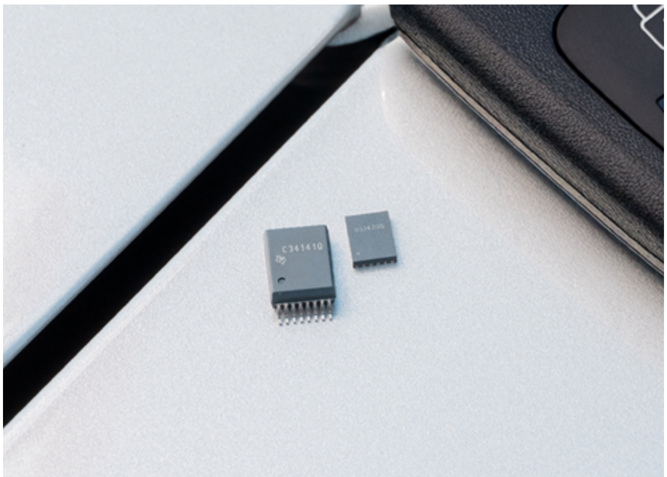
STMicroelectronics has announced two half-bridge gate drivers that bring gallium-nitride (GaN) efficiency, thermal performance, and miniaturization to power and motion-control applications. The STDRIVEG212 and STDRIVEG612 deliver tightly controlled 5 V gate-drive signals to enhanced-mode GaN HEMTs, powered from a high-side voltage up to 220 V or 600 V respectively. The drivers contain high-side and low-side 5 V linear regulators (LDOs), a high-side bootstrap diode, and protection including under-voltage lockout (UVLO) in a QFN package. An integrated fast-startup voltage regulator stabilizes the supply voltage for the driver output stage, enabling consistent gate control, while an embedded comparator turns off both GaNs on detecting overcurrent. Smart shutdown (SmartSD) automatically holds the switches off long enough to cool down and a fault pin provides overcurrent, overtemperature and UVLO reporting. The propagation delay of 50 ns is matched between high side and low side, with high-side start-up time of 5 µs and ±200 V/ns dV/dt transient immunity, permitting high rotational speeds. The integrated LDOs have high current capability and provide separate sink and source paths, sinking up to 1.8 A / 1.2 Ω, and sourcing 0.8 A / 4.0 Ω. With 20V-tolerant logic inputs and a dedicated shutdown pin the STDRIVEG212 and STDRIVEG612 are able to save power during inactive periods. The EVLSTDRIVEG212 evaluation board is suitable for both devices.



www.st.com

Power Modules with increased Power Density

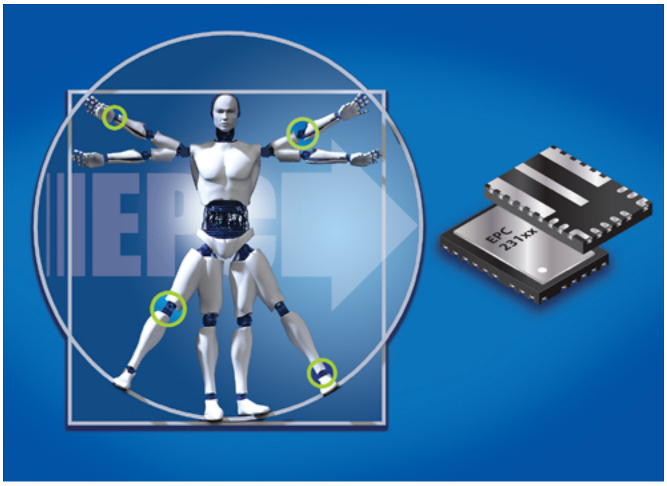
Texas Instruments (TI) unveiled isolated power modules, helping enable increased power density, efficiency and safety in applications ranging from data centers to electric vehicles (EVs). The UCC34141-Q1 and UCC33420 isolated power modules use TI’s IsoShieldTM technology, a proprietary multichip packaging solution that achieves up to three times higher power density than discrete solutions in isolated power designs. The IsoShield technology copackages a planar transformer and an isolated power stage, offering functional, basic and reinforced isolation capabilities. It enables a distributed power architecture, helping manufacturers meet functional safety requirements by avoiding single-point failures. The result is compact packaging while delivering up to 2 W of power, enabling designs for automotive, industrial and data center applications that require reinforced isolation. Evaluation modules, reference designs and simulation models are also available.



www.ti.com

100 V Integrated GaN Power Stages

Efficient Power Conversion (EPC) has introduced its next generation of 100 V integrated GaN power-stage ICs – EPC23108, EPC23109, EPC23110 and EPC23111 – targeting high-performance motion and power systems such as humanoid robots, drones, and other compact battery-powered platforms. The devices are designed to simplify implementation and improve operational robustness in real-world environments while preserving the efficiency and power-density advantages typical of integrated GaN technology. Each IC integrates the high-side and low-side eGaN® FETs together with the gate driver and level shifting circuitry in a thermally enhanced QFN package. They support operation up to 100 V, with load current capability of 35 A (EPC23108, EPC23109) and 20 A (EPC23110, EPC23111), enabling reliable high-frequency switching performance. The control interface has an active-low fast-shutdown and standby input with a built-in 65 kΩ pull-up, which makes it work with industrial logic standards. As a result, designers can connect the devices directly to standard controllers without having to do any extra signal conditioning. This makes the design easier and makes sure that the devices work the same way on all platforms. Operational safety is improved through deterministic shutdown behavior. When standby is asserted, PWM switching stops immediately and the driver enters a low-quiescent-current state from the VDRV supply. If the driver supply is lost, an active gate pull-down ensures both the high-side and low-side FETs remain off, maintaining system control during fault conditions and enhancing reliability. The family also supports continuous 100% duty-cycle operation, which is necessary for full-torque and uninterrupted conduction modes.



www.epc-co.com

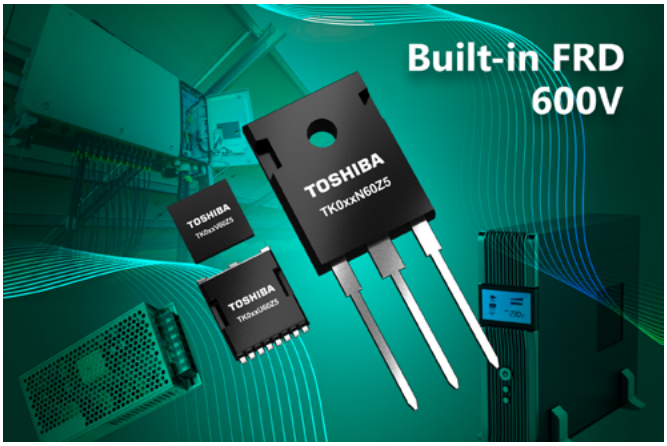
Full-Brick 48 V AC/DC Supply with up to 94 % Peak Efficiency

Advanced Energy Industries has extended its range of AIF full-brick board-mounted AC/DC power supplies for telecom and industrial applications with the AIF13WAC, 48 V 600 W, with a peak efficiency of up to 94 %. The AIF13WAC integrates full digital control and monitoring (via PMBus) and active current sharing along with internal inrush limiting functionality. Compared to the previous generation, the AIF13WAC increases output power by 20 % in the same form-factor and therefore is compatible with all accessories created for previous generations, including case-kits, heatsinks and EMI filters. For contact-cooled, fanless applications such as IP-sealed designs, there is now an upgrade path to deliver greater power than the previous generation of 500 W products. The AIF13WAC accepts a input voltage range of 90 to 264 V_{AC}, and delivers a 13 A, 48 V_{DC} nominal output alongside a 10 V (250 mA) auxiliary output. It can run with up to three units in parallel. The input EMI filter, hold-up capacitors, and output capacitors are the only external components required for the realization of a successful application design.

www.advancedenergy.com

600 V Super Junction Power MOSFETs

Toshiba Electronics has added the DTMOSVI 600 V HSD (High-Speed Diode) N-channel power MOSFETs to the DTMOSVI 600 V Series featuring a super junction structure. The seven additional products are available in TO-247, TOLL and DFN8×8 packages, providing engineers with options that balance power handling, thermal performance, switching efficiency, and system miniaturization capabilities for diverse application needs. A product highlight is the TK058V60Z5, which achieves an drain-source on-resistance ($R_{DS(ON)}$) of 50 mΩ (typ.) in a DFN8×8 package. Applications include switched-mode power supplies (SMPS) for data center servers, uninterruptible power supplies (UPS), and photovoltaic power conditioners. These products employ lifetime control technology, which intentionally introduces defects into the diode to enhance carrier recombination speed. This technique enhances the reverse-recovery performance of the body diode, a critical requirement for bridge and inverter circuit applications. Compared to Toshiba's existing DTMOSVI 600 V series without a built-in high-speed recovery diode, the reverse recovery time (t_{rr}) has been reduced by approximately 60 %, and the reverse recovery charge (Q_{rr}) by approximately 85 % (measurement conditions: V_{DD} = 400 V, V_{GS} = 0 V, I_{DR} = 20 A, $-di_{DR}/dt$= 100 A/µs, T_a = 25 °C). Both G0 SPICE and G2 SPICE models are available as well as an online circuit simulator.



www.toshiba.semicon-storage.com

TLVR Quad Phase Module exceeding 2 A/mm^2

Infineon Technologies announced a high-current-density quad-phase power module with TLVR (trans-inductor voltage regulator) inductors. The TDM24745T is an OptiMOS™ quad-phase power module designed to meet the rapidly growing power requirements of next-generation AI accelerators. Integrating four power stages, a TLVR inductor and decoupling capacitors into a 9 x 10 x 5 mm^3 package. The module delivers a current density exceeding 2 A/mm^2.

The TLVR architecture can reduce the required output capacitance by up to 50 percent. TDM24745T offers up to 320 A peak current capability. The TDM24745T power module integrates directly into Infineon's end-to-end AI server power delivery ecosystem, which spans everything from the grid interface to the core processor rails.

www.infineon.com

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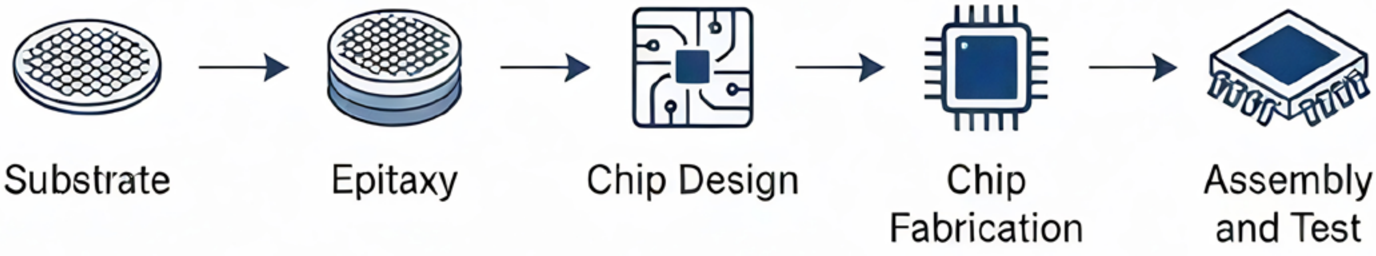
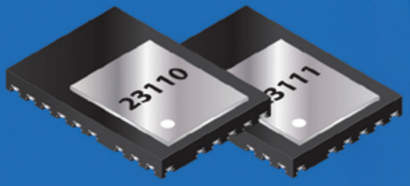


EPC
EFFICIENT POWER CONVERSION
EPC

23108
109



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