

# Bodo's Power Systems®

Electronics in Motion and Conversion

July 2026

## EPC GaN

IS THE

# BENCHMARK

for Every Voltage Node

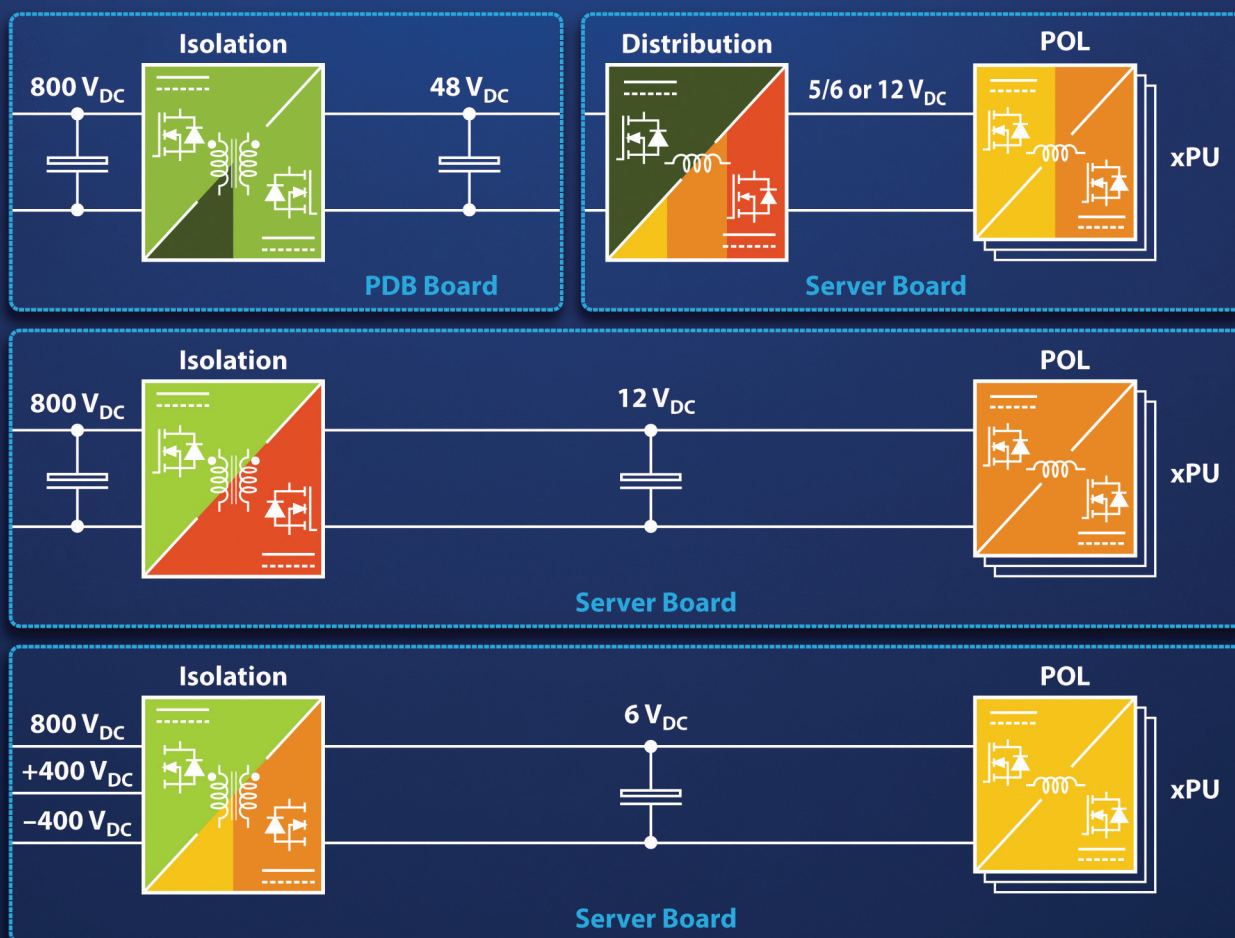
EPC2376 150 V

EPC2367 100 V

EPC2377 40 V

EPC2378 25 V

EPC2370 18 V



See back cover for details



# POWER CHOKES TESTER DPG10/20 SERIES

Inductance measurement  
from 0.1 A to 10 kA

## KEY FEATURES

Measurement of the

- Differential inductance  $L_{diff}(i)$  and  $L_{diff}(\int U dt)$
- Amplitude inductance  $L_{amp}(i)$  and  $L_{amp}(\int U dt)$
- Flux linkage  $\psi(i)$
- Magnetic co-energy  $W_{co}(i)$
- Flux density  $B(i)$
- DC resistance

Also suitable for 3-phase inductors

## WIDE RANGE OF MODELS

7 models available with maximum test current from 100A to 10000A and maximum pulse energy from 1350J to 15000J

## KEY BENEFITS

- Very easy and fast measurement
- Lightweight, small and affordable price-point despite of the high measuring current up to 10000A
- High sample rate and very wide pulse width range  
=> suitable for all core materials

## APPLICATIONS

Suitable for all inductive components from small SMD inductors to very large power reactors in the MVA range

- Development, research and quality inspection
- Routine tests of small batch series and mass production





INTRODUCING

# UX3 SERIES HIGH TEMPERATURE UNLYTIC® 125°C



The UX31 / UX32 / UX34 / UX35 UNLYTIC HIGH TEMPERATURE UX3 SERIES represents the best choice for high power DC application featuring operation to 125°C with no voltage derating and **acts as a drop in replacement** to existing standard polypropylene capacitors.



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**Bodo's Power Systems®**  
Electronics in Motion and Conversion



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# Supporters & Friends

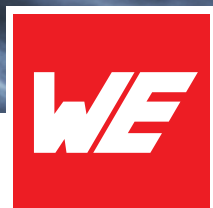
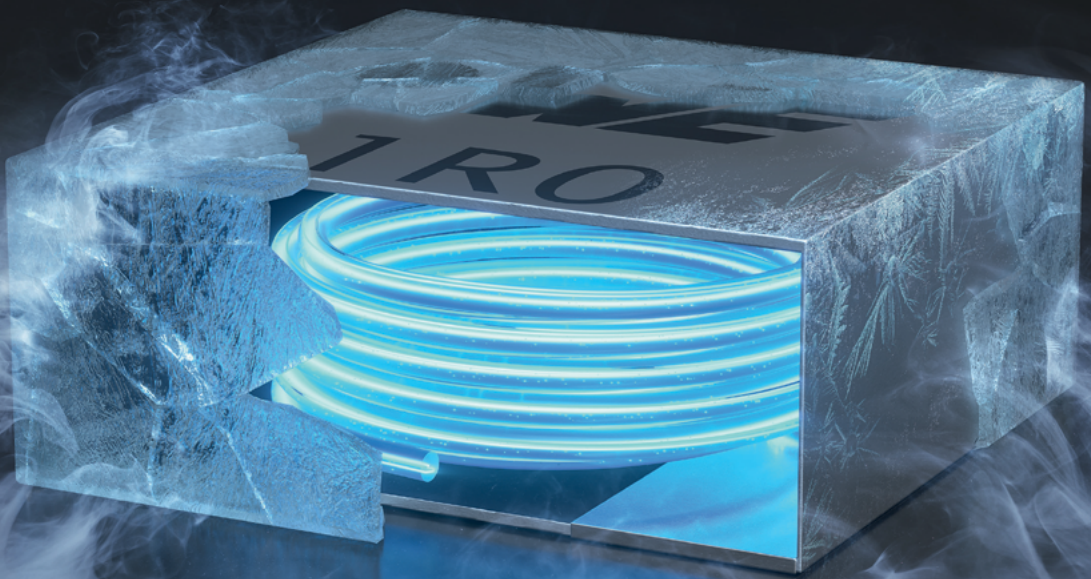




WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

# ULTRA LOW LOSSES

## WE-MXGI



**WE are here for you!**

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[www.we-online.com/webinars](http://www.we-online.com/webinars)

With the WE-MXGI Würth Elektronik offers the newest molded power inductor series. It combines an innovative iron alloy material that provides high permeability for lowest  $R_{DC}$  values combined with an optimized wire geometry.

Ready to Design-In? Take advantage of personal technical support and free samples ex-stock.

[www.we-online.com/WE-MXGI](http://www.we-online.com/WE-MXGI)

### Highlights

- Extremely high power density
- Ultra low  $R_{DC}$  values and AC losses
- Magnetically shielded
- Optimized for high switching frequencies beyond 1 MHz

#UltraLowLosses



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cause whatsoever.

# Rockets are fine, but Power is always a must

We recently heard about the IPO of SpaceX on the stock market. Everybody heard of it, even people who are not even interested in the stock market. And why? Because it was the biggest launch (sic!) ever with the highest market capitalization in history. Yes, SpaceX does rocket science, but the physics apply everywhere, and even spacecrafts use "normal" products, however in high-rel quality.

Consumer products and products used in space share several similarities, because in both applications the products need to be small and lightweight. Like all systems, the systems heading into and operating in space need control, and the control devices need to be powered. So far, so good.

Without adequate high-rel power systems no rocket will take off and no satellite or interstellar spacecraft will operate. However, while the public interest often admires the rocket manufacturers, only very minor interest is dedicated to the power (supply) electronics even though this is an absolute prerequisite for the rest of the system. The providers of power systems for extraterrestrial use remind me of the hardware suppliers during the California gold rush, who sold shovels, spades, tarps, nails, clothes etc. to the gold prospectors. While the vast majority of these gold adventurers lost (almost) everything, a few of them did make a fortune. However, the hardware suppliers consistently increased their business with solid earnings because everybody needed their supplies. Considering the elementary importance of power circuits, I ask myself why there is no power hype on the market?

In terms of technology, semiconductors used in space applications need to be very tolerant towards radiation. That's why silicon-based devices need to be "radiation-hardened". However, as we know, the intrinsic material properties of GaN assure that Gallium-Nitride semiconductors are



very tolerant towards radiation, making GaN-based devices a very interesting option for space applications.

If you are interested in GaN and SiC solutions, please mark December 1 & 2, 2026 in your calendar because our next wide band-gap event will take place on these days, in Munich. You will find more details at [www.bodoswb.com](http://www.bodoswb.com) towards the end of the summer.

For more than 20 years Bodo's magazine has been delivered by post to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. And don't miss our Chinese version at [bodospowerchina.com](http://bodospowerchina.com). An archive of every issue of the magazine is available for free at our website [bodospower.com](http://bodospower.com).

**My green tip of the month:**

When you plan your stock market investment, think of power companies as well. Perhaps companies who are active in the green sector can be attractive investments – especially when it comes to renewable energy supplies as their "fuel" is supplied free of charge by mother nature.

*Alfred Vollmer*

## Events

**WPTCE 2026**

Halifax, Canada July 6 – 9  
<https://ieee-wptce.org>

**PCIM Asia 2026**

Shenzhen, China August 26 – 28  
<https://pcimasia-shenzhen.cn.messefrankfurt.com>

**SEMICON Taiwan 2026**

Taipei, Taiwan September 2 – 4  
[www.semicontaiwan.org](http://www.semicontaiwan.org)

**ECCE Europe 2026**

Valencia, Spain September 14 – 18  
[www.ecce-europe.org](http://www.ecce-europe.org)

**electronica India 2026**

Bengaluru, India September 16 – 18  
<https://electronica-india.com>

**WiPDA Europe 2026**

Aalborg, Denmark September 20 -22  
[www.energy.aau.dk](http://www.energy.aau.dk)

**INTELEC 2026**

Nuremberg, Germany September 20 – 23  
[www.intelec.org](http://www.intelec.org)

**ESREF 2026**

Vienna, Austria September 21 – 24  
[www.esref2026.org](http://www.esref2026.org)

**PEMC 2026**

Tallin, Estonia September 23 – 25  
[www.ecpe.org](http://www.ecpe.org)





# Combine highest SoC estimation accuracy with ASIL D readiness

## HSU Series

The main challenge that high-voltage battery experts are trying to solve is how to improve the battery autonomy while operating in the safest environment for the driver. How to translate this challenge at the sensor level?

The new HSU is the first hybrid sensor on the market. It combines two technologies, shunt + hall, in a standard shunt footprint. It offers gain on space, weight and cost and has been designed to minimize integration effort for a faster time-to-market while allowing ASIL D compliance at system level.

[www.lem.com](http://www.lem.com)



- **Non-heterogeneous redundancy**
- **Galvanic isolation on Hall part**
- **Separated communication lines (shunt signals and digital bus for Hall)**
- **NTC signal for shunt T°C compensation**
- **2 references sizes of standard shunts**

# LEM

Life Energy Motion



## Collaboration on high-voltage SiC Technology for Railway Systems

Mitsubishi Electric Europe B.V., Semiconductor Division, and Siemens Mobility GmbH, Business Unit Rolling Stock, are strengthening their collaboration on high-voltage silicon carbide (SiC) technology for railway traction applications with the signing of a long-term agreement. Building on the Memorandum of Understanding (MoU) signed in 2022 and leveraging their complementary strengths, both companies are advancing the development, qualification, and industrialization of SiC-based power modules to support more energy-efficient and high-performance railway drive systems. The collaboration provides a framework for ongoing technical exchange and the evalu-

ation of next generation SiC solutions for future railway platforms. High-voltage SiC technology has already demonstrated its capabilities in railway applications. Traction systems equipped with SiC-based modules are operating in regular passenger service in selected Siemens Mobility projects, contributing to improved efficiency, lower energy consumption, and reliable system performance under real-world conditions. Based on these operational experiences and a well-established, reliable supply relationship, Siemens Mobility and Mitsubishi Electric Europe B.V., Semiconductor Division, continue to explore the application of advanced SiC module technologies in up-



coming railway projects. Activities include the qualification of new module generations, optimization of system integration, and validation under demanding operating conditions typically required for high-capacity commuter and regional rail services.

[www.mitsubishielectric.com](http://www.mitsubishielectric.com)

## Partnership on Power MOSFET Manufacturing in the US

Polar Semiconductor, LLC and Nexperia B.V. announced a strategic collaboration to manufacture next generation power MOSFET devices at Polar Semiconductor's U.S. based wafer foundry. The partnership supports an expanded power MOSFET portfolio while strengthening supply for customers worldwide. By combining Polar's expertise in power semiconductor manufacturing and ongoing capacity expansion with Nexperia's power MOSFET technology, the collaboration addresses rapidly growing demand across AI server infrastructure, robotics, industrial, and automotive applications. Polar Semiconductor, a U.S.-based foundry with fully domestic manufacturing operations, runs a high volume wafer manufacturing facility in Minnesota. Polar is IATF 16949 certified. Under the collaboration, Nexperia is developing a portfolio of next generation power MOSFETs.

[www.nexperia.com](http://www.nexperia.com)



## PCIM Top Innovation 2026 Award

BeeMagnetics has won the PCIM Top Innovation 2026 award for its system-level approach to power electronics design. The company's main product, BeeMagnetics Engine, stands out as a next-generation design decision engine that brings together critical engineering steps before PCB layout and prototyping within a single framework. It brings together system-level design, topology evaluation, design

priority evaluation, magnetic design, EMI filter design, loss calculations, reports, BOMs, simulation-ready models, and manufacturable outputs in one unified structure. The platform enables system-level evaluation of different power electronics topologies, including LLC, Totem-Pole PFC, PSFB, Flyback, Non-isolated DC/DC, DAB, PFC, and Two Stage isolated DC/DC. With its planar and conventional magnetic design capabilities, BeeMagnetics Engine also provides transformer and inductor design outputs, winding strategy, loss calculations, FEM-based magnetic flux density analysis, and magnetic flux path visualization.

Unlike tools that only verify a predefined design, BeeMagnetics Engine focuses on creating stronger, more predictable, and manufacturable design outputs starting from system requirements. With up to 98% verified system-level accuracy, it aims to reduce early-stage design work from months to minutes.

This approach helps engineering teams make more mature design decisions before PCB layout and prototyping, while reducing unnecessary revisions, repeated prototypes, and technical risk. As a result, BeeMagnetics Engine contributes not only to faster and more optimized design processes, but also to more sustainable engineering practices.

[www.beemagnetics.com](http://www.beemagnetics.com)





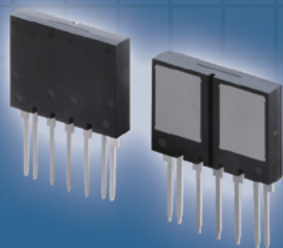
# Meeting your needs. Portfolio expansion. SiC Power Modules

**HSDIP20**



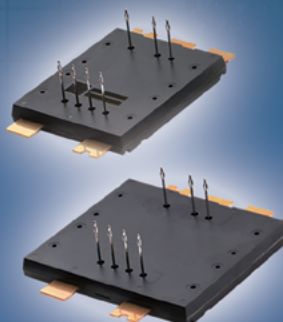
- Compact 4-in-1/6-in-1
- Circuit-oriented element layout (4-in-1, 2-in-1, etc.)
- Improved heat dissipation characteristics

**DOT-247**



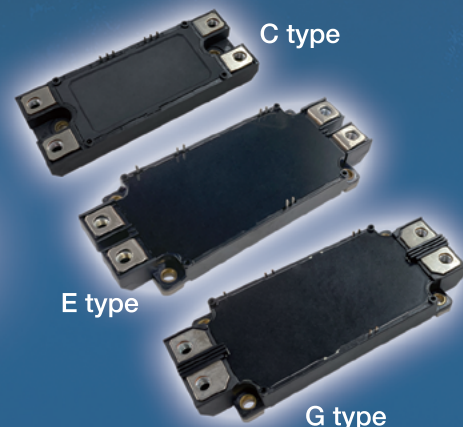
- 2-in-1 TO-247-4L
- Improved heat dissipation performance
- Half-bridge/source common

**TRCDRIVE pack™**



- Parallel multi-chip configuration provides high current capability
- Low Ls improves switching performance
- Reduced size through improved heat dissipation performance

**Case type**



- Parallel multi-chip configuration provides high current capability
- Gel encapsulation in case



TRCDRIVE pack™ and EcoSiC™ are trademarks or registered trademarks of ROHM Co., Ltd.



## APEC 2027: Call for Technical Sessions Digest Submissions

APEC 2027, to be held in New Orleans, Louisiana/USA, from March 7-11, 2027, is now accepting digest submissions for the Technical Sessions. Interested authors wishing to present a Technical Session paper must submit a digest for consideration by August 14, 2026. Instructions for submissions are available at: <https://apec-conf.org/speakers/ts-author-info/>. To facilitate higher-quality digest and final manuscript submissions, APEC 2027 offers significantly expanded submission windows for both. Topics of interest are divided into fourteen tracks, each with a diverse set of subtopics: AC/DC Converters, DC/DC Converters, DC/AC Inverters, Devices and Components, Magnetics, Power Electronics Integration and Manufacturing, Control, Modeling and Simulation, Motor Drives, Power Electronics for Utility Applications, Renewable Energy Systems, Transportation Power Electronics, Wireless Power Transfer, Power Electronics Applications. The Technical Sessions digest should explain the problem the paper addresses, its major results, and how it differs from the closest existing literature. Technical Session papers presented at APEC must be original material and not have been

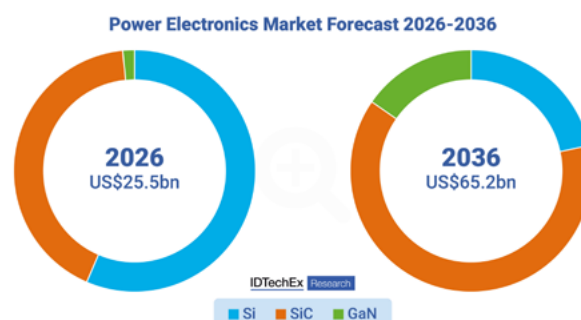


previously presented or published. The principal criterion used by reviewers in selecting digests for the program will be the usefulness of the work to the practicing power electronics professional. They also value evidence of completed experimental work. Authors will be notified of the decision of paper acceptance on October 12, 2026. Accepted papers final manuscript must be submitted and author registration completed by December 7, 2026.

[www.apec-conf.org](http://www.apec-conf.org)

## How 800V EV Innovations are Redefining AI Data Centers

According to IDTechEx forecasts in the market report "Power Electronics Market 2026-2036: Data Centers, Electric Vehicles, and Renewables", the power electronics market for data centers is expected to grow 2.5-fold by 2036. A paradigm shift in data center power architecture is coming over the next few years in the form of HVDC (800 V<sub>DC</sub>) data centers, which will unlock an order-of-magnitude increase in rack power. This overhaul in data center power architecture is directly influenced by 800 V EV power electronics, from the materials used to high-voltage safety and protection mechanisms. In its study IDTechEx tracks innovations across EV and data center power electronics, drawing deep, cross-application conclusions between EV and data center power electronics. Rack power levels have exploded from around 20 kW pre-ChatGPT to 100 kW today, with rack power expected to reach over 1 MW by the end of the decade. With incumbent Si power electronics and 480/54 V data center architecture, a 1 MW rack would require the whole rack space to be dedicated to power conversion and would need over 200 kg of copper. Data center efficiency was and still is a key consideration in data center design. Data center power density, the amount of power processed per unit volume, will become an increasingly



critical metric for AI data center design. GaN will likely enjoy faster uptake in data centers than in electric vehicles. Reference designs for 8 kW and 12 kW power supply units (PSUs) across leading power electronics players, such as Infineon and Navitas, feature SiC for high-voltage conversion stages and power factor correction (PFC), and GaN for low-voltage conversion stages.

[www.IDTechEx.com](http://www.IDTechEx.com)

## Swiss Company acquires Chinese Developer of high-voltage Circuit Protection Solutions

SCHURTER has completed its acquisition of Biaodi, a China-based developer of high-voltage circuit protection solutions for electric vehicles and new energy applications. Biaodi's product portfolio significantly expands SCHURTER's high-voltage offering and includes fuses for EV onboard mobility applications, pyrotechnic (pyro) fuses for safe disconnection in electric vehicle applications as well as AC fuses for charging stations, energy storage systems, data centers, wind power and other high-current applications.

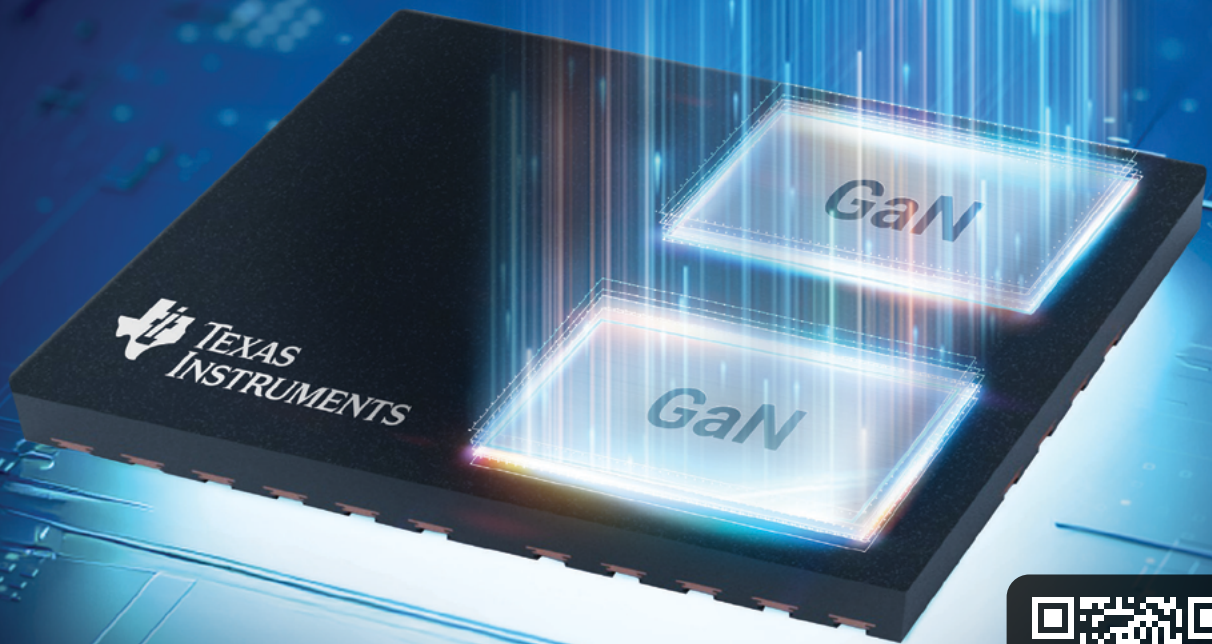
[www.schurter.com](http://www.schurter.com)





# Innovation powered by GaN

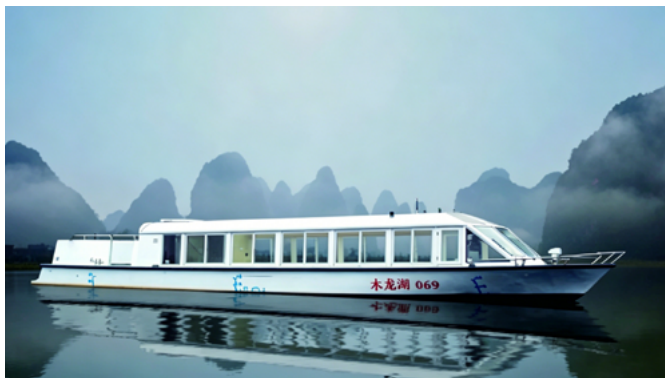
Discover how the industry's  
first buck and boost converters  
with integrated GaN FETs achieve  
best-in-class efficiency in up to a  
50% smaller footprint.





## All Battery New Energy Vessel in China

Dukosi announces the launch of China's first all-battery new energy vessel equipped with the Dukosi Cell Monitoring System (DKCMS®).



The all-battery vessel features a contactless battery management system (BMS) developed by Guangxi Yichuan Intelligent Technology ("Yichuan") powered by lithium-ion battery cells supplied by Eikto New Energy. The adoption of battery power of China's rivers and inland waterways is primarily driven by national "Dual Carbon" goals and the aspiration to reduce pollution. With over 127,000 km of navigable rivers and canals, China operates the world's largest business inland waterway system. Eikto has developed DKCMS-based battery management system (BMS) for marine applications that meet stringent safety standards required for type approval certification. The flexibility and scalability of the DKCMS contactless architecture allows Yichuan to cost-efficiently develop and validate class-leading battery systems for a wide range of vessels and power demands and accelerate their time to market.

[www.dukosi.com](http://www.dukosi.com)

## EU flagship Project Moore4Power to drive the next Generation of sustainable Power Electronics

Europe has launched an ambitious semiconductor R&D project involving 62 partners: Moore4Power (More than Moore for Disruptive Innovations in Power Electronics). Led by Infineon Technologies this chips joint undertaking initiative unites large entities, small and medium-sized enterprises and research institutes from 15 European countries to develop the next generation of smart, efficient and sustainable power electronics. With a total project volume of € 91 million, Moore4Power will run for three years aiming to deliver breakthrough innovations that strengthen Europe's technological sovereignty and sustainability in the field of power electronics. For decades, progress in electronics followed Moore's Law: smaller transistors, delivering higher performance at lower cost. Today, traditional scaling is reaching physical and economic limits. Moore4Power addresses this challenge by shifting the focus from individual components to system-level innovation. Combining technologies, materials, and functions in smarter, application-driven ways, the initiative unlocks major gains in efficiency, reliability and power density. At the core of Moore4Power is heterogeneous integration, which combines different semiconductor technologies such as silicon (Si), silicon carbide (SiC) and gallium nitride (GaN), together with sensing, control and communication functions to form tightly integrated systems. Each technology is used exactly where it performs best, enabling higher efficiency, improved reliability and more compact designs. Power chiplet technology enables scalable



architectures and more flexible product variants at globally competitive cost levels. Moore4Power focuses on high-impact sectors where power conversion drives cost, CO<sub>2</sub> reduction and reliability. One central achievement is the Digital Product Passport (DPP), embedded directly into power modules via wireless access. The DPP will provide lifecycle data such as operating conditions, state of health and remaining lifetime throughout the product's use.

[www.infineon.com](http://www.infineon.com)

## Distribution Agreement for GaN Devices

**EPC and Mouser**  
Announce Global  
Distribution Partnership

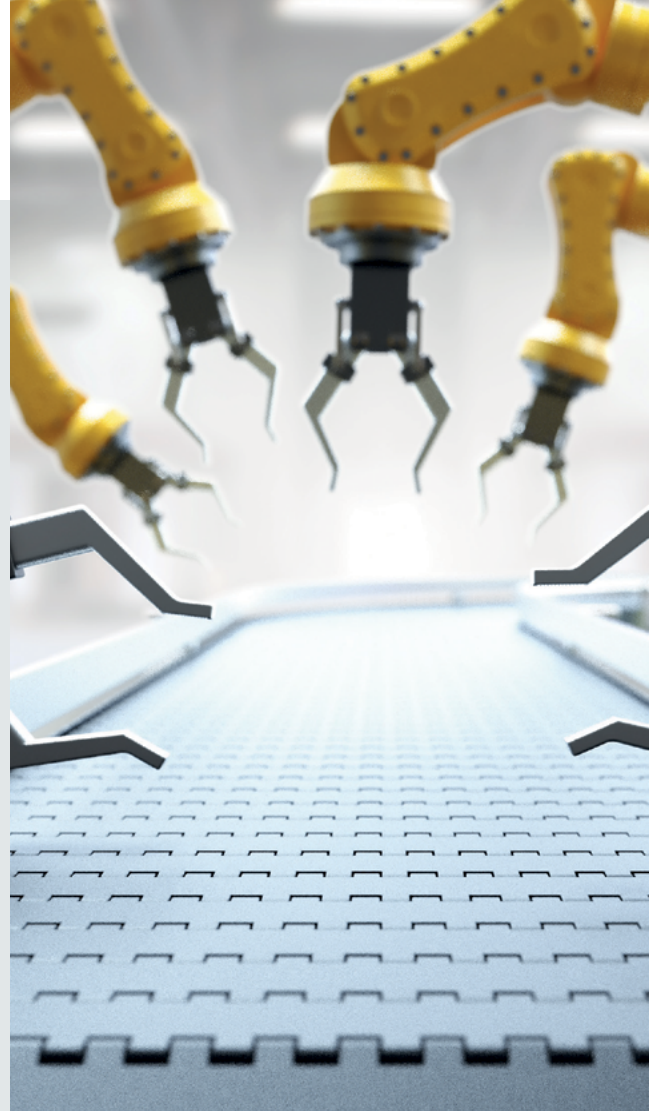
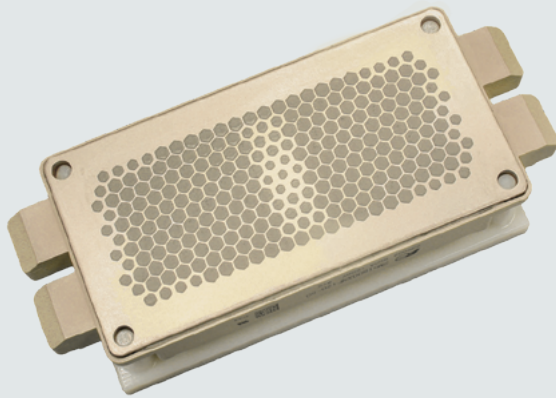


Efficient Power Conversion (EPC) announced a global distribution agreement with Mouser Electronics. This partnership will see Mouser Electronics distribute EPC's complete portfolio of eGaN® FETs and ICs. This agreement will give Mouser's customers the opportunity to use the latest EPC GaN technology devices in their designs, enabling the development of smaller, faster, and more efficient power conversion systems across a broad range of applications, including power converters, motor drives for eMobility, robotics and drones.

[www.epc-co.com](http://www.epc-co.com)



# Industrialized process for pre-pasted Thermal Interface Material (TIM)



## MAIN FEATURES

- Optimized for Fuji modules
- Increased lifetime of IGBT
- Advanced IGBT power density
- Thermal – Benefits
  - Higher thermal conductivity
  - Uniform thermal resistance
  - Increased reliability and lifetime
- Process – Benefits
  - Outsourcing of a “dirty” process
  - Stable quality level
  - Computer controlled automated process
  - Increased System reliability

UPS



MV-INV



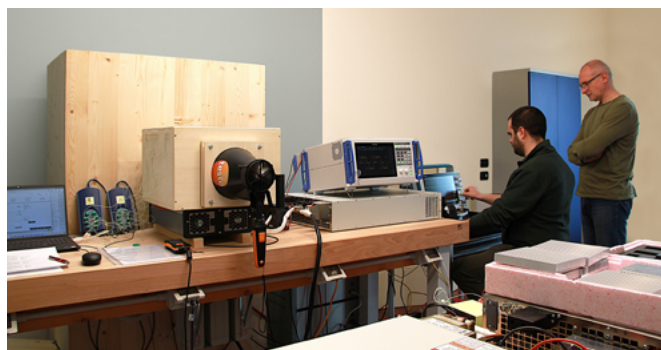
SERVO





## A Calorimetric Chamber as a Key in Developing HF Power Transformers

The power electronics market demands technologically advanced components, with particular attention to energy efficiency, thermal management, and industry quality standards. Transformers, of course, are no exception: for this reason, Sirio Elettronica (Italy) has established a new research department for high-frequency power transformers, equipped with a brand-new laboratory. The heart of the experimental setup is a full-bridge converter, which powers the transformers under test. Other instrumentation includes power supplies and active loads up to 15 kW, a broadband oscilloscope, and a multichannel power analyser. Noteworthy is the use of a calorimetric chamber to evaluate thermal performance and power dissipation for efficiency analysis. Prototypes can now be electrically and thermally tested while actually operating at full load under nominal conditions. Theoretical efficiency and actual dissipation can be compared, launching an ultimate phase of design that goes far beyond the limits of calculation, and making a step further from validation by simulation. Internal temperatures are also accurately recorded.



Sirio is currently developing a new series of planar transformers, with the laboratory playing a key role in this effort. By adapting prototype construction with support from the calorimeter, an efficiency close to 99% has been achieved.

[www.sirio-ic.com](http://www.sirio-ic.com)

## Teaming up to establish U.S. Gallium Supply Chain

Indium Corporation® and Ames National Laboratory have announced a research and development partnership to expand U.S. production of gallium. The alliance will focus on developing the technologies needed to establish a domestic supply chain for an element that currently relies almost exclusively on imported sources.



In the U.S., gallium is recovered as a byproduct of well-established, high-volume aluminum refining operations. Called the Bayer process, this method uses caustic liquids and high temperatures to extract and refine aluminum from raw ore. Gallium is typically present in the refining process waste in low concentrations of about 100 parts per million. Liquid-based refining methods typically use specialized polymers (resins), that can separate and concentrate metals from mining solutions. For this project, Ames Lab researchers are designing a heat-stable, efficient resin that is selective for gallium. Ames Lab's robotic lab capabilities can generate high-quality data quickly. When paired with AI tools, the data can be rapidly analyzed to uncover patterns, optimize processes, and guide the iterative design of materials. These accelerated workflows can shrink the development timeline from decades to as little as two to three years. Scaling the technology is a joint effort, which will be done through a Cooperative Research and Development Agreement (CRADA): Indium Corporation will provide a U.S. resin testbed that mirrors high-volume production and techno-economic models to define the required material properties, and Ames Lab will synthesize materials up to the hundreds-of-grams scale. Future scale-up to kilograms and tons will continue collaboratively.

[www.indium.com](http://www.indium.com)

## Acquisition of Power Semiconductor Company

Analog Devices, and Empower Semiconductor announced that they have entered into a definitive agreement under which ADI will acquire Empower in an all-cash transaction for \$1.5 billion. As AI compute scales, power density – not just total watts – has become the limiting factor. Delivering high-density, high-efficiency power at the point of compute, while responding to fast-changing demands, is now one of the most critical challenges in system design. Together, ADI and Empower intend to help shape the power delivery architecture for AI and other compute-intensive applications. By enabling power conversion closer to the processor, the combined solution shortens the power delivery path and improves efficiency to support higher-performance, higher-density systems. Building on its know-how in power management, ADI is investing in its system-level platform to deliver a step-change in performance, density, and



efficiency from grid to core. The transaction is expected to close in the second half of calendar year 2026.

[www.analog.com](http://www.analog.com)

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# Low Voltage GaN Surpasses MOSFETs in AI Power Density

*Artificial Intelligence (AI) workloads are reshaping computing server power delivery requirements. Low-voltage GaN is emerging as a key enabler of higher efficiency and greater power density than silicon MOSFETs in next-generation AI infrastructure.*

*By Alex Lidow, CEO, Alejandro Pozo, Director of Applications Engineering, and Michael De Rooij, GaN Applications Fellow, Efficient Power Conversion (EPC)*

Artificial intelligence is integrating into our professional and personal lives at an unprecedented pace. By streamlining software development, tackling complex analytical challenges, and automating routine documentation, AI is no longer just a tool, it's a fundamental shift in how we create and solve.

These new-generation AI servers come at a cost based in large part on an exponentially increasing demand for power. The center of this power consumption is the Graphics Processing Unit (GPU) made from billions of microscopic transistors compacted on a silicon substrate with features as small as 20 Å (That's approximately the width of the DNA molecule's double helix). The power required to activate these billions of processing agents is going up as fast as their computation capabilities. Table 1 shows an example that uses Nvidia's published roadmap through 2028.

| Architecture | Year | Typical GPU TDP   | Cooling Method       |
|--------------|------|-------------------|----------------------|
| Blackwell    | 2024 | 1,000 W – 1,400 W | Air / Liquid         |
| Rubin        | 2026 | 2,300 W – 3,600 W | Liquid (Mandatory)   |
| Feynman      | 2028 | 4,400 W – 6,000 W | Immersion / Embedded |

Table 1: Power Requirements for AI GPUs [1,2].

The NVIDIA Vera Rubin architecture typically features two Rubin GPUs on a single server board. These are paired with one Vera CPU to form what is known as the Vera Rubin Superchip. Each board requires as much as 12 kW delivered to all the various elements in addition to the Superchip. A standard NVIDIA Vera Rubin NVL72 server rack typically contains 18 server boards for a total requirement of 216 kW per rack.

By the time Feynman is released, that number at least doubles, with a 1 MW rack not too far in the future.

## Delivering the Power within the rack

Distributing 216 kW within a rack is not easy. Today the rack is provided with 3-phase 415 V<sub>AC</sub>, delivered with a neutral so that individual power supplies within the rack can be powered from 240 V<sub>AC</sub> each. Internally each power supply converts the 240 V<sub>AC</sub> to 400 V<sub>DC</sub>, and then further to 48 V<sub>DC</sub> while providing safety isolation. All this resides in power trays co-located inside the data server rack. The 48 V<sub>DC</sub> is then distributed to each server tray where the electrons proceed to be processed down to less than 1 V<sub>DC</sub>. The Blackwell-generation server board requires up to 3 kW. That is 62.5 A going to the server board from the power supply in the rack. However, for a Rubin system at 12 kW, that current increases to 250 A, which is quite difficult to handle through commonly available connectors and bussing. Now triple that number for the Feynman generation and the amount of current becomes impractical to deliver through the connectors to the board.

The inevitable solution involves higher voltages delivered to the server board and distribution within the rack. The prevailing thought is this new voltage will be either 800 V, or +/- 400 V. In either case, the current flowing to the board is reduced to 15 A for a typical Vera Rubin server board.

Three different power delivery architectures are shown in figure 1. The distribution voltage of either +/- 400 V or 800 V comes from a separate designated power rack called a "sidecar". In the lower two cases, the high voltage is bussed to the server board directly where it is converted to either 6 V<sub>DC</sub> or 12 V<sub>DC</sub>. Both voltages are planned by different server manufacturers. The last case shown at the top of figure 1 maintains the more traditional configuration where the 800 V is converted to 48 V<sub>DC</sub>. There are two scenarios for this approach where the first maintains the traditional power shelf with 48 V distribution taking advantage of the higher power density of the power supply but would require much thicker power bussing throughout the rack. The second approach uses a compact 800 V to 48 V converter locally at each server board but those occupy precious area needed for the processor. Overall, these 48 V approaches maintain utilization of traditional hardware on the server board thus easing transition to higher power levels as the server rack design evolves.

The server board is considered precious real estate, and therefore the power delivery needs to take up as little space as possible while maintaining extreme conversion efficiency. Any power converter on the server card would need not only occupy the least amount of space but would have to be extremely thin to accommodate the tight board-to-board spacing as well as the aggressive thermal management systems (see table 1) that would be deployed throughout the board.

One solution that demonstrates the highest efficiency, highest power density, and thinnest form factor is the ISOP converter (Inputs in Series, Outputs in Parallel) [3,4]. The basic ISOP configuration, shown in figure 2, uses low voltage devices in a stacked series of LLC converters with their outputs connected in parallel. An ISOP operating from 800 V can be realized using 8 modules configured with 150 V rated GaN FETs [5], instead of 650 V rated devices as would be used in a two-stage converter. Lower voltage devices yield much lower conduction losses and have a higher effective operating duty cycle thus reducing ripple current losses compared to higher voltage counterparts. In addition, the higher number of stages allows for better thermal distribution and lower output ripple current when the LLC module operation is interleaved. There are also EMI benefits to using a higher number of modules in the ISOP configuration due to the reduced voltage of the high dv/dt transitions as shown in figure 3.

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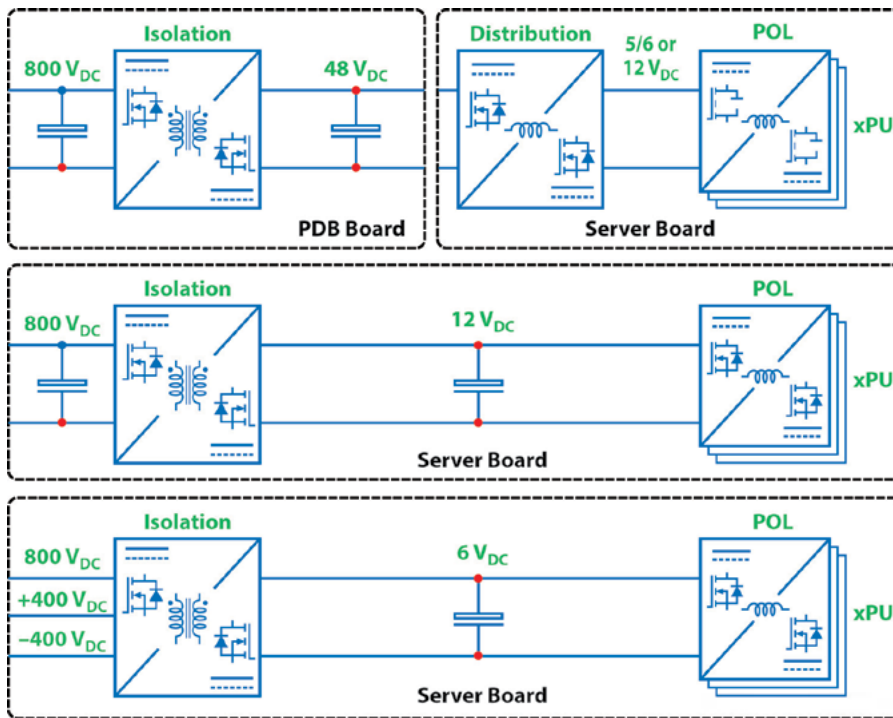


Figure 1: Three different power delivery architectures under consideration for the next generations of AI servers.

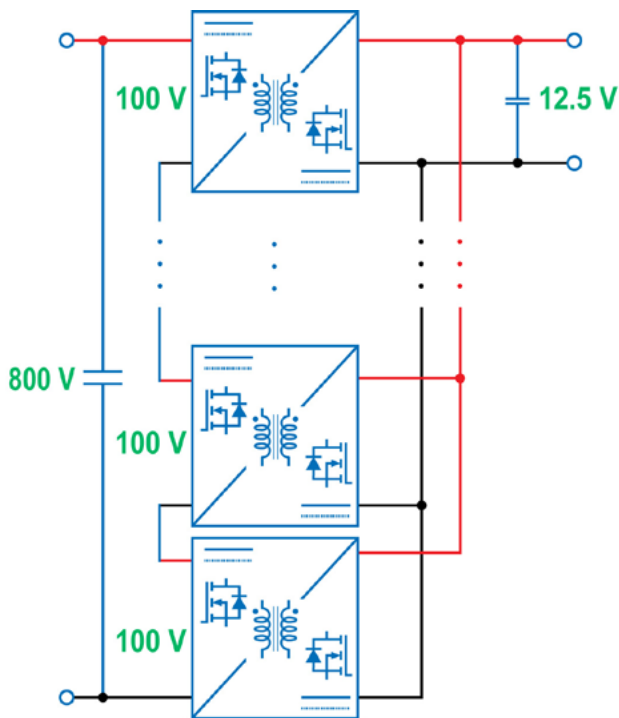


Figure 2: The basic ISOP concept is to use low voltage devices in a stacked series of LLC converters with their outputs connected in parallel.

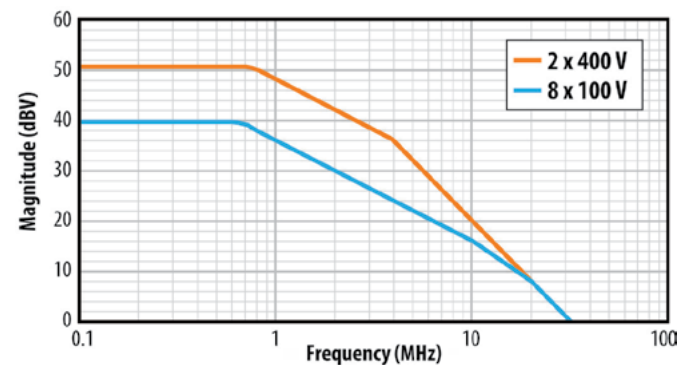


Figure 3: Difference in E-field generation between a two-stage ISOP with 400 V bus and eight-stage ISOP with 100 V bus for a system operating from 800 V and switching at 1 MHz

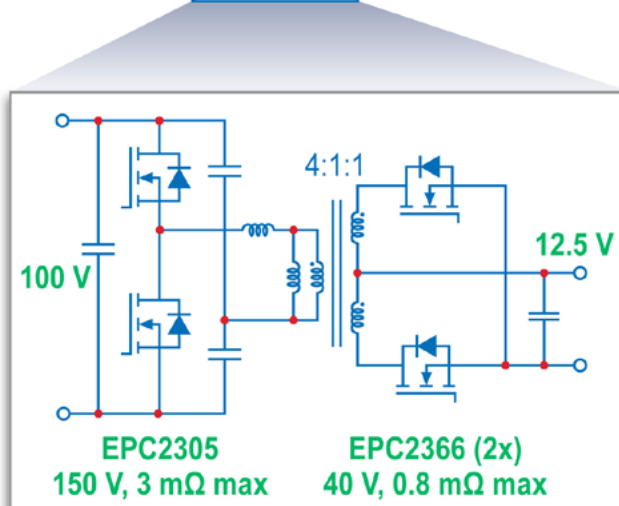
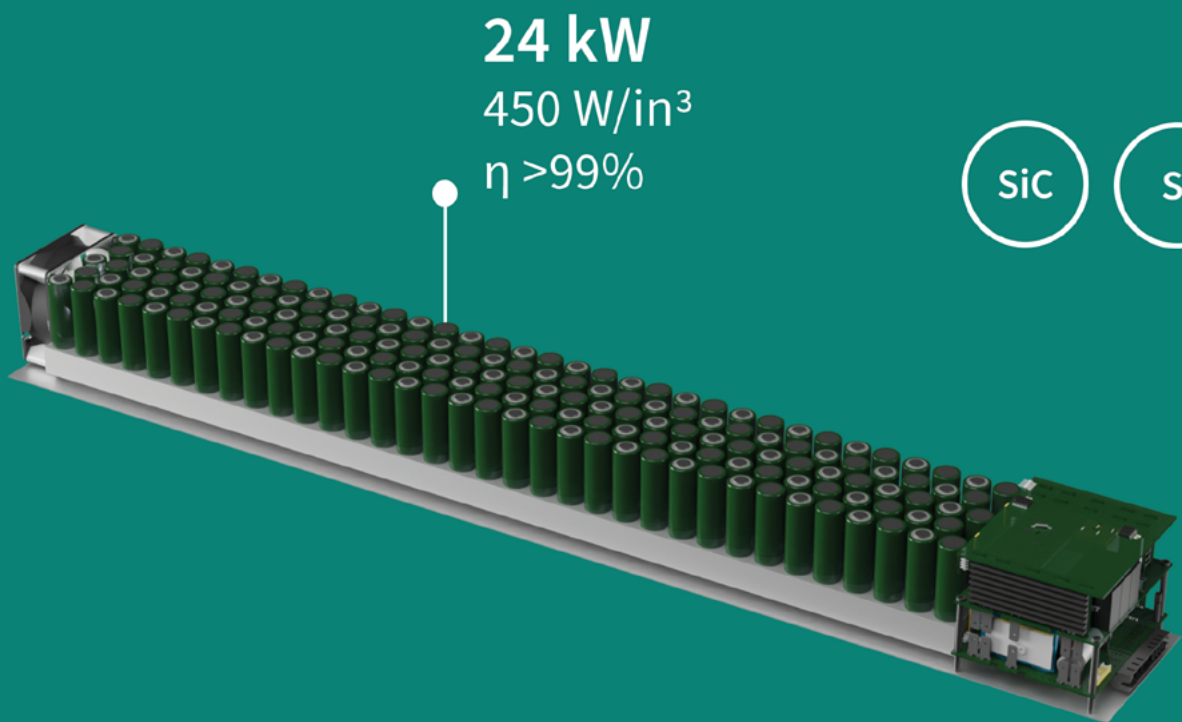


Figure 4 is an example of a 6 kW ISOP converter that has an input voltage of 800 V<sub>DC</sub> and an unregulated output voltage of 12.5 V<sub>DC</sub>. The conversion efficiency at full load is 97%, and the entire converter occupies less than 5,000 mm<sup>2</sup> with a thickness of just 8 mm. A similar ISOP approach can yield a thin, small and efficient 800 V<sub>DC</sub> to 6 V<sub>DC</sub> on-board converter.

The choice between distributing the voltage on the server board at 12 V or 6 V is a challenging trade off between distribution losses and conversion losses. At 12 V the losses on the server board are four times less for the same amount of copper routing. A 6 V bus can be more easily and efficiently converted using a single stage to sub-one-volt level, especially considering the newest generation GaN transistors made for lower voltage conversion, but the higher losses throughout the server board may compensate.



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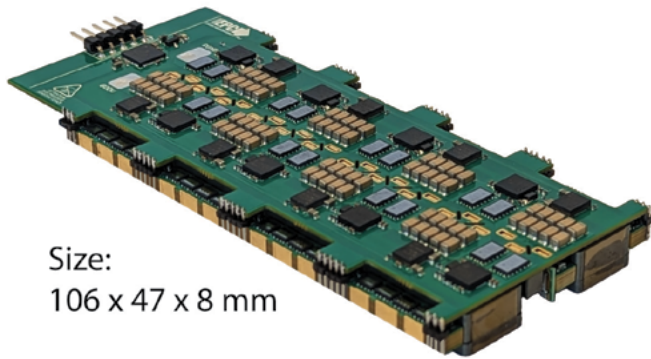


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## EPC91123: 800–12.5 V, 6 kW, End-to-End GaN



Size:  
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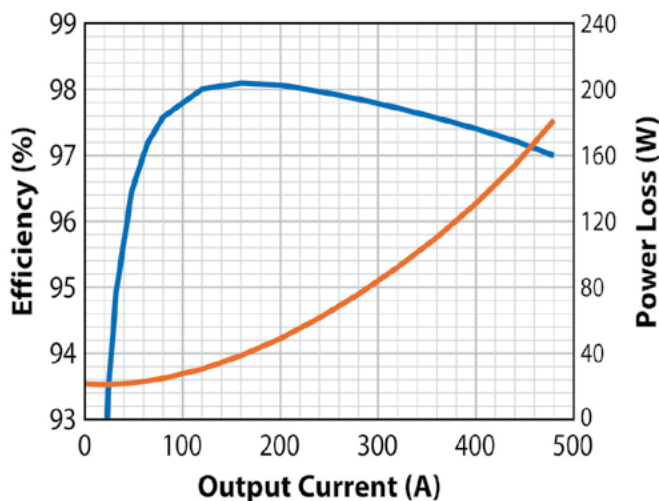


Figure 4: The EPC91123 is an 800 V<sub>DC</sub> – 12.5 V<sub>DC</sub> 6 kW, eight-stage ISOP DCDC converter that is only 8 mm thick and is designed to be mounted directly on the server board. This converter has a peak efficiency of 98.3% and a full-load efficiency of 97%.

| 150 V          | R <sub>DS(on)</sub><br>(mΩ) | Q <sub>G</sub><br>(nC) | Q <sub>OSS</sub><br>(nC) | Package             | Applications                                          |
|----------------|-----------------------------|------------------------|--------------------------|---------------------|-------------------------------------------------------|
| EPC2376        | 1.4                         | 18.4                   | 110                      | 3 x 5 dual cool     | 800 V/48 V,<br>400 V/48 V,<br>LLC, BBU, DC-DC         |
| Best Silicon*  | 10                          | 28                     | 78                       | 5 x 6 dual cool     |                                                       |
| 100 V          | R <sub>DS(on)</sub><br>(mΩ) | Q <sub>G</sub><br>(nC) | Q <sub>OSS</sub><br>(nC) | Package             | Applications                                          |
| EPC2367        | 1.2                         | 17                     | 54                       | 3.3 x 3.3 dual cool | 800 V/48 V,<br>400 V/48 V,<br>BBU, DC-DC, POL         |
| Best Silicon*  | 6.5                         | 27                     | 40                       | 3.3 x 3.3 dual cool |                                                       |
| 40 V           | R <sub>DS(on)</sub><br>(mΩ) | Q <sub>G</sub><br>(nC) | Q <sub>OSS</sub><br>(nC) | Package             | Applications                                          |
| EPC2377        | 0.5                         | 26                     | 34                       | 3.3 x 3.3 dual cool | 800 V/12 V,<br>400 V/6 V,<br>48 V/12 V,<br>DC-DC, POL |
| EPC2366        | 0.84                        | 15                     | 22                       | 3 x 2.6 dual cool   |                                                       |
| Best Silicon** | 1                           | 20                     | 43                       | 3.3 x 3.3 dual cool |                                                       |
| 25 V           | R <sub>DS(on)</sub><br>(mΩ) | Q <sub>G</sub><br>(nC) | Q <sub>OSS</sub><br>(nC) | Package             | Applications                                          |
| EPC2378        | 0.41                        | 34                     | 26                       | 3.3 x 3.3 dual cool | 800 V/6 V,<br>400 V/6 V,<br>48 V/6 V,<br>DC-DC, POL   |
| Best Silicon** | 0.47                        | 32                     | 52                       | 3.3 x 3.3 dual cool |                                                       |
| 18 V           | R <sub>DS(on)</sub><br>(mΩ) | Q <sub>G</sub><br>(nC) | Q <sub>OSS</sub><br>(nC) | Package             | Applications                                          |
| EPC2370        | 0.28                        | 26                     | 17                       | 3.3 x 3.3 dual cool |                                                       |

\*Silicon measured at 8 V<sub>GS</sub>

\*\*Silicon measured at 5 V<sub>GS</sub>

Table 2: The latest generation GaN transistors have lower R<sub>DS(on)</sub> and better switching characteristics than the best-in-class (BiC) silicon MOSFETs.

### Unseating the Aging MOSFET in AI Servers:

Power MOSFETs have been an essential component in power conversion for almost 50 years, while GaN transistors have been in mass production for over 16 years [6]. GaN devices hold the promise of being far smaller and more efficient than silicon MOSFETs, yet, until recently, that promise has only been a reality for devices with voltage ratings between 100 V and 650 V. Recent advances in GaN technology made by Efficient Power Conversion, have resulted in a whole new generation of GaN transistors that outperform silicon MOSFETs in size, efficiency, and speed for voltage ratings all the way down to 15 V and less. Table 2 is the evidence. In this table benchmark GaN devices are shown from 150 V down to 15 V compared with the benchmark MOSFET in the same, or in some cases larger footprint packages.

For applications such as the power-hungry and space-sensitive AI server, there can be no reason to choose an aging silicon MOSFET over the latest-generation GaN devices. In addition, GaN is still a relatively young technology and there are many improvements coming in the next few years that will only make the GaN-silicon gap even wider.

### Conclusions

This article presented the shift in server power architectures brought about by artificial intelligence and explained how GaN FETs provide the solutions to meeting the ever-increasing power density demands. A 6 kW 800 V to 12.5 V input series output parallel converter using low voltage GaN FETs yield power densities exceeding 1.2 W/mm<sup>2</sup> and full load efficiency of 97% was given as an example of GaN FET capability. Newer low voltage devices with extremely low on-resistance and gate charge further further open the door for GaN FETs becoming the new device of choice in point of load conversion.

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# Designing MOSFETs for the real Load Profile of Battery-Powered Motor Drive Applications

## OptiMOS™ 7 40 V: Motor-Drive Optimization beyond low $R_{DS(on)}$

*Imagine having to drill in a couple of screws to put up a painting on a wall. You place the bit into the screw head, press the trigger, and expect the cordless screwdriver to respond instantly.*

*The motor does not get a gentle request. It receives a sudden demand for torque, current, and control. In a fraction of a second, the battery, inverter, gate driver, controller, and power MOSFETs must convert stored energy into mechanical force while keeping heat, voltage overshoot, and electrical stress within safe limits.*

*By Gregor Gruber, Senior Manager, Product Marketing;  
and Dingyi He, Senior Staff Engineer, Infineon Technologies*

For you as the user, the result should feel simple: fast start-up, strong torque, long runtime, and a tool that remains dependable over its lifetime. For the developer, the same moment is a dense engineering problem. A compact power stage must deliver a high peak current, withstand harsh switching transients, support efficient brushless DC (BLDC) motor control, and remain thermally manageable inside a space-constrained enclosure.

That is the design context behind [OptiMOS™ 7 40 V motor-drives optimized power MOSFETs](#). The family is engineered not only for low drain-source on-state resistance ( $R_{DS(on)}$ ), but for the broader stress profile of battery-powered motor drives, including power tools and gardening tools. The portfolio targets 40 V motor-drive systems and is available in package options including SuperSO8 5x6, PQFN 3.3 × 3.3, and SuperSO8 5x6 dual-side-cooled variants.

### Motor-drive optimization starts where the load is most demanding

In a battery-powered tool, the inverter typically drives a BLDC motor from an 18 V to 24 V-class battery system using 40 V MOSFETs. The MOSFETs must handle high current during acceleration, torque peaks, and stall-like conditions, while switching fast enough to maintain control. Field-oriented control (FOC) and block commutation both place strong demands on current sensing, feedback speed, gate-drive behavior, and MOSFET selection.

A lower  $R_{DS(on)}$  directly reduces conduction loss. In practical terms, this gives the product developer more thermal margin for a given current, or the possibility to increase current capability without increasing the size of the power stage. For the end user,

that margin can translate into a longer battery runtime, more consistent torque delivery, or a tool that stays within safe temperature limits during demanding tasks. OptiMOS™ 7 40 V motor-drives optimized reaches an  $R_{DS(on)-max}$  value as low as 0.54 mΩ in the SuperSO8 5x6 device, which is an improvement of more than 20% over comparable OptiMOS™ 6 devices.

But motor-drive behavior is not determined by  $R_{DS(on)}$  alone. Switching loss, gate controllability, safe operating area (SOA), immunity against parasitic turn-on, and thermal paths through the package all influence whether a design performs well in the real tool. OptiMOS™ 7 motor-drives optimized introduces a device architecture specifically tuned for motor-drive conditions, representing the latest generation of Infineon's 40 V power MOSFET technology.

### Robustness where motor drives are the toughest to control

Consider the instant when a tool bit bites into material and the motor slows sharply. Current rises, the inverter operates under higher stress, and the MOSFETs must re-

main inside their safe operating limits. This is where SOA becomes a practical design parameter rather than a chart in the data-sheet. A wider SOA allows higher current capability across voltage and pulse-duration conditions, improving ruggedness during low-speed, high-torque operation, and locked-rotor scenarios. OptiMOS™ 7 motor-drives optimized improves SOA by up to 3× compared with a similar OptiMOS™ 6 40 V device.

Parasitic turn-on is another motor-drive-specific challenge. During high-side switching, the fast-rising drain-source voltage of the low-side MOSFET can couple current through the gate-drain capacitance, inducing gate-source voltage. If the induced gate voltage crosses the threshold, the low-side MOSFET may partially turn on when it should remain off. OptiMOS™ 7 motor-drives optimized improves immunity through a higher minimum gate threshold voltage of 2.4 V versus OptiMOS™ 6, supported by optimized gate behavior for motor-drive switching.

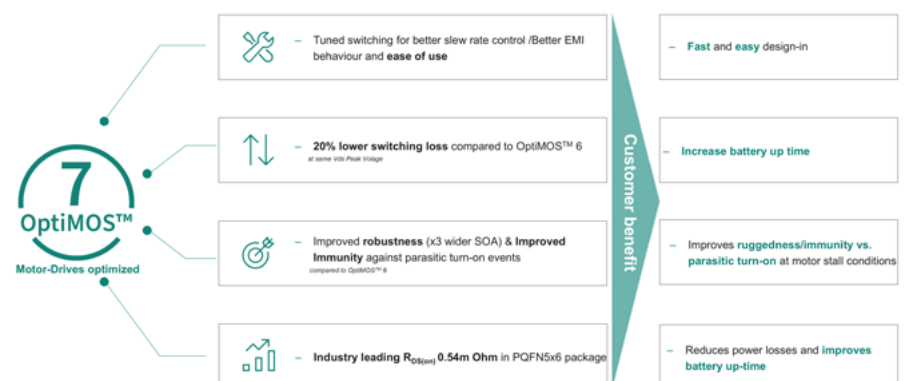


Figure 1: Technology improvement of OptiMOS™ 7 motor-drive-optimized MOSFETs



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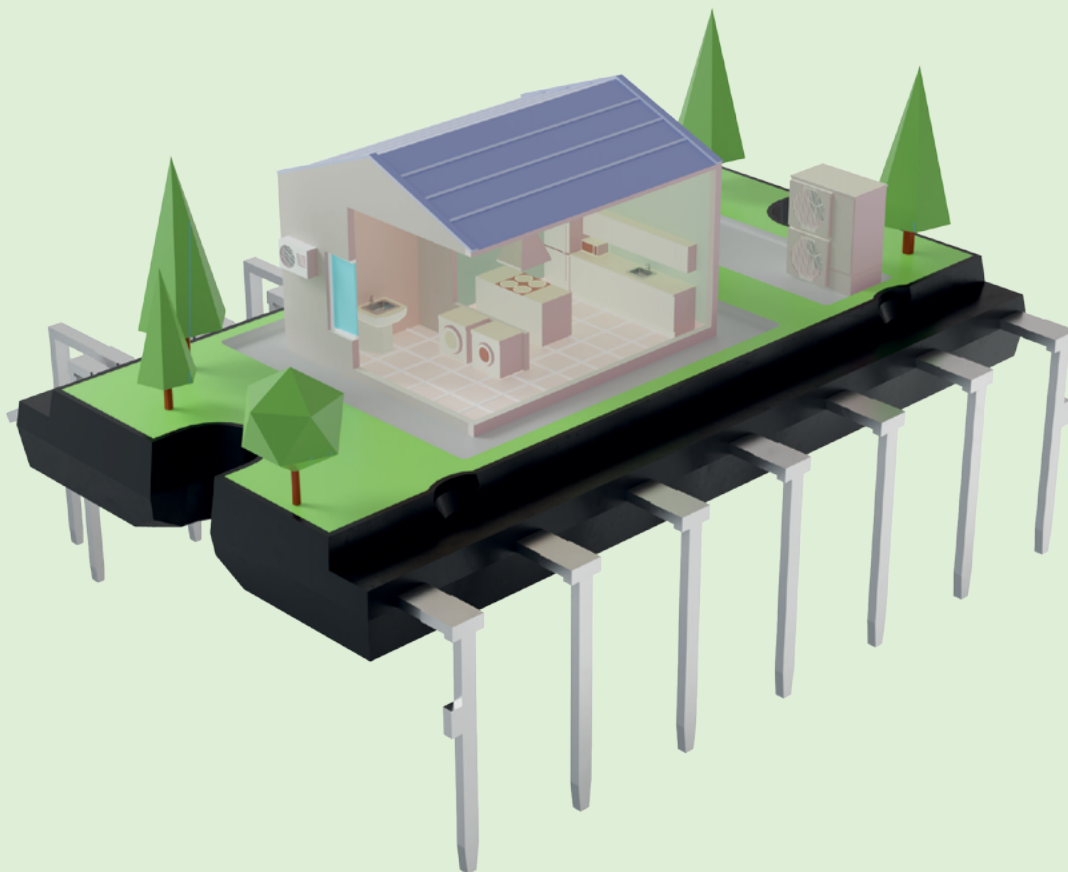
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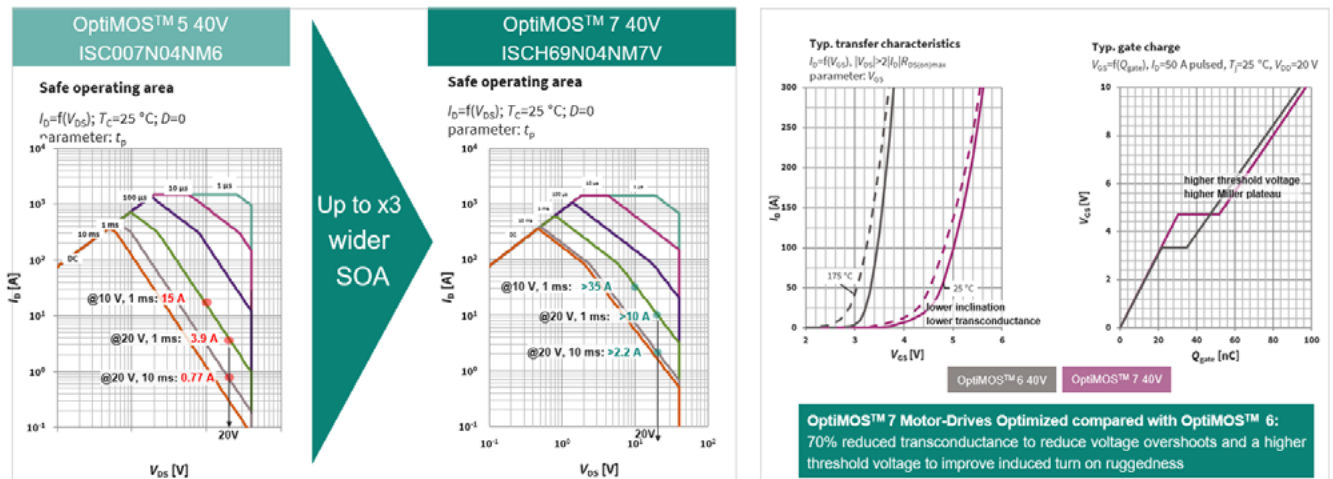


Figure 2: Up to 3x wider SOA in the latest generation

For developers, this helps reduce the burden of overconservative gate-resistor choices and layout compromises. For users, it supports the invisible quality they expect from a premium tool: stable operation under abrupt load changes, lower electrical stress during demanding torque events, and reliable behavior when the motor is pushed hard.

#### Tuned switching supports cooler, denser power stages

Switching behavior is often a balancing act. Slower switching can reduce overshoot and EMI, but it increases switching loss. Faster switching can reduce loss, but may create voltage stress or EMI challenges. For motor-drive inverters, the right answer is tuned switching: enough speed to improve efficiency, enough control to keep the design robust.

OptiMOS™ 7 motor-drives optimized addresses this balance through gate and switching characteristics tuned for motor-drive operation. The behavior has been validated using double-pulse testing, with the turn-off voltage peak controlled to 32 V and turn-on  $dV/dt$  controlled to 100 V/ $\mu\text{s}$ . Under these conditions, OptiMOS™ 7 ISC011N04NM7V achieved 100.4  $\mu\text{J}$  switching loss. A comparable OptiMOS™ 6 device with the part number ISC010N04NM6 reached 128.7  $\mu\text{J}$  under the same evaluation approach, while other comparable 40 V MOSFETs available in the market for the same application class measured 159.3  $\mu\text{J}$ , 190.1  $\mu\text{J}$ , and 251.3  $\mu\text{J}$ .

For a developer, these few degrees can decide whether a compact design passes the thermal budget without a larger heatsink, airflow change, or enclosure redesign. For the end user, it can mean more sustained performance during repeated drilling, fastening, or cutting operations.

#### Thermal paths turn device performance into system performance

Power density is not achieved by silicon alone. The thermal path out of the MOSFET package strongly affects how much current the inverter can sustain in a compact tool. OptiMOS™ 7 motor-drives optimized includes dual-side-cooled package options, allowing heat to be extracted through both the bottom and top side of the package. Typical thermal resistance values show the advantage: SuperSO8 dual-side-cooled 5x6 has typical  $R_{thJC}$  (top) of 0.7 K/W and  $R_{thJC}$  (bottom) of 1 K/W, compared with 15 K/W top-side and 1 K/W bottom-side values for bottom-side-cooled SuperSO8 5x6.

The [REF\\_18VDC\\_MTRC\\_motor-drive\\_inverter\\_reference\\_board](#) shows how these device characteristics translate into a compact application design. The board integrates OptiMOS 7 40 V motor-drive-optimized MOSFETs, the MOTIX™ 6EDL7141 3-phase smart gate driver, and an XMC1402 microcontroller. It operates from 14 V to 22 V, targets 18 V battery-powered tools, and supports sensor-based block commutation control.

The board is rated for 500 W over 10 minutes and 820 W peak power for 10 seconds. At rated power, it reaches a maximum efficiency of 96.6% under the stated 18 V, 25°C, and 20 kHz conditions. In the 500 W thermal test, the compact power-stage area measured 315 mm<sup>2</sup>, supported by a small 35 mm × 14 mm × 12 mm heatsink.

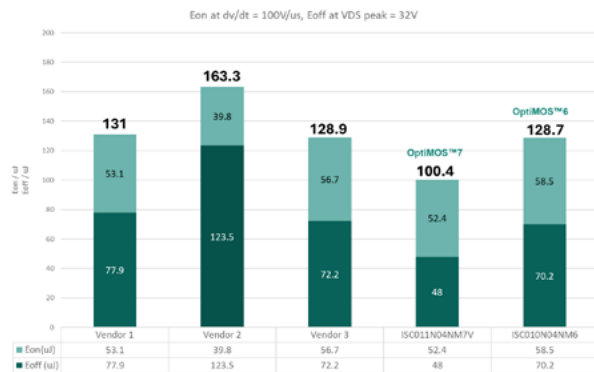


Figure 3: Double-pulse test results, energy losses at  $V_{DS}$  peak (turn-off) = 32 V and  $V_{DS}$   $dv/dt = 100\text{ V}/\mu\text{s}$

At the system level, these microjoules translate into temperature, heatsink size, enclosure constraints, and runtime. In a 3-phase motor-drive test at 20 V input, 20 kHz switching frequency, 2500 rpm, and 600 W input power, the highest case temperature reached by ISCH54N04NM7V was 85.4°C after 12 minutes. That was 4.6°C lower than the comparable OptiMOS 6 device under the same test conditions.

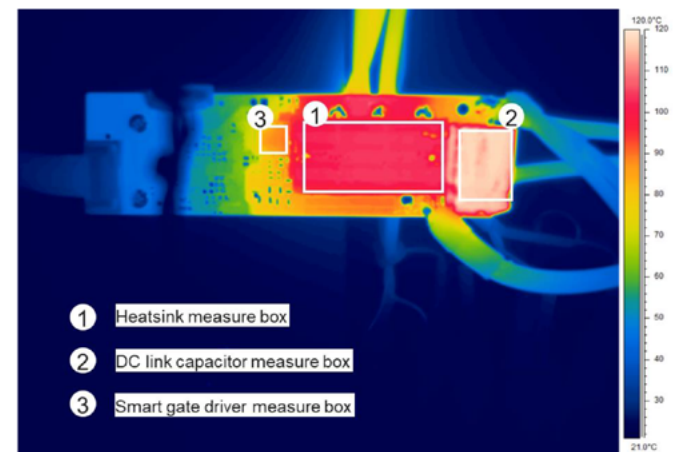


Figure 4: Thermal measurements of REF\_18VDC\_MTRC, which uses OptiMOS™ 7 motor-drive-optimized MOSFETs in the 5 x 6 SuperSO8 over molded and DSC package (PQFN)

For a tool manufacturer, this type of reference design shortens the path from component selection to system validation. It shows how MOSFET behavior, gate-drive programmability, package thermal performance, and control architecture come together in a realistic inverter implementation. For the user drilling a screw, that engineering translates into immediate torque response, sustained power during load changes, and a tool that can keep working without unnecessary thermal derating.

#### A right-fit MOSFET for the motor-drive system

Battery-powered motor drive applications demand more than a low resistance value. The MOSFET must support the full operating profile: start-up torque, continuous current, stall events, switching transients, EMI constraints, thermal limits, and compact mechanical design.

[OptiMOS™ 7 40 V motor-drives optimized](#) represents a new generation of power MOSFETs, offering lower  $R_{DS(on)}$ , reduced switching losses, improved parasitic turn-on immunity, up to 3× wider SOA compared to the current OptiMOS™ 6, and package options for higher thermal performance. For users, those engineering choices appear as the experience they care about most: responsive torque, longer work time, and reliable performance from a compact cordless tool.

Explore the OptiMOS™ 7 40 V motor-drives optimized [portfolio](#) to select the right device for next-generation battery-powered motor-drive designs.

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# Analytical Relationship Between Feedback Loop Properties and Load Transient Response in Voltage Converters

*Many applications impose strict requirements on output voltage response to rapid load changes, motivating an analytical link between frequency-domain loop design and time-domain transient behavior. Phase margin and feedback loop bandwidth are key design parameters in voltage converter control for achieving specified transient performance. Existing models are typically based on specific converter topologies or controller methods, limiting their portability. This article presents a generic loop model formulated directly in terms of loop design parameters, largely independent of specific converter implementation.*

*By Lazar Rozenblat, Formerly Principal Applications Engineer at Microchip*

In frequency domain small-signal output voltage excursion  $\Delta V(s)$  in response to load current step  $\Delta I$  is given by:

$$\Delta V(s) = -\frac{\Delta I}{s} \times \frac{Z_{OL}(s)}{1+T(s)} \quad (1)$$

where  $Z_{OL}(s)$  is the open-loop output impedance,  $T(s)$  – open loop transfer function [1].

Since inductors can't follow rapid current changes, the transient current flows primarily through output capacitance. Therefore for step load transient analysis we can assume that the open-loop output impedance is dominated by capacitance  $C$ . Then:

$$\Delta V(s) \approx -\frac{\Delta I}{s} \times \frac{1}{sC \times (1+T(s))} \quad (2)$$

For a given  $T(s)$  one can solve (2) for the step load response by taking the inverse Laplace transform. Classical approaches based on detailed plant-compensator models yield high-order transfer functions, which make symbolic solutions unwieldy and obscure the direct influence of key design parameters. Besides this, these models are usually based on specific converter topologies or controller structures, limiting their portability. In engineering practice, it is therefore common to approximate the open-loop transfer function by a second-order form with a single pole at the origin and another high-frequency pole above crossover [1], [2]. This approximation is a cornerstone of classical control theory and is well suited for *input* steps analysis which deals with  $T/(1+T)$ . However, when applied to *load* step analysis which deals with  $1/(1+T)$  according to (2), it yields a steady-state DC voltage offset and distortion of the predicted waveform because  $Z_{CL}(s)$  does not vanish as  $s \rightarrow 0$ .

Here, we construct a loop gain formulation that enforces zero DC output impedance while yielding a compact and analytically tractable expression for the transient response in terms of bandwidth, phase margin and output capacitance.

Bandwidth (also called crossover frequency)  $\omega_C$  is defined as the frequency at which the magnitude  $|T(j\omega)|$  equals unity (or 0 dB in logarithmic scale). Phase margin is the difference between the argument of  $T(s)$  at the crossover frequency and  $-180^\circ$ :

$$\Phi_M = \angle T(j\omega_C) + 180^\circ \quad (3)$$

It's well-known that phase margin  $\Phi_M$  and consequently the transient response, are primarily determined by the local slope of  $T(s)$  magnitude at  $\omega_C$  [1], [3]. To analyze the transient response we aim to derive a reverse relationship: to reconstruct  $T(s)$  which results in particular phase margin at given crossover frequency.

## Construction Of Open Loop Transfer Function

In well-stabilized voltage converters characterized by *minimum-phase* behavior the loop gain  $T(s)$  displays a smooth and monotonic magnitude characteristic in the vicinity of  $\omega_C$ . For such systems, the Bode gain-phase relationship, which follows from the Hilbert transform dictates a direct correspondence between the phase margin and the local slope of the gain magnitude at crossover [3], [4].

Let's consider two boundary cases:

- $T(s) = \omega_C/s$  has slope  $m=-1$  or  $-20$  dB/decade yielding phase margin  $\Phi_M=90^\circ$  (stable condition).
- $T(s) = (\omega_C/s)^2$  has slope  $m=-2$  or  $-40$  dB/decade yielding phase margin  $\Phi_M=0^\circ$  (oscillatory-like).

Between these two boundaries the local slope “ $m$ ” varies between  $-1$  and  $-2$  while the resulting phase margin varies between  $90^\circ$  and  $0^\circ$ .

Therefore, in general, for a stabilized converter the  $T(s)$  near  $\omega_C$  can be approximated as a fractional order function:

$$T(s) = \left(\frac{\omega_C}{s}\right)^n \quad (4)$$

where  $1 < n < 2$ .

On log-log scale magnitude of such a function has slope  $m=-n$ .

By substituting  $s=j\omega$  we find phase of the function (4):

$$\angle T(j\omega) = -n \times \frac{\pi}{2} = -n \times 90^\circ \quad (5)$$

Then from (3) phase margin is:

$$\Phi_M = 180^\circ - n \times 90^\circ \quad (6)$$

Rearranging (6) we express power “n” of function (5) in terms of phase margin:

$$n = 2 - \frac{\varphi_M}{90^\circ} \quad (7)$$

Theoretically, by substituting (4) into (2) and taking inverse Laplace transformation one can derive step load transient response. However, with the fractional-order model (4) the result includes Mittag-Leffler function which masks direct influence of key design parameters.

To avoid this complexity while preserving the essential closed loop behavior, we will construct a dynamically equivalent function  $T(s)$  that behaves similar to (4) around the crossover frequency. Namely, we need  $T(s)$  that satisfies three invariants at  $\omega_c$ : unity gain, prescribed phase according to (3), and a magnitude slope approximative that of (7).

Let us examine the following function:

$$T(s) = \frac{\omega_c}{s} \times \frac{\sin \varphi_M \times s + \cos \varphi_M \times \omega_c}{s} \quad (8)$$

The first term in (8) represents  $m=-1$  slope (-20 dB/decade) corresponding to  $\varphi_M=90^\circ$ . The second one is a factor that “shapes” the slope depending on  $\varphi_M$  like “fractional” slope of (4).

To verify the accuracy of the model (8) we will calculate its magnitude, slope and phase at  $\omega_c$ . By substituting  $s=j\omega_c$  it is easy to find that for such function  $|T(j\omega_c)| = 1$ .

The local slope of its magnitude at  $\omega_c$  on a log-log scale:

$$m = \frac{d(\log|T(j\omega)|)}{d(\log \omega)} \Big|_{\omega=\omega_c} = \sin \varphi_M^2 - 2 \quad (9)$$

By comparing (9) to desired slope  $m=-n$ , where “n” is given by (7), one can find that the function (8) provides exact slope match at  $0^\circ$ ,  $45^\circ$ , and  $90^\circ$ . The maximum discrepancy occurs at  $\varphi_M \approx 22.5^\circ$  and  $67.5^\circ$ , where the slope error is less than 6% (approximately 1.2 dB/decade).

The phase of the function (9) at  $\omega_c$  after some algebra is given as:

$$\angle T(j\omega_c) = -180^\circ + \varphi_M \quad (10)$$

Equations (9) and (10) demonstrate that the phase of the function (8) at  $\omega_c$  is exactly related to  $\varphi_M$  (3), and the slope of its magnitude closely approximates desired slope. Therefore the function (8) can adequately approximate behavior of stabilized converters open loop transfer function near crossover frequency.

### Transient Response Calculation

The step load response is obtained by substituting (8) into (2) and applying the inverse Laplace transform. After some mathematics one can find that the resulting expression exhibits three distinct regions depending on the value of  $(\cos(\varphi_M) - \sin(\varphi_M)^2/4)$ . When  $\cos(\varphi_M) - \sin(\varphi_M)^2/4 = 0$ , which occurs at  $\varphi_M = 76.345^\circ$ , the response is critically damped. The response is underdamped for  $\varphi_M < 76.345^\circ$  and overdamped for  $\varphi_M > 76.345^\circ$ .

Remarkably, the critical phase margin, obtained here independently of converter topology within the adopted model assumptions, coincides with the optimal value  $76^\circ$  reported in [2] for a buck converter.

The main practical interest presents underdamped region. In this region by applying the inverse Laplace transform one can find the transient recovery of the output voltage  $V(t)$ :

$$V(t) = -\frac{\Delta I}{C \times \omega_D} \times e^{-\sigma t} \times \sin(\omega_D t) \quad (11)$$

where  $\omega_D = \omega_c \times \sqrt{(\cos \varphi_M - \frac{1}{4} \sin \varphi_M^2)}$  – natural frequency,

$$\sigma = \frac{\omega_c \times \sin \varphi_M}{2} \text{ – decay constant, } \varphi_M < 76.345^\circ.$$

Figure 1 provides examples of transient response calculated from (11) for load step  $\Delta I = 10$  amps, output capacitance  $C = 470 \mu F$ , and crossover frequency  $F_c = 10$  kHz (which is  $\omega_c = 2\pi F_c \approx 62832$  radians).

The curves of Figure 1 show that the phase margin mostly affects the recovery shape and does not affect much peak deviation. The peak deviation depends primarily on the bandwidth and the capacitance which may be selected based on (11).

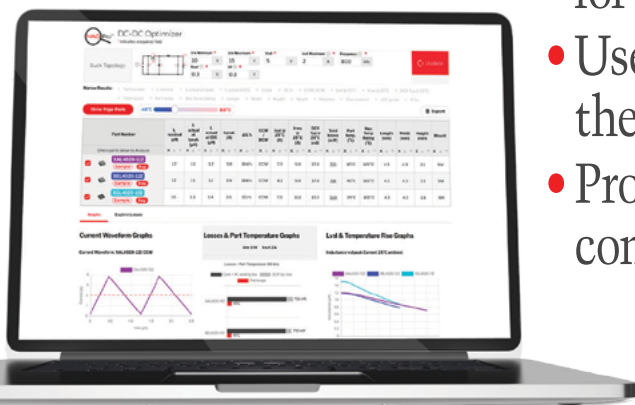
To validate the proposed bandwidth- and phase-margin-based model we simulated the transient response of 3.3V forward converter by using LTspice average model [5]. The component values in the compensation circuit were automatically adjusted for various phase margins at fixed crossover frequency. The resulting phase margins were verified with AC analysis. The simulation was done under the same conditions of load step, bandwidth and output capacitance as used for Figure 1.



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The simulation results confirm that the general dependence of the recovery waveform on phase margin follows the analytical derivation. One can see from the simulation plots that phase margin close to  $76^\circ$  yields practically aperiodic recovery without overshoot as predicted above.

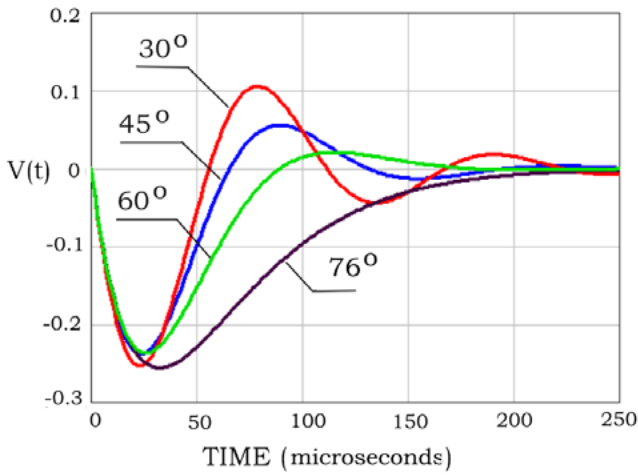


Figure 1: Step load transient response (in volts) at various phase margins

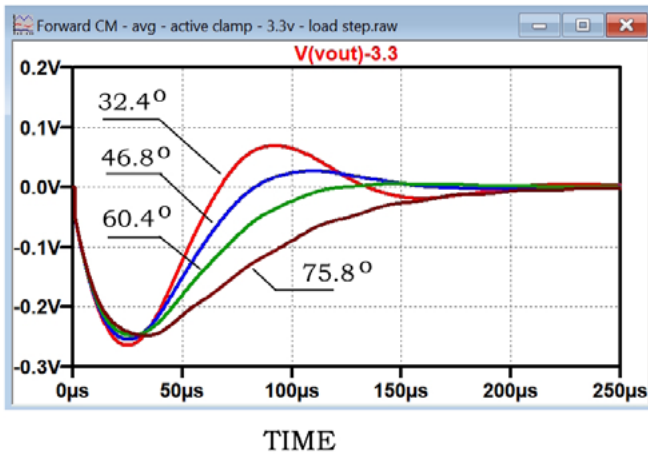


Figure 2: Simulated step load voltage transient response at various measured phase margins

Equation (11) also allows estimation of the desired characteristics of the transient voltage such as settling time and peak overshoot, as functions of three properties:  $\omega_C$ ,  $\varphi_M$ , and  $C$ .

We define settling time as the time from the initial onset of the load transient to the time when  $V(t)$  returns to a specified fraction " $\epsilon$ " of the nominal steady-state value  $V_0$ .

$$|V(t)| \leq \epsilon \times V_0 \quad \exists t > t_{PK} \quad (12)$$

To find the settling time we will first identify time to peak, as the time where the first derivative of  $V(t)$  is zero. By setting  $dV(t)/dt=0$  and solving for " $t$ " after some manipulations we find time to peak as:

$$t_{PK} = \frac{1}{\omega_D} \times \tan\left(\frac{\omega_D}{\sigma}\right) \quad (13)$$

Then from (11) the absolute values of the peak deviation  $V_{PK}$  is:

$$V_{PK} = \frac{\Delta I}{C \times \omega_D} \times e^{-\sigma t_{PK}} \times \sin(\omega_D t_{PK}) \quad (14)$$

The decay time can be estimated as the time from peak to the time when the envelope of  $V(t)$  returns to a specified voltage band:

$$td = \frac{1}{\sigma} \ln\left(\frac{V_{PK}}{\epsilon \times V_0}\right) \quad (15)$$

Then total settling time can be found as:

$$t_S = t_{PK} + td \quad (16)$$

By combining (13) - (16) after some mathematical manipulations we obtain the settling time:

$$t_S = \frac{1}{\sigma} \ln \frac{\Delta I}{C \times \omega_C \sqrt{\cos \varphi_M} \times \epsilon V_0} \quad (17)$$

Figure 3 provides examples of settling time for  $V_0=3.3$  volt and  $\epsilon=0.01$  (1%) for various crossover frequencies under the same load step and output capacitance as for Figure 1.

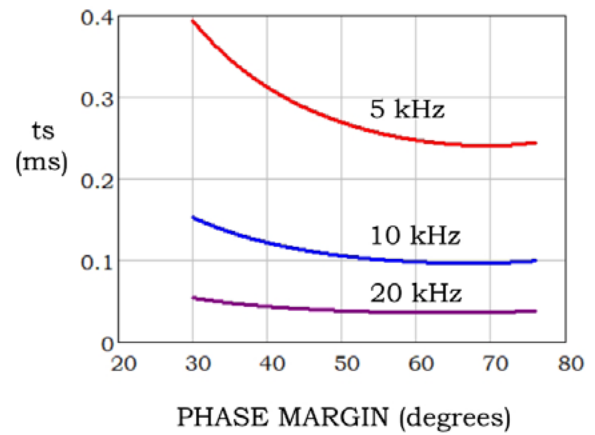


Figure 3: Settling time (in milliseconds) at various crossover frequencies

To estimate peak overshoot (i.e. the peak voltage after it reverses polarity) we note that the time span between the peak deviation  $t_{PK}$  and the subsequent polarity-reversed peak is exactly half of the period of the natural frequency  $\omega_D$ :

$$t_{OS} - t_{PK} = \frac{\pi}{\omega_D} \quad (18)$$

By combining (11) and (18) we find overshoot magnitude:

$$V_{OS} = V_{PK} \times e^{-\sigma \pi / \omega_D} \quad (19)$$

Figure 4 provides examples of the overshoot for various crossover frequencies under the same load step and output capacitance as for Figure 1.

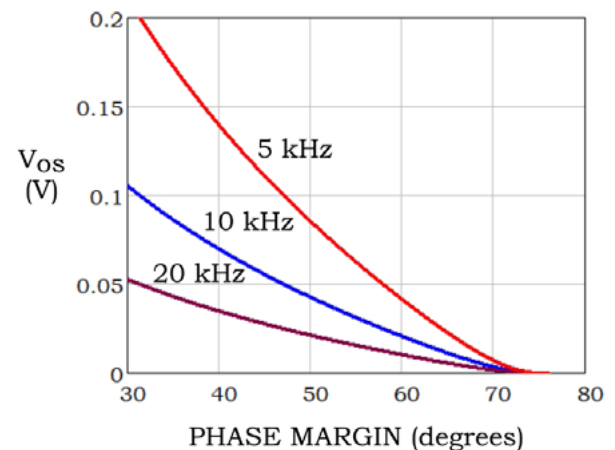


Figure 4: Overshoot (in volts) at various crossover frequencies

The preceding analysis is based on the response to step load where transition mathematically occurs instantly. In practice, of course, load transitions occur over some non-zero time. With a finite slew rate  $di/dt$  assuming load change is still much faster than the response time, the actual time to peak is given as [6]:

$$t_{PK}' = t_{PK} - \frac{\Delta I}{di/dt} \quad (20)$$

As the result, the peak deviation, settling time and overshoot value are reduced accordingly.

Owing to the simplifying assumptions used in the analysis, the obtained expressions are intended for quick qualitative estimation of transient behavior. Consequently, the derived expressions should be interpreted as first-order analytical approximations intended to capture the transient behavior and provide design insight, rather than exact quantitative predictions.

### Conclusion

The proposed approach avoids detailed circuit-level derivations by treating the loop as a behavioral system described by its phase margin, crossover frequency (bandwidth), and output capacitance. A generic, topology-independent representation of the loop gain  $T(s)$  in the vicinity of the crossover frequency enables a simple direct mapping between frequency-domain design parameters and time-domain transient behavior. It was found particularly that phase margin close to  $76^\circ$  yields aperiodic recovery.

The results provide a practical means for establishing design targets that meet output voltage transient requirements, without need of the full circuit-level analysis.

### Acknowledgment

The author thanks Christophe Basso for making available his LTspice models.

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# Why Current-Mode Gate Drivers Represent a New Approach for Wide Bandgap Devices in AI Data Center Power Supplies

*The rapidly increasing power density demanded by artificial intelligence workloads is pushing the industry toward smaller and more integrated gate driving solutions. However, many AC/DC and DC/DC designs require four or more high-voltage wide bandgap transistors in each stage, which makes the isolated gate driver selection a significant footprint concern.*

*By Matthew Segada, Systems Engineer, Skyworks*

Data center power supplies have ever increasing efficiency requirements and achieving the highest efficiency requires driving the transistors aggressively, which increases the current flowing into the parasitic capacitances of the devices. If this displacement current forces the gate to source voltage above its threshold, parasitic turn-on can occur. In the best case, this leads to a loss of efficiency. In the worst case, it can result in permanent and sometimes catastrophic failure.

When a  $dv/dt$  is applied to the FET's drain, the parasitic Miller capacitance,  $C_{GD}$ , and the gate to source capacitor,  $C_{GS}$ , are in series. The combination forms a capacitive divider with the gate node being the output. Assuming that the gate node is left floating, the approximate gate voltage rise can be approximated with  $dV_{GS} \approx \frac{C_{GD}}{C_{GS}} dV_{DS}$ . The capacitance ratio,  $\frac{C_{GD}}{C_{GS}}$ , and the  $V_{DS}$  slew rate directly affect the possibility of parasitic turn-on. If  $V_{GS}$  rises above  $V_{GS(th)}$  then parasitic turn-on can occur. This is especially pertinent for high-electron-mobility transistors (HEMTs) such as SiC and GaN which have low  $V_{GS(th)}$ .

## Eliminating engineering tradeoffs

Traditional Voltage Mode Drivers (TVMDs), without a Miller clamp, will sink the Miller current through their pull-down network, which typically consists of an internal NMOS transistor and an external user-selected gate resistor. To achieve the best clamping of  $V_{GS}$  from this Miller current,  $R_{G\text{OFF}}$  will need to be minimized. However, this means that an engineering tradeoff needs to be made because with a low  $R_{G\text{OFF}}$ , the turn-off  $dv/dt$  will be very large, potentially causing excessive  $V_{DS}$  overshoot.

To prevent the possibility of parasitic turn-on, designers can employ a range of remedies, such as slowing the turn-on  $dv/dt$ , utilizing a negative gate drive voltage, or implementing a Miller clamp. Slowing down the turn-on  $dv/dt$  means that the switching losses will be higher, leaving untapped efficiency on the table. Utilizing a negative gate drive voltage incurs additional BOM and design complexity while also increasing the external power device's body diode losses. Integrated Miller clamps increase the driver pin count and are usually only available on single channel gate drivers. External Miller clamps allow the use of larger discrete devices for stronger clamping, but they take up more board area, add driver pin count, increase BOM, and decrease reliability.

To address these issues, a new current-based gate drive technology called SelVCD™, which stands for Selectable Variable Current Drive, has been incorporated into Skyworks' latest series of isolated gate drivers. Instead of using the usual PMOS pull up and NMOS pull down networks found in TVMDs, this approach uses controlled current sources to charge and discharge the gate. This removes the need for external gate resistors, allowing the driver to apply its full pull-down strength during transient conditions, improving immunity to parasitic turn-on.

The source and sink currents are independently adjustable via two pins, SPD+ and SPD-, allowing real-time tuning from the logic input side. SPD+ controls the sourcing output current and SPD- controls the sinking output current. These settings can be dynamically updated across eight levels to optimize performance under changing conditions such as bus voltage, load current, and temperature. Control signals are transmitted across the capacitive isolation barrier and decoded on the output side.

The SelVCD architecture includes a built-in Miller clamp that engages whenever the output voltage falls to approximately 2 V above the gate driver's ground. At this point, the driver overrides the user-selected SPD- setting and applies the maximum pull-down current (SPD- 7, up to 4 A for the UVLO 15 variant devices), maintaining this state until the next rising logic input transition.

## Putting SelVCD to the test

To show the benefit of the SelVCD-enabled Miller clamp, a half bridge test setup was constructed utilizing two Wolfspeed 1200 V 16 mΩ SiC FETs (C3M0016120K) with TVMD and SelVCD gate drivers being compared as shown in Figure 1. The high side gate driver is pulsed to apply a  $dv/dt$  to the low side FET's drain. The low side FET is attempted to be kept off utilizing the gate driver.

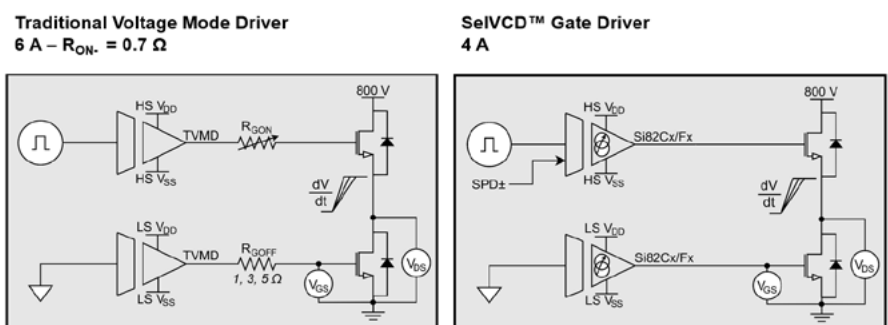


Figure 1: No current,  $dv/dt$  Miller clamp testing.

The FET's datasheet requests a turn-on voltage of +15 V and a turn-off voltage between -3 to -4 V. However, to show the benefit of SelVCD, a 0 V turn-off voltage was used.

A 6 Amp TVMD with an internal pull down  $R_{DS(on)}$  of 0.7  $\Omega$  was utilized. In the TVMD case, the turn-on speed is varied by changing the  $R_{G(on)}$  and in the SelVCD gate driver case, the SPD+ setting is varied from SPD+ 0 to SPD+ 7. For the low side gate driver, the  $R_{G(off)}$  is varied between typical gate resistors of 1, 3, and 5  $\Omega$  while the SelVCD gate driver is directly tied to the gate of the SiC FET.

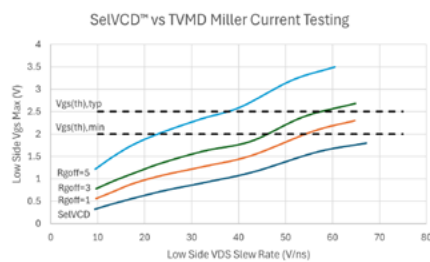


Figure 2: Parasitic Turn-On Testing Results.

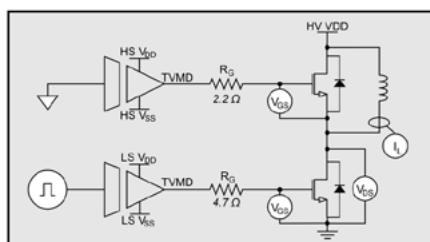
As shown in Figure 2, the traditional voltage mode gate driver in every case will eventually have the possibility of parasitic turn-on. SelVCD™ allows the gate to remain under the  $V_{GS(th),min}$  condition even at the most extreme slew rates.

A customer was shown the previously discussed results and requested validation on their power factor correction (PFC) board, which uses two 750 V SiC FETs. These devices require +18  $V_{GS,ON}$  and 0  $V_{GS,OFF}$ . The existing design employed a 4.7  $\Omega$  turn-on resistor and a 2.2  $\Omega$  turn-off resistor, and the customer requested a comparison. Miller clamp testing was conducted at room temperature across four load conditions, as summarized in Table 1.

| Condition | Bus Voltage (V) | Load Current (A) |
|-----------|-----------------|------------------|
| 1         | 227             | 25               |
| 2         | 455             | 25               |
| 3         | 227             | 45               |
| 4         | 455             | 45               |

Table 1: Double Pulse Test Miller Current Test Conditions.

### Si82E39ABE-IS3



As shown in Figure 3, the low side is pulsed as in a double pulse test and the high side  $V_{GS}$  is viewed using an optically isolated probe. Specifically, the high side  $V_{GS}$  is viewed during the low side's turn-on transition, which causes the high side FET to have current injected into the parasitic Miller capacitor when  $V_{DS,HS}$  goes from 0 V to 800 V. The SPD+ setting (SPD+ 4) of the low side SelVCD gate driver was selected such that the falling  $V_{DS,LS}$  slew rate was tightly matched to the 4.7  $\Omega$  TVMD driver. Both slew rates were within 2 V/ns of each other over all conditions tested.

As seen in Figure 4, the TVMD with the customer's current gate resistor selections would need a negative gate drive rail to mitigate parasitic turn-on. However, this specific FET has an absolute maximum negative  $V_{GS}$  of -4 V. Due to other transients affecting  $V_{GS}$ , the only solution that would work for this FET with the TVMD is to slow down the turn-on transition, increasing the switching losses. However, the SelVCD driver stays well below the minimum  $V_{GS(th)}$ , mitigating these issues with no extra BOM required.

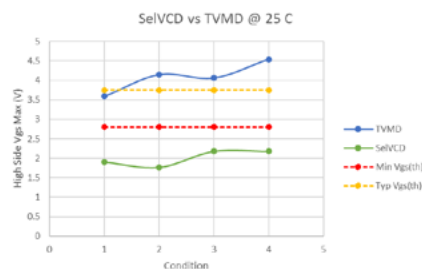


Figure 4: Double pulse test Miller clamp results.

### Conclusion

SelVCD minimizes the risk of parasitic turn-on while allowing removal of the negative gate-drive bias. This allows users to lower their BOM, free up valuable board space, and improve system efficiency. To achieve comparable performance, TVMDs must rely on Miller clamps, reduced switching speeds, or negative gate drive voltages, all of which introduce design tradeoffs.

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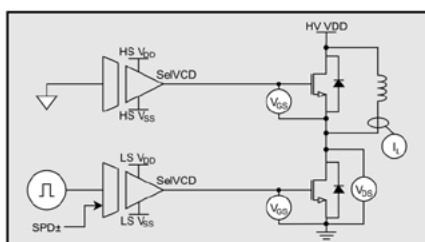


Figure 3: Miller clamp testing during double pulse test.

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# Reduce Silver, Not Performance: High Reliability Preforms for Module-to-Heatsink Attach

*Power modules can be classified in two categories: Frame modules which use plastic housing, filled with silicone gel as encapsulant and transfer molded modules (TMM), which use epoxy mold compounds (EMC) as encapsulant.*

*By Dr. André Schwöbel, Business Development Manager, Heraeus Electronics*

Later ones are an established choice for traction inverters in electric vehicles (EV) [1]. The reliable and cost-efficient attachment of the TMM to a heatsink is a key process in EV traction inverter assembly. Several attachment variants exist in the market: Large area sintering (LASI) using silver- or copper- sinter pastes, large area soldering (LASo) using lead-free low-melting solder preforms or polymer based thermal interface materials (TIM). Large area sintering is predominantly used for premium applications with highest thermal and reliability requirements. Large area soldering offers a good compromise between costs, good thermal performance and reliability.

A LASo process combining a low-melting solder alloy and a solder process based on vacuum/formic acid offers almost void free, low cost and highly reliable solder joints. The alloy system must be chosen in such a way that its liquidus temperature is low and therefore compatible the EMC which has typical glass transition temperature  $T_g$  from 180°C to 200°C [2]. When exceeding the  $T_g$  of the EMC during assembly process, its coefficient of thermal expansion increases significantly which can cause damage to the power module during assembly process and lead to failure of the power module. Based on that, highest care must be taken to properly select the solder alloy and use suitable solder techniques to avoid EMC delamination from the power module.

In this contribution the advantage of the Innolot® solder alloy family, especially Innolot2.0 will be shown based on simulation and experimental data.

## The alloy system Innolot2.0™

### – A cost-optimized solder alloy for LASo

For a successful LASo process the alloy system should have a liquidus temperature as low as possible to limit the stress on the package by a high-temperature solder process and therefore avoid internal EMC delamination. Additionally, the alloy system must show sufficient reliability (i.e. creep properties) and must be affordable (i.e. Ag content). A non-extensive comparison of available solder alloy systems is given in Table 1.

|                      | Innolot® 1.0              | Innolot® 2.0          | SnSb <sub>5</sub> | SAC305     |
|----------------------|---------------------------|-----------------------|-------------------|------------|
| <b>Composition</b>   | SnAg3.8Cu0.7Ni0.1Sb1.5Bi3 | SnAg1.5Cu0.7Sb1.5Bi3X |                   | SnAg3Cu0.5 |
| <b>Melting range</b> | 206-218 °C                | 212-222°C             | 228-243°C         | 217-220°C  |
| <b>Reliability</b>   | +                         | +                     | 0                 | -          |
| <b>Cost</b>          | 0                         | +                     | +                 | 0          |

Table 1: Material properties of various commercially available solder alloys.

+ means most beneficial properties, whereas – highlights non-beneficial properties.

Innolot (here stated as Innolot 1.0) is a well-known alloy in the Tin-Silver-Copper system with small additions of Nickel, Antimony and Bismuth for improvement of creep strength [3]. The combina-

tion of a rather low melting temperature ranging from 206-218 °C with increased creep strength, makes Innolot a good candidate for the large area soldering process. However, Innolot 1.0 has a silver content of 3.8 wt% which adds precious metal costs to the overall alloy price. Driven by the market demand Heraeus Electronics developed a new SAC-based alloy with different additives and significantly lower Ag-content, which is commercially available as Innolot 2.0 [4]. The slightly higher melting temperature range of 212-222°C is still well below the melting temperature range of SnSb<sub>5</sub> (228-243°C) which makes Innolot 2.0 the cost-optimized choice for the attachment of TMMs to heatsinks. The major benefit of Innolot 2.0 is its significantly lower Ag content of only 1.5 wt%. Heraeus Electronics offers Innolot 1.0 and Innolot 2.0 alloys as ribbons and precut preforms.

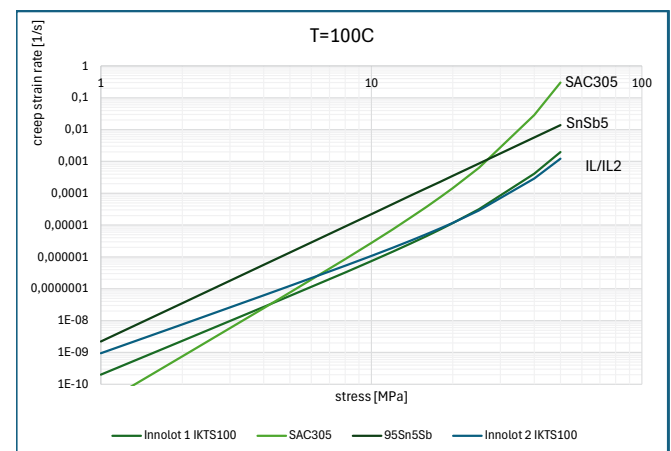


Figure 1: Fitted creep rates as a function of stress at  $T=100^{\circ}\text{C}$ . The values were measured at  $100^{\circ}\text{C}$  using test samples which were exposed to constant stress. Creep rates were extracted, and the measurement points were fitted using the Garofalo equation. Data generated in cooperation with Fraunhofer IKTS.

## Superior creep properties and improved reliability

The superior creep performance and its influence on the thermal shock performance is proven by material characterization, simulation and by thermal shock tests. Figure 1 shows the fitted secondary creep rate as a function of stress of the four alloys from Table 1 using the Garofalo law.

The data is available at multiple temperatures but only shown for  $T=100^{\circ}\text{C}$ . Full material models are available on request. The Innolot family shows lowest secondary creep rates at highest stress which



Vincotech

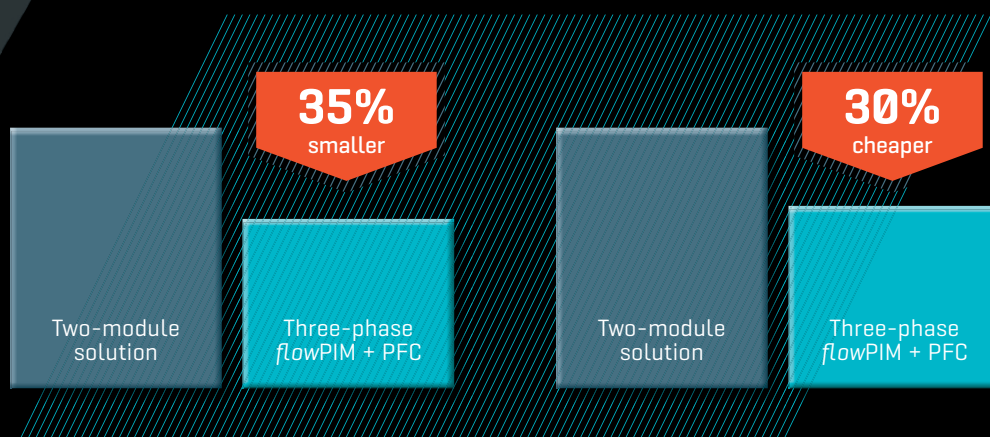
# DEEPER INTEGRATION AT **HIGHER POWER**

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More power, smaller footprint: Engineers tasked to design state-of-the-art heat pumps and HVAC systems have to find a way to satisfy these conflicting demands. Vincotech's 1200 V PIM+PFC is the answer. Its integrated three-phase ANPFC and inverter stage resolve that contradiction to boost efficiency and cut systems costs.

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- / All-in-one solution: three-phase PFC with inverter stage in a compact *flow1* housing allows for more compact designs and higher power density
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indicates highest reliability in the final application as creep is a major contributor to solder alloy degradation.

With the available material data thermomechanical finite element simulations (FEM) of the four alloys under thermal cycling conditions were conducted. The simulation model is shown on the left and center picture of Figure 2. Within the simulation an AMB substrate was soldered with a 100 µm thick solder layer to an Aluminum based heatsink and molded with an EMC. The assembly was cycled within the simulation from -40 °C to +125 °C with a dwell time of 30 min. The strain per thermal cycle was selected as damage parameter to compare the four alloys. Figure 2 (right picture) shows a comparative heatmap of the strain

per cycle within each half-bridge of the four alloys. Clearly visible is that SAC305 and SnSb<sub>5</sub> show higher strain per cycle compared to the Innolot family. Additionally, highest strain per cycle (damage) occurs at the edges of the module. Based on the simulation the Innolot alloys should show less delamination during thermal cycling than the SAC305 or SnSb<sub>5</sub>. Additionally, the solder process of SnSb<sub>5</sub> alone could already damage the EMC/AMB interface due to the high melting temperature range of SnSb<sub>5</sub> compared to Innolot. This effect is not covered in the FEM simulation. The simulation study was repeated using 300 µm thick solder layers. The strain per cycle is significantly reduced. The bond line thickness is therefore another influencing factor on solder reliability but also on cost.

Thermal shock tests confirm this finding from the simulation. For this purpose bare AMB substrates (0.3 mm Cu/0.32 mm Si3N4/0.3 mm Cu) were soldered to Ni plated Cu-core baseplates (3 mm thickness). The soldered area was 27 x 38 mm<sup>2</sup> for each AMB. The assemblies were soldered using 300 µm thick alloy preforms under vacuum/formic acid using a PINK vadu 200 solder equipment. The individual assemblies were not molded within this study. Before and after thermal shock (-40°C/+125°C) scanning acoustic microscope (SAM) images were taken, which are shown in Figure 3. SAC305 shows severe degradation after 1000 cycles. SnSb<sub>5</sub> shows slight delamination at the edges of the assemblies, which matches to the simulation expectation. Innolot 2.0 shows only minor delamination on one of the assemblies, whereas Innolot 1.0 shows no visible delamination at all. The experimental thermal cycling results confirm our simulation results.

Conclusion

Innolot 1.0 and Innolot 2.0 are proven low-melting but high reliable alloys. Our findings based on the conducted material characterizations, simulations and experiments are summarized in Figure 4. Innolot 1.0 and Innolot 2.0 are both commercially available as individual preforms or ribbons.

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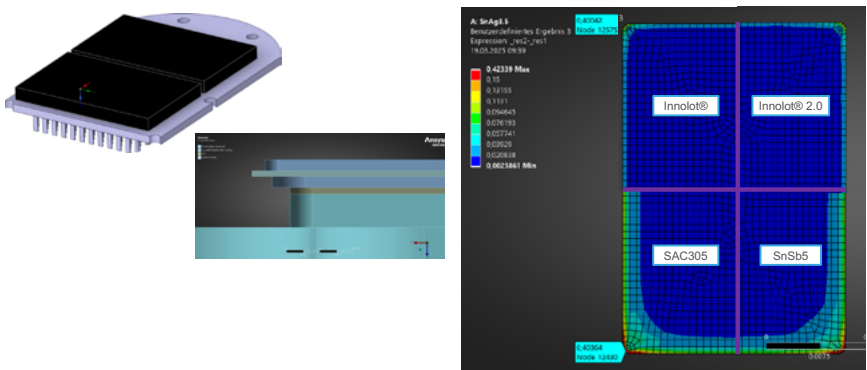


Figure 2: Left and middle picture - Simulation model. Right picture - Creep strain per thermal shock cycle of the 4 alloys. Blue indicates lowest strain per cycle. Red indicates highest strain per cycle.

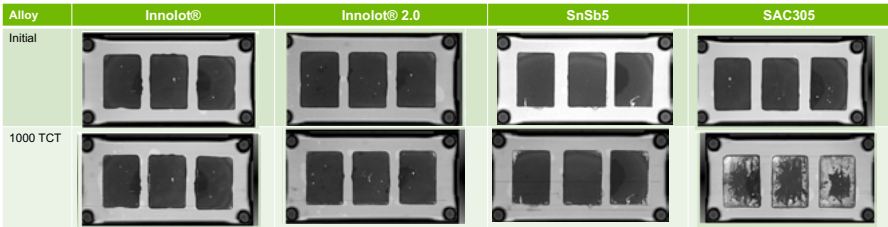


Figure 3: SAM images before and after 1000 cycles of thermal shock.

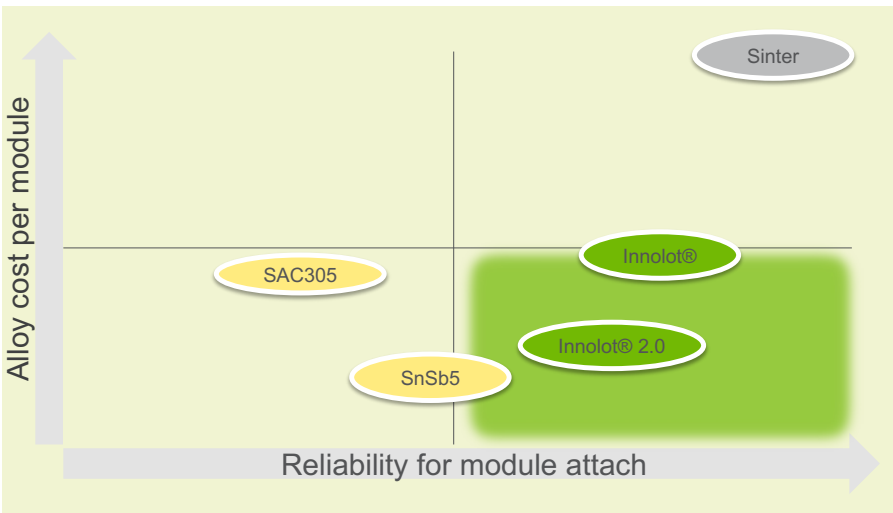
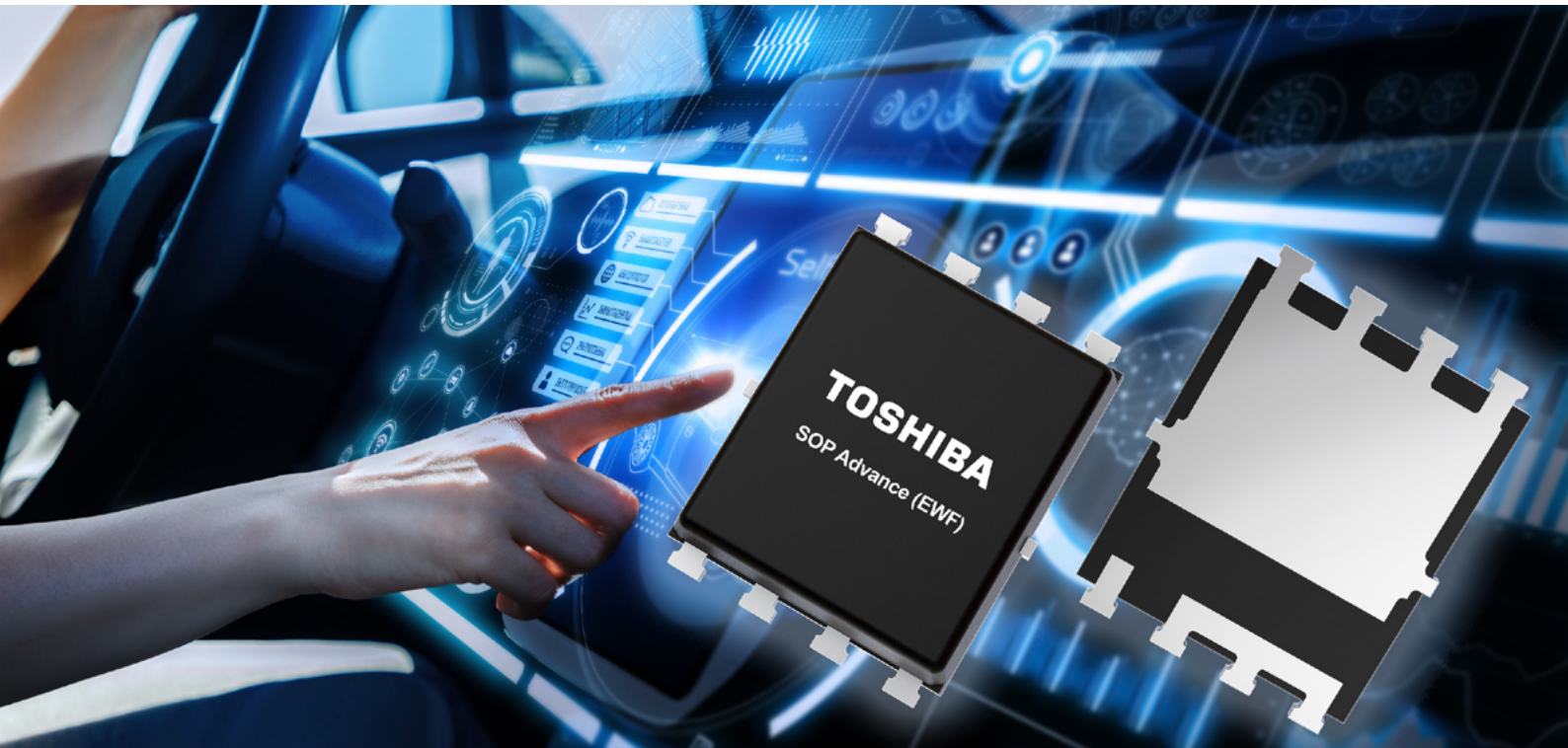


Figure 4: Ranking of the four tested alloys within the Reliability/Cost chart.

## Next Generation MOSFET Packaging



Toshiba's new SOP Advance(EWF) package for Automotive MOSFETs improves product on-resistance performance by increasing the mountable chip size and reducing package resistance.

### Package highlights

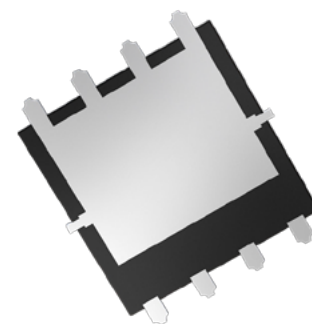
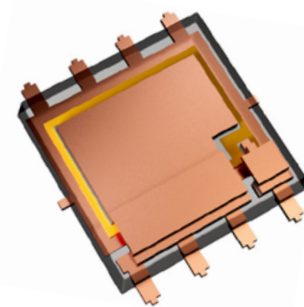
- 38% reduction in channel-to-case thermal impedance ( $Z_{th(ch-c)}$ ) vs. SOP Advance(WF)\*
- Reduced package resistance achieved through improved post structure and source terminal design
- 20% Improvement in drain-current ( $I_D$ ) rating vs. SOP Advance(WF)\*
- Enlarged mountable chip size and improved chip bed frame design
- Compatible with SOP Advance(WF) and other popular 5 x 6mm packages

### Featured products with 40V drain-source ( $V_{DS}$ )

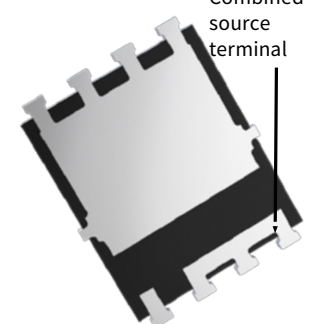
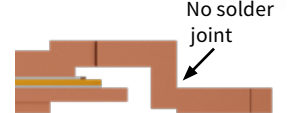
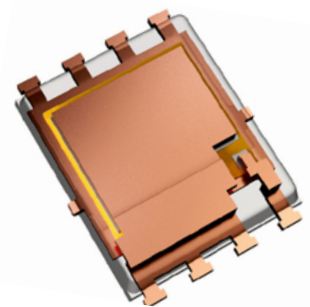
| Part number | Drain current<br>$I_D$ | Drain source on-resistance<br>(Max) $R_{DS(ON)}$ |
|-------------|------------------------|--------------------------------------------------|
| XPMR5904PB  | 180A                   | 0.59mΩ                                           |
| XPMR7004PB  | 160A                   | 0.70mΩ                                           |
| XPMR8504PB  | 140A                   | 0.85mΩ                                           |

\* Comparison between current XPHR7904PS and the new XPMR5904PB

### Current SOP Advance(WF)



### New SOP Advance(EWF)





# Breaking the Silicon Limit and Moving Beyond the SiC Ceiling

High-voltage power conversion is at the heart of electrification, even if most people never see it. Data centers, industrial drives, medical equipment, telecom systems, renewable-energy systems, and EV charging all need power transistors that can handle high voltage, low loss, fast switching, and strong ruggedness. In this field, the question is no longer only how to improve silicon. It is how to push past the old silicon limit and now, how to challenge the current SiC limit as well. That makes device choice a direct system-level decision, not just a component choice.

By Adrian Wong, Senior Application Technologist, IceMOS Technology

IceMOS has built its story around that idea. Its MEMS Superjunction MOSFET platform, or mSJ MOS, combines MEMS-style trench SOI processing with sub-micron CMOS manufacturing to create a high-voltage superjunction structure. IceMOS says the process uses bonded silicon-on-insulator substrates, deep trench etching, and oxide or polysilicon refill. This has already led to commercial silicon superjunction MOSFETs from 600 V to 730 V, and it now supports the company's next-stage substrate roadmap.

The value of superjunction silicon is easy to explain. By using alternating N- and P-type pillars in the drift region, the device can flatten the electric field and lower specific on-resistance without giving up blocking voltage. IceMOS stands out because it does not rely only on the usual epitaxial approach. Instead, it uses a MEMS-based process that aims to improve pillar accuracy, charge balance, and scale-up. In public material, that means low  $R_{DS(on)}$ , low gate charge, high  $dv/dt$ , strong UIS ruggedness, and high peak current capability.

That platform is already in the market. IceMOS lists Gen-1 and Gen-2 products in TO-220, TO-247, DFN8x8, DFN5x6, TOLL, and DPAK packages. Examples include the 600 V ICE32S60W in TO-247 with 32 A and  $0.078 \Omega$  max  $R_{DS(on)}$ , the 650 V ICE24S65L in DFN8x8 with 24 A and  $0.141 \Omega$  max  $R_{DS(on)}$ , and the 600 V ICE47N60W in TO-247 with 47 A and  $0.068 \Omega$  max  $R_{DS(on)}$ . These parts show that IceMOS is not only talking about a roadmap. It already has real devices for high-voltage conversion.

The next part of the story is more ambitious. IceMOS is not stopping at silicon. Its roadmap points to mSJ MOS-Si and mSJ MOS-4H-SiC structures that aim to move the blocking-voltage-versus-specific-

ic- $R_{DS(on)}$  curve beyond today's best silicon and SiC devices. In the roadmap figure, Gen5 and Gen6 are shown as 4H-SiC ideas built around a symmetrical charge-balance cell design. IceMOS says the mSJ MOS-4H-SiC™ GEN6 target is an estimated  $0.2 \text{ m}\Omega\text{-cm}^2$ , or about 10x better than current state-of-the-art SiC. This is a roadmap target, not a shipping spec, but the size of the claim is still important.

This is why the roadmap matters beyond future SiC research. Even for engineers working on present-day 600 V to 650 V systems, it shows how IceMOS sees the next step after commercial superjunction silicon. In other words, the roadmap links today's shipping products to a longer-term device architecture strategy. It also helps explain why the company's roadmap matters to current product decisions.

## Blocking Voltage vs. Specific $R_{DS(on)}$

Enabling Lower Conduction Loss for Next-Generation Power Systems

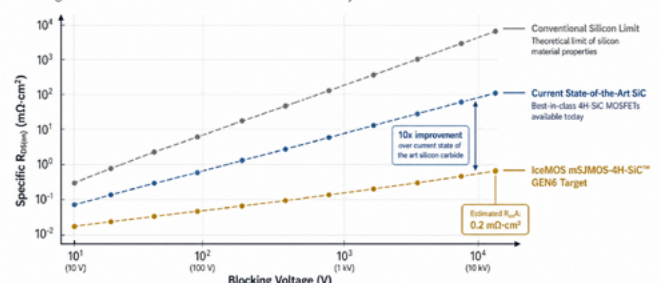


Figure 2: IceMOS mSJ MOS-4H-SiC™ GEN6 target and projected 10x improvement over state-of-the-art SiC.

The figure makes the point clear. It does not show a small step forward. It places the GEN6 target far below the current SiC limit line. That is why the message is stronger than “better SiC.” It suggests a different device structure, not just a small process tweak.

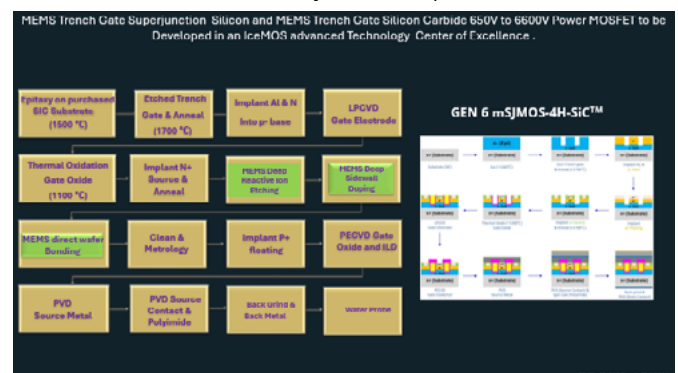


Figure 3: Advancements enabled by MEMS Processes in IceMOS GEN6 4H SiC architecture.

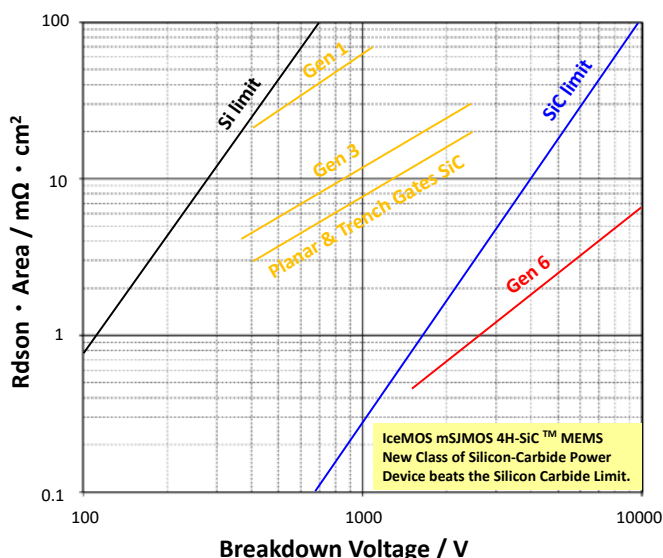


Figure 1: IceMOS mSJ MOS-4H-SiC™ GEN6 roadmap: blocking voltage versus specific  $R_{DS(on)}$  beyond the current SiC limit.

This is the key idea. IceMOS is trying to do to SiC what superjunction once did to silicon: break a trade-off that was once seen as fixed. In silicon, superjunction changed the link between blocking voltage and drift resistance. In the new 4H-SiC roadmap, the same charge-balance idea is being pushed into a wide-bandgap device. If it works, the result is not just a slightly better SiC MOSFET. It could be a new class of high-voltage device with much lower conduction loss.

#### IceMOS mSJ MOS Technology Roadmap



Figure 4: IceMOS mSJ MOS technology roadmap from silicon actuals in 2020 to 4H-SiC superjunction GEN6 target in 2029.

This timeline works better than a patent graphic because it tells the technology story in a simple way. It starts with IceMOS mSJ MOS silicon actuals in 2020, shown as Gen 1 devices from 600 V to 730 V. It then moves to silicon development in 2026, shown as Gen 3, before shifting to 4H-SiC planar and trench-gate work in 2026 and finally to 4H-SiC superjunction GEN6 in 2029. Read this way, the figure shows a real technology path from silicon superjunction products to more advanced SiC structures.

The patent story should be handled carefully, but it still matters. Public material says the patent portfolio is growing, with one 2025 company release referring to over 70 patents and later summaries referring to more than 80 granted patents. In power semiconductors, the real moat is usually not one spec number. It is the mix of process know-how, device design, manufacturing, and freedom to operate. A growing patent base supports the view that IceMOS is building a platform, not just one product line.

The overall logic is still strong. IceMOS describes a path from dielectric isolation and MEMS-enabled silicon superjunction devices to an engineered silicon-carbide drain MOSFET, with support from

NASA Phase I SBIR work and later the UK Space Agency. That shows continuity. The company is not leaving silicon behind. It is carrying the same process idea into a harder SiC target.

That is also why the story should not be read as a single product claim. IceMOS is presenting a process and structure roadmap that starts with commercial silicon, moves through further silicon development, and then extends into 4H-SiC planar, trench, and superjunction concepts. This gives the company a clearer platform identity than a normal one-generation device launch.

For engineers, the short-term value is clear. IceMOS silicon superjunction devices can fit in PFC stages, auxiliary supplies, inrush protection, industrial supplies, and the slow, line-frequency leg in hybrid totem-pole PFC, where SiC or GaN is used in the fast-switching leg. In that topology, the slow leg handles the low-frequency conduction path, so cost and ruggedness matter more than extreme switching speed. That makes advanced silicon a practical choice for the slow leg. That makes it relevant not only for efficiency, but also for cost, thermal design, and packaging choices.

That matters in EV charging, server power, renewable energy, and industrial drives. In these systems, even a small gain in efficiency can reduce cooling, increase power density, and lower total cost. A real step beyond today's SiC limit would therefore be more than a lab result. It would affect the whole system. More importantly, it would mark a structural break in how engineers think about the silicon-versus-SiC roadmap. Instead of choosing between mature low-cost silicon and higher performance SiC, designers could be looking at a new category that changes the trade-off itself. That is why the claim feels revolutionary: it is not about squeezing out one more generation of improvement, but about redrawing the device-performance map.

For this readership, that is the strongest message. IceMOS is not just another superjunction silicon story, and it is not only a wide-bandgap story either. It is a MEMS-derived platform that first broke the silicon limit and now wants to move well beyond the current SiC ceiling. The mix of commercial silicon, a 4H-SiC roadmap, a very aggressive performance target, and a growing patent estate gives the company a clear position: the next big leap may come from rethinking the device structure itself.

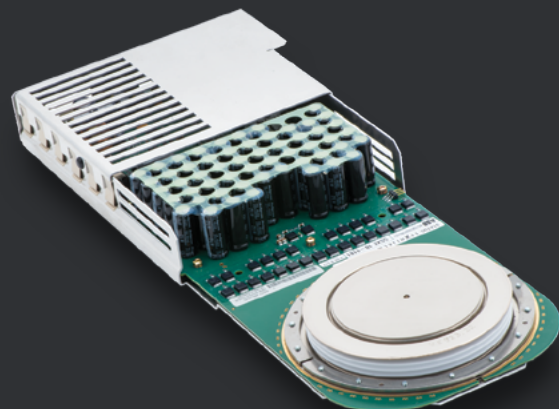
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# HITACHI







# AI-Driven Battery Intelligence for UAVs

*UAV digital twins reduce flight-test cost and accelerate design, but many remain weak where missions most often fail: the battery and power system.*

*This article presents a battery-centric workflow in which new packs are validated through charge-discharge cycling, mission-profile replay, and hardware-coupled emulation. The resulting data feed AI models for state of charge, state of health, and mission-readiness prediction. Deployed on a distributed edge-cloud architecture, the twin becomes a qualification and decision-support tool for mission-critical operations.*

*By Deepak V Katkoria, Marina Delilovic, Younesse Idmalek, Logiicdev GmbH*

## The missing part of many UAV digital twins

Digital twins are now common in UAV development. They help engineers simulate aerodynamics, test control logic, compare mission plans, and reduce risky field trials. Yet a drone that looks safe in simulation can still fail in the air if the model treats the battery as an ideal energy block instead of a stressed electrochemical system.

For mission-critical UAVs, the power system is not a background component. It is the constraint that decides endurance, payload margin, return-to-home safety, and emergency reserve. Research on electric UAV battery health has shown that usable energy depends not only on initial state of charge, but also on battery health, discharge profile, and flight regime [1]. In practical terms, take-off, cruise, payload operation, and landing are different electrical events. A credible twin must know the difference.

This is the central argument of this article: a UAV digital twin becomes an engineering tool only when its battery model is validated against real hardware, real mission loads, and real degradation behaviour.

## Why the battery is the credibility test

Battery behaviour in UAVs is nonlinear. A pack can deliver acceptable energy in a slow laboratory discharge yet become risky in a high-current mission: fast current transients cause voltage sag and thermal stress, and aging compounds this as capacity fades and internal resistance rises.

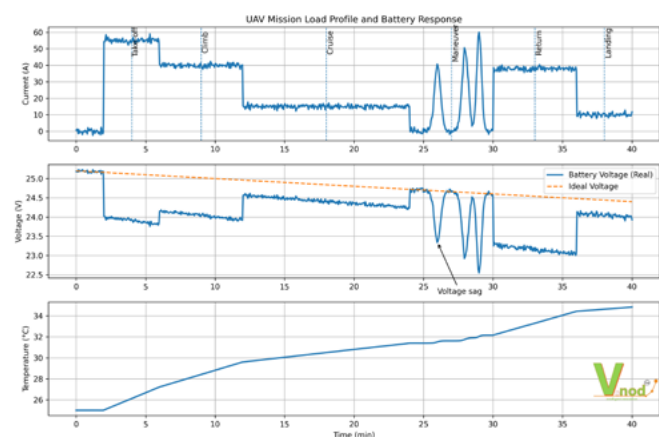


Figure 1: Mission load profile and corresponding battery response under realistic UAV conditions

Supplier variation adds another layer of risk. Two packs can share the same label, chemistry, nominal capacity, and C-rating but behave differently under the drone's real load. This matters for defence, rescue, inspection, transport, and other applications where a forced landing is not just a failed test; it can mean loss of mission, loss of asset, or danger to people.

The practical result is simple: battery trust cannot be imported from a datasheet. It must be earned through validation.

## Mission-profile replay instead of static testing

Constant-current tests establish a baseline but do not represent real flights, which mix idle time, take-off peaks, climb demand, payload activity, wind correction, return-to-home reserves, and landing. A pack that passes a static test may still fail when these events appear in sequence.

Mission-profile replay closes this gap. The real or expected drone load is recorded, transformed into a repeatable test profile, and applied to the battery under controlled conditions. This allows the operator to compare packs, detect weak cells, estimate voltage reserve, and decide whether a battery is approved for a specific mission class.

Recent research validates discharge models under variable power loads in reproducible scenarios [5]. For V.nod™, the validation bench asks not only how much energy a pack stores, but whether it can survive the mission it is expected to fly.

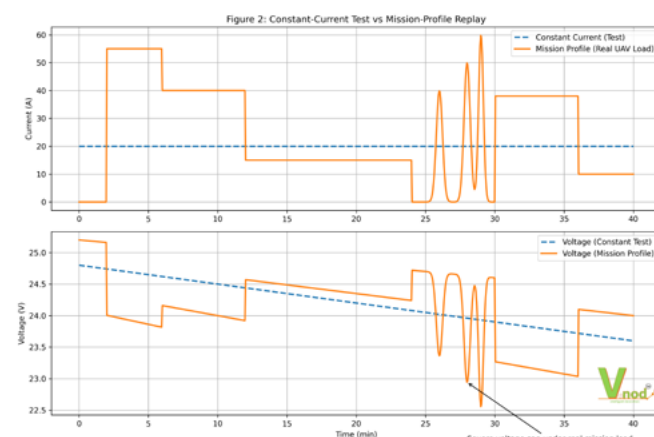


Figure 2: Comparison between constant-current testing and realistic mission-profile replay

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### Battery validation for new or unknown suppliers

A useful digital twin must also answer a business and operational question: can a new battery supplier be trusted? When a new pack enters the system, V.nod assigns it an identity, records its electrical behaviour, and exposes it to repeated charge-discharge and mission-replay cycles before operational use.

The aim is not to test forever. The aim is to create a clear approval gate. If the new pack behaves within validated limits, the existing model can be reused or lightly updated. If the rating, chemistry, thermal behaviour, voltage sag, or degradation pattern changes, the battery must trigger a new validation cycle and a new model version.

This approach turns supplier onboarding into an engineering process instead of a guess. It also creates traceability: every approved battery has a history, a model, and a mission envelope.

### Hardware-coupled emulation: where the twin meets the drone

Simulation alone cannot prove that the UAV electronics will react correctly to a stressed battery. Hardware-in-the-loop and power-hardware-in-the-loop methods solve this by connecting real hardware to a real-time model. Battery-emulator research shows that this approach can make power-electronics testing faster, more reproducible, and less dependent on physically swapping battery packs [4].

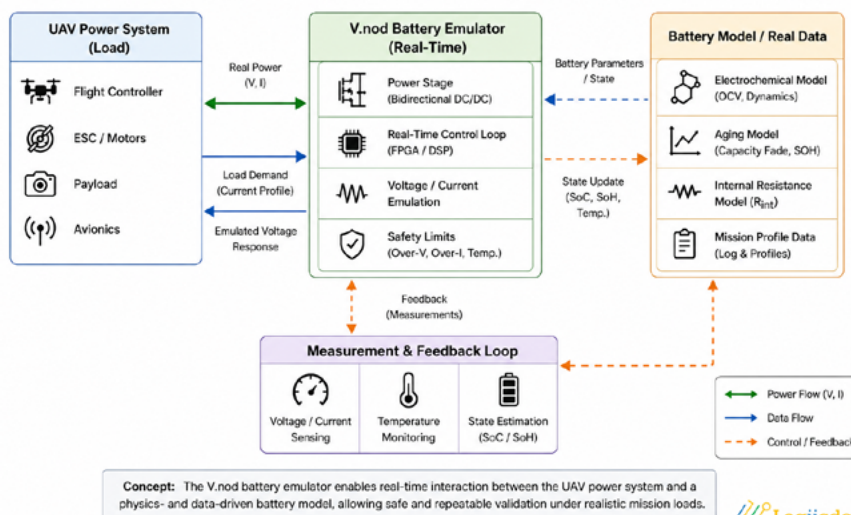


Figure 3: Hardware-in-the-loop battery emulation enabling safe and repeatable UAV validation.

In the V.nod workflow, the emulator can replace the physical battery during selected tests while reproducing the voltage-current behaviour learned from validated packs. The flight controller, power distribution board, ESCs, motors, and payload electronics then experience realistic power conditions without requiring a dangerous flight test.

This is the moment when the digital twin becomes cyber-physical. It is not only predicting the battery. It is driving hardware with battery behaviour.

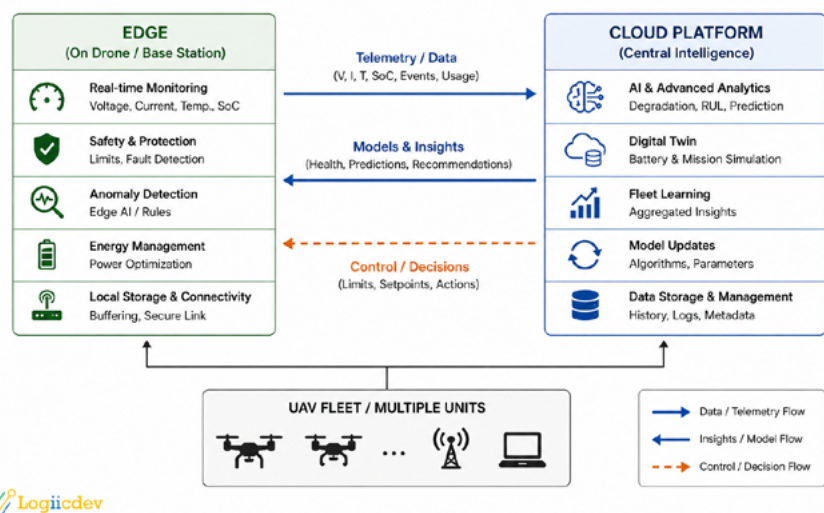


Figure 4: Distributed edge-cloud architecture combining real-time safety with fleet-level intelligence.

### AI-Driven Battery Intelligence

AI is useful here because battery risk is not a single number. Mission readiness depends on state of charge, state of health, temperature, internal resistance, recent usage, cell imbalance, load profile, and expected reserve. Machine-learning BMS work for UAVs has demonstrated the use of current, voltage, and temperature data to predict SoC and estimate SoH, including practical deployment with drone hardware, embedded devices, gateways, and cloud services [2].

The role of AI in V.nod should therefore be framed carefully. It is not a black box replacing engineering judgment. It is a decision layer trained on validated hardware data. At the edge, it supports fast safety decisions: stop charging, limit discharge, flag a weak pack, or block a mission. In the cloud, it supports slower learning: fleet trends, supplier comparison, degradation models, and model version control.

A strong rule is needed: AI models may be reused only inside their validated envelope. When a supplier, rating, chemistry, or mission load changes beyond that envelope, the system must request new validation data.

### Distributed Edge-Cloud Architecture

The proposed architecture separates real-time responsibility from long-term learning. The edge layer sits close to the hardware. It performs measurement, safety checks, battery emulation, charging and discharging control, and mission-profile replay. It must remain fast, deterministic, and safe even without cloud connectivity.

The cloud layer is the memory of the fleet. It collects anonymized battery histories, compares suppliers, trains and validates models, stores model versions, and produces qualification evidence. Battery digital-twin research in other electric-mobility domains also emphasizes the value of connected data pipelines for state estimation and decision support [3].

### Standards Alignment

The V.nod architecture is designed in alignment with relevant international standards for AI systems and digital twins:

- EN ISO/IEC 23053:2023 — Framework for AI systems using ML, applied to V.nod's SoC, SoH, and anomaly-detection components.
- EN ISO/IEC 25059:2024 (and the upcoming prEN ISO/IEC 25059) — Quality model for AI systems, guiding accuracy, robustness, and explainability criteria.
- ISO/IEC 42001:2023 — AI management system, informing model lifecycle governance, validation gates, and version control.
- ISO 23247 — Digital Twin Framework for Manufacturing, whose layered reference architecture is reflected in the edge-cloud structure above.

Together they position V.nod for future qualification, audit, and certification.

### What changes for UAV engineering teams

This battery-centric approach changes the role of the digital twin. Instead of being a visual or mathematical copy of the UAV, it becomes a qualification workflow. It can answer practical questions: Is this battery safe for this mission? Can this supplier be trusted? How much reserve is left under today's load profile? Has the pack aged beyond its approved envelope?

It also reduces repetition in testing. Engineers do not need to discover the same failure mode in flight. They can replay it, emulate it, and qualify against it before the mission. For defence and emergency operations, this is the difference between a useful simulation and a mission-assurance tool.

### Conclusion: From Simulation to Qualification

UAV digital twins become credible only when they include the subsystem that most directly limits endurance and mission safety — the battery. Validation, mission-profile replay, hardware-coupled emulation, and AI-based analytics turn the twin from a simulation aid into a tool that verifies whether the UAV has the power-system capability to fly its mission.

Logiicdev is now scaling V.nod from prototype to qualified product and is actively seeking investors and industrial partners across the DACH region to accelerate this stage. We welcome conversations with stakeholders in defence, public-safety, and industrial UAV operations who share our focus on mission-critical power-system reliability.

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# How to design a PCB Layout for highest Half-Bridge GaN Driver Performance

*This article highlights effective design practices for gallium nitride half-bridge converters driven by a 100 V half-bridge GaN driver, focusing on reducing voltage ringing and enhancing thermal performance. This GaN driver is utilized to optimize the performance of GaN FETs by leveraging their advantages and providing robust overvoltage protection.*

*By Peter Pham, Senior Applications Engineer, Analog Devices,  
and Sam Jafari, Applications Engineer, Analog Devices*

In recent years, gallium nitride technology has significantly transformed the semiconductor industry due to its advantages over traditional silicon MOSFETs, including reduced parasitic capacitance, the absence of a body diode, superior thermal efficiency, and a compact footprint.<sup>1</sup> GaN devices have become increasingly reliable and capable of operating across a broad voltage range. They are now widely adopted to boost efficiency and power density in applications from consumer electronics to automotive power systems.

GaN devices require specialized drivers as they have many distinguishing electrical characteristics, such as low gate voltage limit and high reverse conduction loss during dead time. Due to performance issues and potential device damage, conventional silicon MOSFET drivers are not advised to drive GaN FETs without additional protection circuitries. Despite a growing market for GaN FETs, dedicated GaN drivers remain limited.

Recently, Analog Devices has developed its first 100 V half-bridge GaN driver, the LT8418. This driver offers robust current sourcing and sinking capabilities and features an intelligent, integrated bootstrap switch to maintain a stable bootstrap voltage with minimal dropout from VCC. Furthermore, the device has split gate drivers, which enable fine control over the turn-on and turn-off slew rates, reducing ringing and optimizing electromagnetic interference (EMI) performance. These features make this IC well-suited for demanding applications, including Class-D amplifiers, high efficiency data center power supplies, high frequency DC/DC converters, and motor drives.

However, GaN-based converters operating at high switching speed are particularly sensitive to ringing due to board parasitic elements. Overshooting or undershooting voltage can damage the FET if it exceeds the absolute maximum threshold. Therefore, it is essential to leverage optimal design practices in GaN applications with this device to increase efficiency and improve performance.

## Mitigate parasitic inductance

A rapid change in current during switching events causes parasitic inductance inherent in the PCB layout to resonate with stray capacitance, leading to ringing at various nodes in the converter. At a fast switching speed, the ringing is more pronounced due to the fast di/dt transient. In the half-bridge configuration, the primary contributors to this parasitic inductance are the power loop and gate loop, as shown in Figure 1.

The power loop inductance consists of the FET drain inductance  $L_D$ , the common-source inductance  $L_{CS}$ , and parasitic inductance from input capacitors and PCB traces. The gate loop inductance includes the gate inductance  $L_{GATE}$  and common-source inductance  $L_{CS}$ .

Figure 2 and Figure 3 demonstrate the impact of parasitic inductance, showing more ringing on the switch node voltage and gate signal. This ringing at the switch node increases the switching loss and deteriorates the EMI performance. Meanwhile, the ringing on the gate signal can exceed the gate voltage threshold and absolute rating, resulting in a false turn-on/turn-off of the FET and permanent damage to the gate. Therefore, it is critical to minimize the parasitic inductance in a GaN converter to ensure robust operation.

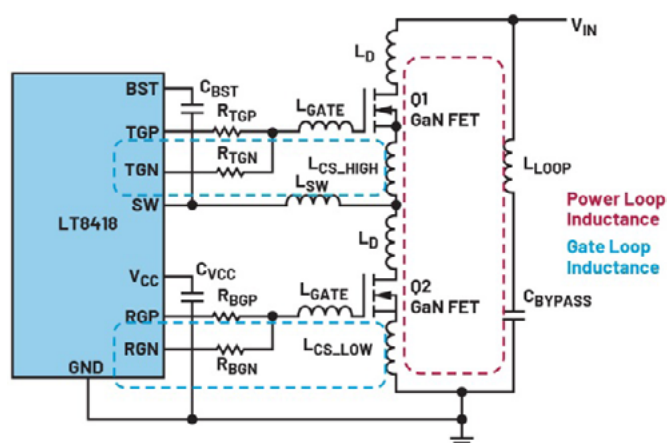


Figure 1: Common parasitic inductance sources in a half-bridge configuration.

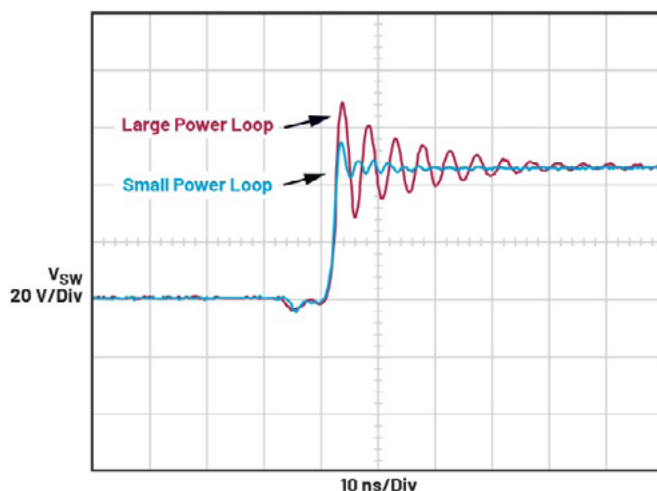


Figure 2: Ringing on the switch node voltage due to hot loop parasitic inductance.

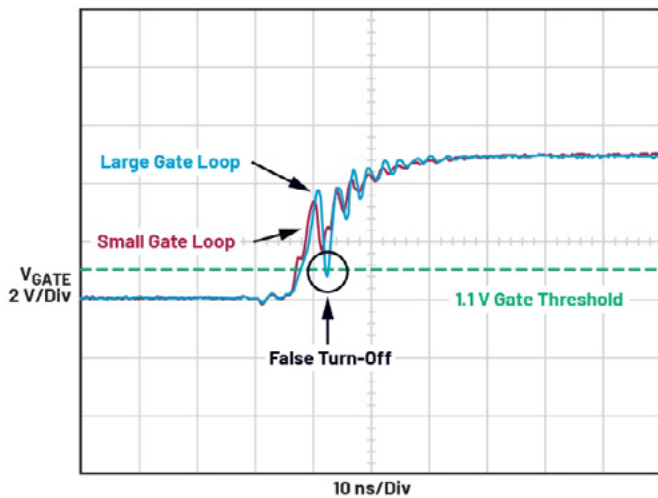


Figure 3: Ringing on the gate signal due to gate loop parasitic inductance.

#### Internal vertical layout minimizes hot loop inductance

Minimizing the hot loop inductance in a buck or boost is essential to mitigate the inductive effect and associated voltage spikes during fast  $dv/dt$  transitions, resulting in improved efficiency and enhanced EMI performance. The hot loop layout defined by the position of GaN FETs and hot loop capacitors is crucial as it determines the physical dimensions of the hot loop and, consequently, its inductance. The internal vertical layout illustrated in Figure 4 is recommended for minimal hot loop inductance.<sup>2</sup>

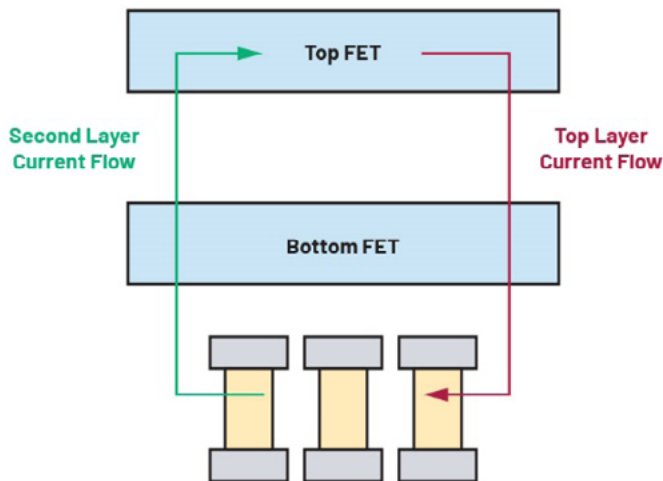


Figure 4: Optimal layout—internal vertical with FETs and hot loop capacitors on the same layer.

In this layout, the high-side and low-side FETs are placed side by side on the same PCB layer. The parallel placement minimizes the length of interconnecting traces. Multiple hot loop capacitors (ceramic capacitors with low equivalent series resistance, ESR) are also placed on the same layer and directly adjacent to the FETs' source and drain terminals. This layout utilizes the first internal layer as the power loop return path, which is in close proximity to the forward path on the top layer, resulting in the minimal hot loop's physical size. It also ensures that the hot loop stray inductance is independent of the total board thickness. Moreover, the induced magnetic fields of the forward and return currents cancel each other out, further reducing the parasitic inductance.<sup>2</sup>

#### Hot Loop Capacitor Position for Optimal Thermal Performance

Due to their compact size and limited contact area, GaN devices can experience extreme thermal stress at high switching frequencies and high loads. Therefore, effective thermal management practices are essential when designing the PCB layout to ensure reliable performance.

In a buck converter configuration, the top FET typically experiences the highest temperature due to the losses from hard switching. To enhance heat dissipation, it is recommended to position high frequency hot loop capacitors closer to the bottom FET. This placement not only optimizes the electrical path for the high frequency loop but also provides additional space around the top FET, allowing for improved thermal dissipation. In this layout, the power plane on the first internal layer, underneath Q1 and Q2, is  $V_{IN}$ . The top layer of this layout strategy is shown in Figure 5a.

In contrast, for a boost configuration, the bottom FET usually undergoes higher thermal stress due to hard switching. Consequently, the high frequency hot loop capacitors should be located near the top FET, leaving room around the bottom FET to improve its thermal dissipation. The return ground plane is on the second layer. This layout is depicted in Figure 5b.

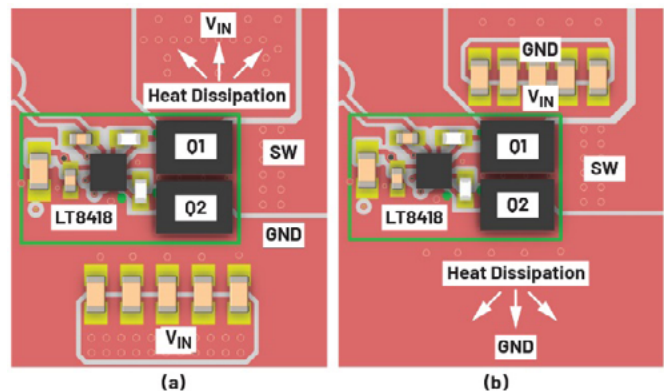


Figure 5: Hot loop capacitor placement for thermal dissipation improvement in buck and boost: (a) Buck layout with capacitors near bottom FET; (b) Boost layout with capacitors near top FET.

#### Vias are tiny but useful

Placing multiple interlayer connection vias directly on the FET's solder pads helps reduce the hot loop parasitic inductance further, as shown in Figure 6. Current flows through these vias in opposite directions due to the interleaving drain and source terminals, forming multiple opposing adjacent magnetic field loops. These magnetic loops lead to magnetic field self-cancellation, significantly reducing the parasitic inductance in the hot loop.<sup>2</sup>

In addition, these vias are used to effectively enhance thermal performance. They transfer the thermal energy from the FET to copper planes on other PCB layers. This helps maintain the device's thermal integrity during high power operation. The vias also distribute the current across multiple PCB layers and minimize resistance. It is advised to fill these vias to prevent outgassing during soldering, as well as solder leakage, and increase both thermal and electrical conduction.

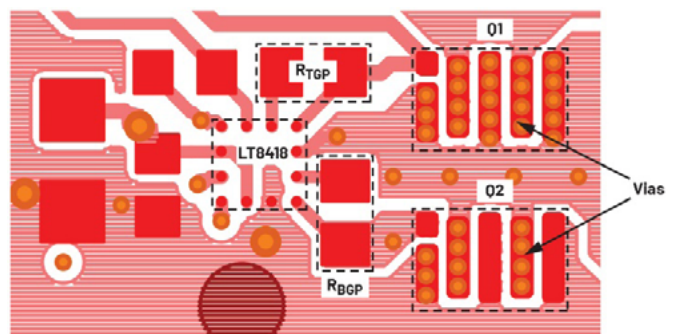


Figure 6: Vias were placed on the solder pads of GaN devices for thermal and electrical conductivity improvement.



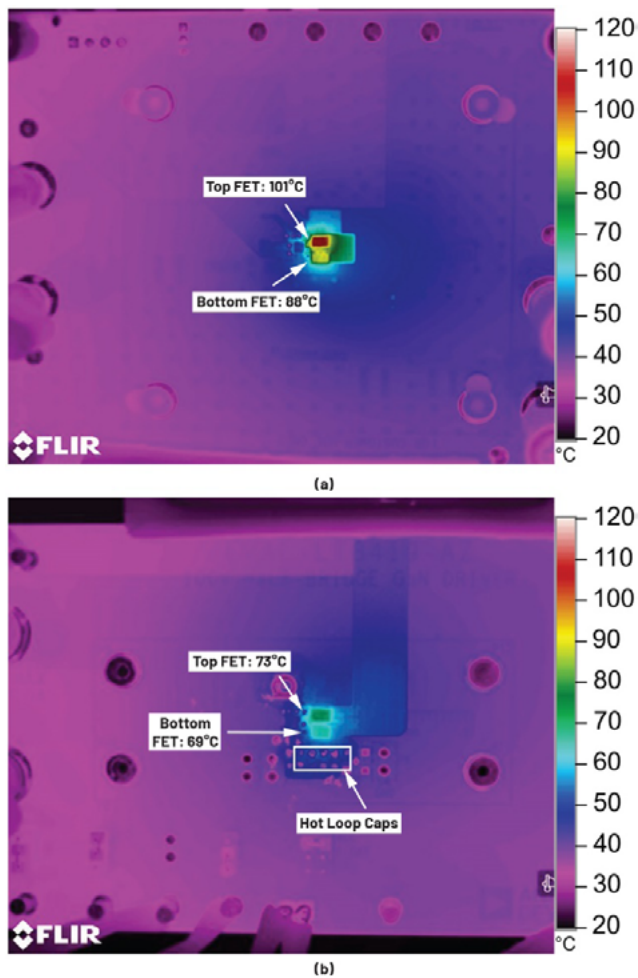


Figure 7: Thermal comparison at  $V_{IN} = 48\text{ V}$ ,  $V_{OUT} = 12\text{ V}$ ,  $I_{OUT} = 10\text{ A}$ ,  $F_{SW} = 500\text{ kHz}$ . Proposed design practices help reduce FET temperature by almost  $30^\circ\text{C}$ : (a) Layout with poor design practices – high FET temperatures; (b) Layout with proposed design practices – cool FET temperatures.

Figure 7 compares the thermal differences between two GaN-based buck circuit boards driven by the LT8418. Under identical operating conditions, the GaN FETs on the board designed with the recommended layout practices remain significantly cooler (up to  $28^\circ\text{C}$ ) than those on the counterpart board.

#### Gate resistors are your friend

GaN FETs have inherently lower absolute maximum gate voltage ratings, commonly around  $6\text{ V}$ , compared to silicon (Si) MOSFETs.<sup>3</sup> Consequently, conventional Si MOSFET drivers are not recommended for driving GaN devices as they are designed for higher gate voltage. Thus, care must be taken when designing GaN converters to prevent damage due to voltage spikes or ringing on the gate.

Switching GaN FETs at excessively high speeds can result in significant voltage overshoot and oscillation at the switch node. As mentioned, this is primarily caused by parasitic inductances and capacitances within the circuit. Moreover, the coupling between the switch node and the gate can induce unintended oscillations, potentially triggering false turn-on events in the FET. Such inadvertent turn-on can lead to shoot-through conditions, where both high-side and low-side FETs conduct simultaneously, causing excessive current flow. This phenomenon not only degrades system efficiency but also poses a serious risk of thermal over-stress and permanent damage to the FETs. Mitigating this issue by adjusting the gate signal's slew rate is crucial for ensuring the reliability and longevity of the circuit.

The LT8418 is designed to drive GaN devices with a gate voltage ranging from  $3.85\text{ V}$  to  $5.5\text{ V}$ , allowing a good safety margin at the gate. The GaN FET should be placed as close to the IC as possible to keep the gate trace short, minimizing the gate inductance. Furthermore, this GaN driver has split gate drives enabling independent adjustment of the turn-on and turn-off slew rate by using gate resistors. This feature enables fine-tuning of switching behavior to match system requirements. Gate resistors are utilized to dampen oscillations in the gate signal by dissipating the energy of high frequency ringing. The gate resistor values should be selected carefully to balance the switching speed, EMI performance, and gate loss.

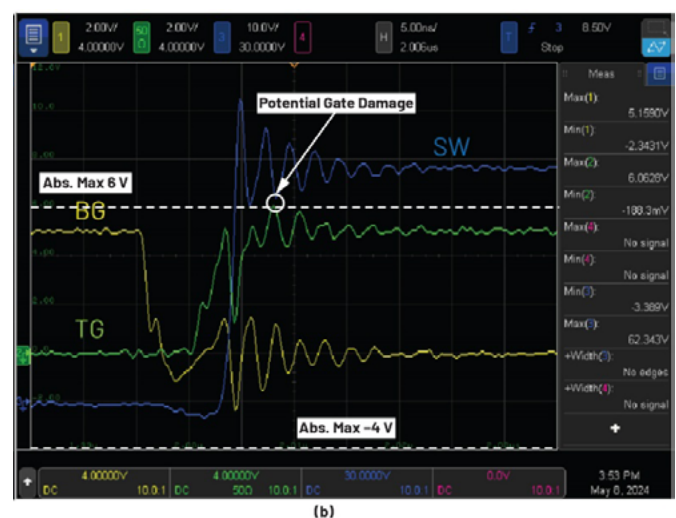
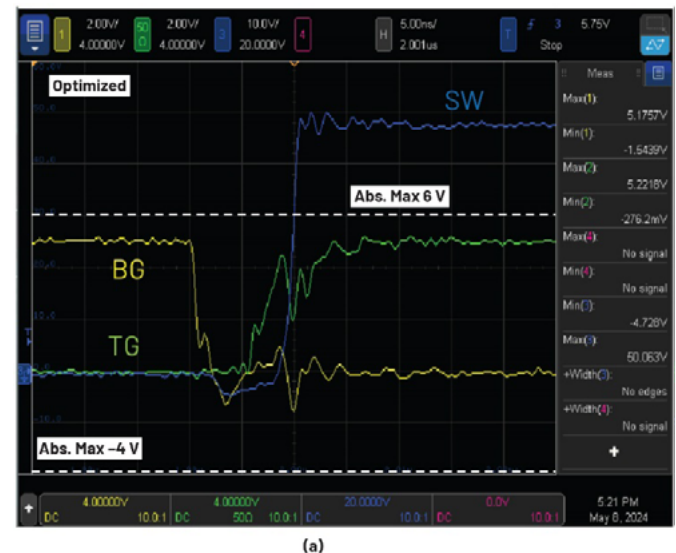


Figure 8: Waveforms of a buck with adequate and inadequate top gate resistor values: (a)  $R_{TGP} = 2\ \Omega$  – Clean waveforms with minimal ringing; (b)  $R_{TGP} = 1\ \Omega$  – Oscillating waveforms exceeding gate max rating.

A good practice for choosing the optimal gate resistor value is to evaluate the gate signal on the bench in the worst-case conditions such as maximum load and highest switching voltage. Begin testing with a higher gate resistor value, such as  $3.3\ \Omega$ , to help dampen any initial ringing and ensure a safe baseline. Reduce the resistance incrementally while monitoring for excessive ringing, overshoot, or undershoot on the gate signal. Ensure the gate voltage waveform has sufficient safety margins below the maximum rated gate voltage and above the threshold voltage. This method optimizes the resistor value for acceptable signal quality and efficiency while maintaining adequate damping.

Figure 8a shows some typical waveforms of a buck with an optimal top gate resistor of  $2\ \Omega$ . The waveforms are clean, with no significant overshoot or ringing. In contrast, Figure 8b highlights the overshoot on the top gate signal exceeding the safe threshold of 6 V because of the inadequate top gate resistor ( $1\ \Omega$ ). This can lead to potential damage to the GaN FET and increased EMI.

#### A bad test point layout can deceive you – be careful

A poorly designed test point layout can introduce parasitic inductance that distorts the observed signals, leading to false readings and potentially misleading conclusions about circuit performance. Thus, a proper test point layout is crucial for measuring accurate gate signals, especially at fast switching speeds.

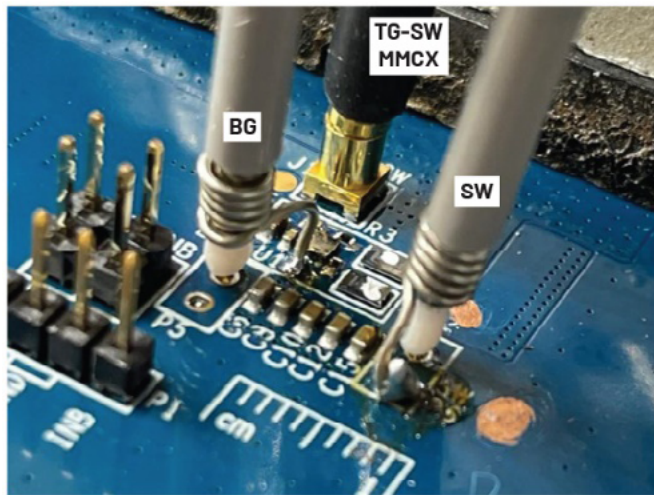
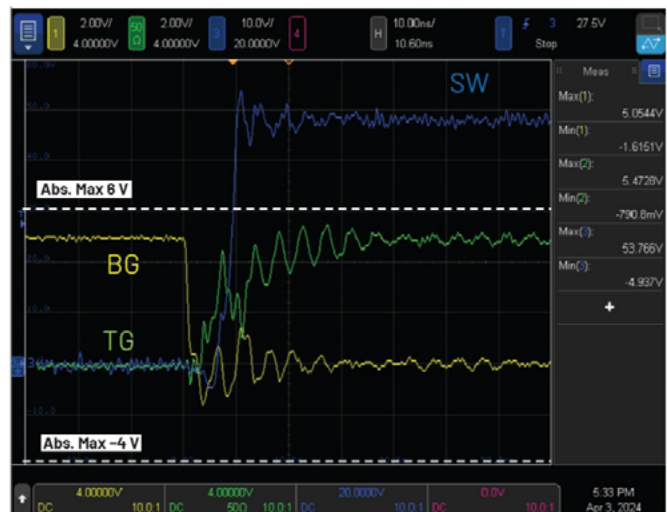


Figure 9: An MMCX connector is recommended for a differential probe when reading gate signals.

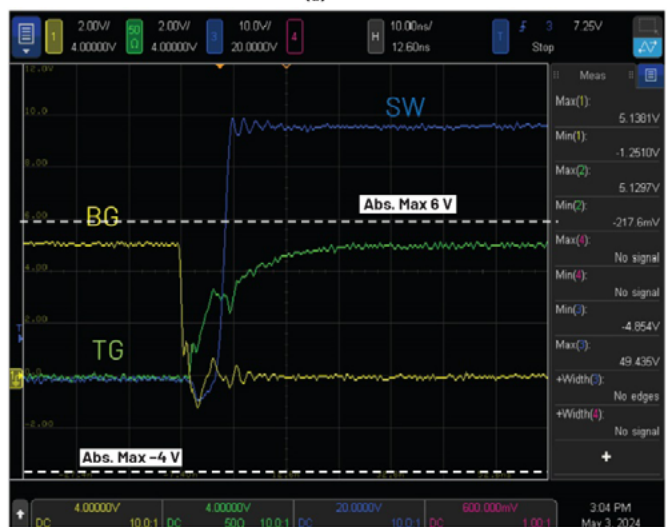
One of the key practices for designing test points is to use the short Kelvin connection. This approach separates the desired reading signal from other noisy signals. It minimizes the impact of shared parasitic elements and ensures the probe measures the true gate signal directly at the FET's terminals.

For measuring the bottom gate and switch node signals, low capacitance passive probes with spring ground leads close to the GaN FET's GND are recommended to minimize the impact of the probe's physical connection. It is more difficult to read the top gate VGS signal as it is referenced to the switch node. A high speed differential probe suits this task. These optical differential probes typically require a dedicated MMCX connector, highlighted in Figure 9, for the best result.

The waveform comparison between an inadequate and proposed test point designs is also demonstrated in Figure 10.



(a)



(b)

Figure 10: Waveform comparison between a bad and a good test point design: (a) false ringing on waveforms induced by a bad test point layout; (b) clean waveforms captured from a good test point layout.

#### Conclusion

Optimized PCB layouts, proper capacitor placement, and fine-tuned gate resistors ensure robust operation, while accurate measurement techniques verify performance. These practices, combined with the device's advanced features, make the LT8418it a good driver for high frequency applications demanding efficiency, compactness, and thermal stability.

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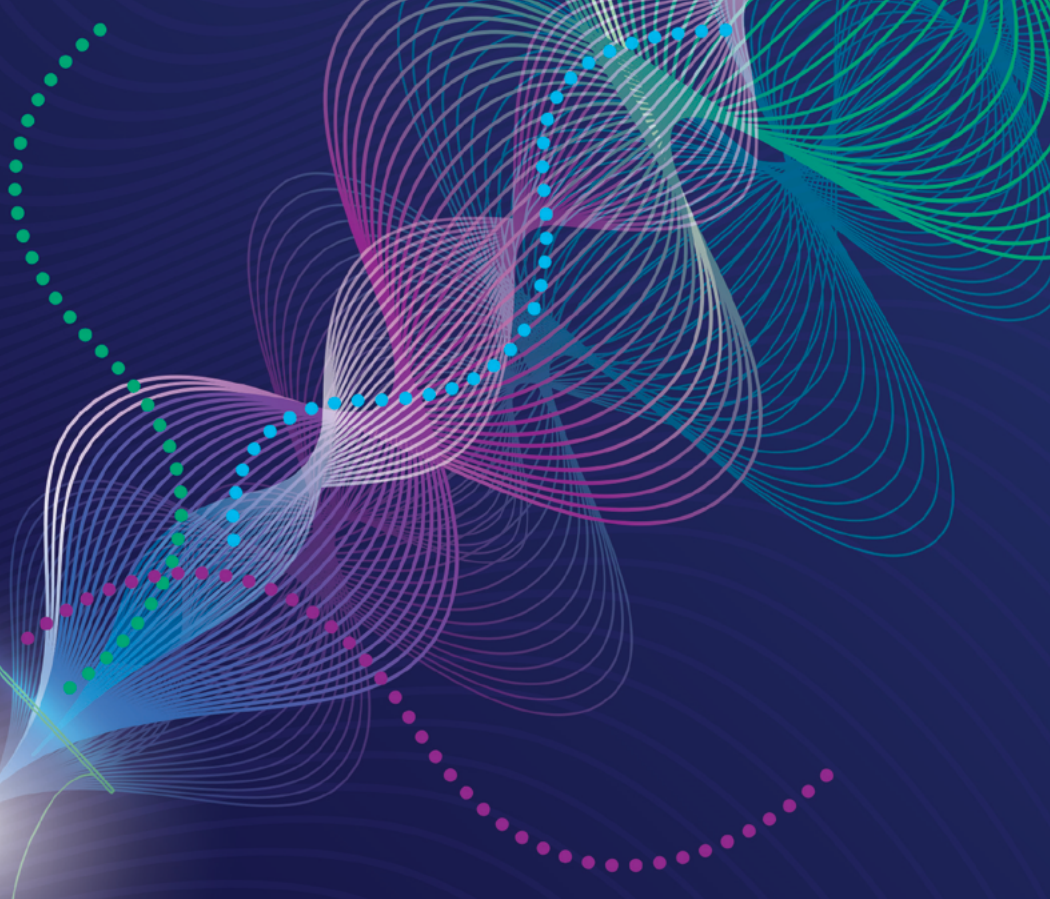
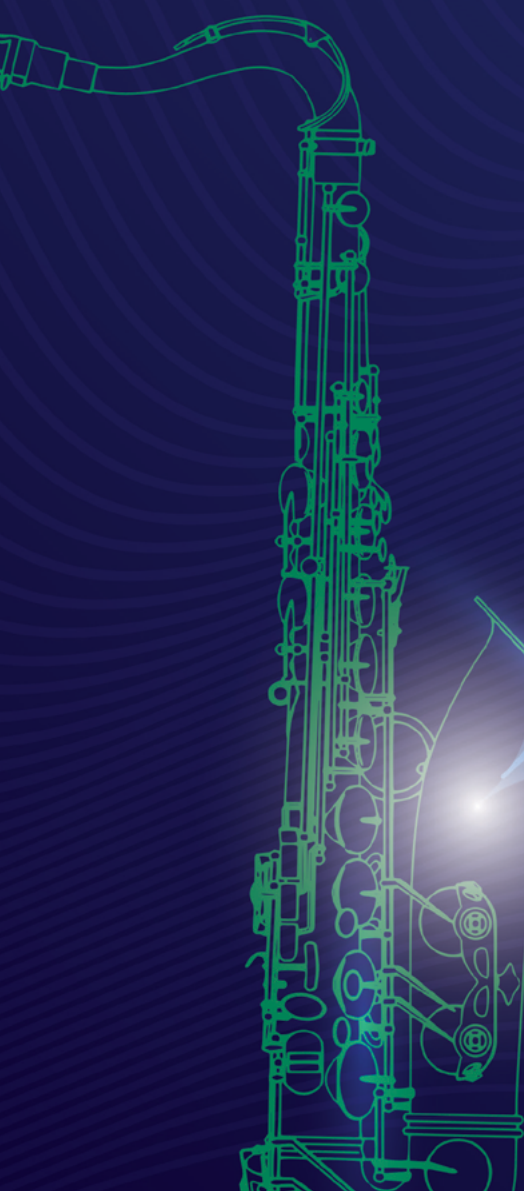
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# High-Power Modules for High-Voltage Energy Systems

Infineon Technologies expands its XHP™ 2 power module portfolio with variants incorporating CoolSiC™ MOSFETs 2300 V, designed for high-voltage power systems. These 2300 V class devices support DC-link voltages of up to 1500 V, addressing the industry trend toward higher system voltages. The modules are available in several variants, offering on-resistance ( $R_{DS(on)}$ ) values ranging from 1 mΩ to 2 mΩ and isolation voltages of 4 kV or 6 kV. By leveraging silicon carbide technology, the devices reduce both switching and conduction losses compared to conventional silicon-based solutions. This enables inverters to achieve higher efficiency and power density, or to operate at higher switching frequencies to reduce harmonics and system size. The



XHP 2 CoolSiC MOSFET modules are well suited for renewable energy applications, including wind, photovoltaic and battery storage systems. Implemented in the XHP 2 package, the modules feature symmetrical switching behavior for direct paralleling

in large power converters and offer a standardized platform that enables developers to balance efficiency and performance according to application requirements. All variants integrate Infineon's .XT interconnection technology, focusing reliability and extended operational lifetime. The modules are also available with a pre-applied thermal interface material, simplifying assembly while supporting consistent thermal performance. These characteristics translate into measurable system-level benefits. In a wind power demonstration system, a power density of 300 kW/l was achieved, while tests in battery storage systems showed semiconductor losses of less than 0.7 percent of the output power.

[www.infineon.com](http://www.infineon.com)

## 3.3 kV Power Modules to Enable Solid-State Transformers for AI Data Centers

Microchip Technology presented its 3.3 kV HV-D3 mSiC® Power Modules, designed to simplify and accelerate the adoption of solid-state transformers (SSTs) in AI hyperscale data centers and other high-voltage power applications. These modules integrate 3.3 kV silicon carbide (SiC) mSiC MOSFETs and Schottky diodes in an industry-standard 62 mm package, enabling efficient power delivery from the medium-voltage grid directly to the server rack. As AI data centers continue to scale, token generation is limited by power availability, while efficiency is a defining factor for return on investment. Microchip's HV-D3 mSiC modules are engineered specifically to meet these requirements. The modules use Microchip's mSiC MOSFET technology, which offers a good  $R_{DS(on)}$  stability over temperature, with packaging that supports 6 kV isolation, incorporates CTI 600-rated materials and features extended creepage distances, designed to allow safe series connection for high-voltage operation. A silicon nitride ( $Si_3N_4$ ) substrate delivers the thermal conductivity and power-cycling capability needed. The HV-D3 mSiC power modules are available in half-bridge and common-source configurations, with and without anti-parallel Schottky diodes, addressing

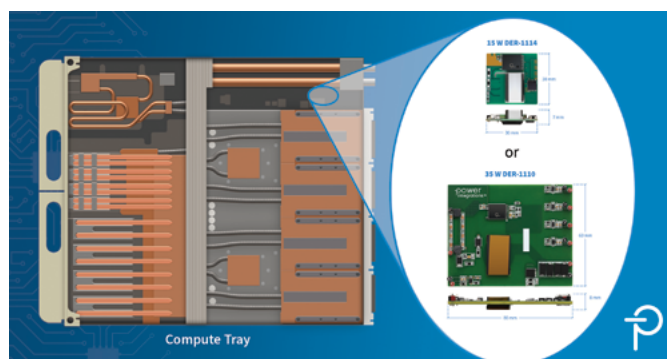


applications in the 100-300 A range. While optimized for solid-state transformers in AI data centers, these modules also address applications like megawatt charging infrastructure for heavy-duty vehicles, auxiliary power supplies for rail/heavy transportation, medium-voltage motor drives, industrial and defense power systems.

[www.microchip.com](http://www.microchip.com)

## Slim Auxiliary PSU Reference Designs for NVIDIA Kyber 800 V<sub>DC</sub> AI Data Center

Power Integrations introduced two slim, compact auxiliary power supply reference designs for 800 V<sub>DC</sub> AI data centers. The single-output, 15 W design is 30 mm by 30 mm with a 7 mm profile, while the isolated, six-rail, 35 W design measures 80 mm by 60 mm with



an 8 mm profile. Optimized specifically for the NVIDIA Kyber liquid-cooled, blade-rack architecture, these ultra-compact solutions free up approximately 30 percent space on densely packed main power distribution boards (PDBs) with an estimated 30 percent reduction in the BOM count - streamlining design and improving overall reliability. These designs are highly efficient with at least 88 percent efficiency across line and load.

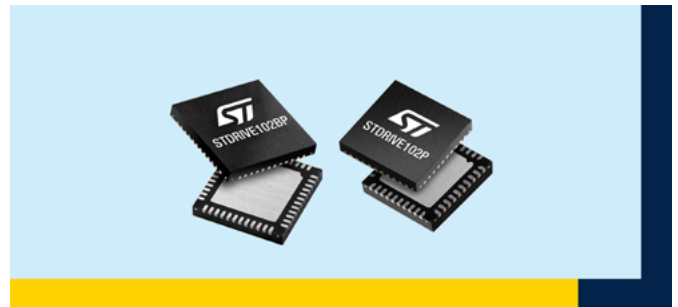
The newly published design example reports describe 35 W and 15 W flyback auxiliary power supplies for high-voltage AI data center applications. Both designs are based on Power Integrations' InnoMux™-2 ICs with 1700 V PowiGaN™ GaN technology. The 1700 V-rated InnoMux-2 IC supports 1000 V<sub>DC</sub> nominal input voltage in a flyback configuration and can deliver flat efficiency of 90 percent in discontinuous conduction mode (DCM) while maximizing power delivery.

[www.power.com](http://www.power.com)



## Gate Driver ICs for three-phase brushless Motors

STMicroelectronics has introduced additional STDRIVE102 gate-driver ICs for three-phase brushless motors, adding the STDRIVE102P and STDRIVE102BP that feature an SPI interface to simplify configuring the gate current and other settings. Designed for supply voltages from 6 V to 50 V, the STDRIVE102 series enables energy efficiency in battery-operated equipment such as power tools and domestic appliances. Able to drive six external N-channel power MOSFETs, the drivers can be programmed to source up to 1 A and sink up to 2 A and provide slew-rate regulation without external resistors. A standby current of 50 nA typ. helps maximize battery life in portable and battery-powered applications. STDRIVE102 components integrate an advanced charge pump. Integrated 12 V and 3.3 V linear regulators (LDOs) power the internal low-side drivers and embedded analog front-end (AFE), and can also be used to supply external components. The STDRIVE102BP includes a configurable AFE with three programmable-gain amplifiers (PGAs) and three comparators for measuring the motor shunt currents. The PGAs and comparators can be enabled and disabled individually, or the



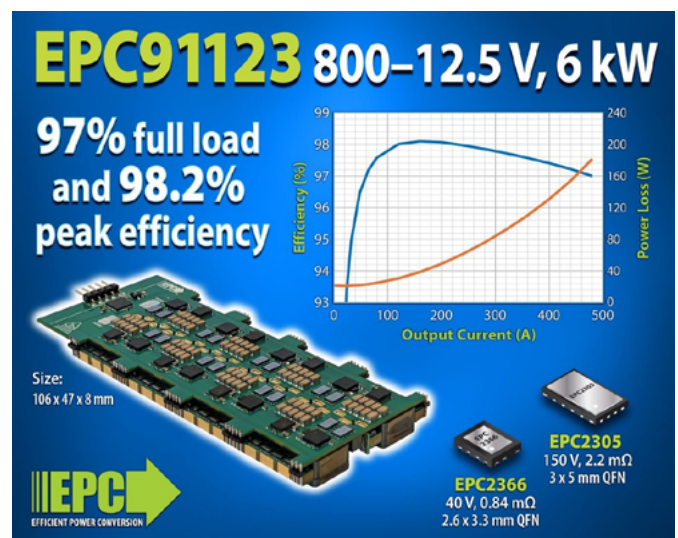
entire AFE can be disabled to save energy. The STDRIVE102P has a simplified AFE with one PGA and one comparator. All STDRIVE102 devices are equipped with a comprehensive set of embedded protection features, including undervoltage lockout (UVLO) to ensure gate drivers operate safely and thermal shutdown. Evaluation boards are available.

[www.st.com](http://www.st.com)

## 800 V-to-12.5 V Power Conversion for AI Infrastructure built on NVIDIA MGX™

Efficient Power Conversion (EPC) has provided details on its EPC91123 evaluation board, an 800 V<sub>DC</sub> to 12.5 V<sub>DC</sub>, 6 kW isolated converter designed to support next-generation AI data center power architectures. As a contributor to the NVIDIA MGX™ AI Factory ecosystem, EPC contributes GaN-based power conversion solutions designed to support emerging 800 V<sub>DC</sub> server architectures, enabling higher power density, improved efficiency, and scalable rack-level power delivery for next-generation AI infrastructure. By enabling direct 12.5 V conversion and eliminating the need for a 48 V intermediate stage, the solution improves overall system efficiency by 1–2 %. The converter is built on an input-series, output-parallel (ISOP) LLC topology and leverages Gen7 devices, including the 3.3 mm × 2.6 mm, 40 V, 0.8 mΩ EPC2366 and 150 V, 2.2 mΩ EPC2305. The solution achieves 98.2 % peak efficiency and 97 % full-load efficiency. Optimized for space-constrained AI server environments, the board delivers high power density in a compact 104 mm × 47 mm × 8 mm form factor.

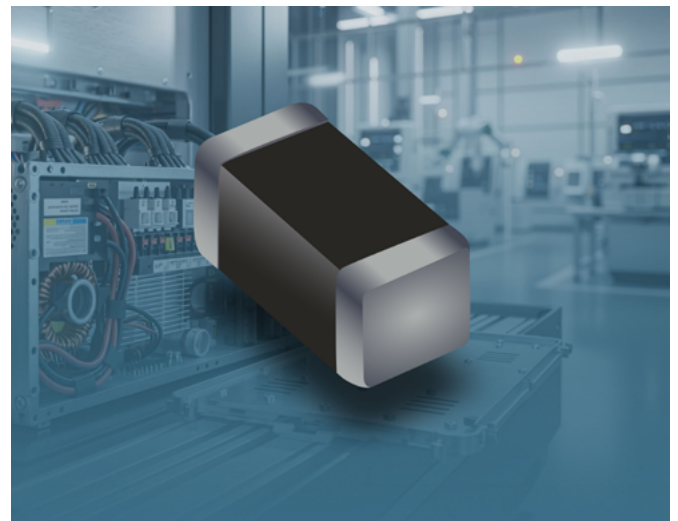
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## High Current Chip Ferrite Beads for EMI Suppression in High Density Power

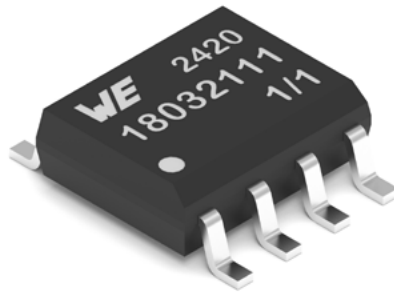
Bourns announced the MH3261 T Series High Current Chip Ferrite Beads, designed to address EMI suppression challenges in high density PCB layouts where current capacity and board space are constrained. The series combines a 3.2 mm × 1.6 mm footprint with a rated current capability up to 11 A, enabling noise suppression without introducing excessive power loss. These characteristics support stable performance in space limited designs. As power densities increase and PCB assemblies become more compact, designers face tighter limits on allowable insertion loss while maintaining effective high frequency noise suppression. Ferrite beads used in these environments must carry higher currents without thermal overstress or impedance degradation. The MH3261 T Series addresses these constraints by pairing low DCR with a wide impedance range, supporting EMI control in dense layouts while operating across a broad temperature range from -55 °C to +125 °C. Its DC resistance is 0.0025 Ω, while the impedance range values from 30 Ω to 1000 Ω at 100 MHz.

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## Isolators for Galvanic Isolation of Digital Signals

Würth Elektronik is expanding its range of digital isolators (WPME-CDIS & WPME-CDIP) with 2-channel bidirectional isolators for I<sup>2</sup>C communication interfaces. WPME-CDI2C enables bidirectional data transmission at up to 2 MHz, making the isolator suitable for most I<sup>2</sup>C communication applications. The SOIC-8NB package is pin-compatible with common standard I<sup>2</sup>C isolators on the market. The WPME-CDI2C isolator – designed for bidirectional I<sup>2</sup>C interface applications with data rates of up to 2 MHz – offers an isolation voltage of up to 3750

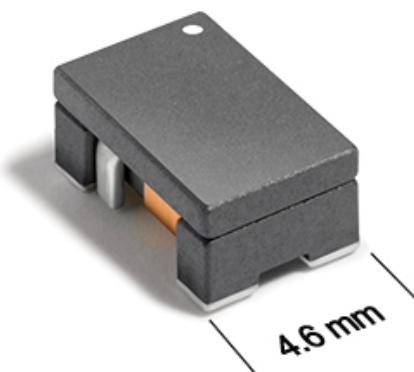


V<sub>RMS</sub> in accordance with UL 1577 and a basic insulation rating in accordance with IEC 60747-17 (VDE 0884-17). It offers high immunity to system noise, with a common-mode transient immunity (CMTI) of ±150 kV/μs. The device is available from stock in two variants: One features a bidirectional serial data line (SDA) and a bidirectional serial clock line (SCL). The other features a bidirectional serial data line (SDA) and a unidirectional serial clock line (SCL).

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## SMT Current Sense Transformers

The CSX7030 series from Coilcraft is a high-isolation, low-loss current sensing transformer designed for high-performance power electronics and automotive applications. It features a chip-style package with a low 3.3 mm profile and is manufactured using a highly automated process to ensure consistent quality and cost efficiency. With a low DCR of 0.52 mΩ on the primary and 1.87 to 34.08 Ω on the secondary side, the series reduces conduction losses and self-heating, making it well-suited for high-current applications up to 20 A. A range of turns



ratios from 1:50 to 1:200 provides design flexibility, while bandwidth up to and beyond 1 MHz enables accurate high-frequency current measurement in fast-switching systems such as DC/DC converters, motor drives, inverters, and power management circuits. The CSX7030 is AEC-Q200 qualified, making it suitable for demanding automotive applications. It is specified for isolation voltages of 1000 V<sub>RMS</sub> and currents of 20 A with terminating resistances between 2.5 and 10.0 Ω.

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[www.pcimasia-shenzhen.com](http://www.pcimasia-shenzhen.com)



# Simulator for Rapid Power Electronics Circuit Verification

ROHM has released the ROHM PLECS® Simulator on its website. This simulation tool enables designers of power electronics circuits and system designers to rapidly simulate the operation of ROHM's power devices online. The tool is based on the PLECS simulation

software. The ROHM PLECS Simulator specializes in loss and thermal calculations. This allows users to simulate power loss and temperature rise in a matter of seconds to minutes by selecting a power electronics circuit topology from a list on the website and choosing from the various power devices offered by ROHM. This reduces the time and effort required for optimal device selection during the early stages of circuit design. Twenty different topologies are already available, and ROHM plans to expand the range of device models and topologies in the future, including SiC devices, IGBTs and power modules. It is possible to perform end-to-end simulation, ranging from design loss and thermal verification to waveform checking.



[www.rohm.com](http://www.rohm.com)

# 80 V N-channel MOSFET support 48 V Automotive Systems

Toshiba Electronics Europe introduced two AEC-Q101 compliant 80 V N-channel MOSFETs supporting 48 V automotive systems. The XPH2R608QB and XPH3R908QB are the first products from the latest-generation U-MOSX-H process to be housed in the SOP Advance (WF) package with wettable flanks. The  $R_{DS(ON)}$  for the XPH2R608QB is 2.55 m $\Omega$  (max.) with a total gate charge ( $Q_g$ ) of 95 nC (typ.), and 3.9 m $\Omega$  (max.) and 63 nC (typ.) for the XPH3R908QB – both with a gate-to-source voltage ( $V_{GS}$ ) of 10 V (max.). Additionally, the SOP WF package with a copper connector structure reduces MOSFET package resistance, improving efficiency, enhancing heat dissipation, and increasing system reliability. The wettable flank design of the package enhances the visibility of solder fillets, making it easier to verify board mounting conditions using automated optical inspection (AOI) equipment, improving overall system reliability. The XPH2R608QB and XPH3R908QB are suitable for use in N-channel type brushless DC motor drive and non-isolated DC/DC



buck converter circuits. In addition to 28 V automotive systems, other applications include motor drives, switching power supplies, and load switches.

[www.toshiba.semicon-storage.com](http://www.toshiba.semicon-storage.com)

# SMD Fuse for High-Current 48 V<sub>DC</sub> AI Data Center Protection



Littelfuse announced the NANO2® Surface-Mount 708 Series Fuse, a surface-mount fuse offering a 14,000 A interrupting rating at 80 V<sub>DC</sub>. Engineered for next-generation 48 V<sub>DC</sub> power architectures, the 708 Series addresses the growing protection demands of AI servers, hyperscale data centers, and high-density power distribution systems. As power levels rise and board space shrinks, designers have been forced to rely on oversized, manually installed through-hole or bolt-down fuses. The 708 Series provides an automation-friendly alternative without compromising performance.

It provides current ratings of 60 A to 200 A in a surface-mount package. The 708 Series is designed as supplemental overcurrent protection for circuits where high fault current is anticipated, including power distribution units (PDUs), power shelves, battery backup units (BBUs), and power supply units (PSUs). It is also suited for AI server clusters, networking equipment, and hyperscale data center infrastructure. Additional applications include renewable energy systems and battery management systems (BMS), where compact, high-power protection solutions are critical.

[www.littelfuse.com](http://www.littelfuse.com)

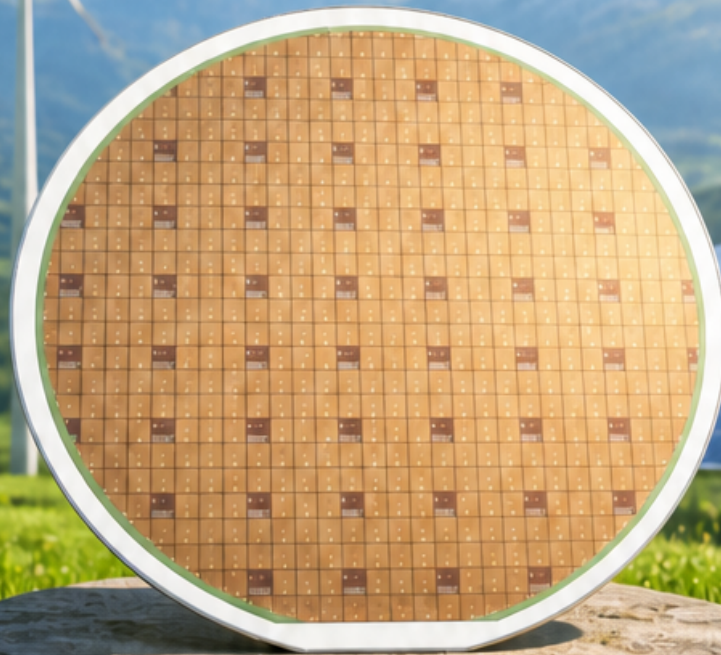
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# Gen 7 Clear Advantage over Best in Class Silicon

| 150 V          | $R_{DS(on)}$<br>(m $\Omega$ ) | $Q_G$<br>(nC) | $Q_{OSS}$<br>(nC) | Package             | Applications                                          |
|----------------|-------------------------------|---------------|-------------------|---------------------|-------------------------------------------------------|
| EPC2376        | 1.4                           | 18.4          | 110               | 3 x 5 dual cool     | 800 V/48 V,<br>400 V/48 V,<br>LLC, BBU, DC-DC         |
| Best Silicon*  | 10                            | 28            | 78                | 5 x 6 dual cool     |                                                       |
| 100 V          | $R_{DS(on)}$<br>(m $\Omega$ ) | $Q_G$<br>(nC) | $Q_{OSS}$<br>(nC) | Package             | Applications                                          |
| EPC2367        | 1.2                           | 17            | 54                | 3.3 x 3.3 dual cool | 800 V/48 V,<br>400 V/48 V,<br>BBU, DC-DC, POL         |
| Best Silicon*  | 6.5                           | 27            | 40                | 3.3 x 3.3 dual cool |                                                       |
| 40 V           | $R_{DS(on)}$<br>(m $\Omega$ ) | $Q_G$<br>(nC) | $Q_{OSS}$<br>(nC) | Package             | Applications                                          |
| EPC2377        | 0.5                           | 26            | 34                | 3.3 x 3.3 dual cool | 800 V/12 V,<br>400 V/6 V,<br>48 V/12 V,<br>DC-DC, POL |
| EPC2366        | 0.84                          | 15            | 22                | 3 x 2.6 dual cool   |                                                       |
| Best Silicon** | 1                             | 20            | 43                | 3.3 x 3.3 dual cool |                                                       |
| 25 V           | $R_{DS(on)}$<br>(m $\Omega$ ) | $Q_G$<br>(nC) | $Q_{OSS}$<br>(nC) | Package             | Applications                                          |
| EPC2378        | 0.41                          | 34            | 26                | 3.3 x 3.3 dual cool | 800 V/6 V,<br>400 V/6 V,<br>48 V/6 V,<br>DC-DC, POL   |
| Best Silicon** | 0.47                          | 32            | 52                | 3.3 x 3.3 dual cool |                                                       |
| 18 V           | $R_{DS(on)}$<br>(m $\Omega$ ) | $Q_G$<br>(nC) | $Q_{OSS}$<br>(nC) | Package             |                                                       |
| EPC2370        | 0.28                          | 26            | 17                | 3.3 x 3.3 dual cool |                                                       |

\*Silicon measured at 8 V<sub>GS</sub>

\*\* Silicon measured at 5 V<sub>GS</sub>



For product details:  
<https://lead.me/EPCPSG>  
[epc-co.com](https://epc-co.com)

