Reducing Size, Noise, and Field Failures of Transportation APUs

Designers are finally able to extract disruptive system-level benefits of SiC technology to shrink the size, noise, and field failures of auxiliary power units (APUs) in transportation vehicles.

By Kevin Speer, Nitesh Satheesh, and Marc Rommerswinkel, Microchip Technology

As vehicle electrification proliferates the consumer EV segment other forms of transportation are also chasing the global macrotrend, including railway, aircraft, delivery trucks, off-highway vehicles, and more. Common across all forms of electrified vehicles are two electrification systems: the traction power unit (TPU), which provides vehicle propulsion; and the auxiliary power unit (APU), which supplies power for all other on-board loads, from lighting and doors to air conditioning and power outlets.

Unlike consumer EVs which put a premium on range-per-charge other transportation use cases may have different priorities addressed through improvements in the APU. Cabin space comes at a premium in light rail, for example, as free space allows more paying passengers. Field reliability is paramount for mining vehicles, where downtime is measured in millions of dollars per day. And across all use cases, passenger comfort is critical in a market served by competitive OEMs targeting choosy buyers.

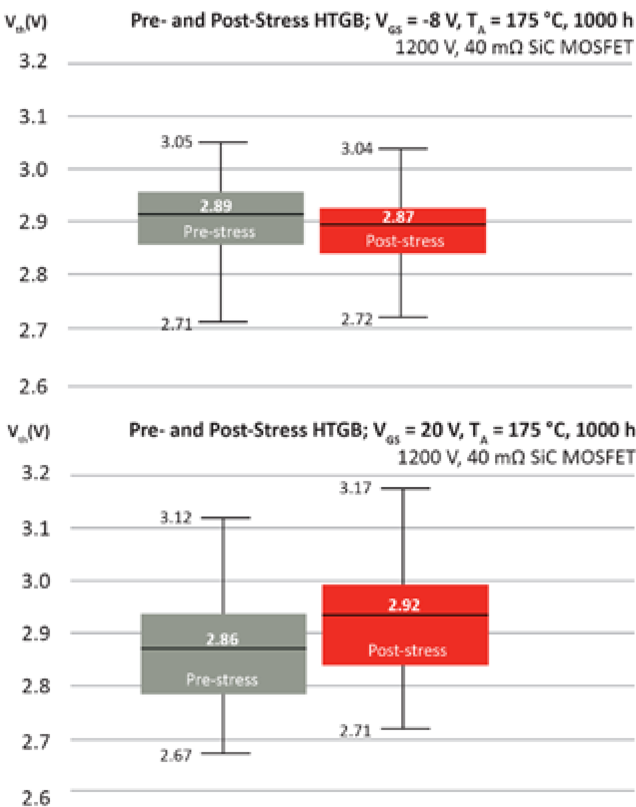

Figure 1: Threshold voltage of production-grade SiC MOSFETs before and after (top) negative and (bottom) positive high-temperature gate bias stress

The high switching losses of silicon IGBTs have blocked transportation APU improvements. By limiting switching frequency, IGBTs fix the minimum size of the APU's largest physical components, the isolation transformer and heatsink. With SiC, one can drastically downsize the isolation transformer by switching at higher frequencies; and with switching losses reduced by 80% or more, heat sinks shrink in turn. In addition, APU switching frequencies can extend beyond the audible range, eliminating the high-pitched whine that is tiresome for passengers. Last, efficiency is essential because the APU is continuously operating, often under light load; the conduction losses of SiC MOSFETs are lower than competing IGBTs under light load conditions.

SiC Up to the Task?

The toughness of the SiC MOSFETs across wide-ranging conditions is essential for APUs that power both convenience and emergency loads. One must verify: 1) the stability of the MOSFET's gate oxide, a known issue for SiC MOSFETs; 2) the lifetime of the gate oxide; 3) the stability of the MOSFET's body diode; and 4) failure toughness measures such as avalanche ruggedness and short circuit survival.

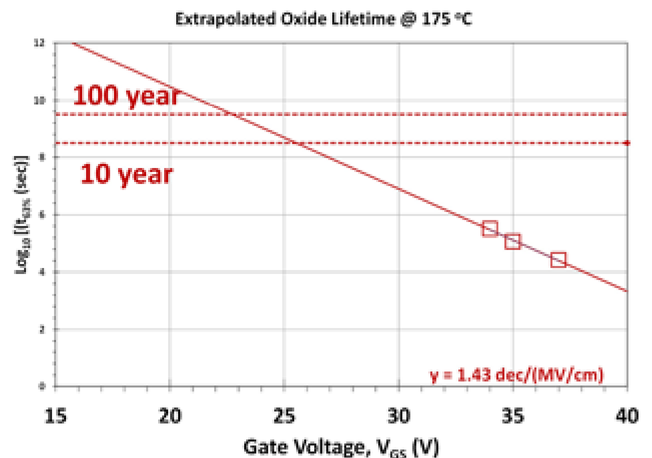

Figure 2: Example of extrapolated oxide lifetime of production-grade SiC MOSFET from Microchip

Gate oxide integrity

Should the threshold voltage shift, device performance changes (e.g., increased on-resistance), leading to erratic system behavior and possible APU failure. Figure 1 shows how Vth data for production-grade SiC MOSFETs should exhibit no meaningful change after 1000 h of stress at 175 C.

One can predict gate oxide lifetime by accelerating samples to failure using elevated temperature and electric field. Activation energy is extracted for each failure mode, and an Arrhenius equation is used

to extrapolate oxide lifetime (see Figure 2). A production-grade SiC MOSFET gate oxide can last well beyond 100 years at high stress, ensuring confidence in routine, reliable APU operation beyond the designed service lifetime.

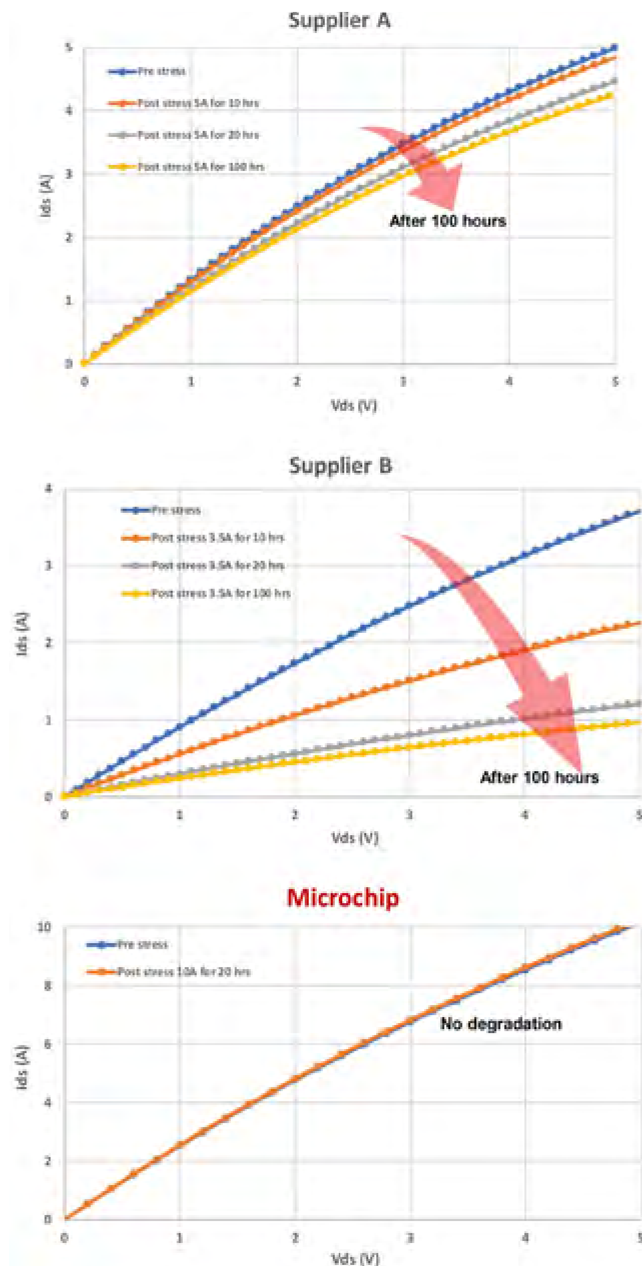

Figure 3: Pre- and post-stress R_{DSon} for commercially available SiC MOSFETs, revealing varying quality of the intrinsic body diode from three suppliers [1]

Body diode stability

Unlike the IGBT, the SiC MOSFET can conduct reverse current using its intrinsic body diode. In some devices, this diode degrades over time, leading to an increased RDS,on and more heat than designed. Figure 3 shows body diode I-V curves and MOSFET ON-state drain–source resistance (RDSon) after many hours of constant forward current stress [1]. Wide variation was seen across suppliers. One supplier had noticeable degradation; another became unusable. Selected devices should show no perceptible shift. Using a SiC MOSFET with stable body diode enhances reliability and cuts cost by eliminating the antiparallel diode.

Field survival: Short circuit and Avalanche

Transportation APUs are susceptible to a variety of fault conditions, demanding SiC MOSFETs designed to safely ride through these events and maintain consistent performance before and after faults.

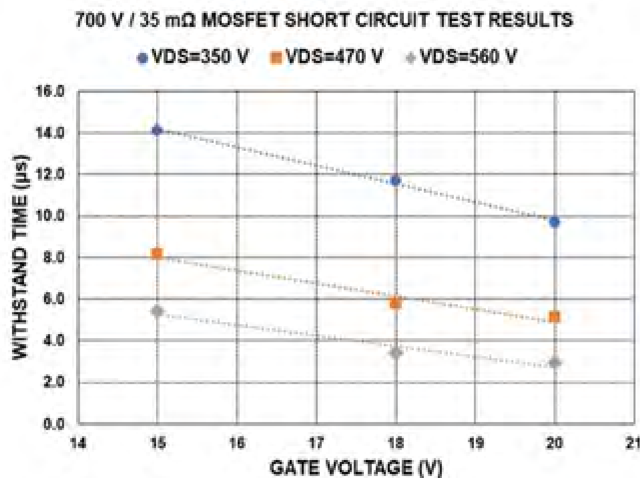

Figure 4: Short circuit withstand time for production-grade SiC MOSFETs from Microchip

Short circuit withstand capability measures the MOSFET's ability to survive an instantaneous short of the dc link across its drain-source terminals. The MOS channels are enhanced, allowing a properly designed device to safely distribute peak currents across the MOSFET die area. Figure 4 shows short circuit withstand times (SCWTs) for production-grade SiC MOSFETs – the Microchip example is between 3 and 14 microseconds, with dependence on dc link voltage and applied VGS. This is sufficient for many commercially available gate drivers. An advanced driver, such as that described in the next section, adds intelligence to short circuit detection.

Avalanche ruggedness is even more demanding: the load current is suddenly dumped into the MOSFET, forcing the drain-source voltage to rise to breakdown. Unlike short circuit, the MOS channels are not enhanced; avalanche current crowds the die edge, rapidly taking the device to its thermal limitations.

Repetitive unclamped inductive switching (R-UIS) is used to evaluate a device's avalanche ruggedness. Figure 5 shows time-dependent dielectric breakdown (TDDB) for commercial SiC MOSFETs before

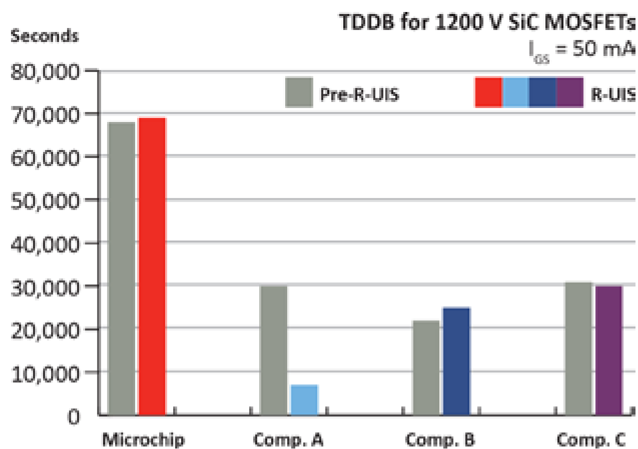

Figure 5: Time-dependent dielectric breakdown before and after repetitive avalanche failure for commercially available SiC MOSFETs from four suppliers

and after 100,000 cycles of R-UIS. Many suppliers maintain oxide strength but the ability to demonstrate up to four times the toughness alongside stability in R_{DSon} and drain-source leakage [2] reinforces the SiC MOSFETs' ability to safely ride through the most demanding electric overstress conditions.

Switch Faster with Low-inductance Packaging

Combined with high edge rates, problematic inductances in a power system cause higher switching losses, excessive overshoot voltages, non-compliant EMI, and potentially, APU failure. The preventative measures designers must take to slow down the MOSFETs' speed may leave them wondering what happened to SiC's value proposition.

Microchip's low-inductance SP6LI package illustrates how these problems can be solved. The phase leg-configured format inserts less than 3 nanohenries of parasitic inductance to the power loop. Internally, layout optimizations have been made to ensure identical timing and current sharing. Thermal performance can be improved with the use of silicon nitride ceramics (aluminum nitride also offered), and baseplate options include copper and AlSiC. Externally, the power terminals allow a low-inductance connection to the dc link and optimal paralleling in two orientations. The SP6LI allows the designer to drive the SiC MOSFETs at higher speeds with maximum efficiency and reduced EMI, shrinking APUs while precluding EMI-related failures.

Gate Drivers Keep APUs on Track

APU performance and reliability can also be optimized using digital programmable gate drivers that enable overshoot voltage and switching losses to be fine-tuned on the fly. This allows designers to reduce APU cost and size with lower-voltage parts and smaller heat sinks – and eliminating hours with a soldering iron and bin of gate resistors.

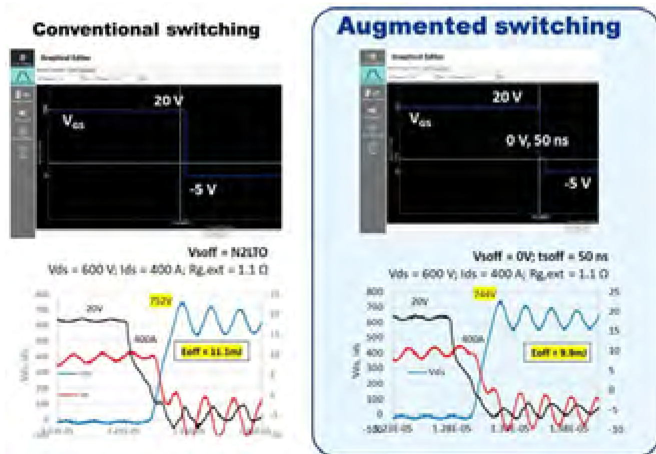

Figure 6: Graphical user interface for programmable AgileSwitch™ gate driver and turn-off waveforms using (left) conventional switching and (right) augmented switching

Figure 7: Demonstration of how augmented switching (right) can reduce peak voltage and peak current during short circuit event compared to conventional switching (left)

The impact of augmented switching may be seen in Figure 6. Unlike conventional turn-off (left), augmented turn-off begins with an on-stage voltage of 20 V, moves to a user-programmed intermediate level for a specified dwell time, and finally to the off-state of -5 V. The effects are modest due to the SP6LI's extraordinarily low inductance; results are published elsewhere showing more pronounced influence [2,3]. In addition, short circuit events are quickly arrested, reducing peak voltage and current by 60% and 10%, respectively (Figure 7).

Total SiC System Solution

Designers wishing to streamline from double-pulse evaluation through volume production will need accelerated development kits that unify all three pieces into the total SiC system solution for transportation APUs: rugged SiC power devices, low-inductance power package and intelligent gate driver. Figure 8 shows how Microchip's solution may be dropped into an APU circuit.

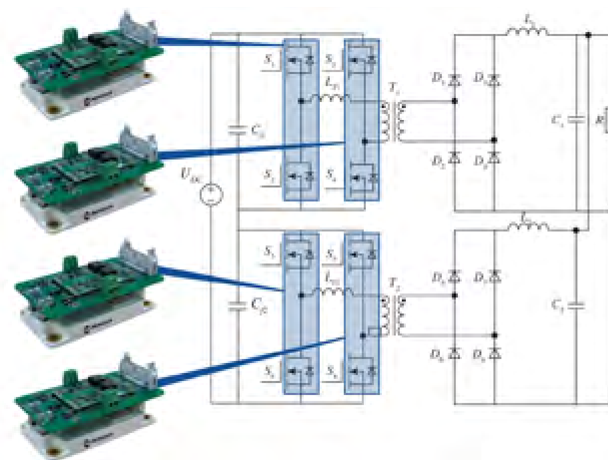

Figure 8: Proposed phase-shifted full bridge implementation of the Microchip ASDAK+ in the DC-DC section of a transportation APU [4]

Summary

The use of SiC MOSFETs in auxiliary power units for transportation vehicles offers disruptive benefits over silicon IGBTs with respect to the APU's size, weight, efficiency, and noise. However, these benefits may only be realized with high field reliability using rugged SiC MOSFETs, low-inductance packaging, and a gate driver intelligent enough to take control of SiC's agile performance. Designers can now solve the challenges with total SiC system solutions that simultaneously enable a reduction in size, noise, and field failures.

References

[1] Agarwal, A. and Kang, M., private communication, 2020.

[2] Speer, K., Satheesh, N., Kashyap, A., and Bontemps, S., "Streamlined SiC Development With a Total System Solution," IEEE Power Electronics Magazine, Vol. 7, No. 4, pp. 28-35, 2020.

[3] Satheesh, N., Robins, C., and Fender, A., "The State of Intelligent SiC MOSFET Gate Drivers," Bodo's Power Systems, pp. 30-33, February 2018.

[4] Satheesh, N., "Silicon carbide MOSFETs: Handle with care," in Proc. Applied Power Electronics Conference (APEC), San Antonio, Texas, USA, 2018.

[5] Hayashiya, H. and Kondo, K., "Recent Trends in Power Electronics Applications as Solutions in Electric Railways," IEEJ Transactions on Electrical and Electronic Engineering, vol. 15: 632-645, 2020.

www.microchip.com