750V Gen 4 SiC FETs Enable Higher Efficiency Power Designs

Silicon carbide adoption has accelerated dramatically in recent years, thanks to solid technological progress in the quality and performance of components, their availability, and the emergence of applications that benefit from that performance. UnitedSiC has pursued a strategy of continuous technological innovation, to deliver the lowest Rds(on) power components in the 650V-1200V range [1], built on the excellent characteristics and high yields of our proprietary SiC JFET technology.

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With the recent launch of the Gen 4 (G4) UJ4C SiC FET series, we open the next chapter in the expansion of SiC usage in power conversion and inverter applications with a large improvement in device characteristics, aimed at providing users with the next level of performance and system cost benefits.

Comparative characteristics of available technologies
The first UJ4C products from UnitedSiC (see Table 1) target a 750V $V_{DS(MAX)}$ rating instead of 650V, in order to tackle applications using a 500V DC Bus, while serving the traditional 300/400V bus applications. The devices maintain the +/-20V gate rating, built in ESD protection, and the ability to use simple unipolar gate drives enabled by the 5V V_{TH}, that are all features of the SiC FET's cascode architecture. In high frequency applications, gate drives as low as 0 to 10V may be used, with minimal impact on conduction loss. The ultra-low specific on-resistance of this technology (SiC JFET 0.7mohm-cm2) allows about half the resistance in a given package size relative to 650V SiC MOSFETs.

At a given resistance, the chips are shrunk, which leads to much lower capacitances. This in turn leads to lower switching losses. The TO247-3L and 4L packages use Ag sinter technology to enhance thermal resistance in conjunction with chip thinning, to mitigate the effects of the smaller JFET die, and allow excellent junction-to-case thermal resistance R_{THJC} to be achieved. The devices preserve the ability to handle avalanche events and are especially good at handling lower energy high current avalanche events up to 2X rated current. Excellent third quadrant behavior with low V_{FSD} (<1.5V) and low temperature independent Q_{RR} is another feature of SiC FETs, and G4 devices have much reduced Q_{RR} than their earlier G3 counterparts, driven by the C_{OSS} reduction.

In Table 2, we compare technological parameters for state of the art SiC MOSFETs, Superjuncton devices and G4 SiC FETs. The rows showing R_{DSA} indicates the resistance mohm-cm^2 of active chip area at 25C and 125C. This is resistance of the JFET used to construct the cascode SiC FET, and the additional resistance of the LVMOS may add 10% to this number. The 5V V_{TH} of the G4 SiC FET in conjunction with the 0 to 12V gate drive is unique and delivers the best available Qg.V figure-of-merit for gate drive loss. Operating these devices at 500kHz-1MHz can be accomplished without overheating standard gate drivers.

The cascode construction allows for the lowest available V_{FSD} body diode drop of all the wide-band-gap options, allowing the use of these devices in non-synchronous rectification mode. Since the reverse recovery performance Q_{RR} is also excellent, the overall figure-of-merit V_F*Q_{RR} is unmatched for G4 SiC FETs. This allows for excellent hard switching performance and prevents device failures in ZVS circuits if hard switching occurs under any load conditions. The figures of merit R_{DS}*E_{OSS} and R_{DS}*$C_{OSS,TR}$ based on the net cascode resistance are used to assess the fundamental capability of the technology for hard and soft-switching applications and can be seen to be best-in-class. These devices can allow a simpler implementation of higher frequency soft-switched circuits such as LLC, CLLC, DAB and PSFB.

PRODUCT	Irated Tc100	Voltage rating	RDS(on) @25C	RDS(on) @125C	Tj (max)	Rth,j-c (max)	Qg	VFSD @25C	Eoss (400V)	Coss, tr (400V)
UJ4C075018K3S UJ4C075018K4S	60A	750V	18mΩ	31mΩ	175C	0.3C/W	38nC	1.2V	12uJ	280pF
UJ4C075060K3S UJ4C075060K4S	21A	750V	58mΩ	106mΩ	175C	0.75C/W	38nC	1.3V	4uJ	94pF

Table 1: Key parameters of the first Gen 4 SiC FET products

TECHNOLOGY	G4 SiC FET	SiC MOS1	SiC MOS2	SiC MOS3	SJ (fast)
Voltage Rating [V]	750	650	650	650	600
RdsA @25C (mohm-cm2) SiC	0.7	2.1	2.1	2.8	8
RdsA @125C (mohm-cm2) SiC	1.26	2.6	2.6	4.3	14.4
VTH	4.8	4.5	2.3	3.1	3
Preferred Gate drive	0 to 12V	0 to 18V	-4 to 15V	-5 to 18V	0 to 10V
Qg.V (uJ)	0.36	1.13	3.57	3.73	2.51
VFSD(25C) [V] Nominal Current, VgsOff	1.6V(50A)	4V(38.3A)	5.4V(55.8A)	4.3V(50A)	1V
125C Rdson x Eoss [mOhm-uJ]	372	732.6	714	754	826.5
125C Rdson x Coss,tr [mOhm - nF]	8.7	12.1	8.8	13.7	108.2
VF x Qrr [V-uC]	0.17	0.96	2.33	1.59	1.56
Rdson, Nominal	18m	27m	15m	20m	15m

Table 2: Comparison of parameters for G4 750V SiC FETs with similar 650V SiC MOSFETs and 600V Superjunction fast diode FETs

Switching waveforms and managing switching speed

Figure 1 shows the half-bridge switching waveforms of the 60mohm and 18mohm 750V devices in a TO247-4L package measured at 400V, 20A and 50A respectively. Waveforms are shown with comparing a large Rg to control the turn-on and turn-off vs. using a RC snubber across the device with a low Rg at the gate. Both circuits employ a RC snubber from the DC bus to ground, referred to as a bus snubber [2].

The upper row of Figure 1 shows the switching behavior of the 60m, 750V SiC FET UJ4C075018K4S. The difference in turn-on loss using just an Rg=25ohm (171uJ) vs a low Rg of 1ohm along with a 10hm, 95pF drain-source RC snubber (142uJ) is small. The turn-on di/dt is significantly slower with the Rg=25ohm, but the peak recovery current is not much different. The maximum dV/dt during turn-on is similar, since it is set by the SiC JFET, and not altered by the Rg applied to the LV MOSFET in the SiC FET. The turn-on delay is higher with the 25ohm Rg.

The turn-off behavior for the cases using a 20ohm Rgoff (37uJ), vs. a Rgoff of 1ohm along with a 10hm, 95pF drain-source RC snubber (17uJ), shows that using a snubber, lower losses can be obtained, while preserving a short turn-off delay and somewhat lower VDS overshoot and reduced ringing. The losses shown include the snubber loss, which is separately extracted in the datasheet, and is very small [2, 3]. However, at lower currents like 20A, the snubber is not needed in many applications, since the added losses with simple Rg control are not excessive. The use of bus snubbers is still recommended, since it improves ringing performance with minimal loss impact.

At 50A however, the waveforms using snubbers are far superior and allows a reduction in E_{ON}+E_{OFF} total switching loss by nearly 36%. Using the low Rg, delay times can also be kept low. In the lower curves in Figure 1, the switching data at 50A, 400V for the UJ4C075018K4S (18m, 750V) is compared for the cases using a 25ohm Rgon/50ohm Rgoff vs. a Rg=1ohm with a 10ohm, 300pF RC snubber across the drain-source of each device. The low Rg of 1ohm can only be used if the snubber is in place to manage the overshoots and ringing. This arrangement allows switching at a much faster di/dt with reduced turn-on delay time. The turn-on loss (including snubber loss) is now seen to be 418uJ vs 483uJ driven by the faster operating di/dt. Note however, that this faster di/dt did not come with any significant increase on peak recovery current.

Similarly, the 50A, 400V turn-off waveforms in the bottom right of Figure 1 show that the much faster switching and reduced delay time with the Rg=1ohm plus RC snubber case is achieved without excessive V_{DS} overshoot or phase node ringing. The turn-off delay

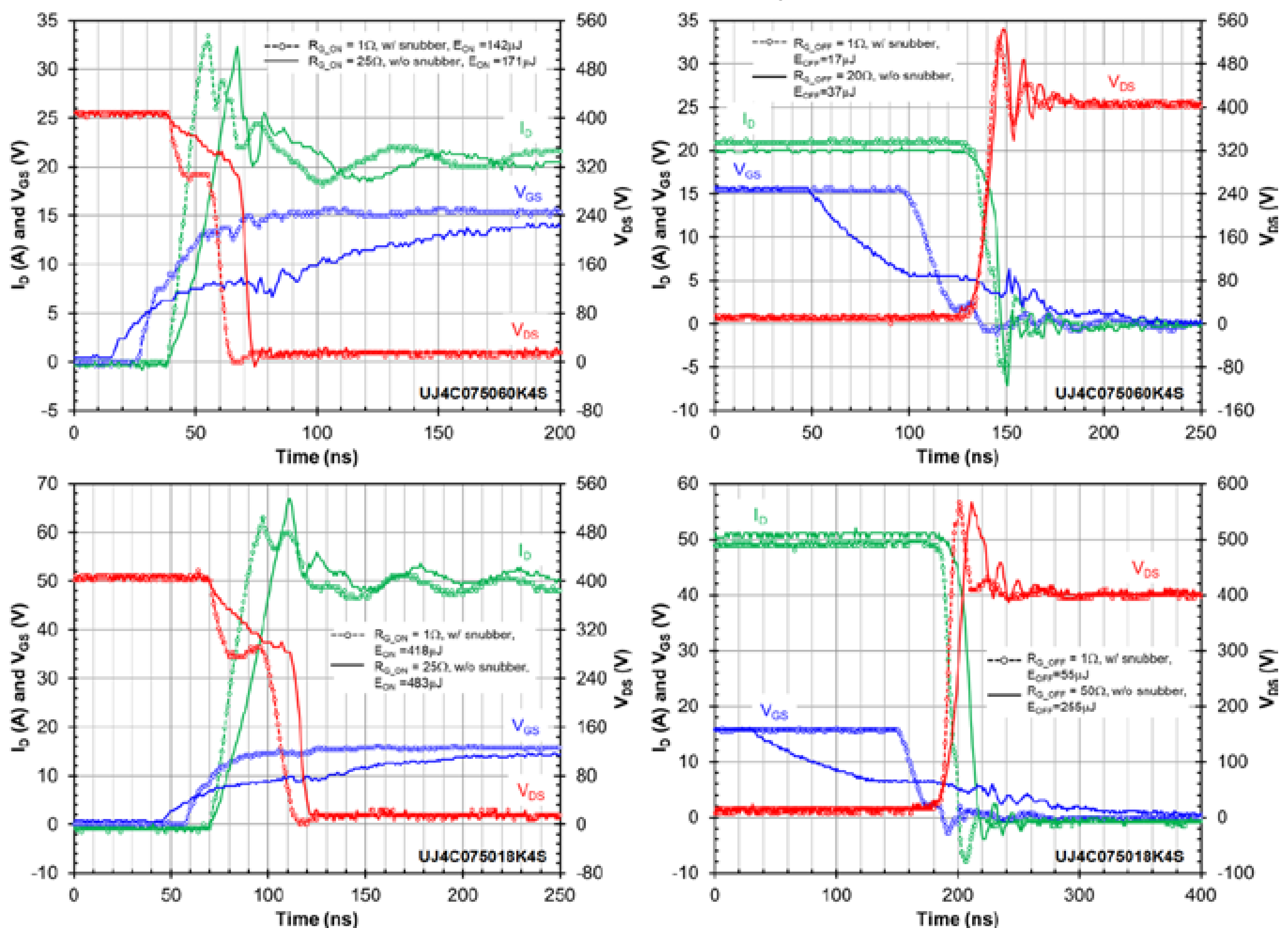

Figure 1: Half bridge-switching waveforms for the G4 SiC FET products. The upper row shows the behavior of the 60m, 750V device at 20A, 400V while the lower row shows the behavior of the 18m, 750V device at 50A, 400V. The left column shows the turn-on waveforms, the right column shows the turn-off waveforms. The dashed lines use a low external RG along with a RC snubber on the PCB between drain-source for each device, while the solid lines use high external RG values to slow down switching. In all cases, a bus snubber is utilized, i.e. a resistance in series with the bus de-coupling ceramic capacitors (2.5ohm, 100nF) and a 0 to 15V gate drive is used.

time is kept very short as well. Given that the E_{OFF} with the Rg=1ohm with RC snubber is just 55uJ compared to the 255uJ when a 50ohm resistor is used to bring down the voltage overshoot to a comparable level, it is clear that using the snubber is very advantageous for higher current applications >20A.

The exact choice of snubber can be dependent on the application, overall circuit inductances, and peak current levels for turn-off, and may not be necessary if the currents are below 25A. The loss in the snubber resistor is best measured directly by integrating the V^2/R loss at turn-on and turn-off. These values are indicated in the product datasheets [2] and are 1.7uJ at 20A, 400V for the UJ4C075060K4S with a 10ohm, 95pF snubber and 9.5uJ at 50A, 400V for UJ4C075018K4S with a 10ohm, 300pF snubber.

It is recommended that the device simply use a 0 to 12V or 15V gate drive, although with appropriate changes to R_G values [4], -5V to 15/18/20V and other common gate voltage rails may all be used. Often 0 to 10V is employed when switching above 300kHz.

Figure 2 compares the half-bridge switching waveforms for the 18m, 750V device and 60m, 750V device using the TO247-4L vs TO247-3L package, with 0-15V gate drive, using only a bus snubber. The upper row shows the turn-on and turn-off waveforms for the 60m, 750V device using a the same Rgon=1ohm, Rgoff=20ohm for both devices. The solid lines are for the 3L package, while the dashed lines are for the TO247-4L.

The faster turn-on di/dt is, of course, expected for the TO247-4L since the common-source inductance is bypassed, leading to lower E_{ON} despite a higher current peak. The gate V_{GS} ringing is much improved using the TO247-4L. V_{GS} ringing for the TO247-4L is also better at turn-off, although here, the peak V_{DS} overshoot is lower with the 3L package along with a higher E_{OFF}.

The lower half of Figure 2 looks at the use of the two package types for 50A, 400V switching of the 18m, 750V device in a half-bridge, each with a 10ohm, 300pF snubber, Rg=1ohm and 0-15V gate drive. There is now a much larger difference in the waveforms and switching losses between the 3L and 4L package types. The 3L devices have significantly higher turn-on (1.67x) and turn-off loss (4X) with similar V_{DS} overshoot and dV/dts, and with greater V_{GS} ringing, especially at turn-off. Clearly, for using TO247 packages at higher currents, using the combination of the 4L package with the device RC snubber allows for peak performance with well managed switching waveforms.

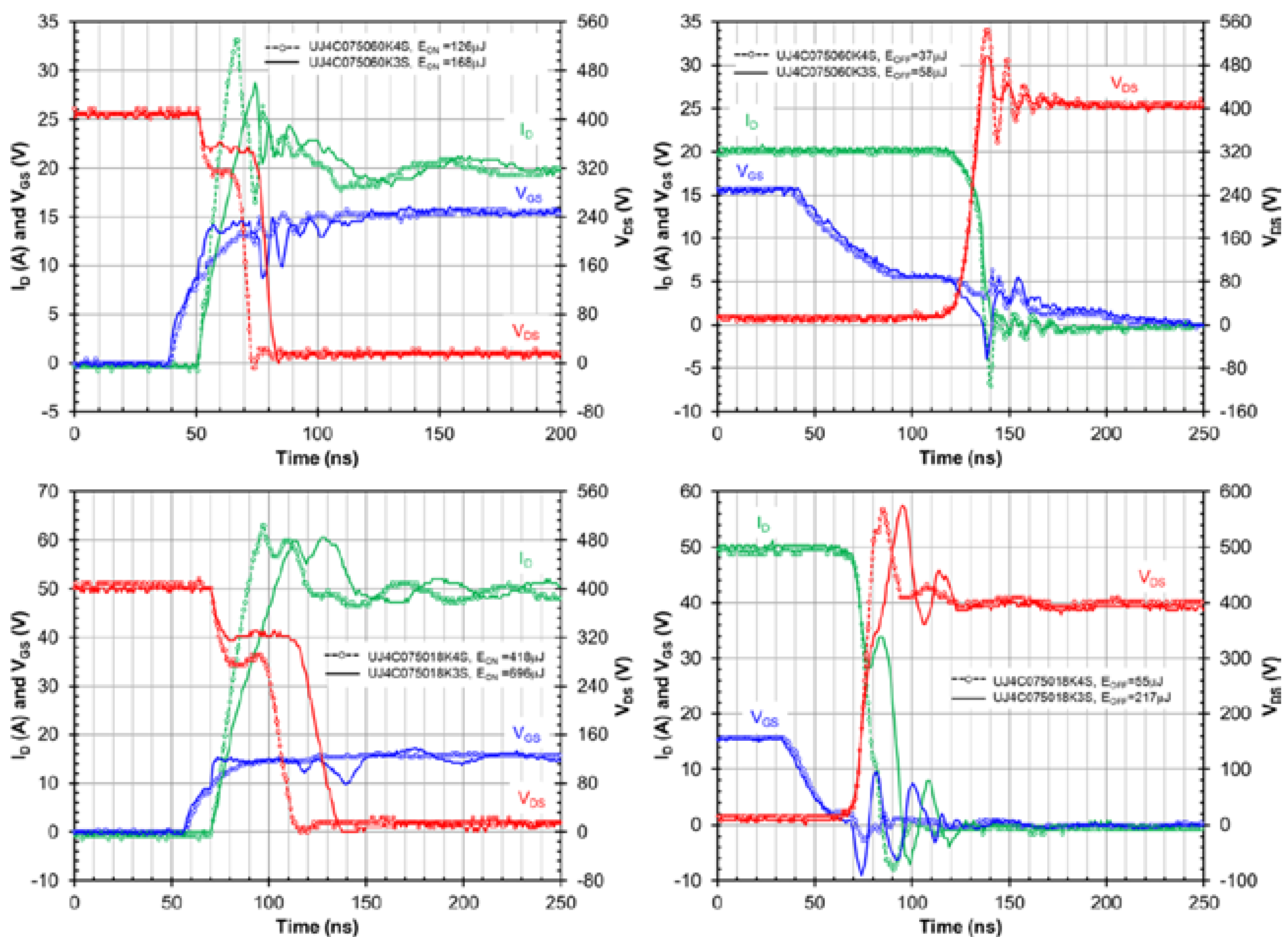

Figure 2: Half bridge-switching waveforms for the G4 SiC FET products in TO247-3L vs TO247-4L packages. The upper row shows the behavior of the 60m, 750V device at 20A, 400V while the lower row shows the behavior of the 18m, 750V device at 50A, 400V. The left column shows the turn-on waveforms, the right column shows the turn-off waveforms. The dashed lines are used for the Kelvin source K4S TO247-4L package, while the solid lines are used for the K3S standard TO247-3L package. In all cases, a bus snubber is utilized, i.e. a resistance in series with the bus de-coupling ceramic capacitors (2.5ohm, 100nF) and a 0 to 15V gate drive is used. For the upper row, the 60m, 750V devices in the two packages are measured with Rgon=1ohm, Rgoff=20ohm, but without any RC device snubber. In the lower row, given the high 50A, 400V switching, a 10ohm, 300pF drain-source snubber is applied across each 18m,750V SiC FET and an Rg=1ohm is used.

Overview of Application Benefits

We can now look at how these features of G4 SiC FETs impact a range of device applications. Figure 3a shows an example of using the 60m, 750V in a 3.6KW Totem Pole PFC circuit. The semiconductor efficiency plotted is calculated from the measured conduction and switching losses of the devices, accounting for the temperature rise, but not including controller, inductor or other system losses. The low conduction and switching losses, excellent diode recovery, and simple gate drive leads to the high efficiency seen here. This efficiency meets or beats that achievable by costlier SiC MOSFET options that require more complex gate drives. Both the 3L and 4L versions of the TO247 package are supported. Figure 3b shows the same data, comparing the efficiency with the slow leg of the TPPFC replaced with a Si rectifier diode instead of a SiC FET. The Si diode option is more cost effective, saving two transistors and gate drives, but a 0.2% drop in efficiency occurs at high line. While one 60mohm FET is sufficient for 1.5KW applications, one unit of the 18mohm, or two of the 60m paralleled are best for 3 to 3.6KW. The single 18mohm device option requires lower gate drive power and consumes less space.

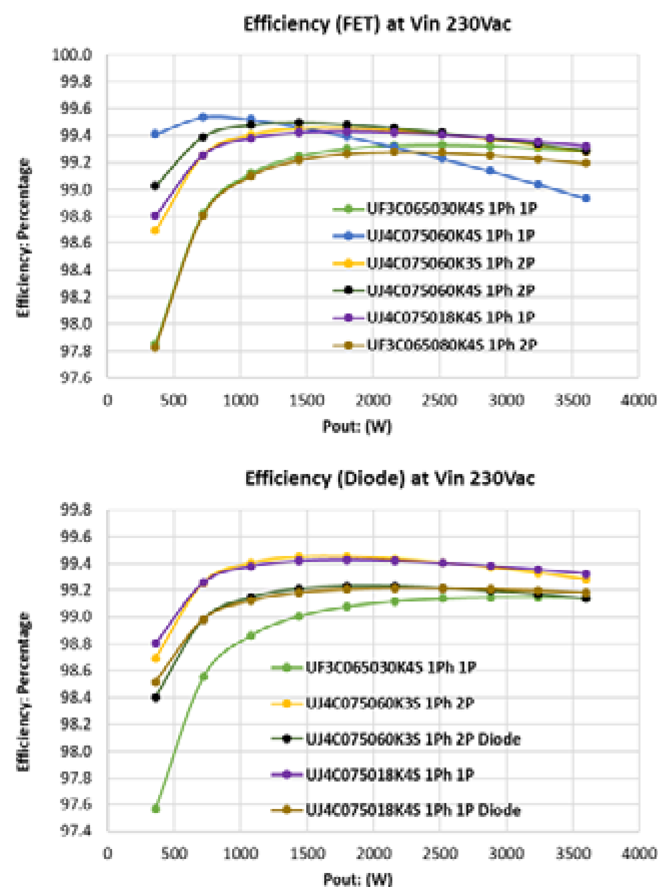

Figure 3: Semiconductor efficiency using various SiC FETs in a Totem-Pole PFC circuit at 65kHz accounting only for the losses in the power device. The plot on the left uses SiC FETs for both the fast switching and slow switching legs, while the plot on the right compares the difference using SiC FETs on the fast leg (1x UF-3C065030K3S), with Si rectifier diodes on the slow leg. The Si diode option reduces efficiency by about 0.2%. The term 1Ph 2P indicates 1 Phase with 2 parts in parallel. UF3C devices are G3 devices, included here to show the performance relative to UJ4C G4 devices.

Table 3 is a similar estimation of semiconductor losses using the 60m and 18m, 750V SiC FETs in a 3600W LLC application. The conduction, gate drive, and diode losses are added to estimate the net loss per device at maximum load. Using either 2 paralleled 60m SiC FETs or a single 18m SiC FET, losses can be kept under 6.3W per FET even at 500kHz, allowing for very high efficiency with minimal need for heat sinking. While losses are dominated by conduction losses, the relative contributions of turn-off, gate drive and diode conduction losses are also shown, and are seen to be very low using the characteristics of the G4 SiC FET.

The use of UnitedSiC FETs provide a simple path to higher efficiency in these soft switched applications without much need to change the gate drive. In this case, when ZVS operation is lost, the ability of the device to hard switch without poor diode recovery ensures no failures occur. The additional voltage headroom also helps with longer field life when that is needed.

Summary

In this article, we reviewed the parameters of the new G4 UJ4C 750V SiC FETs from UnitedSiC compared to SiC MOSFETs and Superjunction FETs in the 600/650V class. We then delved into the switching characteristics of devices in both the TO247-4L and TO247-3L packages and demonstrated the benefits of using the TO247-4L package and for currents >25A, the value of RC snubbers to manage switching waveforms while minimizing losses. We used the known device parameters to extract the losses both in a Totem-Pole PFC and an LLC example, showing how these devices can allow a path to 80Plus Titanium efficiency with a simple gate drive implementation. The advantages in both hard and soft-switched applications, coupled with the easier gate drive and the extra 100V margin, make this a compelling new entry in the rapidly expanding universe of SiC transistors targeting the 600-750V range of applications in EV chargers, EV DC-DC converters, Datacenters, Telecom power, Renewable energy and Energy storage. A wealth of additional information can be found on the UnitedSiC website [2,3,4].

References

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Pout (W)	Device	# of Devices in Parallel	fsw (kHz)	Pcond (W)	Poff (W)	Pgate (W)	Pdiode (W)	Loss per device (W)
3600	UJ4C075060K3S	1	300	24.08	2.35	0.11	0.88	27.42
		2	300	3.88	0.37	0.22	0.53	5.00
		2	500	3.89	0.62	0.36	0.88	5.75
3600	UJ4C075018K4S	1	300	4.37	0.58	0.11	0.45	5.51
		1	500	4.37	0.97	0.18	0.75	6.27

Table 3: Semiconductor losses in a 3600W LLC circuit using G4 SiC FETs at various frequencies. Very high efficiencies are possible, with each device contributing <6.27W losses even at 500kHz