

Unleashing GaN with High-Performance Gate Driving

GaN technology is a true enabler for power stages, today providing performance that was unthinkable in the previous decade. The maximum performance and benefits from GaN are obtained only when the gate driver matches the same degree of performance and innovation as the transistors. After many years of research and development, MinDCet has overcome the pitfalls in GaN gate driving by introducing the MDC901 gate driver.

By Mike Wens, CEO, Managing Director, MinDCet NV

Introduction

Since the introduction of the first gallium nitride (GaN) transistors over ten years ago, their advantages in power electronics over silicon MOSFETs have become well-known. Indeed, the material properties of GaN offer lower parasitic capacitances for a given on-resistance, inherent fast switching transients, lack of reverse recovery and high temperature operation capability. These excellent properties are seemingly the perfect combination for high performing power converters.

However, two important aspects must be considered to achieve GaN's performance potential. Firstly, it is a common conception that GaN's fast transient switching capability will directly lead to significantly higher switching frequencies and resultantly, higher efficiencies. When GaN is switched at optimal speed it will indeed show lower switching losses compared to MOSFET technology, for a given frequency. The primary reason for the comparatively lower GaN switching losses is the decreased time during the switching transient, the time when voltage and current are simultaneously present over and through the switch. The Joule losses caused by this switching loss increase linearly with frequency. Eventually, when operating GaN at increasingly higher switching frequencies, the resulting GaN efficiency may become equal or potentially lower than a MOSFET-based converter. Although there are diminishing efficiency benefits of GaN at higher switching frequencies, the GaN-based converters additionally benefit from the use of smaller storage passives, equating to a higher power density.

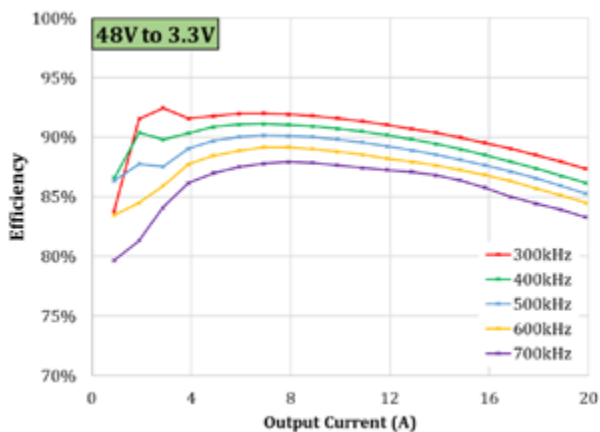


Figure 1: The measured efficiency as a function of the output current for a 48V to 3.3V GaN-based buck converter, at different switching frequencies.

This effect is demonstrated with a 48V to 3.3V step-down buck converter, built around the MinDCet MDC901 gate driver, a GaN Systems GS61008P half-bridge and a WE-HCF 1.4uH/31.5A power inductor, as depicted in Figure 5. The low converter duty cycle benefits from the fast switching transient speeds, resulting in a 10 to 15 percent efficiency increase over an equivalent MOSFET-based converter at the same switching frequency. The buck converter measurement in Figure 1 exemplifies that despite GaN's capabilities, the conversion efficiency decreases as switching frequency increases. Already at moderate switching frequencies of 300 kHz, a clear decrease of nearly 1 percent efficiency per additional 100 kHz in switching frequency can be observed over the measured frequencies from 300 to 700 kHz.

For a 48V to 12V buck converter this trade-off changes. Examining Figure 2, the GaN converter efficiency benefits from a higher switching frequency at low- to moderate loads (up to about 10A) over the 300 to 700 kHz range. To be noted is that the selected inductor has an impact on converter efficiency. Care must be taken in making the right trade-offs in the GaN-based converter design.

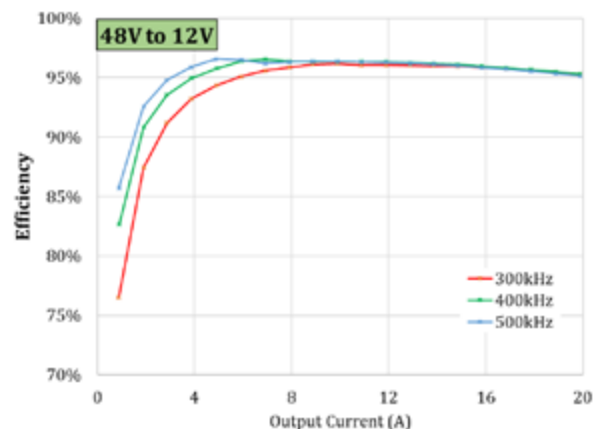


Figure 2: The measured efficiency as a function of the output current for a 48V to 12V GaN-based buck converter, at different switching frequencies.

Secondly, to enable the true intrinsic benefits of GaN, it is necessary to switch at high transient speeds. Values from 10V/ns up to 100V/ns and beyond are possible. The main component responsible for transient speed is the gate driver. Naturally, proper circuit design, specifically power routing, gate-loop routing and decoupling, needs to be implemented to enable the gate-driver and GaN to do their work optimally. In general, a standard MOSFET gate driver may in

unique cases be able to drive GaN, but optimal performance will not be reached. As a consequence the benefits of using GaN are partly lost. A gate driver that switches GaN at high transient speeds must fulfill specific requirements while simultaneously being subjected to significant stresses. These stringent requirements can only be met by a gate driver carefully developed to work with GaN.

Pitfalls for GaN Gate-Driving

GaN transistors in power applications have a lot of potential : higher power efficiency, higher power density, potential heat-sink/fan-less design,... However getting the maximal benefit from a GaN stage requires careful driving, avoiding the pitfalls along the road.

High Slew Rates

Driving GaN transistors is very ambiguous. These devices are chosen for their inherently large voltage slew rates (in excess of 100V/ns), which leads to very low switching losses (losses incurred when V_{ds} and I_{ds} are not zero). The quick switchover between low and high-side transistors causes the load current to alternate very quickly between load and input voltage (e.g. buck converter applications). This poses hard constraints to the bus voltage decoupling, as PCB tracks to the half-bridge cause overshoot, highly defined by the bus loop inductance. Additionally, the high slew rates inject large peak currents into the gate driving path through the drain source capacitance of the off-state transistor.

Parasitic Turn-On

In a half-bridge configuration, parasitic turn-on can occur to the transistor that is turned off, when its drain-source voltage is suddenly increasing to the bus voltage, either actively by the opposing transistor or inductively through the load current. This current will be converted to a non-zero gate voltage both by the gate driver pull-down impedance and the gate-source loop inductance. If this voltage is higher than the threshold voltage, a cross current will occur between the high-side and low-side switches of the half-bridge. Low gate loop inductance is only possible in monolithic co-integration of the power-stage and gate-driver, where a separate pull-down and pull-up path for each GaN transistor is very desirable.

Dead-Time

Dead-time in a half-bridge is the time between the turn-off event of one transistor and the turn-on event of the complementary bridge transistor. Granular control of the dead-time is essential. Too short of a dead-time will cause excess losses as the GaN drain-source capacitance is discharged by the complementary GaN. Zero voltage switching occurs at larger dead-times, allowing the drain-source

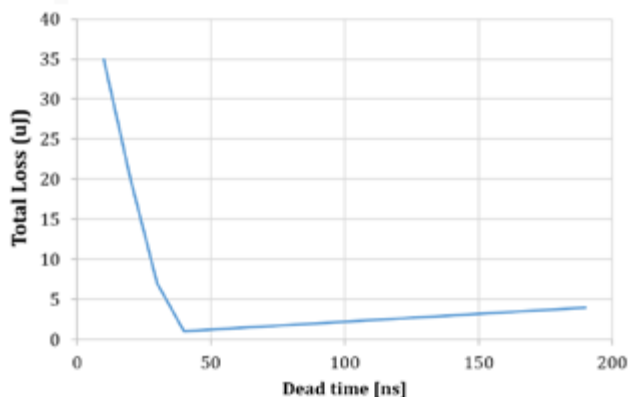


Figure 3: The energy loss as a function of the dead-time in a GaN-based buck converter. Note that the lowest loss does not coincide with the smallest dead-time.

capacitance to be discharged by the inductor (in a buck converter). Consequently, this energy is not dissipated. Too long dead-times will introduce larger losses as the reverse conduction of a GaN with zero V_{gs} is subject to a larger voltage drop (of a few volts) compared to a diode. Fixed dead-times lead to a suboptimal efficiency and must be tuned to the proper dead-time for minimal loss, which is highly application dependent.

Gate Overcharging

In non-isolated gate-drive applications, the gate driver is often supplied through bootstrapping of the low voltage supply. This technique will charge the high-side gate driver supply decoupling capacitor through a fast high-voltage diode. This generates a floating voltage that is used to supply all floating circuitry used to drive the high-side predriver. As explained before, the non-zero deadtime will cause the drain-source voltage of the low-side GaN transistor - depending on the current magnitude direction of the load - to go below zero. This effectively causes the bootstrap capacitor to charge beyond the input supply. A GaN gate is known to be notoriously sensitive to gate over-voltages, therefore the gate needs protection against overcharging to ensure reliability of the converter. In practice this is reduced through the use of clamping structures, at the cost of increased gate driver power consumption and PCB real estate with its effectiveness limited by PCB parasitics.

Negative Output Voltage Operation

The negative swing of the output driver voltage depends on the parasitic source inductance and the load conditions of the power converter, which can be poorly predicted. For predictable operation, a guarantee that the converter bridge can always be controlled is required, even when going negative in voltage compared to the supply grounds. In a DC coupled level-shifter, special precautions must be taken to allow operation below supply ground.

High duty cycle operation

Bootstrapped operation of a gate driver is a simple and effective means to provide charge to control the high-side transistor, for example, in a half-bridge. Unavoidably, there is temperature dependent leakage and bias for supporting circuitry needed in the predriver system - which causes the bootstrap voltage to leak away. If the bootstrap voltage decreases below a certain minimal voltage (often monitored through on-board undervoltage detection circuit), the predriver circuit may act erroneously and in the worst case detrimental to the converter. For a given bootstrap capacitance and power converter application, this sets a maximum on the duty cycle that can be maintained or limits the modulation depth that can be used.

The MinDCet Answer: The MDC901

High-end, high-power density and fast switching applications call for a GaN powerstage - where a specific driver is needed to ensure reliable driving and protect the valuable GaN stage.

To tackle the pitfalls previously described and provide the performance GaN demands, MinDCet introduced the MDC901 GaN gate driver. The depicted block diagram in Figure 4 provides an overview of the key functionality, solving the major pitfalls described in the previous sections.

Separate pull-up and pull-down paths allow for tuning of the turn-on speed and consequently the slew-rate of the output stage while maintaining a low impedance pulldown path for the GaN transistor. This keeps the gate-source voltage under control in off-state avoiding parasitic turn-on, even under high drain-gate capacitive currents.

The dead-time for turn-on and turn-off can be set through a series of digital inputs. This allows static tuning of the dead-time for a given application or in conjunction with a controller, this could be performed dynamically for optimal efficiency. Additionally, dead-time can be set in automatic mode. A closed loop senses the GaN gate voltages and the gate is only turned on when the complementary GaN gate is off. This is a fail-safe operation mode.

The risk of gate-overcharging during negative voltage operation is solved by placing fully floating regulators both in the high-side and low-side domain after the bootstrap diode. This results in a well defined and robustly protected gate driver voltage.

Negative output voltage operation is guaranteed down to -4V, allowing accurate gate control even under high inductive currents. This has been accommodated by a specifically designed level shifter and floating supply generation.

For high-duty cycle applications (e.g. motor drivers and class-D amplifiers), it is mandatory to maintain a high-side on-state for longer periods of time. This functionality was implemented by an integrated charge pump, compensating for DC bias under 100% duty cycle conditions.

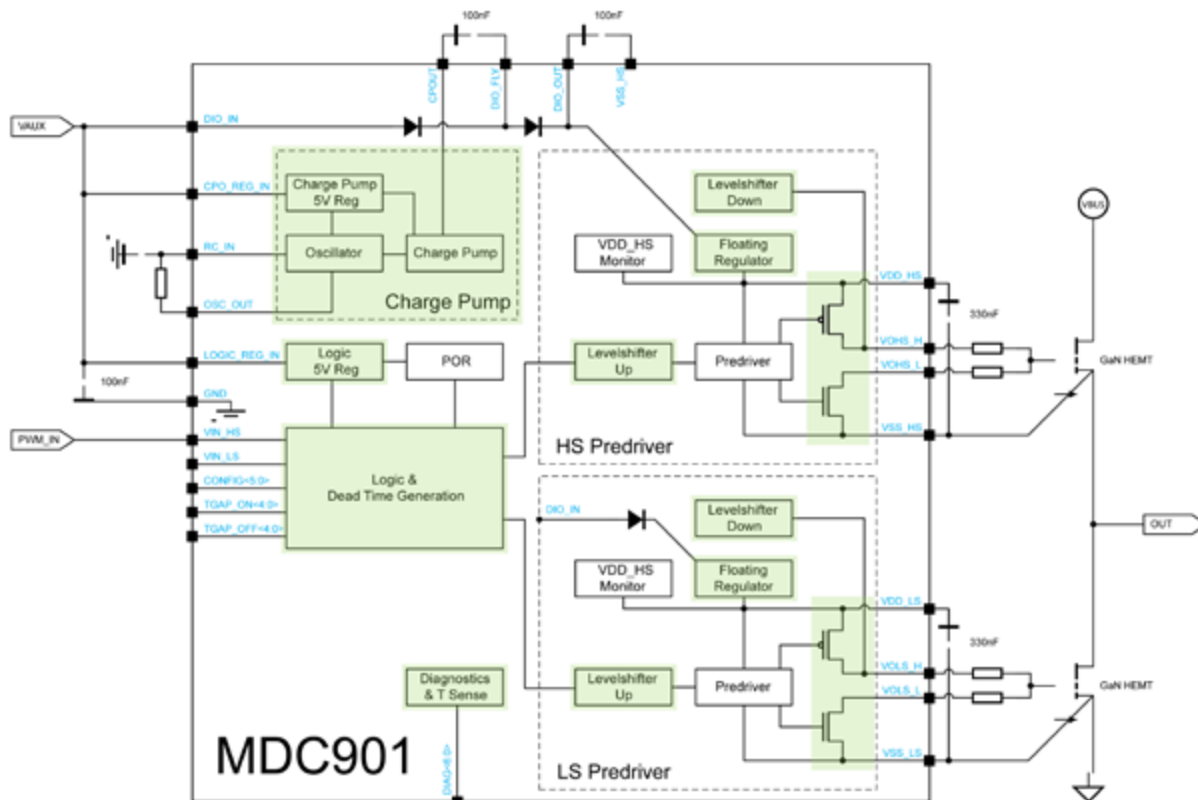


Figure 4: The block diagram of the MDC901 GaN gate driver.

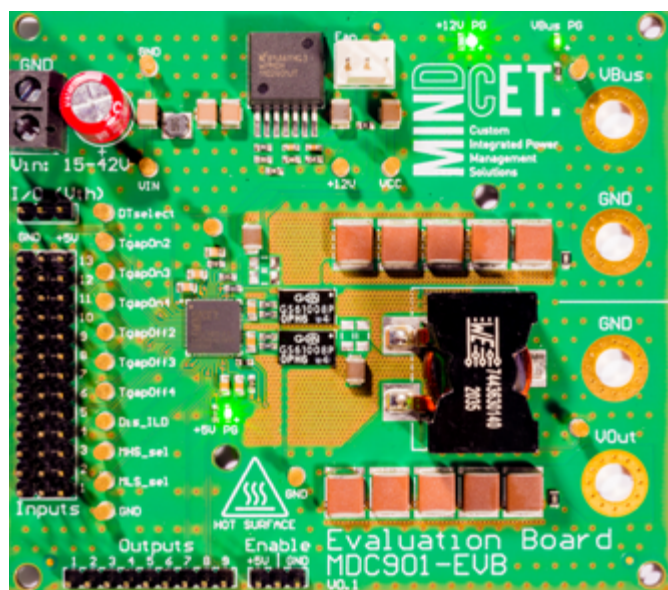


Figure 5: The MDC901 100V half-bridge evaluation board.

The MDC901 provides a high-end and feature-rich solution to driving GaN transistors in a reliable way for maximizing performance in the given application. The driver was developed for DC-DC solutions, but can be used for all other GaN driving applications like LIDAR, motor drivers, and electronic fuse applications requiring true 200V capability. To enable easy and fast design-in of the MDC901 gate driver in a variety of applications, a 100V half-bridge evaluation board in a buck-converter topology, as displayed in Figure 5, was developed for assisting power electronics designers.

Conclusions

Enabling the true benefits of GaN power stages requires implementing an optimized gate-driver that is designed specifically to work with GaN transistors. Resultantly, the GaN can be pushed to the limits, yielding the highest possible performance, which provides for a maximum return on the technological and monetary investment. A discrete gate-driver such as the MDC901 provides the user with the flexibility, diagnostics and an expanded feature set for choosing the best-suited GaN transistors for the given application.