Near Chip-Scale WBG Half-Bridge

Near chip-scale Type IV µMaxPak enables higher power-density, lower inductance and lower thermal resistance, relative to benchmark Types, I & II µMaxPak, by a factor of two.

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Type IV µMaxPak Building Blocks

The fundamental µMaxPak Near Chip-Scale SMD architecture provides benchmark power-density while enabling minimum parasitics and minimum thermal resistance for high-power, high-speed WBG power switches. These switches accommodate high-voltage & high-current industrial products once limited to large industrial power IGBT modules. Early feasibility studies have shown that Near Chip-scale SiC Type III µMaxPak can be extended to Electric Vehicles and potential are scalable to Locomotive Traction. Such near chip-scale SMD packages are both necessary & sufficient to allow power WBG devices to operate at full performance & efficiency. Therefore, they are "Inevitable for Power WBG packaging." [1] [4]

µMaxPak near chip-scale packages uses proprietary technology protected by U.S. patent US9,214,416. It provides examples of QFN and LGA µMaxPaks. The patent and supporting technical articles, papers, and presentations show three basic µMaxPak structures, Type I, II, & III, described herein. These examples show single power FET die switches but can include multiple paralleled FETs & anti-parallel diodes and even support integration like Gate-Driver die & passive components. The single-switches (SS) can be extended to multiple "Lateral" switches like Half-Bridge (HB), Full Bridge (FB), & 3Ø-Bridges. The Type I, II & III combination can create the Stacked/ Vertical Type IV µMaxPak HB. The three (3) building blocks are:

Type I µMaxPak, Standard Type with all bottom-side SMD pads contain a power FET in a QFN with die drain pad exposed on package bottom-side, and source and gate & sense pads are soldered into the bottom-side by the leadframe cavity. The leadframe extends to the bottom-side of the package, creating external connections and a secondary/parallel thermal path. The package is constructed with QFN assembly technology, contains a single-piece leadframe with no leads and wire bonds. Type I µMaxPak accommodate bump-chip integrate gate-drivers that are not shown.

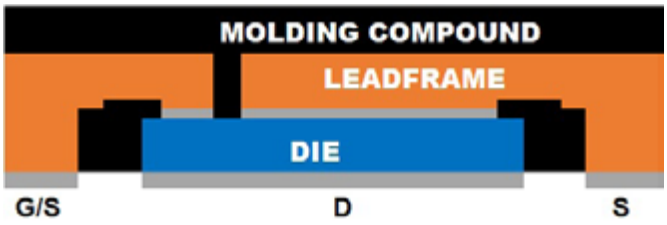

Figure 1: Type I µMaxPak

Type II µMaxPak is also built with QFN assembly technology. The die is inverted compared to Type I with all bottom-side pads. The die source, gate & sense pads are exposed on the package bottom-side. The power FET die drain is soldered into the leadframe cavity. The leadframe extends to the package bottom-side creating an external drain and second parallel paths. The package contains a single-piece leadframe with no leads or wire bonds. This µMaxPak QFN This Type II µMaxPak, in Figure 2, can accommodate horizontal integrated gate-drive IC but cannot accommodate vertical integration.

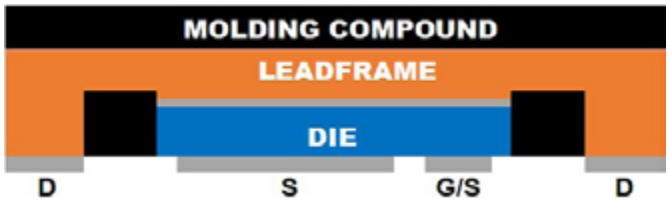

Figure 2: Type II µMaxPak

Type III µMaxPak Inverted (and Standard) die contains electrical & thermal pads on both top & bottom sides. This option is shown in Figure 3, with the die source, gate, & sense pad exposed on the bottom side. The die drain pad is soldered into the bottom-side leadframe cavity, which extends drain to bottom side pads. The top of the leadframe is exposed at the top of the package, creating the drain connection and a paralleled thermal path. This type also contains no leads or wire bonds and is built with QFN technology. The double-sided thermal package pads accommodate both top & bottom DBCs & heatsinks, cutting thermal resistance (Rjc) in half. Type III µMaxPak is ideal for higher power EV traction and scalable to Locomotive traction. [2]

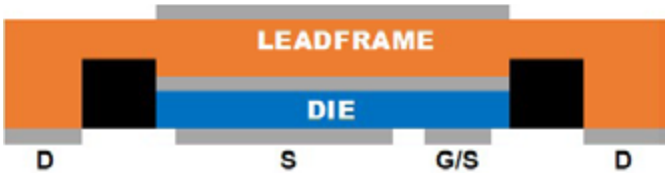

Figure 3: Type III µMaxPak

New Type IV µMaxPak HB Architecture & Performance Advantages

New Type IV µMaxPak HB is a unique Vertical/Stacked architecture. The Half-Bridge configuration contains a low-side switch in the bottom-side leadframe cavity and a high-side switch on top of the leadframe. All external pads are on the package bottom-side, except the high side drain, which is on the top-side of the package. See the cross-section of Type IV µMaxPak HB in Figure 4. It too contains all proprietary features in U.S. patent US9,214,416. The patent also extends the IP to LGA Types I, II, III & IV µMaxPak.

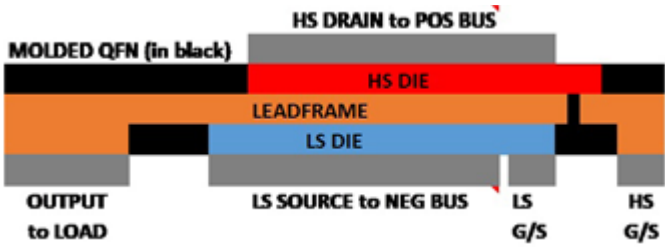

Figure 4: Type IV µMaxPak HB

This cross-section example shows a basic HB with a single SiC vertical MOSFET die for both switches. The switches can include paralleled MOSFETs die, anti-paralleled diode die, and other special devices.

Additional perspective, details, and sizes are shown in a conceptual design of 600V/350A (1200V/150A) Type IV µMaxPak 10 x 6 x 1mm HB drawing in Figure 5, which illustrates a Top X-ray view and a Cross-Section view with stacked high-side & low-side switches. The corresponding Package Outline Drawing in Figure 6 provides an external pad configuration for this Type IV µMaxPak HB example.

The initial conceptual 650V/350A Type IV µMaxPak HB design was 650V, and 1200V products based on SiC die suitable for industrial products but may be possible for EV Traction. I_{DC}(max) was calculated based on SiC die sizes and current-densities, and rated continuous @ TJC(max)=150°C. See the results in Table1 a & b.

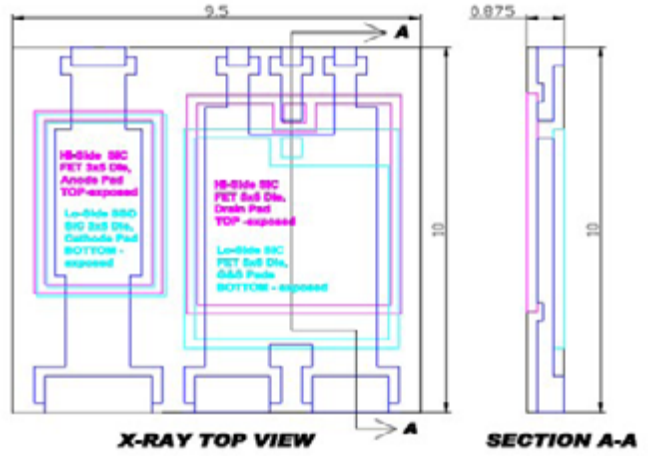

Figure 5: Type IV µMaxPak HB X-ray & Cross-Section View

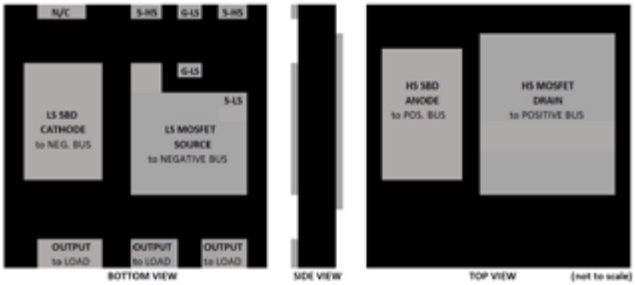

Figure 6: Type IV µMaxPak HB Package Outline Drawing

650V MOSFET DIE (mm)	650V SBD DIE (mm)	MOSFET DIE $R_{JC/RC}$ (°C/W)	Assumed Max. Current-Density @ Tj=150°C	µMaxPak HB Size (mm)	*Continuous I_{DC}(max) (A)*
5.0 x 4.0	4.0 x 3.0	0.090/9.029	14.1A/mm^2	9.0 x 8.5	225
6.0 x 5.0	5.5 x 3.0	0.060/0.019	14.1A/mm^2	10.0 x 9.5	350
7.0 x 6.0	7.0 x 3.5	0.043/0.014	14.1A/mm^2	11.0 x11.0	500
8.0 x 7.0	7.0 x 4.5	0.032/0.010	14.1A/mm^2	12.0 x 13.0	675
9.0 x 8.0	8. 0x 5.0	0.025/0.008	14.1A/mm^2	13.0 x 14.5	900

1200V MOSFET DIE (mm)	1200V SBD DIE (mm)	MOSFET DIE $R_{JC/RC}$ (°C/W)	Assumed Max. Current-Density @ Tj=150°C	µMaxPak HB Size (mm)	Continuous I_{DC}(max) (A)
5.0 x 4.0	4.0 x 3.0	0.090/9.029	7.6A/mm^2	9.0 x 8.5	90
6.0 x 5.0	6.0 x 3.0	0.060/0.019	7.6A/mm^2	10.0 x 9.5	150
7.0 x 6.0	7.0 x 3.5	0.043/0.014	7.6A/mm^2	11.0 x11.0	225
8.0 x 7.0	7.0 x 4.5	0.032/0.010	7.6A/mm^2	12.0 x 13.0	325
9.0 x 8.0	8.0 x 5.0	0.025/0.008	7.6A/mm^2	13.0 x 14.5	425

Table 1a & b: Type IV µMaxPak HB Projected Ratings

Key Type IV µMaxPak Advantages

1) Power Density is Double that of the benchmark Lateral µMaxPak HB packages, made possible by stacking high-side & low-side switches.
2) Thermal resistance (Rjc) is Half of Lateral µMaxPak HB benchmarks by dissipating heat from both the top & bottom of the package reduces the Rjc, plus added heat removal by leadframe between high- & low-side switches. This technique is most effective with a thin power die, and a higher thermally conductive SiC die.
3) The Type IV with vertically stack switches can achieve even higher I_{DC}(max) current ratings. In many HB applications, each HB switch operates at 50% duty cycle and must be de-rated for DC operations, like motor control in stall or low RPM operation. By removing heat through both the OFF & ON switches, I_{DC} & I_{AC} ratings are the same, with no de-rating is required.
4) Package Loop Inductance & Resistance is virtually eliminated (L ≤ 0.1 nH) with Vertical/Stack structures. The higher power-densities/smaller packages allow tighter packing, minimizing system interconnects, further reducing inductance & resistance.
5) Die on both sides of leadframe balances CTE mismatch between die & leadframe, minimizing warpage during die attach & operation. The balanced CTE enhances both assembly yields and reliability, making larger die possible. Leadframe & multiple die pads are essential tools to reduce stresses & warpage.

Enhanced Type IV Performance & Efficiency

The much lower Rjc(max) reduces Tj(operation), significantly reduces Rds(on) in today's WBG devices, and improving overall efficiency. A much lower loop inductance further increases switching efficiency.

When Tj(operation) is reduced for SiC from 175°C to 150°C, conventional Pb-free (Sn/Ag) solders are suitable for die attach. These soft solders develop less stress during solder processing and operation. Using standard QFN solders is simpler, requiring minimal process/material development. In principle, Sintered-Ag and Sintered-Cu die attach are possible for µMaxPak assembly but require additional design, process, and equipment development.

Long-term, Sintered-Ag and Sintered-Cu die attach for higher temperatures (Tj) SiC die attach at higher power levels. Locomotive traction and EV applications are already using Sintered-Ag die attach.

Estimated potential current ratings for Type IV HB switches vary with SiC performance, operating condition, manufacturers, and other factors. To get an approximate quantitative feel for what is possible for Type IV µMaxPak near chip-scale half-bridges products, estimates were made based SiC die sizes, Tj(operation)=150°C, Tj(max)=175°C, 99.5% efficiency @ Tj=150°C, and maximum SiC current densities for 650V and 1200V SiC. See estimates in Table 1.

Inverter Architecture with Type IV µMaxPak Half-Bridges

The µMaxPak Half-Bridge is a Double-Sided Near Chip-Scale SMD package, ideally enabling maximum system integration, providing the highest system power-density, and minimizing system parasitics, cost, size & weight. Since product applications and power levels dictate much of the systems, systems are outside the scope of this article. Still, it is possible to show some structure and process examples. Type IV µMaxPak can use SMD assembly on Power PCBs, but at higher power levels discussed herein, µMaxPaks will require assembly on DBC substrates with large heatsinks or cold-plates. DBC/AMB substrates provide HV isolation and the highest power dissipation. Power dissipation is primarily a function of thermal conductivity of DBC/AMB ceramic substrate materials (A2O3, Si3N4, or AlN) with ceramic area and thickness determining thermal resistance, case-to-sink. WBG die in µMaxPak packages generally uses smaller DBC substrates, which can often be thinner than in larger conventional modules. Thinner Ceramics reduce thermal resistance and material costs.

Power PCB are easier to assemble & interface, resulting in lower costs and easier integration. DBC substrate can provide the lowest thermal resistance but increase assembly complexity & costs. Figure 7 illustrates a single phase cross-section with Type IV µMaxPak HB (1/3 Inverter), an example of a higher power Type IV µMaxPak HB system architecture. Although 3Ø Inverter integration is possible with DBC Modules, µMaxPak packages can enable much more complex and complete system architecture, ideally with No internal Screw Terminals. Only entry & exit to the System-Enclosure would have screw terminals. Examples of such "System Enclosures" are common for EV Motor-Drives. These system boxes are large because they contain large modules with redundant internal terminals and other unnecessary mechanical structures.

Type IV µMaxPak HB and Systems described in this article assume the use of common Pb-free (Sn/Ag) solders, which can enable SiC Tj(continuous) to 150°C and Tj(max) to 175°C. Lead-free solders are ideal for many SiC & GaN power products today, with SiC Rds(on) increasing significantly above Tj=150°C. That said, very high power SiC product for applications like EV & locomotive traction already operate with higher Tj, and Tj(max) will increase as power WBG devices evolve. Higher power devices will require higher temperature die attach & package solders/materials. Sintered-Ag & Sintered-Cu are already being used for higher temperatures. These materials are compatible with µMaxPak, but require processes & equipment development.

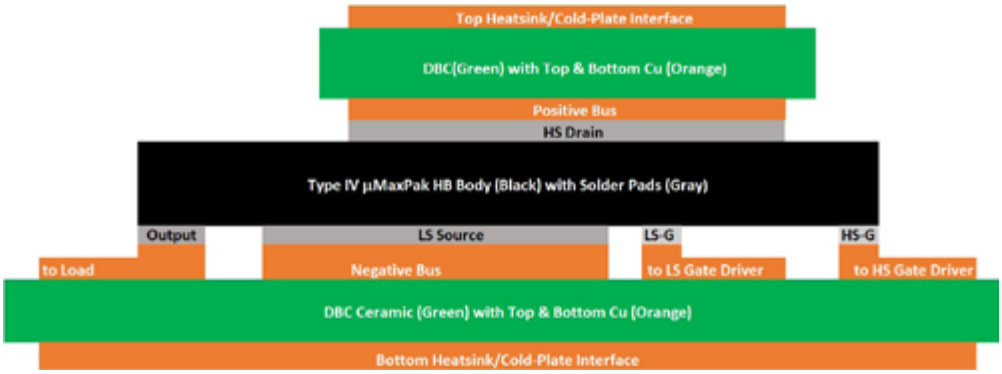

Figure 7: 1/3 Inverter with Type IV µMaxPak HB

High power-density µMaxPak enables much higher system packing density, with corresponding no leads, no wire bond, and no internal screw-terminals. These µMaxPak chip-scale SMD packages allow improvements to systems, often exceed power-density, performance, parasitics, and efficiency advantages of the µMaxPaks themselves. And significantly reduce system complexity, cost & size.

Inevitability – The long game may well be sooner than we think!
Today's Power WBG devices are evolving quickly, but products do not always keep pace. We get excited about gains relative to silicon devices, blinding us to how far we fall short of real WBG potential. Some of today's short-fall results from not selecting the best circuit topology for WBG devices, but much of the short-fall belongs to basic package parasitics and limitations.

Near Chip-Scale packages are Inevitable for Power WBG devices and a big step for Traditional Power mindset and infrastructure. Traditionally modules & systems were developed for high-voltage (HV) SCR, Thyristor, and Diode switches & bridges. These packages adapted easily to High voltage IGBT & MOSFET products. These newer Si Semiconductors improved performance and efficiency with minimum module changes, and manufacturing equipment & tooling was expensive and had proven reliability. As HV IGBT device performance, speed & efficiency increased, there were continuous incremental improvements. Although bulky and costly, these refined modules did not significantly reduce IGBT performance & reliability but pushed the limits. Power WBG (SiC & GaN) are not incremental changes and require near chip-scale packages with today's power WBG devices, and they are still evolving!

1) WBG die power density is an order-of-magnitude larger than Si die, or the die is an order-of-magnitude smaller. Power dissipation from such a small die is difficult, even if losses are reduced by 80%. Power dissipation from both sides of the die in Type I & II is helpful but insufficient in higher power products like EV and Locomotive Traction. The µMaxPak Types III & IV are necessary to remove the heat from the top & bottom of the packages.
2) Switching speeds can be a few orders of magnitude higher, requiring much lower loop-inductance and common-source inductance. The µMaxPak virtually eliminates package inductance by eliminating leads & wire bonds and enabling die to be placed closer in the package, making the end-system Much smaller.
3) Near chip-scale SMD packages reduce package and system assembly material, labor & tooling costs, and small low-profile SMD components & connectors, making systems easier to coat or pot for HV isolation, and for environmental protection.
4) Smaller size not only improves system performance, efficiency & cost, but smaller and lighter is always an advantage, especially for applications like EV & Locomotive.

The higher the power levels, the bigger payback for more efficient power Near Chip-Scale packages. However, new approaches take time for development and acceptance, especially when devices, packages, system, and application changes must occur simultaneously.

After many years designing, qualifying & manufacturing high-power IGBT modules, and designing over 100 custom QFN & LGA packages for high-power, high-voltage, RF & multi-chip products, it was clear to the author that QFN & LGA packages are a proven, flexible and economical technology platform for high power WBG µMaxPak technology is a practical implementation of near chip-scale QFN technology to replace traditional Silicon power modules.

For time to market and marketability based on proven working product, the author advises starting with the Type I & II µMaxPaks; to quickly develop industrial products, experience & confidence, and then extend it to Type III & IV higher power Industrial products and EV Traction. Pb-free (Sn/Ag) soft-solders are the most logical place to start, but as SiC moves to higher operating temperatures, Sintered-Ag or Sintered-Cu die attach will replace soft solders.

References

1. "Inevitability of Near Chip-Scale Packages Replacing Even New WBG Traditional Modules" will be presented at 3D-PEIM Symposium, Osaka, Japan, June 21-23, 2021
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