Lowest On-resistance SiC FETs Offer Rugged Short-Circuit Performance

The largest growth area for silicon carbide FETs is expected in the electric vehicle traction inverter, offering extended range, lower battery costs and higher power density. UnitedSiC (now Qorvo) has recently released low on-resistance SiC FETs, 750V/6mOhm in a standard TO247-4L package.

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The FETs are compelling for inverters designed with 400V-500V bus voltage, offering superior conduction losses and switching losses compared to their Si IGBT or WBG alternatives. In addition to low losses, it is also essential for power switches in motor drive inverters to offer short-circuit protection to allow detection and safe shut down to avoid catastrophic system failure. These 6mOhm/750V SiC FETs offer a useable short-circuit widthstand time of 5 microseconds. In this article, we discuss the importance of this feature and why these 4th generation SiC FETs are uniquely positioned to meet this demand without compromising on $R_{DS(on)}$.

Introduction

Silicon carbide FETs have established themselves in many applications including on and off-board charging of EVs, datacenter power supplies, solar inverters etc. The largest growth area for silicon carbide FETs is expected in the EV traction inverter, offering extended range, lower battery costs and higher power density [1,2]. Already introduced in 400V battery system, SiC FETs have perhaps an even more compelling case with higher bus voltages (500V or 800V) [1,2]. The drivetrain inverters in these systems are conventionally 3-phase, 2-level voltage source inverters operating at frequencies below 20kHz. In this application, it is paramount for the switch to offer low conduction and switching losses across the full load range. SiC FETs are a great candidate with their absence of knee voltage (improved light load efficiency), and low conduction and switching losses. However, one area where silicon carbide switch options have not met the application need until now is short-circuit ruggedness. In this article we will discuss why UnitedSiC/Qorvo's 4th generation cascode SiC FET is an ideal candidate to minimize on-resistance while maintaining a useful (up to 5 microsecond) short-circuit widthstand time for designers.

Short-circuit ruggedness is an especially important feature for power semiconductor switches in motor drive inverters to possess, requiring some fault ride-through protection allowing for the system to detect and safely shut down avoiding catastrophic system failure. Figure 1 depicts the various short-circuit faults that commonly occur in a motor drive inverter system. The system can experience a direct short of the DC-bus when there is a shoot-through condition of one of the inverter phase legs. This can happen if one of the phase leg switches fails short while the other switch's gate drive remains functional. Alternatively, a shoot-through condition can occur if an erroneous signal from the gate driver is applied to one of the phase leg FETs. A short-circuit across phase legs (phase-to-phase) can occur when insulation in the windings of the motor fails. Finally, a phase-to-ground failure can occur if there is a failure in the motor winding insulation such that a short is created to the motor casing. In each of these failure modes, the power semiconductor switch must endure a direct short-circuit of the entire DC bus voltage or share bus voltage in short-circuit with the complementary switch in the phase leg. Under these harsh conditions, it is the power semiconductors which catastrophically fail first (within microseconds), rendering the entire system inoperable.

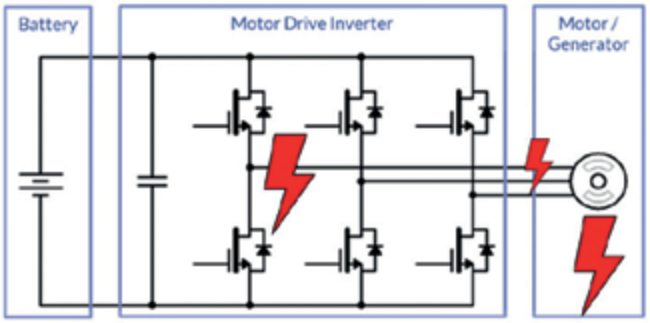


Figure 1: Schematic of traction inverter showing location of commonly encountered short-circuit faults, Phase leg shoot-through, Phase to Phase short, or Phase to Ground failure

Multiple methods of detecting a short-circuit have been proposed, but most fall into either current measurements or de-saturation (deSat) detection of the switch Drain-to-Source voltage (or collector-emitter voltage of IGBTs). Figure 2 depicts a standard deSat approach on the low-side switch of a phase leg. A fast, high-voltage deSat diode is used to allow monitoring only during the switches on-time. In the event that the voltage across the switch is higher than expected while the switch is gated on, a threshold level is tripped (typically 7-9V) indicating an overcurrent or short-circuit event. The state of the deSat signal is used to shut down the gate driver output and the switch is turned off before catastrophic failure. However, care must be taken to prevent false tripping of the deSat signal. A blanking time is used to censor the time between the start of turn-on and the switch reaching its nominal Drain-to-Source voltage during conduction. Additionally, avoiding spurious deSat trips often includes filtering (RC etc.) of the input to avoid noise induced trips, which can further increase the practical minimum detection time. Thus, a trade off exists between noise immu-

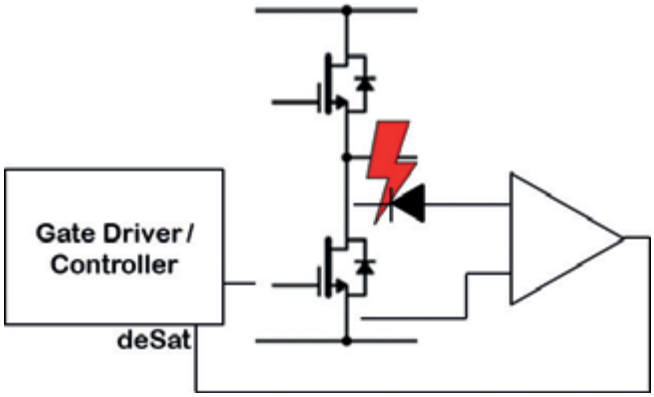


Figure 2: Schematic of commonly employed desaturation detection

nity and short-circuit detection and shutdown time. Designers can find these constraints challenging to implement in systems without several microseconds of assumed ride-through capability. To date, wide bandgap devices, with their low on-resistance and smaller die sizes, have underperformed their traction IGBT counterparts which have historically offered more than 10 microseconds of short-circuit ride-through capability. However, as Si IGBTs have continually lowered $V_{ce,on}$ and switching losses, along with improved gate drivers, short-circuit ride-through ratings have decreased to below 10 microseconds [3].

There are several characteristics associated with a power semiconductor switch that impact its ability to handle short-circuit faults. To understand these characteristics, we can first look at the typical failure mechanisms that occur when FETs are subjected to short-circuit conditions as represented in Figure 3. In the figure, a typical I-V characteristic of a Type-1 short-circuit is represented with the bus voltage being applied across the device. There is a small dip/overshoot in the otherwise constant voltage associated with the drop across the power loop stray inductance under the high di/dt portion. In the figure, the device's short-circuit current (black curve) increases rapidly as the FET's impedance is low in the on-state. During this phase, the device's junction temperature is heating rapidly as the high instantaneous power is contained in the FET's active layer. As the junction temperature and current rises, eventually the FET reaches its current saturation regime limiting the peak short-circuit current (Isc-peak). The large instantaneous power dissipation continues to heat the FET and the short-circuit current begins to decrease from the self-heating and the resultant decrease in saturation current.

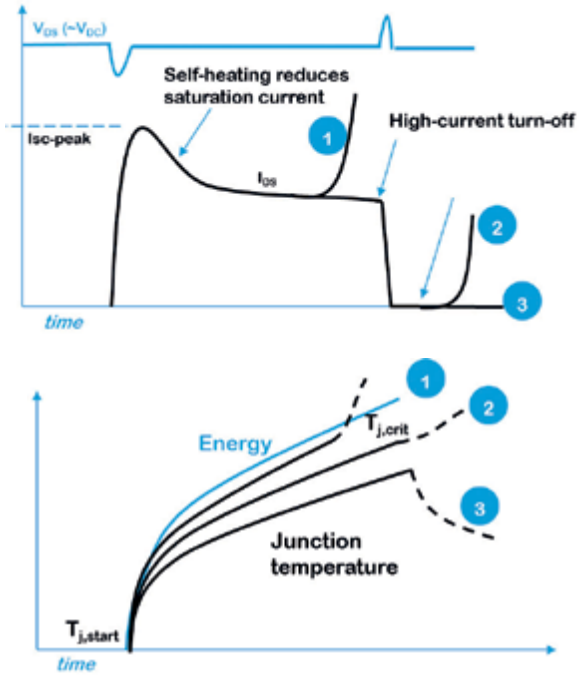


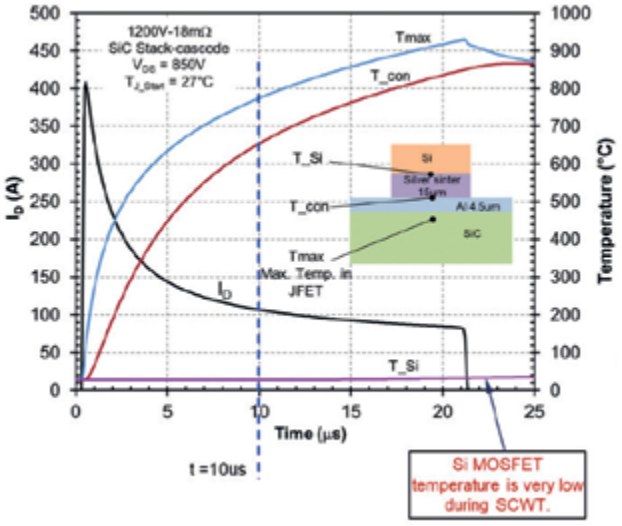
Figure 3: Typical short-circuit I-V waveforms (top) and resulting temperature rise (bottom) exhibited by a power FET under short-circuit

If the device's junction temperature reaches a thermally unstable level prior to the gate driver shutting off the channel of the FET, a runaway event can occur as illustrated by bubble1 in Figure 3. In the case of conventional SiC MOSFETs, failure prior to shut down can also occur if the gate oxide ruptures in the presence of high electric field and high junction temperatures [4,5]. The failure mode 2 depicted in the figure represents thermal runaway after the FET is turned off. In this mode, the device's leakage current at high temperature (can be more than 600°C) can lead to thermal runaway or latch the device's internal parasitic transistor causing catastrophic failure to occur. Finally, in the case of mode 3, the device can safely shut down the short-circuit fault and the device's junction temperature slowly returns to its nominal running temperature. In state of the art SiC FETs operating with practical bus voltages, the short-circuit period on the microsecond scale can be thought of as an adiabatic process. Silicon carbide's 3-6x smaller die sizes and associated reduced thermal capacity results in a larger temperature rise for a given short-circuit energy than their Si counterparts.

SiC FETs Offer Breakthrough Performance

From the discussion around Figure 3, it is clear that the optimum power switch is one that can reduce $I_{sc\text{-}peak}$ without compromise of on-resistance, thereby keeping the short-circuit energy low, reducing temperature rise and avoiding thermal runaway. The switch should also avoid secondary failure modes such as gate-oxide rupture and avoid any parasitic bipolar transistor latch up. While p-n junction leakage at high temperature is unavoidable, the optimal switch should also maintain a sufficiently high threshold voltage versus temperature to diminish channel leakage components that adds to thermal runaway.

These characteristics are all found in vertical SiC JFETs. SiC JFETs offer the lowest specific on-resistance of any technology from 650V-2kV+, while also offering good current saturation. The vertical JFET device structure has no internal parasitic transistor in its primary leakage path (Drain-to-Gate) in the off state. There is no gate oxide in the device structure and the threshold voltage versus temperature is flat compared to Si or SiC MOSFETs. When configured with a low voltage Si MOSFET, the normally-off cascode SiC FET offers a superior trade-off between on-resistance and short-circuit ruggedness [6]. It can also be shown that during the short-circuit fault (up to 10 microseconds), the heat is concentrated in the SiC JFET and



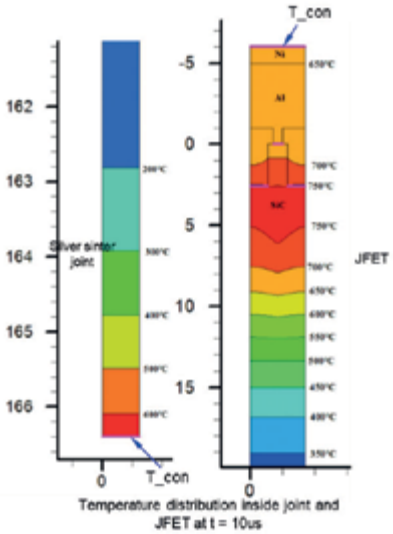


Figure 4: Electro-thermal TCAD simulation of a SiC Stacked- Cascode FET under short-circuit (top) simulated short-circuit current and temperature rise in bulk of SiC, at top of SiC JFET power metal and bottom of Si MOSFET (bottom) temperature profile in bulk of JFET and top of contact at 10 microseconds after start of short-circuit

the low voltage Si MOSFET in the stacked cascode FET does not see significant temperature rise. Figure 4 illustrates an electrothermal TCAD simulation of a SiC stacked cascode FET under short-circuit. Up to 10 microseconds, the temperature rise (up to >700°C) is primarily contained in the SiC JFET bulk and topside metallization. Here, the Si MOSFET, which does not enter the current saturation regime remains well below its maximum junction temperature. Thus, it is the SiC JFET that determines the short-circuit capability of a SiC cascode FET.

UnitedSiC (now Qorvo) has exploited these features with its 4th generation of SiC FETs. The new UJ4SC075006K4S product boasts the industry's lowest on-resistance of 6mOhm in a standard discrete package. The device offers a voltage rating of 750V which allows plenty of design headroom for 400V or 500V bus applications. The superior on-resistance (less than half of the nearest competitor) is offered with all the additional advantages that users have grown accustomed to with UnitedSiC FETs such as the easy 0-12V or 0-15V gate drive, excellent integral diode, and low switching losses afforded by the lower device capacitances (C_{oss}).

For the first time with a SiC power switch, rugged short-circuit performance is achieved without compromising cost or efficiency. The 750V rated SiC JFETs boast a specific on-resistance less than 1/3rd of their 650V SiC MOSFET competitors. The UJ4SC075006K4S 750V/6mOhm SiC FET has also been designed with a useable short-circuit withstand time of greater than 5 microseconds. Figure 5 shows the Type-1 short-circuit characteristics of a typical UJ4SC075006K4S SiC FET with a bus voltage of 400V. The device safely shuts off after a 10 microsecond short-circuit when the starting junction temperature is 25°C and passes 8 microseconds even when starting from the devices' $T_{j,max}$=175°C. The devices are designed with current saturation (800A shown at $T_{j,start}$=25°C, 600A at $T_{j,start}$=175°C, respectively) between 5-10x nominal, which is sufficient to allow for overcurrent surge events but low enough to achieve adequate short-circuit withstand time for safe shut down.

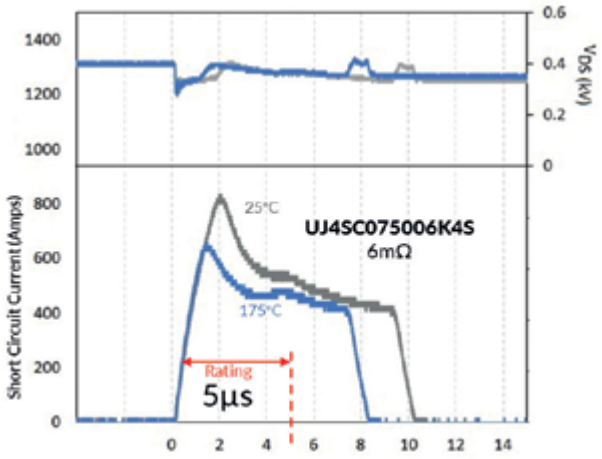


Figure 5: Short-circuit waveform of UJ4SC075006K4S 750V/6mOhm SiC FET, Vgs=15V, Vbus=400V, starting temperature = 25°C (grey) and 175°C (blue)

The UJ4SC075006K4S can be safely shut down with commercial gate drivers offering deSat protection. In the Figure 6, we've illustrated a phase leg short-circuit with UJ4SC075006K4S in both switch positions. The short-circuit detection and safe shut down with a commercial (ADuM4136) gate driver from Analog Devices [7] occurs when the V_{DS} of the low-side switch was above the deSat threshold (9.2V) after the blanking time of 312ns. In the test, the short-circuit current reaches a peak of 880A, respectively, before the device's self-heating reduces the fault current to approximately 500A prior to turn-off. The deSat protection safely shuts down the short-circuit within 2.7 microseconds, well below the UJ4SC075006K4S short-circuit withstand time rating of 5 microseconds.

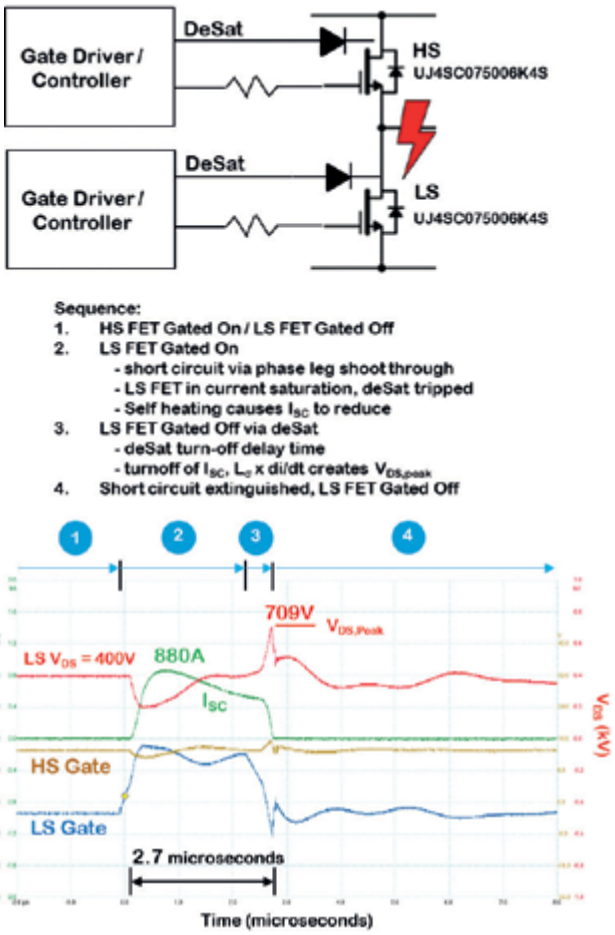


Figure 6: DeSat detection and shutdown example of UJ4SC075006K4S half-bridge w/ 400V dc-bus using commercial gate driver ADuM4136. Short-circuit turned off after 2.7us with low-side switch deSat engaged. Tested with Rg,ext=33ohms, V_{GS}=-5V/15V, Each FET has device snubber RsCs = 4.7ohm/680pF.

Conclusion

UnitedSiC (now Qorvo) has recently released the industry's lowest on-resistance 750V, 6mOhm SiC FET leveraging its 4th generation technology with breakthrough performance. By virtue of the excellent ruggedness afforded by its internal SiC JFET, this new FET offers designers a useable 5 microseconds of short-circuit withstand time, even at high temperature, without sacrificing on-resistance. The new UJ4SC075006K4S allows designers to use deSat protection found in standard drivers and is a great choice for 400V or 500V bus applications.

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