Power Packaging for the GaN Generation of Power Conversion

Since the launch of GaN-on-Si enhancement mode power transistors in March 2010 there has been a slow but monotonic shift towards adoption and replacement of silicon-based power MOSFETs. Initial adoption came from risk-taker visionaries in applications such as lidar, high-end audio amplifiers, robots, vehicle headlamps, and high-performance DC-DC converters.

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These were companies that had much to gain from the performance of these new-technology devices. EPC was the first company to go into mass production with our eGaN® FETs, all of which were in a controversial wafer level chip scale (WLCS) format such as in figure 1.

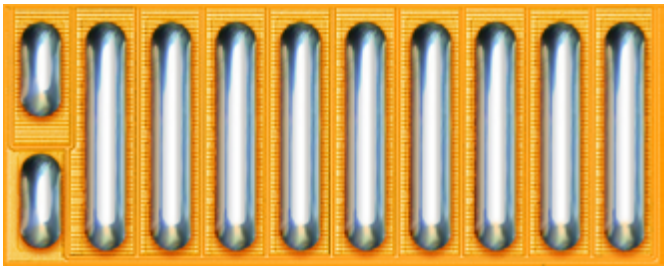

Figure 1: The 7 mm2 WLCS EPC1001 was among the first GaN-on-Si products introduced in March 2010 by EPC.

The reasoning behind the elimination of the packaging was that GaN devices were initially targeted at the highest performance requirements from early-adopter companies. These companies were primarily looking for speed and size reductions. Traditional power semiconductor packages had significant internal inductance and added a lot of size to a final design in addition to the actual GaN chip.

Over the next several years the applications and volume expanded by factors of hundreds and then thousands. The customer base for WLCS eGaN devices, which started to include integrated circuits in 2014, rose to over 1,000 active users in over 60 countries. Adoption rates, however varied depending upon the manufacturing capabilities of the companies purchasing the products. In some circumstances, particularly in lower volume applications, the small pitch between terminals as well as the brittle nature of the WLCS caused unwanted design iterations and increased manufacturing cost. For the expansion of GaN for power conversion to get beyond the early adopters, a more user-friendly format needed to be developed. This format, however, needed to preserve the key attributes of small size, low RDS(on), high speed, excellent thermal conductivity, and low cost. In other words, the best package would be the least amount of package technically possible.

Enter the PQFN

The Power Quad Flat No-Lead (PQFN) package was the logical starting point. EPC's PQFN design encases the GaN device with a minimum amount of epoxy along the sides of the device to protect against chipping during handling but leaves an exposed substrate that can be used as a thermal pad on the upper surface as shown in figure 2. This upper surface is designated "case" and is connected to source potential for discrete devices. For power stage integrated circuits it is tied to the source of the low-side FET. The opposite side of the device contacts with the printed circuit board (PCB) in the same manner as for WLCS devices and is designated "board".

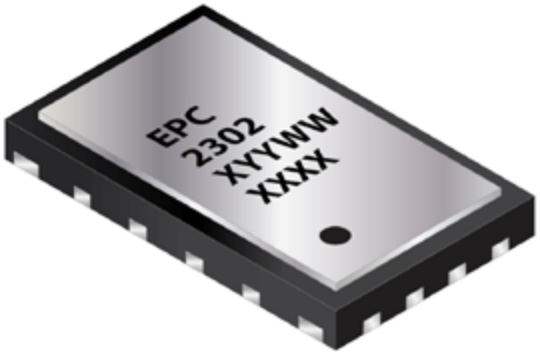

Figure 2: eGaN FET in a PQFN package.

Figure 3 shows a cross section comparison between the WLCS and PQFN devices and highlights some key differences and similarities together with the thermal paths from junction to board and case.

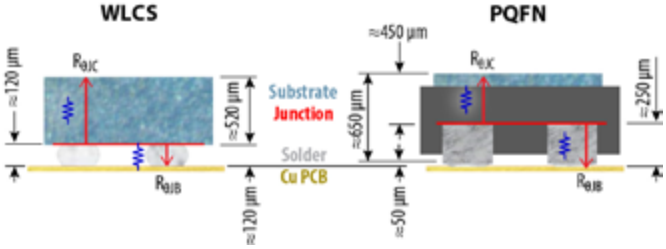

Figure 3: Cross-sectional view comparison between the WLCS and PQFN eGaN FETs with junction to board and case thermal resistances highlighted.

At its best, the size adder from this packaging approach is about 20%. For the largest GaN device in a 3mm x 5 mm the PQFN increases the outside dimension from 12.5 mm^2 to 15 mm^2. There is no significant increase in package inductance or resistance compared with a WLCS device and therefore there is no measurable impact on conduction losses, switching speed, or EMI-generating ringing.

Thermal performance is also quite comparable to WLCS devices. A comparison between the thermal resistances of eGaN FETs and Si MOSFET in various packages can be made with junction-to-board ($R_{\theta JB}$) shown in figure 4 and junction-to-case ($R_{\theta JC}$) shown in figure 5. The metric used for the device areas is the outer dimensions of the packaged part.

Figure 4 shows that the PQFN packaged eGaN FET has higher thermal resistance of junction-to-board compared to WLCS devices, but the difference is small due to the high thermal conductivity of the materials in this path and larger device area. The overall area for eGaN FETs, however, is smaller than packaged MOSFET devices and the best method to overcome this is by PCB design that effectively increases the heat-spreading area of the GaN FETs [2,3,4]. All PCB

layout and thermal techniques applicable to WLCS devices remain applicable to PQFN devices too. Thus, when all the devices, eGaN FETs and Si MOSFETs, are compared on a PCB level from junction to ambient, the thermal differences become negligible [3]. When relying on PCB only cooling, the key converter performance improvements are driven by eGaN FETs superior electrical characteristics over that of Si MOSFETs [5].

Figure 5 shows that the PQFN packaged devices have *lower* thermal resistance of junction-to-case compared to WLCS devices due mainly to the thinner substrate that improves the ability to cool the devices when using a heatsink [1,4,5,6]. The difference in comparison with Si MOSFETS becomes even greater, including dual sided cooling packages such as Super SO8 Dual Cool [7].

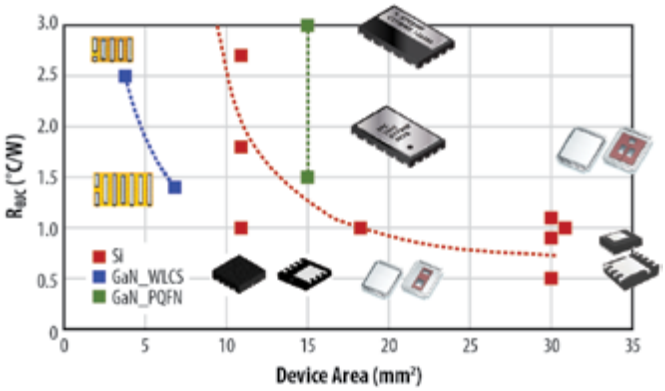

Figure 4: Junction to board thermal resistance comparison of various devices and packages.

Additional PQFN Advantages

One of the key reasons GaN power devices are so small is the lateral conduction of electrons through a two-dimensional electron gas (2DEG) [5]. This lateral conduction mechanism results in a significant contribution to the final device $R_{DS(on)}$ coming from metal layers deposited during wafer processing. The farther apart the WLCS bumps or bars, the higher the $R_{DS(on)}$ of the final device. This is the basic reason for the tight pitch found on WLCS devices. With the addition of a copper leadframe in the PQFN package, the spacing between the terminals can be expanded to meet IPC-2221A [3] creepage and clearance requirements without sacrificing device conductivity. In addition, by extending the leadframe to the edge of the device the flanks become solderable, leading to improved thermal cycling capabilities and easier manufacturing process controls that visually inspect for thorough solder coverage.

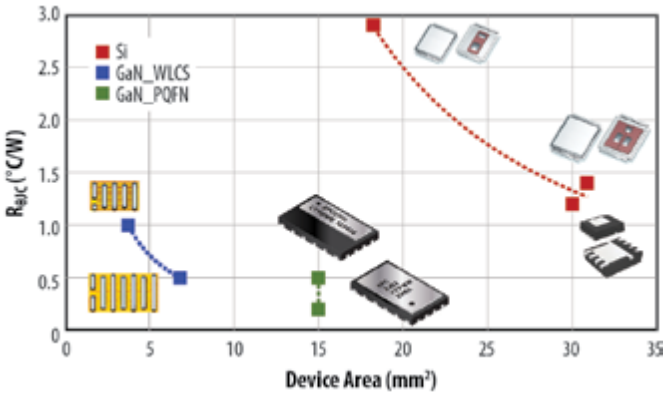

Figure 5: Junction to case thermal resistance comparison of various devices and packages.

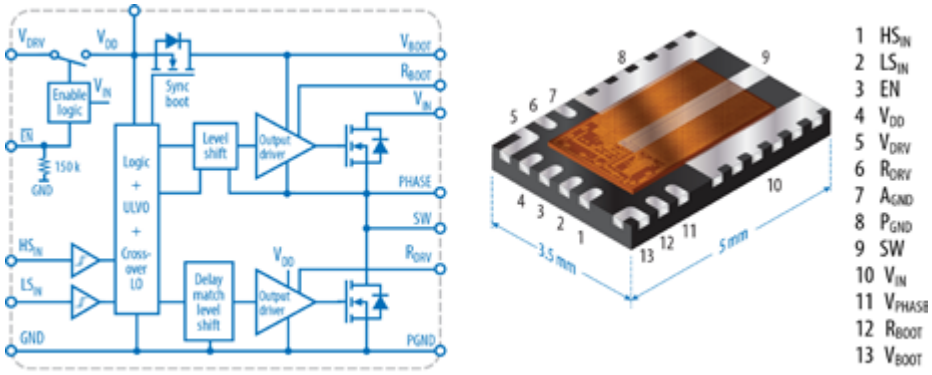

Figure 6: Detailed block diagram symbol and photo with pin assignments of the EPC23102.

For integrated circuits there is the added advantage of enabling more output pins without significantly increasing die area. Figure 6 shows a block diagram and a see-through illustration of the EPC23102 GaN monolithic power stage IC in a PQFN [8].

Summary

GaN transistors and ICs in PQFN packages maintain the performance and size advantages of WLCS GaN devices that are in widespread use in demanding applications such as automotive, satellites, enterprise computing, and e-mobility. Advantages include ease of manufacturing, excellent thermal performance, wider lead spacing in conformance with IPC-2221A standards, and, in the case of integrated circuits, the ability to accommodate a higher pin count. Indications are strong that this highly optimized package is attracting a broader group of customers with faster design cycle requirements.

References

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