Towards Vertical GaN Power ICs

Two trends are currently emerging in GaN power technologies: One the one hand, the monolithic integration of system peripherals to the power transistor, which can reduce system costs, the bill of materials and, last but not least, improve performance. On the other hand, vertical transistors are being developed to increase breakdown voltages and thus achieving higher switching power. Combining lateral and vertical geometry is the aim of Fraunhofer IAF with the development of vertical GaN power ICs and their related technologies.

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Combining the best of both worlds is the motto behind the development of vertical GaN power ICs. The lateral GaN technology with its HEMT-design has revolutionized the field of power electronics as it offers significant performance advantages and increasingly lower costs compared to conventional Si-based power transistors. Another benefit of the lateral structure is the potential of integrating active or passive devices to the GaN power HEMT on-chip, enabling functions like gate drivers, sensing or protection circuits—known as a GaN power IC or GaN power integration. However, commercial lateral GaN transistors currently have a limited breakdown voltage of typically 650 V (in some cases even 1200 V since a few years) and a switching power capability of a few kilowatts. The aim is to overcome these limitations with vertical GaN transistors, which also have the advantage of increasing the breakdown voltage without enlarging the chip size. Furthermore, the reliability and thermal management can be improved by moving the peak electric field and dissipation of heat from the surface into the bulk substrate. There are four major vertical GaN device approaches such as Trench MOSFET, FinFET, JFET, and CAVET (current aperture vertical electron transistor). Toyoda, Panasonic, or Start-Ups like Oddysey Semiconductor and the recently dissolved NexGen Power Systems already showed promising normally-off vertical GaN transistors, but these are not yet commercially available. One of the biggest challenges currently facing vertical GaN devices is their economic viability, mainly due to the high cost of GaN wafers. Today, 6-inch GaN substrates are under development, while 2- and 4-inch are in mass production [1], but the cost of wafer including epitaxial layers is currently high at 40-60$/cm² compared of ~7$/cm² for 4-inch SiC [2] or ~1$/cm² for 8-inch GaN-on-Si [2]. This relatively high price must be reduced to ensure the breakthrough of vertical GaN transistors despite a theoretical improvement in the unipolar $R_{ON} \times A$ figure-of-merit compared to SiC MOSFETs. In the above-mentioned vertical device structures, only the CAVET features the same heterostructure as the conventional HEMT with the same gate module. While different epitaxial layers are used as vertical depletion zone, the process technology can be widely adopted from the known lateral devices. This unique selling point of the CAVET opens a way to continue lateral GaN power integration in vertical device concepts to a vertical GaN power IC (see Figure 1) and could become a promising vertical structure of the future.

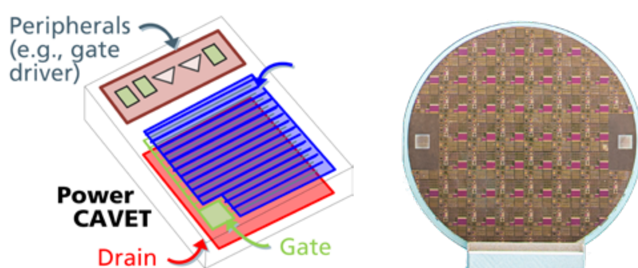

Figure 1: a) Schematic 3D view of a vertical GaN power IC and b) photograph of a fully processed 2-inch GaN-on-GaN wafer.

Co-Integration of Lateral HEMTs and Vertical Power CAVET

The Fraunhofer IAF has developed a technology, which combines a co-integrated large-area vertical GaN power transistor with lateral devices for the realization of peripheral functions on a single chip. The aforementioned CAVET combines a well-known gate module of the lateral HEMT with a vertical depletion- and drift-zone. Consequently, the same normally-off concepts used for the HEMT (e.g., p-GaN gate) can be applied to the CAVET. This technology starts with a highly negatively doped (n^+) GaN substrate and subsequent homoepitaxy, which has significantly better dislocation densities than heteroepitaxy on foreign substrates such as Si or Sapphire and can therefore positively influence breakdown voltage and reliability. With the help of MOCVD (metal-organic chemical vapor deposition), a weaker n-doped (n^-) GaN layer with a few micrometers is grown on top, which serves as a depletion- and drift-zone. A positively doped (p) GaN current blocking layer (CBL) is then manufactured by Mg-implantation, which acts as an insulating layer separating the source from the drain, while an aperture allows vertical current flow below the gate area. Finally, an un-intentionally doped (uid)-GaN channel, an AlGaN heterostructure and a GaN cap or alternatively p-GaN are regrown above, which build the access region of the vertical transistor and the channel region of the lateral HEMTs. The devices are fabricated in our III-V process line. Details on the epitaxy and fabrication can be found in [3–6]. The same active and passive components as in the lateral GaN technologies are available. Figure 1b) shows fully processed 2-inch GaN-on-GaN wafer, which could also be realized on larger diameters in future. A simplified cross-section of the technology and a TEM cross-sectional image of a fabricated CAVET are shown in Figure 2a) and c).

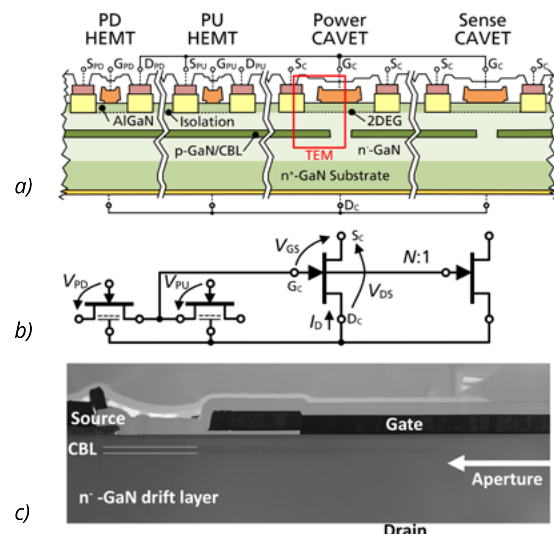

Figure 2: CAVET technology with quasi-monolithic integrated HEMT gate driver stage and sense CAVET as a) simplified cross-section and b) corresponding circuit diagram. c) TEM image of a section of the vertical CAVET device marked in red in a).

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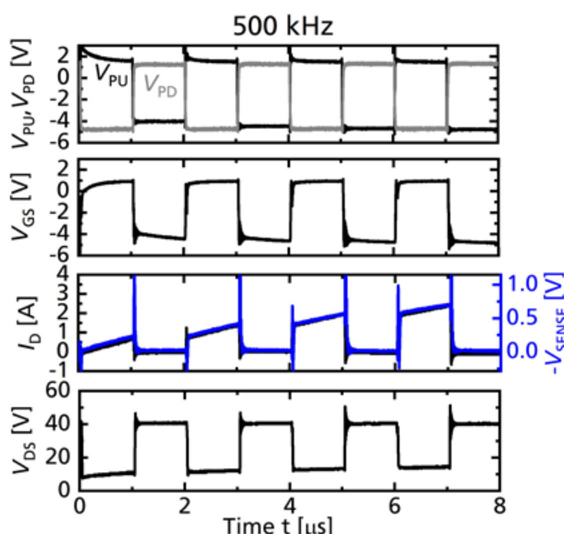

Figure 3: Switching measurement of the power CAVET device controlled by lateral co-integrated HEMTs and sense CAVET at 500 kHz and 40 V.

Experimental Results

To demonstrate the development towards vertical GaN power ICs, several vertical and lateral devices were manufactured in the same technology. After processing, the components were diced for flexibility reasons, but should behave like monolithically integrated on one die/chip if the backside or drain potential D_C is the same or connected together, see circuit diagram in Figure 2b). The experimental proof-of-concept is shown using a large-area CAVET power device controlled by a quasi-monolithically integrated lateral HEMT push-pull driver stage with current sensing via a sense CAVET. Figure 2b) shows the corresponding circuit diagram/symbols and indicates the current direction (lateral vs. vertical) by the orientation of the symbols. The push-pull HEMT stage consists of a pull-up/down (PU/PD) transistor and the current-mirror ratio N is ~229.

The GaN-based devices were statically characterized in detail and presented in [3–6]. The dynamic switching measurements are carried out in a double-pulse test setup at 40 V, up to 2.4 A, and 500 kHz and the gate-source voltage of the PU/PD device V_{PU}/V_{PD}, the gate-source voltage of the power CAVET V_{GS}, which corresponds to the V_{GS} of the sense CAVET, the drain-current I_D and drain-source voltage V_{DS} of the power CAVET are shown in Figure 3. The drain current of the power CAVET is measured by a voltage drop of a coaxial shunt and the mirrored current through the sense transistor is converted into the voltage V_{SENSE} using an external transimpedance amplifier. Further details of the GaN gate driver stage with more switching measurements are given in [4] while more information on the current monitoring is given in [5].

Summary

The development of vertical GaN power ICs aims to merge the benefits of lateral GaN technology with a vertical transistor structure. Not only traditional parameters such as higher voltage and current should be addressed, but also the advantage of monolithic functional integration and the associated reduction in system costs. This is intended to provide a further sales argument for the vertical GaN transistors, which are currently still in an early development state, and commercially rarely available. However, the research results show their great potential. Vertical GaN power ICs will push the performance of this technology even further and will be continued in ongoing projects at Fraunhofer IAF.

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