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Electronics in Motion and Conversion

March 2018

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Bodo's Power Systems is available for the following subscription charges: Annual charge (12 issues) is 150 € world wide

Single issue is 18 € subscription@bodospower.com

circulation print run 24 000

Printing by:

Brühlsche Universitätsdruckerei GmbH & Co KG; 35396 Gießen, Germany

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Waiting for Spring !

APEC in San Antonio: Texas gets the power family together again. It is always a great opportunity in March for a nice warm place to work, and moving important information out to engineers who will develop the more efficient designs of the future.

With wide band gap devices we have new challenges – getting the packaging right and the passive components to match the speed and thermal performance of GaN and SiC devices. All manufactures of power semiconductors are facing up to the challenge of SiC and or GaN. We see GaN now up to a kilovolt or a little above. SiC is capable of several kilovolts for applications that require high voltage. The future is in improved efficiency over previous designs. Products have become mature and applications are running at end users.

Wide Band Gap devices have paved a road to our future designs. We are now in a phase of adoption that requires a wider group of engineers to get familiar with wide band gap devices for their new designs. Higher switching speed, potentially higher temperature, and lower losses present challenges: for passive components, for the measurement of signals, and for switching interference. APEC in San Antonio is a place for experts to present their latest developments. We will be present with our team to get you up to date with their progress.

It is important that we have enough power to speak out for freedom in the world.

I still look forward to see fair treatment of journalists in the world. It is not acceptable



that journalists be held in jail, without any accusation, for a full year. Too bad if their reports are critical of what they see. We have to work for the freedom for Deniz Yücel. Journalism keeps freedom alive for us all – there are innumerable examples from our past to teach us.

Bodo's Power Systems reaches readers across the globe. If you are using any kind of tablet or smart phone, you will find all of our content on the new website www.eepower. com. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com

My Green Power Tip for March:

If it is cold outside and freezing, wear an extra pullover. You will be able to do more walking in wintertime.

PCIM 2018

Nuremberg, Germany, June 5-7 www.mesago.de/en/PCIM/The conference/

Welcome/index.htm

SMT Hybrid Packaging 2018

Nuremberg, Germany, June 5-7 https://www.mesago.de/en/SMT/For_visitors/

Welcome/index.htm

SCAPE 2018

Stockholm, Sweden, June 11-12

www.acreo.se/projects/sic-power-center

CWIEME Berlin 2018, Germany, June 19-21,

www.coilwindingexpo.com/berlin

Best Regards

APEC 2018

San Antonio TX, USA, March 4-8 www.apec-conf.org

Power Electronics Expo 2018 Telford, UK, March 15 www.powerelectronicsexpo.co.uk

CIPS 2018

Stuttgart, Germany, March 20-22 www.cips-conference.de

AMPER 2018

Brno, Czech Republic, March 20-23 www.amper.cz/en.html

Smartsystemintegration 2018 Dresden, Germany, April 11-12 www.mesago.de/en/SSI/home.htm

Events

SEMICON Southeast Asia 2018 Kuala Lumpur, Malaysia, May 8-10 www.semiconsea.org

> IPEC ECCE Asia 2018 Niigata, Japan, May 20-24 www.ipec2018.org

HEVC 2018 London, United Kingdom, 27-28 June http://events.theiet.org/hevc

> ISPSD 2018 Chicago IL, USA, May 13-17 www.ispsd2018.com

EV Tech Expo 2018 Hannover, Germany, May 15-17 http://www.evtechexpo.eu

March 2018

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Enargy Power Signs Distribution Agreement with WPG Americas

Enargy Power announced that it has signed a non-exclusive distribution contract with WPG Americas headquartered in San Jose, CA. The agreement covers the sale of Enargy's products within the North America market and enables servicing of contract manufacturers globally. The agreement is a significant advancement in Enargy Power's efforts to expand customer base in the U.S. market. Enargy Power's products, now available from WPG Americas, are focused on low and medium power desktop power adapters for medical and industrial applications. Enargy's ultra-thin AC/DC desktop BladeAdapters[™] with 60W and 90W power ratings are IEC60601-1 certified and meet 4th Edition EMC and DoE Level VI efficiency requirements. These industry-leading medical-grade AC/DC adapters are complimented by other desktop solutions with power ratings from 36W to 160W. "WPG Americas is our first distribution partnership in North America," commented Todd Hendrix, Director of Sales & Marketing at Enargy Power. "The relationship greatly enhances our fulfilment and business development capabilities for fast growing small and medium sized manufacturers of medical devices and industrial equipment." "The addition of Enargy Power's extensive range of cost-effective AC-DC supplies allows WPG Americas to offer our customer base a unique, cost effective solution," said Rich Davis, President, WPG Americas. "This agreement positions us to address the power requirements for general medical device applications and especially the high-growth home healthcare marketplace."

www.enargypower.com

Peregrine Semiconductor Is Now pSemi™

Peregrine Semiconductor Corporation announced its corporate name change to pSemi[™] Corporation, a Murata company focused on semiconductor integration. The name change coincides with two major milestones—the company's 30-year anniversary of RF-CMOS innovation and the shipment of its 4 billionth chip. pSemi will serve as Murata's semiconductor arm and is tasked with growing rapidly to support its expanding product portfolio and the hiring of engineers and professionals globally.

The new name is derived from Peregrine Semiconductor and reflects its proud 30-year history. pSemi will have the same experienced semiconductor team at the helm, but it will have a broader scope and an expanded product portfolio. Building on its strong foundation in RF integration, pSemi's product portfolio will span power management, connected sensors, optical transceivers, antenna tuning and RF frontends.

"We've challenged the pSemi team to broaden their scope, increase their intellectual property (IP) portfolio and grow on a global scale



to support more semiconductor innovations," says Norio Nakajima, senior executive vice president, module business unit at Murata. "As a Murata company, pSemi will leverage the breadth of Murata's manufacturing and technology leadership, while maintaining a level of autonomy that accelerates its path to semiconductor integration. pSemi will serve as the hub for Murata's semiconductor activities, and we are investing in its aggressive growth strategy to fuel our move into more advanced and intelligent modules."

www.psemi.com

Device and Packaging Technology for High-Frequency Power Conversion

The Power Sources Manufacturers Association (PSMA) Semiconductor Committee is sponsoring the Industry Session at APEC 2018 titled "Latest Advances in Device and Package Technology for High-Power, High-Frequency Switching Devices." The session will take place on Tuesday, March 6th, 2018, from 8:30 a.m. to 11:55 a.m. in Room 206 of the Henry B. Gonzalez Convention Center in San Antonio, Texas. Focusing on new and evolving technologies and applications that play important roles in power electronics, Industry Session (IS01) comprises seven technology presentations by experts from Navitas, VisIC, Infineon Technologies, GeneSiC, Unted Silicon Carbide and Microsemi Corporation. The purpose of this session is to provide an overview of advanced topologies and applications operating at high frequencies – and how they are enabled by the latest silicon and wide bandgap power devices. The session's presentations will cover a wide representation of silicon (Si), Gallium Nitride (GaN) and Silicon Carbide (SiC) topics.

One of the key motivations of this session is to alert the community to new applications operating at high frequencies and to show them how these applications are being enabled by the latest semiconductor devices, particularly wide bandgap (WBG) devices. In addition to being very informative, this Industry Session will provide an opportunity for attendees to interact with other professionals who are active in this area and to learn about the present and future impact of power semiconductors on the power electronics industry. Tim McDonald, Chairman of the PSMA Semiconductor Committee, encourages APEC attendees to register and attend this valuable industry session, and to consider participating in the other PSMA-sponsored meetings during the week.

www.psma.com

Features InFORMS[®] Preforms and Reinforced Solder Ribbon at APEC 2018

Indium Corporation is redefining solder with its InFORMS preforms and patent-pending solder ribbon for automated assembly. According to Seth Homer, Product Manager, InFORMS are a composite fabrication consisting of solder and a reinforcing matrix that stabilizes bondline thickness. "Using an InFORM between the baseplate and substrate will ensure bondline planarity, giving your assembly

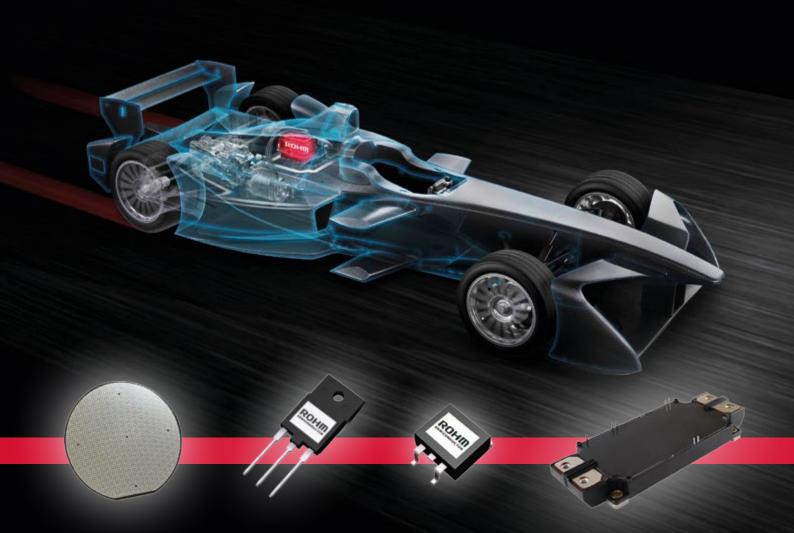
a much more stable joint and increasing the reliability of your end product."

InFORMS are available in a variety of alloys, including SAC and SnPb alloys.

www.indium.com/inform

SMALLER STRONGER FASTER





The Formula E Venturi team has adapted the latest range of ROHM inverters derived from full SiC module technology in its electric-powered racing cars. ROHM has enabled the broad implementation of e-mobility by delivering the next generation of power semiconductor-based SiC modules. It produces these in-house using a vertically integrated manufacturing system, thus guaranteeing high quality and consistent supply to the market.

SMALLER

SiC technology allows the chip to be reduced in size, leading to a SMALLER inverter in terms of dimensions and weight.

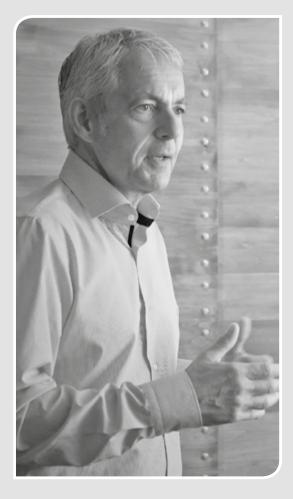
STRONGER

SiC increases thermal efficiency and power density for a STRONGER performance.

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SiC helps vehicles to cross the finish line FASTER and supports fast-charging solutions.





NON HIRING

More Than a Few Great Men and Women

Innovative Semiconductor Company Makes Big Push to Attract the Best and Brightest

An Interview with CEO Stefan Wolff by JT Konstanturos

tefan Wolff is someone who tells it like it is. The pragmatic CEO of pSemi™, a company with 30 years of RFIC history and backed by electronics giant Murata, speaks with passion and a deep understanding of what is expected to attract top engineers in today's competitive marketplace. Wolff's direct, nononsense demeanor makes a strong case for anyone looking for a workplace that encourages people to reach their highest potential while working on products that will shape our connected world.

JTK: Thanks for taking the time to speak to me. Tell me about the new name, pSemi, and what the future holds.

SW: The pleasure is mine. I thrive on the exciting time this is for pSemi, and it is a privilege being its CEO. pSemi was formed to provide focus and resources to take semiconductors to the next level. Our new name is derived from Peregrine Semiconductor and reflects its proud 30-year RFIC history. Fastforward to the present: We are a Murata company with the backing and integrity of that electronics giant. Murata has challenged us to broaden our scope, increase our IP and grow on a global scale to support inventions that are coming in our not-so-distant future.

JTK: What sets pSemi apart from other semiconductor companies, and what's different now?

SW: We are innovation junkies pure and simple. With well over 500 issued and pending patents, our patent portfolio was named one of the technology world's most valuable portfolios by the *IEEE Spectrum* "Patent Power Scorecard" for the last two years. What that says is our patents are not only innovative but very useful to the industries we serve. So, what is different now? The industries we serve are growing. Smaller, faster, lighter is the mantra we hear all the time from inventor companies, and we are rising to meet that challenge through very novel and intelligent semiconductor integration and packaging.

JTK: Sounds like quite a challenge. When will you reach your goal?

SW: The honest answer to that question is never. You can't stand still in this time of electronic revolution. You have to keep moving forward at all times to succeed. We have never shied away from the tough challenges, and now is not the time to start.

JTK: What does pSemi have to offer the best and brightest engineers?

SW: We are growing, and we are hiring. pSemi offers an engineering-driven environment with fascinating projects for

perfect San Diego lifestyle.

And yes, we do take full advantage of it all! Even beyond San Diego, pSemi has offices around the world—and plans to have offices—wherever there is a hub of semiconductor talent that supports our growing "dream team."

JTK: How do you plan to build your "dream team" of engineers?

SW: Well, we are already making it happen. With the right people, we will get there even faster. This year alone, we have acquired businesses and hired entire teams. Chip designers frequently do not leave a to know everything about our industry; no one does. I ask a lot of questions, and I really want to hear what our employees think. I do have a few expectations of our employees. First and foremost is respect. We expect it at all levels. Not far behind is integrity. That means we tell the truth. You can expect me to tell the truth, and I will expect the same. The truth has no politics and no taboo subjects. If it will make the company better, it should be talked about candidly. Third is quality and customer satisfaction. We strive for it in everything we do. Our customers

"We are growing, and we are hiring. pSemi offers an engineer-friendly environment with fascinating projects...and a work-hard, play-hard philosophy."

challenging applications like 5G, IoT and battery management. Since our inception, we have invented breakthrough technologies for emerging markets, such as switches and antenna tuners for smartphones in the 2000s, and today, we are spearheading Murata's efforts in new semiconductor growth markets. The foundation of our whole-person support is a workhard, play-hard philosophy. Yes, that means we have wellness programs, parties and special-recognition dinners, and yes, our headquarters are near beautiful beaches with the

job they hate because they love their team. We say, "No problem. We will take the entire team too if they are the right fit." We are leaning on our "dream team" to design the products of the future. Think smartphones, small cells, portable computing, data centers, smart homes, electric vehicles and healthcare. It is an exciting time in our industry, and we are grateful to have the backing and support of Murata in this next chapter.

JTK: Any last words?

SW: Definitely! I do not pretend

expect it, our parent company is known for it, and it makes us proud of our efforts. Last, but not least, is teamwork. Without it, we can't do any of this. We are so fortunate that our parent company not only shares these values but has weaved them into every aspect of their business.

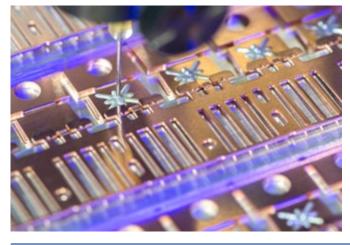
If you would like to join our team, I would like to hear from you. Please send your resume to Stefan@psemi.com. For more about pSemi and our innovative products, please go to psemi.com.



ADVERTORIAL

Heraeus Electronics and Nihon Handa agree on Patent Cross-License

Heraeus Electronics is strengthening its collaboration with Nihon Handa by concluding a cross-license agreement for sinter pastes. The Japanese company is a global manufacturer of materials and equipment for the electronics industry. The cross-license will provide both companies' clients with access to a wide product portfolio. Both



companies have long-standing expertise in sinter technologies. Sinter pastes are used particularly in power electronics modules. The two patent portfolios in combination refer to various aspects such as morphology, metallic particle size, or sintering tools. Health aspects and price competitiveness have led Heraeus Electronics and Nihon Handa to use micro silver powder rather than nanopowder. "With the patent cross-license we strengthen our leading material competence and support our customers more targeted with innovative products," said Dr. Frank Stietz, President of Heraeus Electronics Global Business Unit. He also states, "Only through substantial investments in research and development can we meet today's demand in power electronics. Therefore, the protection of our technology by patents is an important element of our strategy, which we enforce worldwide." Mr. Makoto Asami, President of Nihon Handa, also comments that global compliance of fair trade and protection of intellectual property rights are indispensable for proper advancement in technology and innovation in our electronic industry.

www.heraeus.com

www.nihonhanda.com

Würth Elektronik honoured for INTAKT

The INTAKT BMBF innovation cluster, which was organised by IBMT in Frauenhof, was one of the 100 innovative award winners in the "Extraordinary places in the land of ideas 2017" competition. It was



presented with the award at a celebratory awards ceremony that took place on 26 June 2017 in Berlin. The award consisted of a certificate which was signed by the German Federal President as well as a commemorative plaque. A panel of judges of the highest calibre judges chose INTAKT from around 1,000 entries. The "Germany – land of ideas" initiative and the Deutsche Bank have been coming together to host the competition now for twelve years.

The BMBF INTAKT (interactive microimplants) innovation cluster, beat out around 1,000 other entries to be crowned one of the 100 innovative prize winners by a high calibre panel of judges at the "Extraordinary places in the Land of Ideas 2017" competition.

Würth Elektronik is researching new biocompatible materials, the properties that make such materials biocompatible, as well how to process the materials for circuit board production. Moreover, we tested new approaches in order to successfully transfer energy using etched planar coils or embedded inductivity.

www.we-online.com

PSMA's Safety & Compliance Committee to Host APEC Industry Sessions The Power Sources Manufacturers Association (PSMA) Safety & day, March 6, from 8:30 a.m. to 11:55 a.m. I

The Power Sources Manufacturers Association (PSMA) Safety & Compliance Technical Committee is sponsoring two Industry Sessions as part of APEC 2018. The sessions are: "Comparisons and Tradeoffs of Integrated Gate Driver Isolation Technologies" (IS04) and "Isolation Topics in Power Supply Applications" (IS09). Both sessions will take place in Room 4 of the Henry B. Gonzalez Convention Center, San Antonio, Texas, during the APEC conference. The sessions feature presentations by industry experts and are designed to include ample time for audience participation during the Q&A period following each talk.

Session IS04 on gate driver isolation techniques will be held on Tues-

day, March 6, from 8:30 a.m. to 11:55 a.m. For this session, seven industry experts will provide the presentations.

PSMA Safety & Compliance co-chairs, Kevin Parmenter of Excelsys (an AEI company) and Jim Spangler of Spangler Prototype, issued a joint statement: "Isolation techniques and strategies are of growing importance as designers contend with higher switching speeds. We look forward to two lively and informative sessions. We encourage attendees of APEC 2018 to attend these and other PSMA-sponsored meetings during the week."

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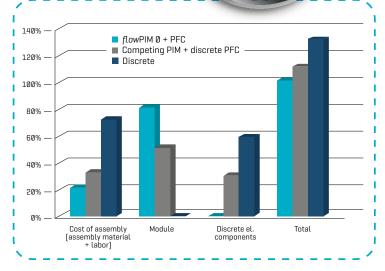
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In addition to the Technical Center, the Analytical Center is the heart of the daily customer support provided by Zestron's Application Technology department. In the Technical Center, customers have the opportunity to compare cleaning systems from leading manufacturers and test them with their own electronic assemblies or SMT stencils under real production conditions before making a purchase decision. They also have access to a wide range of analysis methods for purity qualification in the Analytical Center. These are of great relevance, for subsequent protective coating processes or wire bonding, and many others. Therefore, Zestron's customers have the option of ensuring surface quality directly after cleaning tests using high-resolution methods. For this purpose, methods such as ionic contamination measurement, ion chromatography, particle extraction and analysis and others are available. Thus, PCBs are safely checked in accordance with IPC, VDA or ISO standards.

After tests are done, customers receive a comprehensive technical report including test documentation and recommendation for the cleaning process as well as suitable analysis methods.

www.zestron.com

Pre-APEC Power Magnetics at High-Frequency Workshop

The Power Sources Manufacturers Association (PSMA) and the IEEE Power Electronics Society (IEEE PELS) are jointly sponsoring the third high-frequency magnetics workshop, "Power Magnetics @ High Frequency – Eliminating the Smoke and Mirrors," on Saturday, March 3, 2018. The workshop will be conducted on the day before and in the same venue as APEC 2018 at the Henry B. Gonzalez Convention Center in San Antonio, Texas.

This day-long event will continue the workshop series' focus on identifying the latest improvements in magnetic materials, coil (winding) design, construction and fabrication, evaluation and characterization techniques and modelling and simulation tools to target the technical expectations and requirements of higher application frequencies while addressing two specific issues of interest: measurement and reporting of data to improve modelling of ac power loss measurements and the impacts of fringing effects on power magnetics performance. The target audience for this workshop is anyone working to achieve higher power densities, low profile aspect ratio, higher efficiencies and improved thermal performance.

The first two workshops were completely sold out, so individuals interested in attending this year's event are encouraged to register early.

www.psma.com/technical-forums/magnetics/workshop

ROHM Semiconductor Opens Test Lab for Power Components



Christian André

With its newly established European "Power Lab", ROHM Semiconductor demonstrates the deployment of its global strategy on the Power semiconductor's market in Europe which is one of the very potential regions for Power devices. "Quality is our top priority" has been the company mission statement for 60 years. The new state-of-the-art power electronics lab confirms this high standard.

The Power Lab is located at the European Headquarter facilities at the

Willich-Münchheide location near Dusseldorf. The project took several months and ended with the TÜV's approval in 2017. The 300m² lab's purpose is the analysis of power components and systems to provide the customers with the best support at the application level. To that end, the test lab is equipped with several test benches with a separate high voltage area.

"Electric vehicles, charging station infrastructure, industrial machinery, solar and wind power plants as well as white goods such as washing

machines require more and more Power semiconductors to comply with the energy efficiency requirements, which have to be tested and validated at early stage of the development phase", explains Head of the Power Lab Aly Mashaly, Manager Power Systems Department. "Because there were no suitable test benches on the market, we decided to develop and design the test benches based on our own requirements subsequently. In this way, we ensure the high scalability of the test benches and their flexibility for future modifications." The test benches have the state-of-the-art laboratory equipment using latest technologies with high safety features.

ROHM can electrically characterize all of its semiconductor components like SiC MOSFET Transistor, SiC Diode, IGBT, Si Power MOSFET Transistor and Gate driver, just to name some of them, with voltages up to 8000VDC.

This investment shows our determination to be one of the major suppliers in SiC and Si Power discrete and integrated device technologies, thus to play an important role in the growing power market," says Christian André, President ROHM Europe. "The new Power Lab is a central piece of our quality and reliability scheme."

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Hitachi Europe Limited, Power Device Division email pdd@hitachi-eu.com

Littelfuse Completes Acquisition of IXYS Corporation

Littelfuse, Inc. announced the completion of its acquisition of IXYS. IXYS is a global pioneer in the power semiconductor market with a focus on medium- to high-voltage power semiconductors across the industrial, communications, consumer and medical device markets. "Today marks a significant step forward in our company strategy to accelerate growth within the power control and industrial OEM markets," said Dave Heinzmann, President and Chief Executive Officer of Littelfuse. "The combination of our companies brings together a broad power semiconductor portfolio, complementary technology expertise and a strong talent pool."

The transaction is expected to be immediately accretive to adjusted EPS. Littlefuse expects to achieve more than \$30 million of annualized cost savings within the first two years after closing. The combination is also expected to create significant revenue synergy opportunities longer term, given the companies' complementary offerings and combined customer base. In conjunction with the close of the transaction, IXYS founder Dr. Nathan Zommer has been appointed to the Littlefuse Board of Directors, increasing the size of the board to nine members.



Expertise Applied Answers Delivered

With today's transaction close, each former IXYS stockholder is entitled to receive, per IXYS share held immediately prior to the closing, either \$23.00 in cash or 0.1265 of a share of Littelfuse common stock. In total, 50% of IXYS stock was converted into the cash consideration and 50% into the stock consideration.

www.littelfuse.com

Space Industry's First Radiation-Hardened 100V and 200V GaN FET Power Supply Solutions

Renesas Electronics announced the space industry's first radiationhardened, low side Gallium Nitride (GaN) field effect transistor (FET) driver and GaN FETs that enable primary and secondary DC/DC converter power supplies in launch vehicles and satellites, as well as downhole drilling and high reliability industrial applications. These devices power ferrite switch drivers, motor control driver circuits, heater control modules, embedded command modules, 100V and 28V power conditioning, and redundancy switching systems.

The ISL7023SEH 100V, 60A GaN FET and ISL70024SEH 200V, 7.5A GaN FET use the base die manufactured by Efficient Power Conversion Corporation (EPC). The GaN FETs provide up to 10 orders of magnitude better performance than silicon MOSFETs while reducing package size by 50 percent. They also reduce power supply weight and achieve higher power efficiency with less switching power loss. At 5m Ω (RDSON) and 14nC (QG), the ISL70023SEH enables the industry's best figure of merit (FOM). Both GaN FETs require less heat sinking due to reduced parasitic elements, and their ability to operate at high frequencies allows the use of smaller output filters, which achieve excellent efficiencies in a compact solution size. Manufactured using a MIL-PRF-38535 Class V-like flow, the ISL70023SEH and ISL70024SEH offer guaranteed electrical specifications over the military temperature range and lot-by-lot radiation assurance for high dose rate 100krad(Si) and low dose rate 75krad(Si).

"We are pleased to see Renesas Electronics continue Intersil's six decades of spaceflight product development and leadership," said Alex Lidow, EPC's co-founder and CEO. "It is especially gratify-



ing and exciting to see our innovative enhancement-mode gallium nitride-on-silicon (eGaN®) FET technology at work with Renesas' new radiation-hardened GaN FET driver. These products demonstrate how eGaN technology increases the performance and reduces the cost for applications currently being served by MOSFETs."

www.intersil.com/products/isl70040seh

www.renesas.com

Indium Corporation Senior Product Manager to Present at APEC 2018



Indium Corporation's Andy C. Mackie, PhD, MSc, Senior Product Manager, Semiconductor and Advanced Assembly Materials, will present at APEC 2018, March 4-8 in San Antonio, Texas

Dr. Mackie will present Joining Materials' Reliability for Evolving Power Applications. This presentation will discuss the impact of form, application, and regulatory considerations on materials design criteria. It will also demonstrate how one materials supplier is meeting the plethora of customer needs for analog and power device manufacturability and reliability.

Dr. Mackie is an electronics industry expert in physical chemistry, surface chemistry, rheology, and semiconductor assembly materials and processes. He has more than 20 years of experience in new product and process development, and materials marketing in all areas of electronics manufacturing, from wafer fabrication to semiconductor packaging and electronics assembly.

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- Libraries and design examples to jump start your development
- ▶ Feature-rich dsPIC33EP "GS" family of DSCs







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VersaSense Honored with IoT Sensor Company of the Year

VersaSense, an exclusive supplier of Industrial IoT products for Digi-Key Electronics has been selected as the winner of the 2018 "IoT Sensor Company of the Year" award from IoT Breakthrough.



The mission of the IoT Breakthrough Awards program is to recognize the innovators, leaders and visionaries from around the globe in a range of IoT categories, including Industrial and Enterprise IoT, Smart City technology, Connected Home and Home Automation, Connected Car, and many more. This year's program attracted more than 3,000 nominations from companies all over the world. "IoT sensors are the backbone to the Internet of Things market. VersaSense products enable customers to connect in a secure, reliable and easier way while reducing the total cost of ownership for industrial sensing and control systems," said David Stein, VP, Global Semiconductors at Digi-Key. "We want to congratulate our partner VersaSense on being named the 2018 IoT Sensor Company of the Year by IoT Breakthrough."

www.versasense.com

www.digikey.com

Renesas Electronics Reports Full Year 2017 Financial Results

Renesas Electronics Corporation reported financial results for the fourth quarter ended December 31, 2017 (October 1, 2017 to December 31, 2017) and financial results for the year ended December 31, 2017 (January 1, 2017 to December 31, 2017).

"We have been continuously improving our gross and operating margins by pursuing sales growth and cost efficiency", said Bunsei Kure, Representative Director, President and CEO, Renesas Electronics Corporation. "Our fourth quarter non-GAAP semiconductor sales increased by 28.0% year on year, driven by increased sales mainly in the automotive and industrial businesses, in addition to the integration of Intersil. We expect to achieve traction in semiconductor sales during the coming quarter on a year-on-year basis." Following the completion of the acquisition of Intersil in February 2017, Renesas integrated Intersil into its operations and reformed its business organization into three business units. To align with this change, Renesas redefined its semiconductor sales breakdown to: "Automotive," "Industrial" and "Broad-based," the three application categories that constitute the main business of the Group, and "Other semiconductors," that constitute the businesses that do not belong to the above three application categories.

www.renesas.com

PCIM Europe 2018: Conference Program now Published

For over 35 years, the PCIM Europe Conference has been one of the most important events for the power electronics industry. Set to start off the new season with highly topical subjects, the internationallyoriented event will be hosting a line-up of renowned experts from research institutes and companies. Presenting their latest product innovations and research findings in over 300 oral and poster presentations in first publications, relevant issues in the industry will be illuminated from different angles.

The PCIM Europe Conference addresses all central topics along the entire value chain of power electronics including recent developments in power semiconductors, passive components, thermal management products, energy storage, sensors and new materials. The fee-based registration options for PCIM Europe Conference will be available as from February 2018.

At the international exhibition, which takes place at the same time, attendees will have the opportunity to engage in expert discussions and

e Program now **pcim** EUROPE

Nuremberg, 5 – 7 June 2018 International Exhibition and Conference

establish new contacts with more than 450 exhibitors. The PCIM Europe Welcome Party also provides an additional possibility to network in a relaxed atmosphere. For the first time, participants will be able to visit the impulse-presentation entitled "Fit for Stage" with a variety of thematic content. Here, an expert will introduce the principles of presenting successfully in a new and entertaining light.

www.pcim-europe.com

Future Electronics Joins the Electronics Representatives Association

Electronics is now an active member of the Electronics Representatives Association (ERA), the only organization that serves and speaks for electronics industry reps, manufacturers and distributors who are field sales partners. "Future Electronics is one of the most forwardthinking electronic components distributors in the industry," said ERA CEO Walter Tobin. "Its dedication to service-excellence, world-class demand creation initiatives and supply chain programs continue to delight customers worldwide. ERA is excited to welcome Future Electronics as its latest global distributor member." Since 1935, the ERA has worked to advance and support the professional field sales function in the global electronics industry through programs, services and activities that educate, inform and advocate for manufacturers' representatives, the principals they represent and the distributors who are representatives' partners in the marketplace. The rep community continues to bring enormous value to the Americas customer base, and Future Electronics looks forward to strengthening its partnerships with all the member organizations that are part of the ERA. "Future Electronics is deeply committed to the Americas rep community, and we are thrilled to be part of the ERA," said Karim Yasmine, Corporate Vice President of Strategic Supplier Development. "This engagement is a natural evolution of our Rep Council initiative, the longest-running active Rep Council in Americas distribution. We look forward to deepening our rep engagements and customer alignment through the many local ERA Chapters."

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High Fidelity Real-Time Simulation of Electrical Drives

Electrical drives are more and more widely spread in all industries, including energy (Low-voltage to High-voltage converters), automotive (Electrical Vehicle, Hybrid Electrical Vehicle), aerospace (More Electrical Aircraft, drones), and so on. Validating innovative drives with more complex controls, ensuring more accuracy and efficiency, is quite a challenge, especially when considering very fast-switching converters. OPAL-RT Technologies, the world leader in real-time simulators based on PC and FPGA, manufactures real-time simulators ready to take up the challenge.



The objective? To ally performance and ease of use to let engineers validate their most complex and demanding electrical drives.

The concept? To take advantage of the HIL approach, where the controller under test is connected to simulated converters and electrical machines.

The means? To combine CPU and FPGA processing units to bring the computation power and a comprehensive electrical circuit editor to describe the circuit to be simulated.

OPAL-RT has released the 3rd Generation of its eHS solver (electrical Hardware Solver), which lets system engineers implement models of electrical circuits directly on FPGA, without the need of any FPGA coding skill, just in a few clicks. Any inverter topology (2-level, 3-level, N-level, including more complex cases with other AC/DC & DC/DC converters) coupled with one or multiple electrical machines (PMSM, IM, SRM, etc.) can be implemented and simulated with sub-microsecond time-steps. No predefined circuits, user can design his own topology, down to every single switch, resistance, capacitor or inductance.

eHS brings many benefits, such as an increase of productivity and quality of the validation of controllers: it's really easy to use, tailored

to system engineers, can be deployed within minutes, with first closed-loop results within hours. The electrical circuits can be **recon-figured** by user any time, in order to adapt to each project or variation of a project. The performance (high simulation speed, low latency and great accuracy) allows the testing of real controllers in conditions very close to reality, even though the converters and electrical machines are simulated.

Moreover, eHS allows a **faster validation process**, with the implementation of **more use cases**, including faulty behavior (open and short circuits anywhere in the electrical circuit), to perform **better tests**, not only in normal conditions, but as well in undesired cases with side-effects.

Finally, eHS allows obviously non-negligible **cost-savings**, because of the software nature of the electrical circuit: **no risk to break the converters** or machines, as they are simulated. The system can be **reused** anytime, to represent any other circuit topology, depending on the project, therefore reducing the need to **create costly physical prototypes** of converters and machines.

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ECI's 125°C metallized dielectric system, combined with unique proprietary process development, yields superior performance and electrical characteristics to traditional 125°C dielectric choices like polycarbonate or PPS. The low loss dielectric system also offers higher corona inception voltages than metallized polycarbonate, and superior self-healing to metallized PPS. ECI's critical process development and testing insures our customers receive only the highest reliability capacitors. 100% of production is dual screened at 125°C burn-in for peak DC equivalent and 400Hz AC rating.

Summary of MH series advantages include:

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- Dielectric system proven in filter applications directly mounted on 400Hz generators in aerospace jet applications since 2002.
- The axial leaded package is well suited for board mounted applications requiring operation at high temperature in harsh environments.
- American made in our ITAR registered design and manufacturing plant to AS9100 quality system requirements.
- All capacitors are dual screened through 100% burn-in at 125°C for both peak DC and 400Hz AC ratings.
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WIRE: round, square, rectangular, and flat foil INSULATION: thermal varnish, epoxy, silicone, oil TEMPERATURE: up to Class H 180 Celsius SAFETY: UL approval service, including class 2 FREQUENCY: 50/60 Hz, 400 Hz, up to 500 kHz POWER: 10 watts to 10,000 watts TOOLING: bobbins, cores, tubes, laminations, bases **TOPOGRAPHIES:** too many to mention!

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Power Amplifiers Specialize in Driving Piezoelectric Capacitive Loads in Inkjet Printer Heads

Choose Either a 4-Channel, 7.5 A per Channel Amplifier, Or a Fixed-Gain Amplifier with -36 V Output Voltage Swing

The MPA106 and MP204 are Apex Microtechnology's newest high power amplifiers targeting the piezeoelectric drive circuits used for inkjet printer heads. The MP106 is a high output power amplifier optimized for producing negative output voltages. The MP204 is a high output current quad-channel amplifier capable of 7.5 A pulsed current per channel. The MP106 is optimized for driving negative voltages up to a -36 V swing across dynamically changing loads of 0-540 nF. For performance in driving inkjet printer heads comprised of multiple nozzles, the output signal for the MP106 is virtually independent from the capacitive load to ensure consistent print quality. The MP204 is a 4-channel power amplifier design that was developed for driving the Ricoh GEN4 and GEN5 print, or those similar. Each channel has a fixed gain of 14 V/V (22.9 dB) and is internally compensated to operate with capacitive print head loading. The MP204 can provide 1.5 A per channel continuously or 7.5 A pulsed, and can handle a maximum 20 W of internal power dissipation per channel.

"The MP106 and MP204 represent Apex's ongoing commitment to advancing high power drive technology for the industrial inkjet printer market" states Apex Strategic Marketing Director Jens Eltze. "By working in tandem with market leaders, we gain understanding into how inkjet print head designs continue to advance. These partnerships provide key insights that challenge our designers to develop new power products that integrate increasingly sophisticated performance features."

www.apexanalog.com



Apex MP106 and MP204



For technical information and samples visit: www.cde.com/THA/THA.htm

Custom Inductors - ONE Design Equation

Over 35 years ago, I started my career in power electronics. I completed a practical power project in my senior year in college, building a 6 KV, 20 kHz AC output power supply. It was a crash-course introduction into the world of power and set the course for my career. Pushing power through a transformer where nothing on the primary touched anything on the secondary seemed like magic, and I was hooked.

By Dr. Ray Ridley, Ridley Engineering Inc.

After university, my first interviews were with computer companies in the Boston area, and I really thought that my future was in logic design. However, as interviewers learned that I knew something anything! - about magnetics and power supply design, I was shunted off to the power department.

In those days, switching power supplies were just beginning to take over the computer industry, and there was a desperate need for design expertise. My first officemate became my mentor - a wonderful man named Spriadon (Dan) Balulescu. On my first day on the job, he put Dr. Cuk's dissertation on my desk and asked me to explain it to him in a couple of days, I think to prove that I was worthy of his time.

Soon after, we embarked on a 1 kW full-bridge power supply for a minicomputer. There was little guidance. FETs were just becoming practical, and there were no current-mode control chips.

I took on the job of simulation, electronics and control design, and Dan did the magnetics design, thermal, and layout. He would work for days at a time on the magnetics, huddled over a notebook, and a working specification would emerge to send off to our vendor. A few weeks later, samples would return. We placed them in the circuit to determine what worked and what didn't. Two iterations were usually enough to get the job done properly.

Throughout the process, over a period of two years, the magnetics design remained a mystery to me. It was the domain of the older, experienced engineers and the magnetics companies. Dan promised me that he would give me all his notes when I left the company to return to graduate school. He was good to his word - but I was no more enlightened after reading them than I was before.

Graduate School and Magnetics

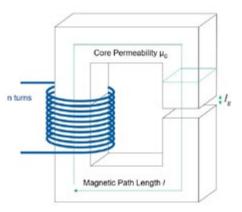
After working for a few years on products at my first job, I went back to graduate school to study under Dr. Fred Lee at Virginia Tech. Dr. Lee had already built a reputation for hiring the best in the world, and I was honored to be included in his group. All graduate students were assigned projects for industry. I was given two - analysis of parallel power converters for IBM, and power converter design optimization for NASA. The NASA project involved writing nonlinear optimization code with Lagrangian multipliers to get to an optimum solution for selection of power parameters.

This is where I was first exposed to the inner workings of magnetics design. The nonlinear optimization code worked to move parameters around (switching frequency, core sizes, etc.) to try to find a minimum objective function. In this case-the weight of a converter. The power loss in components was penalized by the weight of a required heatsink. There were many calculations to estimate the performance of the design, but I found something remarkable at the center of the code. There was only ONE equation that had to be obeyed to make magnetics work.

This was a revelation to me - ONE equation? How could that be? Why did magnetics books make it so complicated? They all had this equation, but quickly moved on to discuss hundreds more. I posed the question to everyone in the research group at Virginia Tech. Did they know that there is only one equation for magnetics? Everyone was puzzled. They each had a methodology, but could not describe the process.

ONE Equation

Figure 1 shows the basic structure of a generic core with a winding. This shows everything you need to build a custom inductor. The core can be any shape, with any cross section - square, rectangular, round, or some other shape. The core material sets the permeability, and the ability to open a gap allows



adjustment in the

Figure 1: The Basic Constituents of a Custom-Designed Inductor

permeability of the structure. The gap can also be embedded in the material, but this is a more specialized case for future discussion. There are negative consequences that come with a pre-gapped core material, along with some advantages. For peak performance the inductor will be a gapped ferrite in most cases.





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There are a lot of design freedoms offered by this structure – core size, number of turns, wire size, permeability, and gap. But where to start with a design? We can look at the basic magnetics equations to decide. The inductance of the structure is given by:

$$L = \frac{\mu n^2 A_e}{l}$$

u – *u u*

The area and the path length are shown in Figure 1. The effective permeability of the core, μ , is given by:

$$\mu = \mu_0 \mu_r$$
$$\mu_r = \frac{\mu_c}{1 + \mu_c \frac{l_g}{I}}$$

We don't have any idea how to deal with the permeability at the outset. It is very variable in the core with a wide tolerance in the specification. We will control this later with the gap in the core.

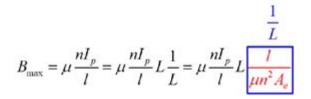
The maximum excitation, H, is given in terms of the peak current in the inductor by:

$$H_{\text{max}} = \frac{nI_p}{l}$$

The maximum flux of the core is then

$$B_{\max} = \mu H_{\max} = \mu \frac{m_p}{l}$$

But we do not know how to select any of these variables. So, we do some math tricks:



Which leads to several convenient cancellations in the equation:

$$B_{\max} = \frac{M_p}{k} L \frac{k}{\mu n^* A_e} = \frac{LI_p}{nA_e}$$

Now we have our one equation that matters, and it is independent of the μ of the structure, and the path length I. In fact, for a given saturation level of material, we are left with just two design variables – the area of the core, and the number of turns. The terms on the right of the inequality are electrical variables that we should already know from simulation of the converter.

$$B_s n A_e > L I_p$$

We have three important magnetics parameters now – the area of the core, number of turns, and the maximum B field that is allowed. For any given core, the area is fixed. If you choose a ferrite, the saturation level is also a constant, as we will discuss later.

Core Area

With few variables involved in the design, the type of core (or core shape) becomes irrelevant. Figure 2 shows several different types of cores – EE, RM, EPC, and pot cores. The only parameter we care about is the area. All core types are then treated the same, and the choice of family is determined by the desired profile, available bobbins, ease of winding and other similarly practical considerations.



Figure 2: Different Core Shapes and Areas

Inductor design is all about energy storage, determined by the inductance and peak current. We can choose any core, see how many turns are needed, and iterate designs to quickly arrive at a good solution. Only one rule is needed – obey the single equation.

Saturation Level for Ferrites

We need to know the saturation level for ferrites. This level must not be exceeded, or the inductor will drastically drop in value. Figure 3 shows the saturation curves for some TDK parts. Experienced designers will immediately know how to read these curves. The "knee" of the curve occurs around 0.3 T. This is the value used by almost all commercial designs. At 0.3 T, there is a small decrease in the Al value for the material. The gap in the core will make this drop undetectable, and the inductor will be constant up to 0.3 T

TDK Power Ferrite Saturation β_{sat}

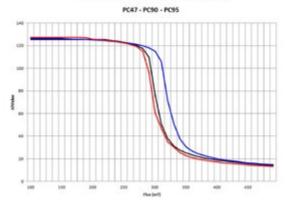


Figure 3: Saturation Level of Ferrite Material. Experienced engineers work with a value of 0.3 T for conservative designs.

Aerospace companies tend to design more conservatively. They will use a value of 0.25 T, or sometimes 0.2 T, to provide plenty of design margin.

The 0.3 T level for saturation of ferrites has been well known for years. However, newcomers to the field tend to look for specifications from the manufacturer, as they have not learned to interpret the curves. Unfortunately, this approach can lead to trouble in the design. The core manufacturers typically do not consider the knee of the

Satur densi Bs		agnetic	flux
(mT) H=11	94A/m		
25°C	60°C	100°C	120°C
530	480	410	380

Figure 4: Manufacturer's specification of saturation level of ferrite materials. The numbers exceed the value that experienced designers would read from the knee in the magnetization curves. curve to be the saturation flux. As you can see in Figure 4, they are extremely optimistic about the value of saturation, quoting numbers from 0.38 T to 0.54 T. Using this number for design can lead to failure.

It is highly recommended to use the curves to derive a comfortable number without exceeding the value of 0.3 T—unless the full data of the core material under all extremes of temperature is studied. Even then, exceeding 0.35 T is never recommended.

Summary

One design equation is needed for creating inductor designs.

Magnetics design is then reduced to a few simple variables. This equation is common in all magnetics books but is not highlighted as the ONE equation that is essential.

Our suggested approach is to use this equation, and then iterate designs to rapidly build experience in inductor design. When choosing a value of saturation flux for design, make sure that you read the curves and do not just accept overly optimistic values provided by core vendors.

References

- Magnetics Design Videos and Articles, Ridley Engineering Design Center.
- (http://www.ridleyengineering.com/design-center-ridley-engineering.html)
- RiidleyWorks Simulation software contains complete magnetics design and advanced analysis.
- Learn about proximity losses and magnetics design in our handson workshops for power supply design www.ridleyengineering. com/workshops.html (The only hands-on magnetics seminar in the world.
- Join our LinkedIn group titled Power Supply Design Center. Noncommercial site with over 7800 experienced and helpful industry experts.
- Join our new Facebook group titled Power Supply Design Center. Advanced in-depth discussion group for all topics related to power supply design.

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Spinning the World of 3D Printers

Smooth Driving for Flawless Printing

3D printing is a new approach for product prototyping. Technological improvements and lower costs are encouraging the technology to spread quickly to professionals and hobbyists. The demand for precision, speed, and smooth print-head movement is a challenge for mechanical systems. A new motor driver can meet all these requirements using a dynamic microstepping operation.

By Dario Cucchi and Enrico Poli, Application Engineers, STMicroelectronics

More than just an alternative method for making objects, 3D printing is a new approach in product development. It uniquely closes the gap between modelling and production by quickly creating components and functional prototypes that can be evaluated and tested during product development. This can reduce costs, increase quality, and accelerate the introduction of the final product.

Starting from a 3D CAD model, a 3D printer can build an object by deposing layer after layer of a fused filament of plastic – or other – material. This printing is, in reality, an additive manufacturing process that allows, among its many benefits, the creation of complex shapes that might otherwise require a big investment of time and/or money. 3D printing can even enable the infill of the reproduced object, saving material and time in production.

The improvements in 3D printing technology, together with the new materials used and the cost reductions of equipment, have accelerated the adoption of the technology in industrial areas such as mechanics, automotive, aerospace, biomedical, as well as in educational. On top of the larger commercial and design organizations using 3D printing, the broad range of maker communities on the Web, which include hundreds or thousands of hobbyists, model builders and modern artists, are also successfully using 3D printers.

Quality in 3D printing

The quality of the printings is evaluated on how the final object matches the original CAD model and whether the print shows visible defects. Other mechanical characteristics, such as fragility and deformability contribute to the overall quality. Quality can be influenced by the material of the plastic filament, its melting temperature and how it is being extruded, the thickness of a single deposed layer, the stiffness of the printer structure, the accuracy of the motor controlling the extruder, and the dimensions of the printing area.

There are always tradeoffs. An important tradeoff is between precision and printing time. Depending upon the dimensions of the object being printed and its complexity, printing can require many hours, so the speed of the extruder must be optimized to achieve the appropriate balance. Moreover, since the extruder has its own inertia, it can introduce defects on square angles and sharp edges, unless the extruder is moved with specific acceleration/deceleration profiles to compensate. The mechanical system of a 3D printer, containing rails, gears, and motors, must be very precise and free of vibrations and deformations, and have tight tolerances to move the extruder quickly and precisely to fulfill the resolution requirements.

Fundamental to guaranteeing a 3D print without defects are stepper motors, and especially because the resolution of a single step is not precise enough, the motors need microstepping driving techniques to move the motor shaft by fractions of a single step. Naturally, the higher the microstepping resolution, the smaller fraction of a step the motor can handle. For example, a printer can better reproduce an area rich with details using a high micro-stepping resolution or change to lower-resolution stepping for less complex areas. The motor-driving technique should adapt and drive these changes of speed and resolution to optimize printing time and resolution. This is where choosing a motor driver IC that can support all these working conditions is crucial.

Smooth and reliable motion control

The requirements listed above-adaptable and precise motion control-are met by STMicroelectronics' STSPIN820 device. With an integrated controller that implements a PWM current control with fixed OFF time, adjustable by an external resistor, the integrated control logic can manage eight different microstepping resolutions from full step mode up to a resolution of 1/256th of a step. This guarantees very smooth, precise, and silent movement. No external power MOS-FETs are necessary to drive the stepper motor since the STSPIN820 integrates two full-bridges rated to operate up to 1.5 Arms each. The device can work with a wide supply range, from 7V to 45V and includes overtemperature protection, overcurrent protection for each of the eight power MOSFETs, and undervoltage lockout which prevents the device from working after a sudden supply-line voltage drop. Each protection mechanism triggers an open-drain pin, which signals the fault to the MCU. Figure 1 shows the basic STSPIN820 block diagram and the few external components required for a typical application.

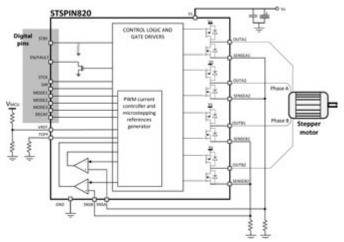


Figure 1: Block diagram of a typical application using the STSPIN820



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Hybrid SiC Power Modules

Portfolio: MiniSKiiP, SEMiX 3 Press-Fit, SEMITRANS, SKiM 63/93



The STSPIN820 comes in a compact TFQFPN 4 x 4 mm package. This small form factor, together with the reduced number of external components needed, saves PCB board size as well as the BOM count for the final application.

Improving precision with microstepping

Although the microstepping driving technique can achieve a high level of precision and reduction in vibrations, the higher micro-stepping resolution means that the MCU must manage the higher step clock (STCK). Since there are acceleration and deceleration profiles to be computed, the higher the STCK frequency, the higher the effort required by the MCU. When high speeds and high resolutions are involved, the required STCK frequency becomes very high, too. Although the STSPIN820 maintains step counting even at frequencies up to 4 MHz, decreasing the microstepping resolution could be an option to decrease the STCK frequency. In fact, when the motor rotates at high speeds, precision in the positioning is not as crucial, and the microstepping resolution can be decreased. Reducing the step clock frequency reduces the MCU overhead-a nice tradeoff between microstepping resolution and rotation speed. Choosing the right microstepping resolution provides a way to limit the step clock frequency without losing performance while still guaranteeing the desired acceleration and speed profiles. Microstepping driving techniques are key for reducing vibration and ensuring smooth movement for high-quality 3D printing.

Testing vibrational results

We mounted the LSM6DSL, which is an inertial module containing a 3-axis accelerometer and a 3-axis gyroscope in a single 2.5x3mm LGA package, directly on the stepper motor and tested the vibration at different microstepping resolutions and speeds. The LSM6DSL has a selectable full scale and a maximum output data rate of 6.66 kHz for both accelerometer and gyroscope. The axes orientation of the module, as it was mounted on the stepper motor, is represented in Figure 2. The measurement of the acceleration along the three axes can give an estimation of the vibration and resonances introduced by the motor shaft on the motor body, while the measurement of angular rate using the gyroscope can give further information about the mechanical response in the system.

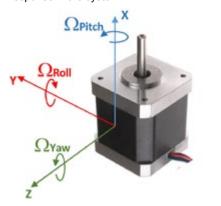


Figure 2: Axes orientation of the inertial module on the motor

The first analysis related to the mechanical response of the system is done by applying a single step on the motor, using the full step mode (the lowest resolution), and then the 1/256th step mode (the highest resolution). Figure 3 shows the mechanical response of the accelerometer (above) and the gyroscope (below) setting the STSPIN820 in the full step mode. A single step clock is applied to get the movement of one step: the motor shaft produces a jerky movement and the mechanical resonance is stimulated. When the shaft settles to the new step position, vibrations decrease so the mechanical response is a damped sinewave with a resonance frequency around 290Hz.

Setting the microstepping resolution to 1/256th of a step, 256 STCK pulses are needed to get the same movement of one mechanical step. In this case, the currents driving the motors are modulated smoothly—they increase with a sinusoidal profile in order to smoothly guide the shaft to the new step position without abrupt movements. The mechanical resonance is minimally stimulated and the mechanical response is cleaner, as shown in Figure 4. In this example, the STCK pulses are applied with a frequency of 12.8 kHz, for 20ms.

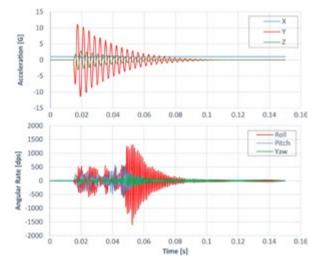


Figure 3: Mechanical response to a single step movement (Full Step resolution mode)

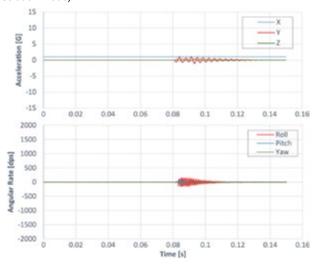


Figure 4: Mechanical response to a single step movement (1/256th Step resolution mode)

When multiple steps are performed consecutively, multiple vibrations occur and contribute to the overall mechanical response. The resonances and the vibrations can be stimulated depending on the speed rotation of the motor.

To analyze vibration versus speed, we consider only the accelerometer data and use five of the eight microstepping resolutions available in the STSPIN820: Full Step, 1/4th, 1/16th, 1/32th, and 1/256th of a step. The motor is driven with a continuous rotation at a specified speed, so for each microstepping resolution, the step clock is set accordingly. To combine the information coming from the three axes, the modulus of the 3D acceleration vector is computed:

$$V = \sqrt{(a_x - 1)^2 + a_y^2 + a_z^2}$$



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where a_x , a_y and a_z are the values of the acceleration read on each axis, represented in G, the gravity acceleration (9.81 m/s²). The accelerometer also senses the gravity acceleration; as the motor is positioned as shown in Figure 2, the gravity acceleration lies along the X axis. Therefore, the value of gravity acceleration (1G by definition) is subtracted from the ax value. The chart shown in Figure 5 represents the trend of the vibration magnitude (the maximum measured value of vibration V) versus the speed of the motor (in rpm), for different microstepping resolutions. At lower speeds, the vibration can be limited by increasing the microstepping resolution. On the other hand, we see that when the speed is increased, the curves tend to converge, and the difference in vibrations between the different resolutions becomes smaller. This happens because at higher speeds, the reference current from the microstepping sequence is changed more quickly than the maximum current slew-rate of the system, which is limited by both phase inductance and back electromotive force. In this case, some of the microsteps (the point composing the sinusoidal current profile) are not physically performed. Consequently, there is no reason for such a high resolution.

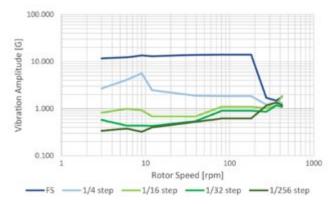


Figure 5: Vibration VS speed at different microstepping resolution

According to these results, higher speeds do not require high microstepping resolution since the advantage in terms of vibration and smoothness is not significant. However, it demands a lot from the MCU in terms of computational effort.

Changing microstepping mode "on the fly"

To optimize step-clock generation and movement precision, the microstepping resolution can be changed dynamically, according to what the application requires. The graph in Figure 5 shows that when small movements are needed, a high microstepping resolution can guarantee excellent vibration and smoothness results. On the other hand at higher speeds, the vibrations reduce, so a high resolution mode is not required. The clock speed can be decreased without an excessive loss of precision and with the advantage of decreasing the MCU computation effort.

With the STSPIN820, the step mode can be modified "on the fly." Figure 6 illustrates an example where the speed of the motor is increased up to the target of 360 rpm. The motor used in the example counts 200 steps at each rotation. The acceleration profile is driven not only by increasing the step clock, but also by dynamically changing the microstepping resolution. In this way, it is possible to keep the step-clock frequency below 15 kHz, while limiting the vibration of the motor shaft and maintaining a high degree of smoothness in the whole movement. Figure 6 shows both the vibration (above) and the step clock frequency (below) versus the speed, when using a dynamic microstep resolution. The change from one step mode to another is represented by the vertical dotted lines. The upper and lower limits obtainable are also shown in the charts. The highest vibrations (upper limit) occur in full step mode, while the lowest ones occur in 1/256th step mode. The dynamic microstepping selection provides a way to keep the vibrations close to the lower limit, thus improving precision. From the STCK point of view, the dynamic mode selection keeps the frequency in a reduced range: it never increases beyond 15 kHz, well below the upper limit.

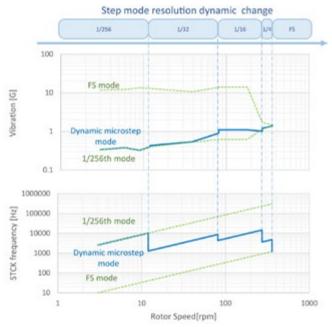


Figure 6: Scaling step clock and microstepping resolution

Once the target speed is reached, it is possible to switch to full step mode, increasing the torque with respect to the torque in microstepping mode. This is an important feature achieved by dynamically switching from microstep to full step mode. The change in full step mode must occur only when an electrical position of 45° is met—when the currents in the two phases of the stepper motor are the same. In this way, only the current amplitude changes without any change in the electrical angle.

The advantages of dynamically switching the microstepping mode are shown using the same example with a static setting: if we use the 1/256th step mode with a 360 rpm target speed, a STCK up to 307.2 kHz is needed. From the MCU point of view, this is very demanding, and there is almost no improvement using the highest microstepping mode at such speeds. On the other hand, setting the full step mode at low speeds results in a very noisy movement, unsuitable for the precise positioning requirements of 3D printing.

Moving to the next step

The new generation of stepper motor drivers, like the STSPIN820, resolves many of the challenges for a wide range of motor-driving applications. Together, the small 4x4mm package and a reduced number of external components equal very compact and cost-effective boards. The world of 3D printing is still evolving, requiring ever more precision and speed to improve prototyping. With a high microstepping resolution up to 256 microsteps and the ability to change step resolution "on the fly," the STSPIN820 proves itself an excellent choice for fast and precise 3D printing—as well as other tricky motor-drive applications.



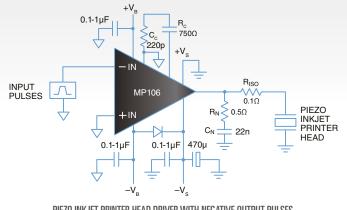
Different Printheads, llitterent Urivers

Industrial

Printhead

The MP106, MP204 power amplifiers drive Ricoh, Samba and similar multi-nozzle inkjet printer heads

The MPA106 and MP204 are Apex Microtechnology's newest high power amplifiers targeting the piezeoelectric drive circuits used for inkjet printer heads. The MP106 is optimized for driving negative voltages up to a -36 V swing across dynamically changing loads of 0-540 nF. For driving inkjet printer heads comprised of multiple nozzles, the output signal for the MP106 is virtually independent from the capacitive load to ensure consistent print quality. The MP204 is a 4-channel amplifier design developed for driving the Ricoh GEN4 and GEN5 print heads, or those similar. Each channel has a fixed gain of 14 V/V(22.9 dB) and is internally compensated to operate with capacitive print head loading. The MP204 can provide 1.5 A per channel continuously or 7.5 A pulsed, and can handle a maximum 20 W of internal power dissipation per channel.



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Cool Running, 144W, 4 × 40A µModule POL Regulator

The LTM[®]4636 is a 40A-capable µModule[®] regulator featuring 3D packaging technology, or component-on-package (CoP) to keep it cool. In addition to dissipating heat from the top through the exposed inductor, the LTM4636 efficiently disperses heat to the PCB via 144 BGA solder balls dedicated to GND, VIN and VOUT—where high current flows.

By Afshin Odabaee and Yan Liang, Analog Devices Inc.

The body of the device is an overmolded 16mm × 16mm × 1.91mm BGA package with an inductor stacked on top to expose it to cooling airflow. The total package height is 7.16mm.

A single LTM4636 is rated for 40A loads; two parallel converters can support 80A; four support 160A. Upscaling a power supply by paralleling LTM4636s is easy: simply copy and paste the single-regulator footprint, as shown in Figure 1.



Figure 1: 3D Packaging of the LTM4636 Puts One of the Hottest Components, the Inductor, on Top, Where Significant Surface Area Is Exposed to Airflow. It Is Easy to Lay Out Parallel LTM4636s to Scale Power Capability—Simply Duplicate the Layout of One Channel and Multiply. The Clean Layout Here Shows Four Channels at 40A Each.

The current mode architecture of the LTM4636 enables precision current sharing among the 40A blocks. Precise current sharing, in turn, produces a power supply that spreads the heat evenly between devices. Figure 2 shows that all devices in the 4- μ Module 160A regulator operate within 1°C of each other, ensuring that no individual device is overloaded or overheated. This greatly simplifies heat mitigation.

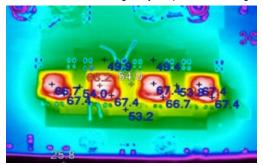


Figure 2: Precision Current Sharing Among Four LTM4636s Running in Parallel, Resulting in Only 40°C Rise in Temperature for 160A Application.

Figure 3 shows the complete 160A design. Note that no clock device is required for the LTM4636s to operate out-of-phase to each other clocking and phase control is included. Multiphase operation reduces input and output ripple current, reducing the number of required input and output capacitors. Here, the four LTM4636s run 90° out-of-phase.

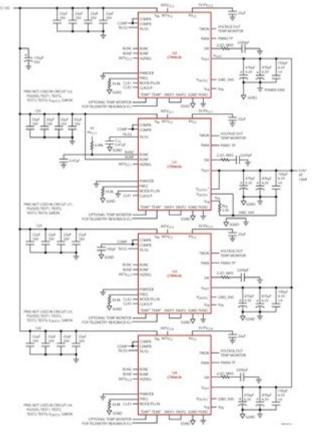


Figure 3: 140W Regulator Features Four LTM4636s Running in Parallel with Precision Current Sharing and High Efficiency 12V Input to 0.9V Output at 160A.

Conclusion

Choosing a POL regulator for a densely populated system requires scrutiny beyond voltage and amperage ratings of the device. Evaluation of package thermal characteristics is essential, as it determines the cost of cooling, the cost of the PCB and final product size.

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Next Generation Automotive Traction Power Module



DCMTM1000 Designed to meet the future demand of Electric Vehicle Drive Trains

By Omid Shajarati, Klaus Olesen, Norbert Apfel, Matthias Beck, Danfoss Silicon Power GmbH

The acceleration of global warming and pollution as well as international carbon emission targets initiated a process to reduce emissions in all parts of our living. These regulations to reduce pollution have even been further emphasized by the announcement that many large cities around the globe (1, 2, 3) plan to ban all vehicles with Internal Combustion Engines (ICE).

Saving energy, increasing efficiency and reducing emissions are trends that many countries and globally operating companies see as one of their important future targets.

Global trends and policies influence the automotive industry in many ways. Automobiles contribute around 12% of the total global carbon emissions, and many governments have started initiatives to increase the number of cleaner cars by either incentives or local rules and limitations (4).

The diesel emissions scandal and fast-moving digitalization of personal mobility increase the pressure on whole industries to radically change their products, themselves and to develop new technologies and business models to cope with the future challenges.

Automotive drivetrain electrification in vehicles is a part of it. It is expected that in 2035 more than 40% of all vehicles are somehow electrified as BEV or PHEV (6).

The development in battery technology and prices, broader electrification and fast-growing markets like China will push time to market and cost efficient technologies. Comparing the price of a traditional vehicles with future xEV designs, cost effective and flexible solutions will be needed to deal with expected price pressure and investments.

One way of providing performance and cost efficiency are scalable mechanical and electrical platform solutions, which can be used in a range of different models/passenger cars. By having more of the same in different combinations, costs, development time and time to market can be significantly improved.

DCM™1000

Danfoss Silicon Power actively supports the automotive industry with electronic components, helping to power up future drivetrain applications and achieving the challenging emission goals.

Most electrified vehicle powertrain traction inverter contains a multichip-semiconductor power module. It can comprise of IGBT and Diodes or MOSFET die, where the typical circuit topologies are half-bridges or six-pack.

Within the modules, efficient use of the semiconductors is key for achieving cost competitiveness in hybrid- and electric vehicle traction applications. As semiconductors are the main cost driver in power modules, roughly representing 50% of the module cost, making the most out of the semiconductors without derating and compromising the reliability and lifetime of the module, becomes a key discipline.

Getting the most of the semiconductors requires a multidisciplinary approach addressing material science, new bonding and joining technologies and innovative thermal management technologies; a holistic approach is key to the success of identifying the optimum solution from a technical and commercial aspect.

Danfoss has - through the past years - developed market leading technologies, addressing all the aspects mentioned above. Well known examples are the Danfoss Bond Buffer[®] (DBB[®]) (7-12) that combines sintered die attach and copper wire bonding, transfer molding processes for robust packages, to liquid cooling technologies namely ShowerPower[®] and SP3D[®] (13-24).

Danfoss introduces the optimized DCMTM 1000 technology platform for traction applications in hybrid electric and battery electric vehicles. Drivetrain inverters are designed to operate under harsh conditions; high temperature cycles, humidity, mechanical shocks and vibrations. The stringent shock and vibration requirements are addressed by the transfer molding process of the power module.

The following overview explains the technologies that are combined in the new DCMTM 1000 technology platform.

Danfoss Bond Buffer[®] technology (DBB[®])

Standard aluminium wire bonding technology is limited by the current carrying capability of the wire. Several manufacturers developed alternatives ranging from the .XT process from Infineon, the SKiN technology from Semikron to the DBB[®] technology from Danfoss, all of which are copper based.

The DBB® technology enables copper wire bonding on standard semiconductor chips. Thin copper foil (the bond buffer) is sintered on the topside semiconductor metallization upon which copper wire bonding can be attached. Sintering of both bond buffer and chip to substrate are done in the same process step. Danfoss Bond Buffer® (DBB®) enables power cycling capabilities that are 15 times higher than seen in Al wire bonded power modules. This lifetime benefit can be used to operate at higher junction temperatures without need for current derating. Increased power cycling capability also reduces the semiconductor area inside a power module leading to reduced cost. Key is the robust top-side copper to copper contact with lower thermo-mechanical stress as well as lower steady state and transient thermal resistances because of the increased contacting surface. The electrical characteristics are improved as well as the copper foil on top of the die reduces voltage drop and adds thermal buffer and heat spreader. Therefore, conduction losses are reduced and short circuit properties are improved (12).

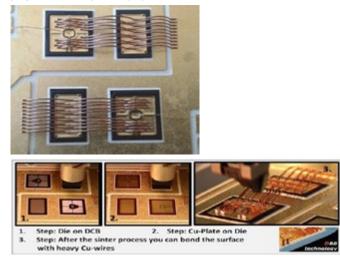


Figure 1: The DBB[®] principle.

Simulations and measurements have proven that the limits for the "lifetime – output current tradeoff" have been pushed. This means that the lifetime improvement for DBB® over standard wire bonding combined with the improved thermal performance of SP3D® over

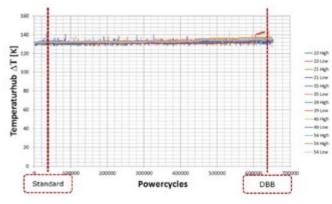


Figure 2: Proven power cycling performance with copper wire-bonds and DBB.

e.g. pin fin coolers, give an increase of output current of 20-30% over the state-of-the-art automotive traction modules using comparable semiconductor areas.

Automotive traction power electronics lifetime requirements have increased dramatically over the last decades as illustrated in the chart below.

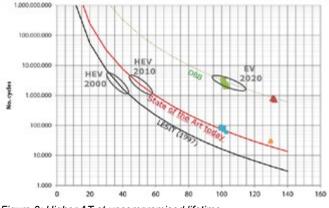


Figure 3: Higher ΔT at uncompromised lifetime.

During year 2000, standard aluminum wire bonding with soldered chips provided sufficient reliability to fulfill automotive lifecycle requirements. During the following decade, the continuous process improvements in the wire bonding technology proved adequate to fulfill the increased performance requirements. But the leap in performance requirements from 2010 to 2020 are so extreme that standard bonding and joining technologies are out of the picture. The improved reliability of DBB[®], with a power cycle capability 15 times higher than state of the art technology, meets the requirements, and thus, is the solution for the future.

ShowerPower[®] and SP3D[®]

ShowerPower[®] is a liquid cooling concept designed for direct liquid cooling of flat baseplate based power modules. ShowerPower[®] coolers for standard modules, like P3 module and EconoPlus modules, have been in production for the last decade. ShowerPower coolers[®] are widely used in industrial and renewable applications. More specifically, more than 30 GW of renewable power conversion capability is today cooled by ShowerPower[®]. Furthermore, ShowerPower[®] has a flawless track record for more than 10 years with no failures due to cooling, coolant leakage or clogging.



Figure 4: ShowerPower[®] for the EconoPlus module and for the P3 module.

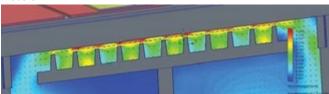


Figure 5: The bypass [13].

The key advantage is highly efficient direct liquid cooling without temperature gradients across the power module baseplate. The core of the concept is a part comprising several meandering cooling channels that guide the coolant along the surface to be cooled.

Because of tolerance issues, there will be a small gap or bypass between the ShowerPower[®] insert and the surface to be cooled. The gap is a few hundred microns wide.

CFD investigations have demonstrated that a bypass of 200-500µm improves the thermal performance and reduces the differential pressure drop. The exact value depends on the current design boundary conditions and design goals.

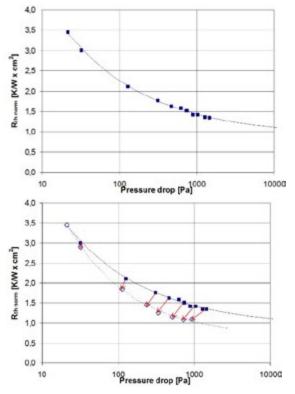


Figure 6: CFD simulations on a family of meander channel geometries, without and with a bypass.

As seen in Figure 6, the bypass has a positive impact.

One explanation for the improved performance is the swirl effect in the cooling channels. The flow in the channels is laminar because of the relative low Reynolds numbers. This is good from a pressure drop perspective but not so good regarding cooling efficiency because of

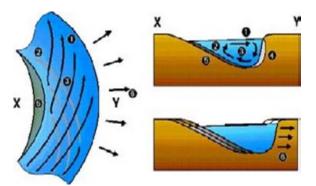


Figure 7: Swirl effect in rivers [14].

classical build-up of boundary layers that inhibit effective heat transfer. But the changes of direction of the flow force the fluid flow into a rotation, or swirl, due to the conservation of momentum. The phenomenon is often observed in rivers. Though in the small meandering channels seen here, the effect is difficult to observe.

The bypass creates a flow transverse to the flow direction in the meandering channels thereby amplifying the swirl effect, see the figures below; this means that cold coolant is constantly brought in contact with the surface to be cooled.

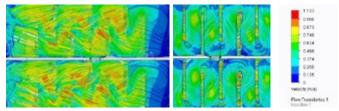


Figure 8: Left: flow through the bypass; right: underside view of the channels. Colors depict velocities.

Enhancing the efficient cooling area by transferring the meandering channels from the plastic part to the baseplate itself almost doubles the effective heat transfer coefficient and thereby reduces the thermal resistance junction to coolant by 25%. This also offers a current carrying capability that is roughly 25% higher than for standard Shower-Power[®]. The concept is called ShowerPower[®] 3D or SP3D[®] for short. Further information on ShowerPower[®] and SP3D[®] can be found here (15-24).

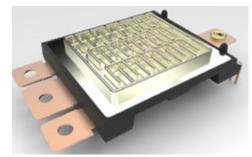


Figure 9: Power module with SP3D[®] baseplate.

The SP3D[®] concept offers several benefits compared to other liquid cooled power module e.g. pin fin coolers. The parallel cooling principle eliminates temperature gradients associated with the serial cooled pin fin concept. It also allows for tailoring the cooling e.g. focus cooling efficiency at local hot spots, a feature that is not possible for the pin fin concept due to "shadowing" effects. The walls of the SP3D[®] cooling channels also bring a considerably extra amount of mechanical stiffness to the module compared to the pin fin allowing for high pressures and pressure pulses in the cooling system.

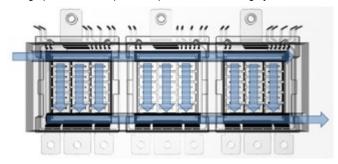


Figure 10: Transparent CAD picture visualizing the parallel flow of the coolant.

Hochschule Reutlingen Reutlingen University

Transfer molding technology

Combining DBB[®] and transfer molding technologies allows for higher junction temperatures and more extreme temperature cycling than standard bonding and joining- and housing technology. Power density can be increased, and the extra power generated can be dissipated by SP3D[®] cooling. The bottleneck is no longer the die solder joint and the soft gel, but the chip itself. So, with DCMTM 1000 the scene is set for applying wide bandgap devices that allows for higher junction temperatures.

Electrical Technology

To meet future challenges with hardware and quality related topics the DCM $^{\rm TM}$ 1000 is designed, built and certified in accordance to the LV324 automotive standard.

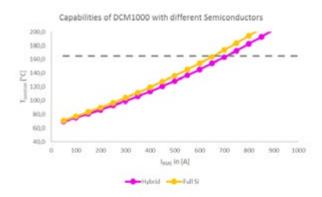
The DCM[™]1000 technology platform is truly flexible since optimized to utilize Si and hybrid modules (Si IGBT's and SiC diodes) and pure SiC semiconductors, while keeping the same footprint. In Figure 11 a comparison of the output current is shown.

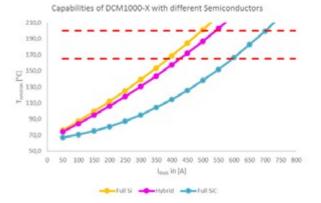
It is evident that the module performance is enhanced while different semiconductors are utilized, Si chipset delivers great performance, especially with DBB a huge increase in life time can be achieved.

A hybrid chipset offers even more current performance because the Eon losses of the IGBTs are significantly reduced due to SiC Diode.

A SiC chipset outperforms every Si or SiC variant at comparable operating points. Furthermore, the junction temperature can be higher compared to Si, i.e. during short boost phases.

According to application need, the diverse chipset ensures maximum efficiency and cost optimal, at the different given operating point considering the stringent inverter requirements.









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The module are scalable in order meet the different voltage classes, covering the different BEV/HEV inverter voltage classes (VDC,Link =450-900V) resulting in blocking voltages of 750 - 1200V, while having different output current classes 350-650A. The nominal output current is defined for fsw=10kHz, Tcoolant=65°C @ 8L/min, m=cos(phi)=1, Tj,op=165°C, note that the junction temperature is only achievable by utilizing the DBB[®].

The definition of the nominal operating point is of great importance, since the boundary conditions have a great impact on the module performance. The impact of the alternating boundary conditions on the nominal output current of the module is shown in Figure 12- Figure 13.

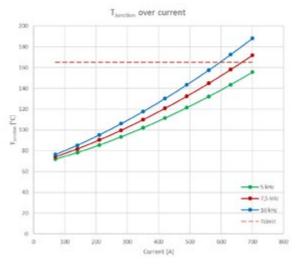


Figure 12: Impact of the switching frequency on nominal output current.

The coolant can be varied with 2 parameters, the coolant temperature and coolant flow rate. The impact of coolant temperature is quantified in Figure 13.

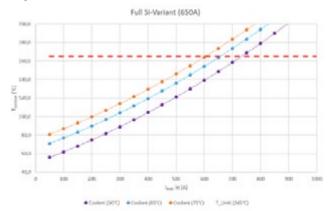


Figure 13: Impact of coolant temperature, here @ 10kHz switching frequency and 8L flow rate.

Any customization of the DCM[™]1000 technology platform, like different semiconductor brand or type, different connector to fit the exact customer needs of the different traction inverters is an option on request.

Easy integration

DCM[™]1000's compact form factor makes system integration easy and offers a range of mechanical designs to optimize the inverter design. Possible configurations range from simple planar assemblies to advanced 3D setups - a few examples are shown below. The standard planar configuration with three modules placed in a row. The cooler is a laboratory design, placement of flow inlet and outlet is flexible.

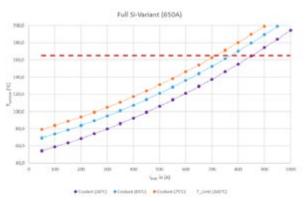


Figure 14: Impact of coolant temperature, here @ 6kHz switching frequency and 10L flow rate.

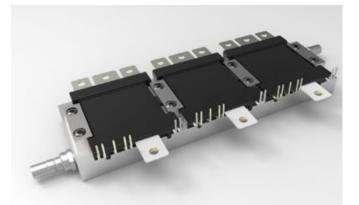


Figure 15: Planar configuration

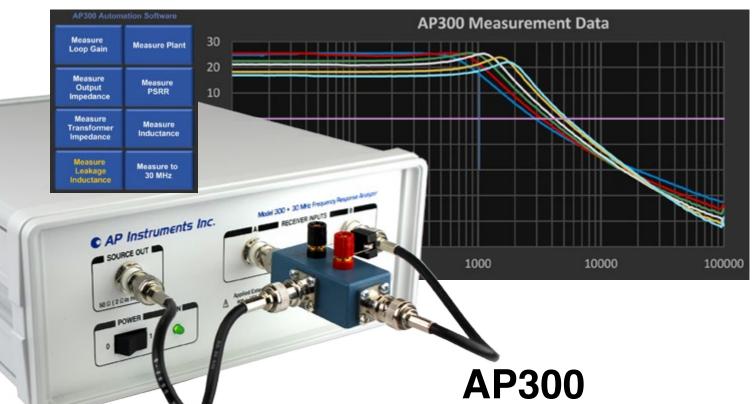
The circular configuration offers the opportunity for easy integration of the DC-link capacitors for low stray inductance and high symmetry in switching. A laminated busbar, shown in Figure 16, connects the power modules to the capacitors.



Figure 16: Circular configuration.

The three modules are assembled on a triangular cooler on top of the DC-link capacitor in Figure 17.

For larger motors the modules can be coupled in parallel; the example below shows six modules placed on the inside of the stator of the motor.



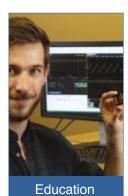
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Summary

Danfoss' DCM™1000 is the next generation technology platform for automotive traction inverters.



Figure 17: Triangular configuration.

The technology platform is well-defined, based on known and proven technologies, and yet open enough to be scalable and customized to meet specific requirements. In addition, the technology platform is versatile in application and performance as a consequence of combining materials and technologies in the best possible way. Qualification tests according to LV 324 and openness to any automotive qualified semiconductor reduce risk of failure and allocation.

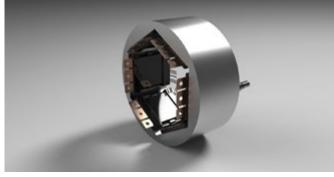


Figure 18: Motor configuration, the modules are placed on the inside of the stator.

With the introduction of DCM[™]1000 technology platform, Danfoss Silicon Power further strengthens it's customized power module offering. The DCM[™]1000 will be on display at APEC. Visit the Danfoss Silicon Power booth for a first impression and introduction.

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Semiconductor Solutions for Energy Storage Systems in Light Traction Vehicles

The requirements regarding modern light traction vehicles, such as trolleybuses and trams, gradually increase. Special focus is set to operation without trolley power supply temporarily while remaining free of emissions. Efficiency, power density, volume and weight of the system become more important. At the same time, low acoustic noise and restrictive EMI-standards have to be met.

By Martin Schulz, Infineon Technologies AG, Warstein, Germany

These particular requirements can be met using energy storage systems based on Lithium-Ion traction batteries or supercapacitors. To fully utilize the capabilities of the storage systems, it is necessary to employ suitable power converters to manage the flow of energy in both, charging and consuming. This correlates to DC-DC converters which have to handle substantial cyclic loads at potentially high operating temperatures.

The ability to temporarily operate without the trolley power supply is a feature found more often among the requirements regarding light traction vehicles. This mode of operation is utilized within the urban areas lacking the catenary infrastructure such as historical centers. It also applies for connections between separated lines and is needed for emergency vehicle operation during power blackout as well. In addition, low-noise, high-comfort, zero-emission operation is demanded, ruling out the diesel-electric drive train as it was commonly used in the past.

The sum of requirements can be met installing an electric/electric hybrid approach.

In this, traction batteries or super-capacitors are installed as energy storage systems, providing intermediate power to the electric drive train.

Figure 1 is a scheme of a tram with the power converters installed on top of the train.

Inside the roof unit, the DC-DC-converter to manage the energy flow to and from the batteries is one of the power electronic subsystems.

The converter is a compact, often forced air cooled power unit. The development of the electrical equipment focuses on finding the optimal solution for power converters using traction batteries or supercapacitors. To serve the demands, several criteria have to meet:

- In Trolley Mode, well controlled charging of the energy storage from the DC trolley systems has to be possible. This correlates to an input voltage range from 400VDC to 1000VDC.
- In Battery Mode, well controlled power flow from the battery to propulsion inverter, auxiliary converters and vehicle battery charger is mandatory.
- In both modes, safe handling of short but repeating bursts of load up to 200kW for 60 seconds has to be possible even if exposed to relatively high temperatures with limited forced air cooling capabilities.
- 4. Achieve high operational efficiency while occupying low volume at evenly low weight.

To meet the criteria 1 and 2 and depending on the boundary conditions, there are two topologies for DC choppers to be considered.

If the energy storage system operates at higher as well as lower values than the trolley voltage level, using a 2-quadrant DC-chopper is mandatory. A suitable scheme is depicted in Figure 2.

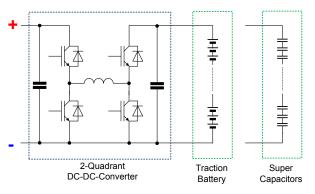


Figure 2: opology of 2-Quadrant DC-Chopper

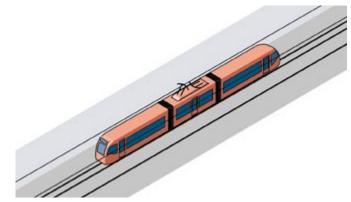


Figure 1: Position of the electric equipment on a tram

If the voltage of the energy storage system always stays below the trolley voltage, a buck-boost DC chopper as given in Figure 3 is most suitable.

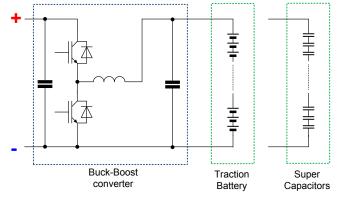


Figure 3: Topology of a Buck-Boost DC-Chopper

In Trolley Mode, the converter works as a step-down chopper providing a voltage lower than the trolley supply to the trolleybus' internal systems. In Battery Mode the converter works as the step-up chopper supplying the electric systems with a voltage higher than the storage system's output.

To meet the criteria 3 and 4, suitable power semiconductor devices are needed. The solution using IGBT modules within the 1700 V class needs to support sufficient current range, low conducting and switching losses as well as a robust package with low thermal resistance. In addition, a favorable cost/performance ratio on system level is demanded.

IGBT modules belonging to the PrimePACK[™] family equipped with the 4th generation of IGBT/FWD chips pose a suitable solution. This IGBT module family includes IGBTs in half-bridge topology in 1200 V and 1700 V classes, offering nominal currents in the range of 600 A to 1400 A. The modules are available with two types of durable robust packages, all equipped with an integrated NTC sensor to capture the module's base plate temperature.

These components, depicted in Figure 4, are dedicated to be used in heavy duty mobile applications [1,2] and allow considering scalable designs.



Figure 4: PrimePACK[™] 2 and 3 with applied thermal interface material (TIM)

To achieve safe operation and full power utilization of the IGBT module, a suitable gate driver needs to be chosen. For evaluation, the 2ED250E12_F dual-channel IGBT-driver as well as the booster stage MA300E17 are available to help designers develop their dedicated solution. Both devices can be seen in Figure 5.

The thermal situation for the power section demands most accurate thermal measurement to be implemented into the control strategy to exploiting the power to the maximum without exceeding the specified operating limits. Very often, the surface temperature of the heat sink had been monitored with an external temperature sensor. Based upon this feedback, the power output of the converter had been tuned by the control system. There is however a significantly higher temperature on the base plate of the IGBT modules and thus the temperature of the sensitive transistor and diode chips inside. For safety reasons, a rather conservative value of the temperature that triggers the reduction of the converter's output power had to be chosen.



Figure 5: Dual-Channel driver 2ED250E12_F and booster stage MA300E17 mouinted to the according power module

To get more accurate information, the design of monitoring the thermal load and triggering the overheating protection should use the temperature measured by the NTC inside the IGBT modules [3,4].

This approach provides a more realistic view about the thermal load of the semiconductors in the real operation. Especially if the thermal correlations between chip-temperature and NTC-reading are determined accurately, robust information for static operation can be extrapolated [3, 4].

The number of energy storage systems like traction batteries or supercapacitors in light traction vehicles is continuously increasing. It is safe to assume, that higher demand regarding the power capacity of the DC converters becomes a trend, also there is pressure to reduce their weight and size including smoothing DC chokes. To meet these requirements in the near future, new IGBT modules in the form of a 5th generation IGBT module featuring Infineon's .XT technology offer an excellent choice.

These new modules have significantly higher performance compared to existing modules. As a consequence of lower total power losses 25 °C higher junction temperature of Tvjopmax = 175 °C, the modules feature a higher power density [5]. At least 30 % higher output power from the same footprint is expected. This allows designing higher performance converters with the same type of the IGBT module packages, thus reducing the effort for redesign and upgrade.

Furthermore, thanks to the advanced interconnection technology, the internal module structure based on the .XT technology achieves significantly higher lifetime in terms of power- and thermal cycling load [6].

In the medium term, focus of evaluation is set on the application of power components based on the Silicon Carbide (SiC) MOSFET in Trench technology recently introduced [7]. Thanks to the exceptional properties of these components, especially considerably low switching losses compared to the Si IGBT modules, several improvements are expected in the properties of the DC choppers that employ such power components:

- Higher output power at switching frequencies exceeding 20 30 kHz while reducing the chopper's volume
- Higher efficiency and lower energy consumption with a positive impact on the cooling system's size and construction

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- Because of the high switching frequency, substantially reduced size and weight of the passive components such as power film capacitors and the DC chokes
- · Significantly reduced acoustic noise
- The cooling requirements for converters with the same output power will be significantly reduced, leading to smaller size and weight of the heat sinks and fans. Vice versa, a converter with the same size is expected to feature far higher output power

Dedicated power units are mandatory to properly operate energy storage systems especially in sensitive mobile applications. Besides the electrical performance, power density and efficiency mater but special attention has to be paid to the consequences resulting from cyclic load. In addition to the optimization in cooling and control of power flow, modern power semiconductor solutions allow reducing the losses which eases power dissipation in limited space. Wide band gap materials reveal outstanding electrical performance and the higher switching frequencies can be helpful in reducing the amount of material used in magnetic components. Despite all innovations in semiconductor development, proper thermal design, accurate temperature measurement and suitable thermal models remain an important part in the development flow for power electronic components.

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7th Generation 1700 V IGBT Modules: Loss Reduction and Excellent System Performance

For power electronic systems like industrial drives and converters for renewable energy applications, the major system requirements are: high reliability, high efficiency, high power density and competitive costs. In order to meet these requirements, power loss reduction is a key factor. Power loss reduction enables designs with higher power densities and lower IGBT junction temperatures. As a result, higher reliability can be achieved and the cooling system can be accordingly optimized. Therefore, Mitsubishi Electric has developed the new 1.7 kV 7th generation IGBT modules with improved performance.

By Masaomi Miyazawa, Thomas Radke and Narender Lakshmanan, Mitsubishi Electric Europe B.V.

1. Introduction

Power module performance affects the overall efficiency of the power electronic system. Accordingly, power modules have to be carefully chosen for a given application depending on various electrical and thermal performance parameters. Mitsubishi Electric had launched the latest 7th generation industrial IGBT modules in the 650 V and 1200 V classes [1]. These modules have already been well accepted by the market due to the advantages with regards to the key system requirements: high power density, high efficiency and high reliability. Subsequently, the 1700 V IGBT modules were developed to support applications with system voltages of 690 Vac.

For renewable applications, the AC-grid filter size can be reduced by increasing the IGBT switching frequency. In case of motor drives, higher switching frequencies are considered beneficial especially for operation at high output frequencies. Unfortunately, the switching loss behavior of the existing 1700 V modules available at the market has not encouraged the designers to explore the possibility of increasing the switching frequency for availing system level benefits. In order to enable operation at reasonable switching frequencies (above 1000 Hz) with the 1.7 kV IGBT modules, the 7th generation IGBT chips and the RFC (Relaxed Field of Cathode) diode chips [2] were developed and optimized for achieving a significant reduction in power loss.

An optimized line-up from 100 A to 600 A current rating has been developed. Further module developments with higher rated currents (up to 1200A) are ongoing.

2. 7th generation chip performance

In order to offer the best electrical characteristics, the latest 7th generation CSTBTTM chip [4] and RFC diode have been used in the 1.7 kV IGBT modules. These chips possess an optimized structure and are thinner than previous generation devices. Additionally, the devices have been designed by selecting an appropriate trade-off between the DC performance and the switching performance.

2.1 IGBT chip

The IGBT power loss and the EMI profile has been optimized by designing an optimized MOS structure, advanced termination, and a

reduction of the wafer thickness. Figure 1 shows the comparison of the trade-off between V_{CEsat} and E_{off} of the 7th generation IGBT with a standard IGBT chip available in the market today. The E_{off} of the 7th generation IGBT is approximately 30 percent lower in spite of the same on-sate voltage drop.

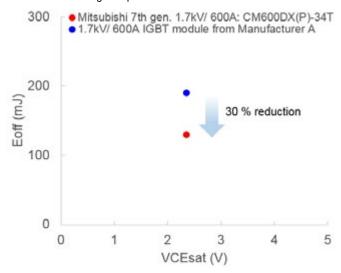


Figure 1: Comparison of the trade-off between V_{CEsat} and E_{off} Conditions: V_{CC} =1000 V, I_C =600 A, T_i =125 °C, R_G min.

2.2 Diode chip

The 7th generation 1.7kV IGBT module is equipped with the RFC diode in order to reduce power loss without generating unnecessary oscillations during switching. The RFC diode has a unique structure in which the P layer is partially added on the cathode side and holes are injected during the recovery period to soften the recovery waveform. Using the RFC structure, it was possible to develop a diode with a reduced wafer thickness and one which does not exhibit snappy behavior. Thus, it was possible to improve the diode trade-off (DC performance versus switching loss). Figure 2 shows the comparison of the trade-off between V_F and E_{rr}. A significant reduction (about 50%) of recovery losses has been achieved.

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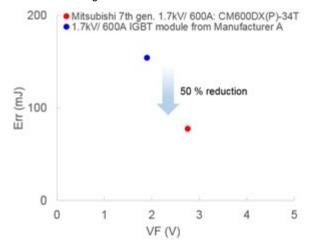
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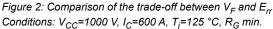


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 CSTBT[™] technology and RFC diodes
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Additionally, the lower recovery charge Q_{rr} results in a reduction of IGBT turn-on switching losses.





3. Power loss comparison

A loss simulation for several application conditions has been performed by using the free simulation software Melcosim [5]. Figure 3 shows the overall power loss comparison of 600A/1700V IGBT module CM600DX(P)-34T [6] with the IGBT module from Manufacturer A. As evident from Fig. 3, the power loss of the 7th generation IGBT module is approximately 30 percent lower under typical application conditions (considering a switching frequency of 2 kHz). It is clear that a major contributor to the loss improvement is the reduction of diode switching losses and the IGBT switching losses. For a heatsink with $R_{th(s-a)}$ =90 K/kW, the resulting IGBT-chip temperature T_i is 22 K lower at the given application conditions. However, if the junction temperature T_i is to be maintained the same, the output current can be increased by approximately 30%. Figure 4 shows the comparison of power loss in the 600A/1700V IGBT module as function of switching frequency. As evident from Fig. 4, the improvement rate is getting higher at a higher frequency. For example the power loss of the IGBT module from Manufacturer A at 2 kHz is almost the same as the overall power loss considering the 7th generation technology's performance at 4 kHz switching frequency. As a result, by maintaining the same efficiency, the switching frequency could be doubled from 2 kHz to 4 kHz. This increase in the switching frequency enables a remarkable size and cost reduction of passive components like filter chokes.

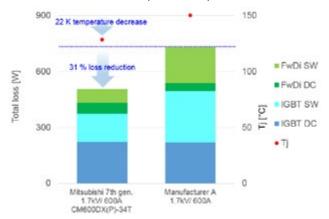


Figure 3: The Power loss comparison of the 600A/1700V IGBT module at 2 kHz

Conditions: V_{CC} =1000 V, I_{O} =270 A peak, f_{c} =2 kHz, $cos(\varphi)$ =0.8, M=1, T_{a} =40 °C, $R_{th(s-a)}$ =90 K/kW, R_{G} min.

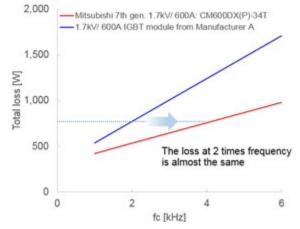


Figure 4: The power loss comparison considering the 600A/1700V IGBT module for several switching frequencies Conditions: V_{CC} =1000 V, I_0 =270 A_{peak} , $cos(\phi)$ =0.8, M=1, T_i =125 °C, R_G min.

4. Expanded line-up

In order to meet various applications requirements, Mitsubishi Electric has developed a comprehensive modules line-up in 1.7 kV class. Table 1 shows the line-up which includes 12 module types in the NX-package ranging from 100 A to 600 A and 6 module types in the standard package ranging from 75 A to 400 A. In the NX-type package, both solder-pin and press-fit-pin options have been developed for each current rating. They have different terminals. The press-fit-pin package can be assembled by solderless press process to the PCB board.

Furthermore, in the NX-type module, the SLC (Solid Cover) technology delivers an improved thermal cycle capability by combining a resininsulated metal baseplate and direct potting resin [3]. The advanced SLC technology enables the elimination of the internal bond wires between multiple ceramic substrates which resulting in lower parasitic inductance and higher reliability.

In the standard-type module (refer to Table 1), the TMS (Thick Metal Substrate) technology eliminates the solder layer under the substrate and increases the thermal cycle capability [1]. The parasitic inductance has been reduced by improving the internal layout. In addition, the main terminal pitch for the 62× 108 mm package is 28 mm, which is compatible to the existing package in Europe.

The 7th generation IGBT modules are available with the pre-applied PC-TIM (Phase Change Thermal Interface Material) optionally. It contributes to the simplification of the assembly process and improves the thermal contact between module base and heatsink.

Package Type	Model	Current Rating	Voltage Rating	Circuit	Packge Size W × D (mm)	Features
NX-type Package Solder-pin/ Press-fit-pin	CM100TX(P)-34T	100 A	1.7 kV	6 in 1	62 × 122	-
	CM150TX(P)-34T	150 A				
	CM225DX(P)-34T	225 A		2 in 1	62 × 152	
	CM300DX(P)-34T	300 A				-
	CM450DX(P)-34T	450 A				En:
	CM600DX(P)-34T	600 A				
Standard-type Package	CM75DY-34T	75 A		2 in 1	34 × 94	-000
	CM100DY-34T	100 A				
	CM150DY-34T	150 A			48 × 94	BBB
	CM200DY-34T	200 A				
	CM300DY-34T	300 A			62 × 108	DO D
	CM400DY-34T	400 A				

Table 1: Expanded line-up in 1.7 kV class. In the NX-type package, there are two pin types (solder and press-fit) in the each current rating.

To support applications requiring higher power ratings, a new industrial IGBT module with a half bridge configuration is under development. This new power module package which is shown in Figure 5 has a dimension of 100x144x40 mm³. IGBT modules based on the 7th generation chip technology, with a current ratings up to 1200 A in the 1700 V category are under consideration. In case an application requires higher current (more than 1200A) this module is an ideal solution since it is optimized for parallel operation thereby providing a scalable and an efficient solution for high power applications.

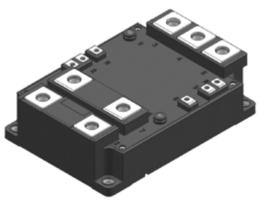


Figure 5: New industrial IGBT module

5. Summary

In the analysis presented here, the IGBT chip performance exhibits approximately 30% improved trade-off between the V_{CEsat} and E_{off}. The diode chip performance exhibits 50% lower E_{rr}. By utilizing these devices, the overall power loss is approximately 30% lower and Tj is

22 K lower than the performance of the IGBT module from Manufacturer A at 2 kHz and even more significant in case of higher switching frequencies. This enables either 30% higher output power or doubling the switching frequency (cost saving of passive components).

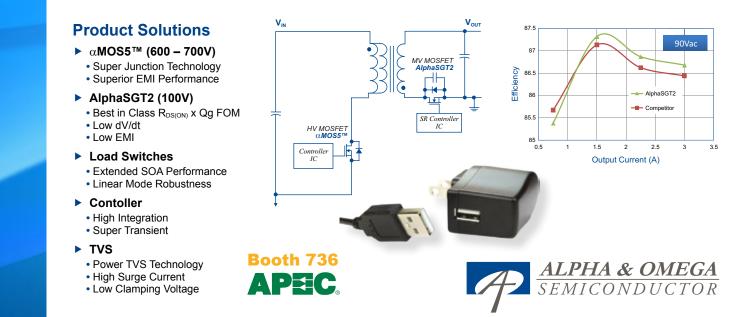
It is evident that Mitsubishi Electric offers several different types of power semiconductor modules (18 types of module designs) utilizing latest technologies in order to deliver the best system performance and the highest system reliability in the 1700 V category.

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Any type of power conversion system (e.g. solar inverter, electric drive, UPS, HVDC) requires an auxiliary power supply to provide a low voltage bus of e.g. 12V or 24V to supply gate-drivers, microcontrollers, displays, sensors or fans for proper system operation. The auxiliary power supply will need to operate from either a three-phase 400/480V AC supply in case of typical industrial equipment or a high DC voltage in the case of a photovoltaic inverter.

> By Christian Felgemacher, Walter Balzarotti and Bastian Lang, ROHM Semiconductor GmbH

The following article introduces an easy to design, cost effective solution, which utilises ROHM's SiC technology.

SiC MOSFET for compact auxiliary power supplies

Figure 1 shows a typical circuit used for auxiliary power supplies. Depending on the input voltage, the MOSFET has to withstand up to 1300V. Since a certain safety margin is desirable it is common practice to use devices rated for at least 1500V. Si MOSFETs with this breakdown-voltage rating are available, but produce high losses and therefore require bulky, expensive heat sinks.

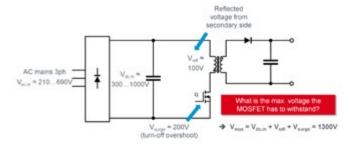


Figure 1: Flyback as typical auxiliary supply topology

One option is to use more complex topologies to avoid the need for 1500V MOSFETs (e.g. a two-switch flyback or a series connection of lower voltage devices); however, this leads to additional complexity and increased component count.

The availability of 1700V SiC MOSFETs with a specific on-state resistance approximately two magnitudes lower than that of 1500V Si MOSFETs (see Figure 2) offers the designer of an auxiliary power supply the option to use a simple single switch flyback topology and achieve good performance with a compact design. ROHM Semiconductor offers high-voltage SiC MOSFETs suitable for this type of application in a surface mount package (TO-268-2L) as well as in a fully moulded, isolated TO-3PFM package. These devices feature extended creepage distances of 5mm and 5.45m respectively.

Control IC enables cost effective SiC-based single-switch flyback topology

The SiC flyback based auxiliary power supply solution gains further attractiveness by the availability of a control IC specifically designed to drive the SiC power MOSFET in this topology in a safe and reliable way without the complexity introduced by a gate driver IC.

With the BD768xFJ ROHM Semiconductor has released a quasiresonant AC-DC controller IC that is compatible with several SiC MOSFETs available on the market today, in particular in terms of the gate-drive requirements of these devices. The best match for efficiency and performance is obtained when combining the BD768xFJ control IC with the ROHM 1700V SiC MOSFET. The BD768xFJ not only implements all the control for the flyback circuit but also takes care of driving the SiC MOSFET with suitable gate-voltage to ensure optimal performance. In addition the gate-clamp and overload protection features ensure the protection of the SiC MOSFET.

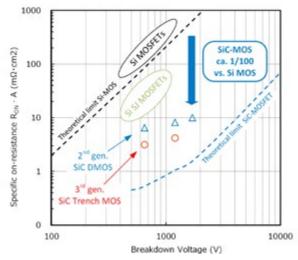


Figure 2: Specific On Resistance of Si and SiC MOSFETs

The control-IC BD768xFJ is housed in a compact SOP8-J8 package and offers a series of functions and protection features, including current sense with external shunt, overload, input brown-out and output overvoltage protection as well as soft-start. In the entire operating region quasi-resonant switching is realised to minimise EMI and ensure low switching losses. To optimise operation at low load frequencyreduction modes as well as burst operation are implemented in the controller.

The principal circuit of a simple yet high performant auxiliary power supply unit based on the BD768xFJ control IC and a ROHM 1700V SiC MOSFET is shown in the following diagram.

Performance of SiC MOSFET based auxiliary power supply To show the performance that can be achieved with a simple auxiliary power supply based on SiC MOSFETs an evaluation board was developed (see Figure 4). In this circuit example the BD768xFJ-LB

3 Phase AC INPUT

Figure 3: Auxiliary power supply circuit using BD728xFJ control IC and 1700V SiC MOSFET



Figure 4: Evaluation board for SiC based auxiliary power supply unit

is used to drive a 1700V SiC MOSFET (SCT2H12NZ) in a quasiresonant switching AC/DC converter. The quasi-resonant operation minimises switching losses and helps to keep EMI low. The current detection is realised through an external resistor. Power efficiency is

> maximised by the use of the controller's burstmode operation and the reduction of the switching frequency under light load conditions.

Switching waveforms of the SiC MOSFET are shown in Figure 5. The waveforms at different output loads illustrate how the controller selects different valleys of the resonating drain-source voltage for turn-on of the SiC MOSFET. This quasi-resonant operation minimises switching losses and EMI. After exiting the burst mode at very light load, the quasi resonant mode is established and a high number of valleys are skipped before restarting a new cycle and switching on the transistor (left picture

at Pout=5W). As the output power is increased, fewer valleys are skipped before restarting the cycle, which leads to an increase in frequency (Picture at Pout=20W). Close to the maximum defined output power (in this case 40W) the last valley is reached. The switching frequency reaches the maximum of 120 kHz at this point.

A higher demand in output power can be served with a slight decrease in switching frequency, to increase the on-time of the primary switch. This increases the primary current peak and therefore the transferred energy (Picture at Pout = 40W). Above the maximum output power level the over current protection is triggered and the switching action is blocked to protect the system from overheating.

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The board operates in discontinuous conduction mode (DCM) for the first two operating points and boundary conduction mode (BCM) is just reached at the last operating point (40W). Depending on the input voltage the transition between DCM and BCM occurs at different output power levels performance of the high voltage Si power MOSFETs. Furthermore, it is not desirable to invest a lot of design effort to design aux power supplies using complex architectures such as two-switch-flyback or stacked MOS-FETs, because this design effort is better spend on the main power system.

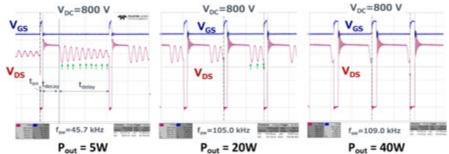
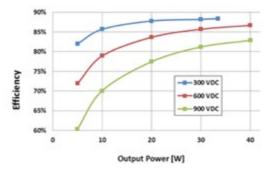


Figure 5: Switching waveforms of SiC MOSFET in quasi-resonant operation



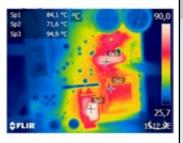


Figure 6: Measurements conducted on SiC auxiliary supply unit

The efficiency for different input voltages across a load range of up to 40 W and an output voltage of 12V is shown in the diagram below. Throughout the measurements, as shown below, it was confirmed that the case temperature of the SiC MOSFET remains below 90°C. The maximum allowable junction temperature of the SiC MOSFET is 175°C. Since the thermal resistance chip-tocase is much lower than case-to-ambient it is safe to assume in this case that the junction temperature is sufficiently lower than the limit, which confirms that operation of this board without a heatsink is possible at up to 40W output power. A higher output power can be achieved if a heatsink is used for the SiC MOSFET and cooling of the output rectification diode is improved. While measurements with DC input voltages are shown here it is also possible to operate the evaluation board from a three-phase AC supply of 400/480V. The required diode bridge for line-rectification is implemented on the PCB

SiC MOSFET technology allows designers to achieve improved efficiency, simplicity, reliability and compactness. Simple, cost effective one-switch-flyback solutions for 3 phase input or with DC input voltages above 400V are not practical with Si MOSFETs at some tens of Watts of power due to the poor The superior performance of 1700V SiC MOSFETs and the availability of the control IC family BD768xFJ allow the design of simple auxiliary power supplies for 3 phase systems or for systems with high DC input voltage with good performance. The SiC MOSFET technology allows designers to achieve improved efficiency, simplicity, reliability and compactness. This can be achieved at a system cost comparable to Si MOSFET solutions as a result of the performance benefits of the 1700V SiC MOSFET. In addition, the cost of expensive components such as heatsinks and magnetics can be reduced. The control IC is optimised to safely drive the SiC MOSFET to help realise a very simple solution that reduces the design effort and minimises the time to market of the system.

An application note with more detailed schematics, a dimensioning guide and a component list as well as further information is available on the ROHM website. Evaluation boards illustrating the operation of the matched combination of control IC and SiC MOSFET for auxiliary power supply units can be obtained by contacting ROHM Semiconductor GmbH.

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SiC Cascodes and Their Advantages in Power Electronic Applications

Silicon carbide cascodes are hybrid devices that give the advantages of a wide band-gap semiconductor switch with the flexibility and ruggedness of silicon MOSFETs. They can be used as drop-in replacements in legacy systems as well as next-generation power converters and inverters.

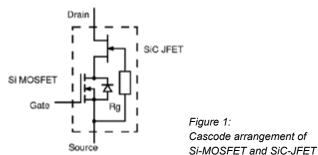
By Christopher Rocneanu, Director Sales Europe & North America, United Silicon Carbide Inc.

Wide band-gap devices make attractive promises, but... It's hardly necessary to describe the qualities of wide band-gap (WBG) devices using silicon carbide (SiC) and gallium nitride (GaN) technology. The headlines promise extreme power densities and matching efficiencies, with examples such as the recent "Little Box Challenge" that saw the target power density for a specified converter beaten by a factor of three. In real systems, designers want normally OFF switches - which SiC MOSFETs and enhancement-mode GaN (e-GaN) HEMT cells provide - but they are not perfect; each has its own limitations and quirks. Both types need very specific gate-drive voltages; SiC MOSFETs have relatively poor body diodes and GaN devices have no classical body diode and no avalanche voltage characteristic. In many practical applications, a body diode or equivalent is needed, for example in "choppers," half-bridges and "totem-pole" PFC stages. For sensible efficiencies, SiC-MOSFETs and GaN HEMTs need a parallel high-performance diode, adding to the overall cost and complexity.

SiC cascodes - a modern twist on an old idea

To try to make the best of WBG technology, manufacturers have revisited an old idea from the 1930s, where vacuum tubes were put in series to form a hybrid device with performance better than either of the individual parts. The technique was christened "cascode" and has re-surfaced over the years in BJT and MOSFET form.

In its WBG implementation, a cascode is a series connection of a Si-MOSFET and a normally ON SiC-JFET (Figure 1). When the gate is high, the MOSFET is ON, shorting the JFET gate-to-source, forcing it ON. When the MOSFET gate is low, its drain voltage rises until the JFET gate-to-source voltage reaches about -7V, turning it OFF and leaving about 7–10V on the MOSFET drain. The hybrid becomes normally OFF, the gate-drive voltages are now non-critical and the body diode of the MOSFET is fast with very low reverse recovery charge and has low voltage drop. These attributes stem from the fact that the MOSFET is a low-voltage type, optimized for the application and typically co-packaged with the SiC die.



The cascode can now stand as a compelling alternative to SiC-MOSFETs, GaN HEMTs and are readily used in legacy designs that currently use Si-MOSFETs and IGBTs. Comparing a typical 650V cascode with other WBG devices and a superjunction Si-MOSFET, Figure 2 gives some headlines.

Technology	SiC Cascode 650V – 45mΩ (UJC6505K)	Commercial SiC MOS- FET Gen 3	Commercial E-GaN HEMT	Commercial Si-Super- junction MOSFET
RDSA	0.75 mΩ- cm ²	$2-3 \text{ m}\Omega\text{-cm}^2$	3-7 mΩ-cm ²	10 mΩ-cm ²
Normalized Die Area	1	2.6x	4x	
EOSS	7.5 µJ	22 µJ	12 µJ	14 µJ
RDS*EOSS	255	660	350	480
VTH	5	2.8	1.3	3.5
Avalanche Capability	YES	YES	NO	YES
Short Circuit	YES	YES	NO	YES
Gate Drive maximum	+/-25V	+22/-6V	+7/-10V	+/-20V
Gate Drive Recom- mended	+12/0V	+18/-0V	+6/-3V	+12/-5V
Intrinsic diode Qrr	85nC	53nC	No diode	13µC
Intrinsic diode Vf	1.5V	4.3V	No diode	0.9V

Figure 2: SiC cascodes compared with other WBG devices and superjunction

MOSFETs

A stand-out value is the figure of merit RDSA, implying a very small die size, all else being equal. This in turn gives low "Miller" input and output capacitance COSS, leading to low switching-loss EOSS, and a class-leading figure of merit for overall losses, RDS*EOSS. Cascodes perform well under avalanche conditions with a natural clamping effect, unlike GaN for example, which has no avalanche rating. Momentary short-circuits of 4µs or more are handled well by cascodes with high saturation currents, "pinching off" the channel. The positive temperature coefficient of ON-resistance also helps. Unlike the other devices, the saturation current is not dependent on the gate-drive voltage and remains near constant after full enhancement at about 8V VGS.

Although die size is small, heat transfer is still efficient, with SiC having thermal conductivity three times better than GaN or Si and a high TJ(MAX), typical of a WBG device.

The wide +/-25V gate-drive voltage swing allowed with cascodes means that systems designed for Si or SiC MOSFETs are directly compatible, so cascodes can be drop-in replacements in this respect. Even IGBT gate-drive swings of typically +15/-9V will drive the cascodes happily, offering the prospect of changing out the old switch technology for better performance, or as older devices become obsolete. A case study with a battery charger manufacturer, changing out IGBTs for cascodes, resulted in 1.5% efficiency savings and 30% more power throughput at the 10kW level [1]. Cascode gate charge is significantly less than IGBTs and, if gate-voltage swing is adjusted to be lower, gate-drive power requirements are cut dramatically.

Cascodes are available in the familiar TO-247 format so will often mechanically drop in to IGBT or Si/SiC-MOSFET sockets, but minor changes to the gate-drive circuit will optimize the solution. Figure 3 shows a typical circuit with separate values for R(ON) and R(OFF), which gives effective control of dV/dt and di/dt levels. The ferrite bead damps oscillations as necessary depending on layout. A negative gate-drive voltage is not necessary to prevent injection of current into the gate from drain dV/dt causing spurious turn-on, as the Miller capacitance is effectively absent. Layout around the gate should anyway follow good practice as shown, as with any switch type, to minimize inductance in the source connection, which might couple voltage transients into the gate from channel di/dt.

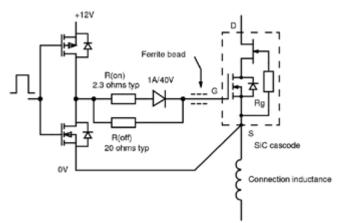


Figure 3: Typical SiC cascode gate drive

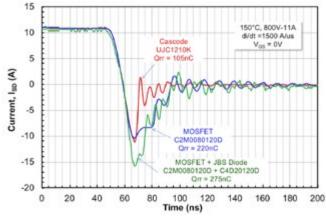


Figure 4: Cascode intrinsic diode reverse recovery characteristics



The comparison table also shows that the intrinsic diode recovery charge of SiC cascodes compares favorably and, combined with its low forward drop Vf, gives minimum energy loss in circuits where the diode conducts. Figure 4 shows comparative waveforms with a cascode and SiC MOSFET, with and without external diode, with an 800V inductive load at 150°C. Using the double-pulse method, as the cascode turns OFF, it clearly shows shorter recovery time and lower dissipated energy.

There is literally no direct comparison with GaN, as the technology has no intrinsic diode, but GaN will conduct in reverse as the channel conductivity increases when the drain gate voltage goes negative. There is no reverse recovery charge, but the voltage drop is relatively high so a parallel diode is usually added when reverse conduction is required, adding in its own recovery characteristics.

The applications

As well as being replacements for IGBTs and Si-MOSFETs in legacy systems, cascodes with their near-ideal combination of specifications and small die size are contenders for new designs in the key areas of

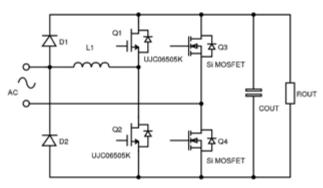


Figure 5: SiC devices in a bridgeless totem-pole PFC stage

motor drives, inverters, PVs, welding, class D audio amplifiers, EVs/ HEVs and more. With a "ground-up" approach to design, the highfrequency capability of the devices can be exploited to leverage gains in magnetics and passive component sizes.

Major benefits are seen particularly in the bridgeless totem-pole PFC application. (Figure 5). Here, previous circuits using Si technology have been limited by the slow performance of body diodes in the MOSFETs typically used. A parallel SiC diode helps, but defeats the object of reducing component count. Critical conduction mode has had to be used, which sets switching current to zero at the end of each conduction period. However, this variable-frequency mode produces high peak currents with consequent stress, necessitating oversized components. Using cascode SiC-JFETs, continuous conduction mode can be used with lower peak currents, increasing efficiency, reducing inductor size and easing filtering and EMI problems with

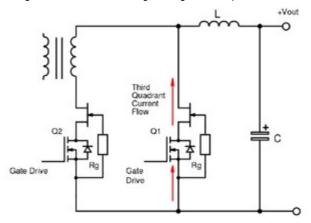


Figure 6: SiC cascodes in synchronous rectification

fixed operating frequency. An example circuit using USCi UJC06505K devices at 1.5kW and 230VAC-line showed an impressive efficiency of 99.4% [2].

Achieving high efficiency in converter primary switches must be matched with similar improvements in rectification for DC outputs. Again, SiC cascodes fit here as they can be configured for "synchronous rectification" (Figure 6). In so-called third-quadrant operation, current flows from source to drain of one or other of the cascodes through the output inductor to the load during the "forward" and "flywheel" periods of forward or buck-derived converters. Current flow through the body diode sets the JFET gate-source voltage to approximately +0.7V, turning it naturally hard ON. If the cascode gate is set high, the internal Si-MOSFET channel conducts and the total ON-resistance becomes the RDS(on) of the cascode, giving low conduction losses. Q1 forms the flywheel rectifier and Q2 the forward rectifier.

Summary

SiC cascodes are an easy introduction to wide band-gap devices, giving benefits in new designs and as replacements for IGBTs and Si-MOSFETs in legacy systems.

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Full SiC Performance in Power Modules – The Tuning makes the difference

Discrete devices such as the TO-247 are fine as a first step towards integrating silicon carbide into various applications, but for more powerful and sophisticated designs, the integration capabilities of power modules make them the first choice. But which packages are suitable for fast switching silicon carbide devices?

By Stefan Häuser, Senior Manager, Product Marketing International, Semikron

Silicon carbide can be the right semiconductor to choose when conventional silicon devices reach their limits in terms of power losses and switching frequency. Up to 30 to 40kHz, the latest-generation silicon IGBTs and diodes combined with new topologies such as multilevel configuration provide the best cost-performance ratio. Hybrid silicon carbide, combining a high-speed silicon IGBT and a silicon carbide Schottky free-wheeling diode, is also a great option, reducing the power losses by up to 50% compared to silicon-only solutions.

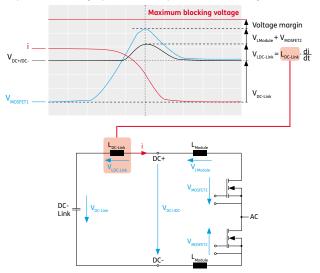


Figure 1: Module and system inductance and their influence on transient overvoltage during MOSFET turn-off

Above 40kHz, SiC MOSFETs can be the best choice, but lead to challenges for the power module and system design. Fast switching incurs steep current slopes and high di/dt values. The module's and system's parasitic inductances, L_{Module} and $L_{DC-Link}$, cause voltage drops due to this di/dt, resulting in voltage overshoot across the chips.

If the current slope is too high, this overvoltage might exceed the maximum blocking voltage, e.g. 1200V, of the SiC device. Decreasing the switching speed or the DC link voltage $V_{DC-link}$ will reduce the overvoltage but compromise the SiC power module's performance. A module and system design focused on low commutation inductance is therefore essential.

The module's commutation inductance is mainly provided by the DC bus terminals with 12 to 18nH, depending on the power module

design. The DBC design, i.e. DBC tracks and wire bonds, contribute another 1 to 6nH. The degree of optimisation freedom depends greatly on the overall power module design.

The SEMITRANS 3 module includes optimised DC bus terminals. Thanks to parallel guidance of the terminals internally, the commutation inductance of the complete package is 15nH. This makes the SEMITRANS 3 very good for medium- and high-power silicon carbide designs using medium switching speeds and frequencies up to approx. 25 kHz. Full SiC half-bridge topologies are available with rated currents of 350A and 500A, with and without a SiC Schottky freewheeling 1200V diode.

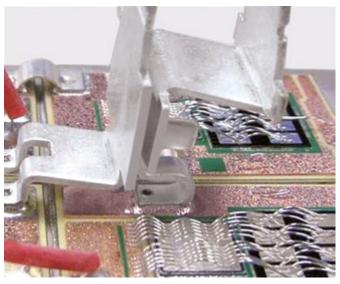


Figure 2: SEMITRANS 3 DC bus terminals: parallel construction minimises stray inductance.

Another example is the MiniSKiiP, a baseplate-less power module using Semikron's SPRiNG system to connect the power and auxiliary terminals to the PCB. Having spring positions fixed by the housing design, commutation inductance can only be improved within the limits of the DBC design. The resulting commutation inductance is around 20nH for 6-pack power modules, which allows full SiC modules for the low- and medium-power range. In full SiC MiniSKiiP is available with 25A to 90A in 6-pack topology for 1200V and with 50A, 100A and 150A with hybrid SiC chipsets. SEMITOP E2 is the baseplate-less module that allows full optimisation. With its pin-grid structure on the top of the housing, the press-fit pins can be freely distributed over the complete footprint. Extensive simulations helped to create a half-bridge design with only 6nH commutation inductance. The module is equipped with 6 SiC MOSFETs in parallel, resulting in an R_{ds,on} of 7.5mOhm at 25°C.

Thanks to the design, the AC and DC sides are separated on opposite edges of the module, so the DC link PCB can be designed to be low-inductance as well. This means DC+ and DC– can remain paralleled within the PCB for a maximum distance, reducing the commutation loop.



Figure 3: SEMITOP E2 with its pin-grid structure

The advantage of optimised commutation inductance is a safe operating area that supports switching speeds of over 50kV/µs at 600V DC link voltage, including a sufficient margin between the blocking voltage of the SiC MOSFET and the overvoltage measured across the MOSFET chips. Fig. 4 shows the switching losses versus the drain current with an external gate resistor of 0.5 Ω in addition to the internal gate resistor of 0.5 Ω .

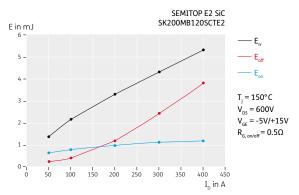


Figure 4: Switching losses of the SEMITOP E2 SiC versus the drain current ID

The overall thermal performance of the power module is also important. The power density of silicon carbide chips is higher than that of silicon devices. SiC MOSFETs demonstrate significantly lower switching losses in general and especially lower voltage drops under partial load than silicon IGBTs with the same nominal current. This produces smaller chip areas under nominal load, with an undesirable higher thermal resistance from chip to baseplate or heatsink (R_{th(j-c)} resp. R_{th(j-s)}).

Yet the chip area might then not be sufficient for overload conditions. Due to the usually positive temperature coefficient of SiC devices, the static or forward losses gain importance and increase the overall losses during an overload. Adding additional SiC MOSFET chips to reduce the $R_{DS,on}$ would increase the overload capability, but also the cost of the power module. SiC is still expensive and only the minimum SiC chip area required should be used. The solution lies in improving the module's thermal resistance.

Within a baseplate power module, the ceramic substrate that electrically insulates the module to the heatsink represents the biggest share of overall thermal resistance. Today, numerous materials exhibiting different mechanical and thermal behaviour are available. Table 1 gives an overview of the most commonly used materials: Aluminium oxide (Al_2O_3), silicon nitride (Si_3N_4) and aluminium nitride (AIN).

Ceramic substrate material	Al ₂ O ₃	Si ₃ N ₄	AIN
Thermal conductivity (W/mK)	~25	~90	~180
Standard thickness (mm)	0.38	0.32	0.63
Resulting thermal performance	100%	~400%	~400%
Bending strength (MPa)	450	650	320
Fracture toughness (MPa/√m)	3.8-4.2	6.5-7	2.6
Mechanical robustness	0	+	-

Table 1: Mechanical and thermal specifications of different ceramic substrates

The standard today is aluminium oxide, providing a good trade-off between thermal/mechanical behaviour and cost. AlN has 9 times the thermal conductivity of Al_2O_3 , but is less mechanically stable. This weakness must be offset with increased thickness, which compromises thermal improvement.

 $\rm Si_3N_4$ has 3.5 times the thermal conductivity of $\rm Al_2O_3$, but has the best mechanical specifications. This material is therefore used in thinner layers, which compensates for the lower thermal conductivity and produces a similar thermal performance to AIN. Table 1 shows an overview of the three materials, summarising their thermal performance and mechanical robustness.

	SEMITRANS 3 Full SiC Al ₂ O ₃	SEMITRANS 3 Full SiC AIN
No. of chips per switch	12	8
Used chip area	100%	66%
R _{th(j-c)} per chip	0.84K/W	0.54K/W
Cont. drain current I _D (T _j =175°C/T _c =80°C)	431A	416A
Module cost	100%	75%

Table 2: SEMITRANS 3 full SiC case study

Table 2 shows a case study for the SEMITRANS 3 full SiC half-bridge power module. Available with Al_2O_3 and AIN substrates, the benefit of a substrate with increased thermal performance is obvious. The Al_2O_3 version uses 12 chips per switch at 100% module cost to achieve a continuous drain current of 431A. If the substrate is changed to AIN and the chips reduced to 8, the continuous drain current remains in the same range while the cost of the power module is reduced to 75%.

Replacing time-consuming production processes with TO devicebased power designs is only possible using silicon or silicon carbide power modules. The specific features of SiC require optimisation of the commutation inductance and thermal performance. As a result, the cost-performance ratio can be improved and the advantages of SiC fully utilised to the application's benefit.

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High Efficiency IGBT M7 Chip Technology utilized in the Mid Power Package VINco E3

....in Response to Market Demands

Power semiconductors are the core components of any energy conversion system and are key for efficient utilization of energy. Achieving minimum power loss is one of the most important goals in the development and use of power semiconductors, and it is fundamental for meeting the market demands for saving energy. Low radiation noise, wide safe operation and high reliability are additional key development goals.

By Dr. Evangelos Theodossiu, Product Marketing Manager, Vincotech GmbH Unterhaching

Current silicon based semiconductors are approaching their physical limits in terms of physical properties. However, there is still room for improvement and semiconductor engineers are working on this continuously. As a result, Mitsubishi Electric has recently introduced the M7 chip technology, its latest generation. Using new technologies, such as ultra-thin wafer processing and new backside doping techniques, they have achieved their goal of improving usability for industrial applications.

Power module packaging technology plays a vital role in ensuring optimal utilization of this new chip technology. VINco E3, a new midpower package based on the so called SoLid Cover (SLC) technology, has been developed with high thermal cycling capability and full compatibility to the standard industry packages. Higher thermal cycling capability helps increase reliability and life time, and compatibility with standard packages ensures ease of use and optimized manufacturing costs. The new M7 chip technology and optimized VINco E3 packaging offers a powerful combination to meet the demands of the market. This article will describe the core features of the new M7 chips and the new VINco E3 package and the benefits of this combination based on an application benchmark.



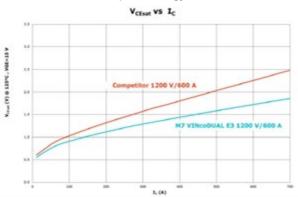


Figure 1: IGBT M7 vs competitor: V_{CE} as a function of IC at 105°C TJ

IGBTs

For the IGBT M7, Mitsubischi Electric is using the same carrier stored trench-gate bipolar transistor (CSTBT) structure as used in gen 6. The IGBT M7 has been improved through ultra-thin wafer processing, resulting in significantly reduced the VCEsat and associated losses. Figure 1 is a comparison of V_{CEsat} between the IGBT M7 and the best competitor, and clearly shows more than 20% (@600 A Ic) lower conduction power losses for the IGBT M7. While usually an IGBT

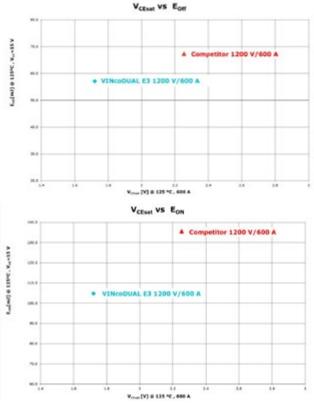


Figure 2: IGBT M7 vs competitor: Improvement in V_{CEsat} and E_{off}/E_{on} leads to a reduction of the total power losses

optimized for very low conduction losses would have higher switching losses and vice versa, figure 2 clearly shows that the IGBT M7 offers both lower switching losses and lower conduction losses. The benchmark was done with the new VINcoDUAL E3 package which is described also in this article. This improvement in both VCEsat and Eoff/Eon leads to a reduction of the total power losses. By thinning the wafer, there is an increased risk of reducing the safe operating area (SOA) capability of the device. However, this risk have been eliminated by a optimization of the MOS structure (gate capacitance). In addition to the improved SOA capability, the controllability (dv/dt) of the device with the gate resistance has been improved compared to gen 6.

Diodes

The M7 diodes, compared to the conventional diffusion wafer diodes, have been developed with the new Relaxed Field of Cathode (RFC) technology adopting a new backside structure and thinner wafer technology. However, reducing the chip thickness increases the risk of chip destruction due stronger snap-off reverse recovery behaviour. This risk has been eliminated with the RFC technology. The turn-on switching wavefrom of the M7 diode in figure 3 shows a lower current overshoot and less oscillation compared to the competitor diode. This allows EMC to be optimized and total sytem costs can be reduced. An additional benefit of the thinner wafer is reduced the forward voltage (V_f) drop. From gen 6 to gen 7, the V_f has been reduced by approximately 20%. The RFC structure of the M7 diode signifcantly improves the Erec without the usual increase in V_f, as seen in figure 4, and leads to more than 40% reduction in reverse recovery losses.

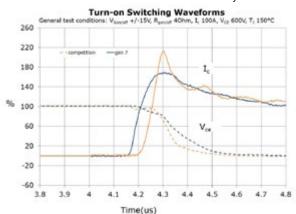


Figure 3: M7 diode vs competitor: Turn-on switching waveform

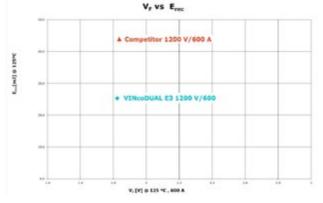


Figure 4: M7 diode vs competitor: Improvement in E_{rec} leads to a reduction of the reverse recovery losses

New Mid Power Package VINco E3

Power modules are the heart of industrial drives and they are responsible for their reliable and cost efficient usage. The continu-

ous improvement of this key component is a major goal of all power module manufacturers. The new SLC technology, a newly developed packaging technology from Mitsubishi Electric, is a big step forward in realizing high reliability power modules. This packaging technology has been utilized in the new VINco E3 product line.

The SLC technology differs from standard package technology with two key features as shown in figure 5; the insulating metal baseplate (IMB) and the direct potting resin (DP-resin) encapsulation.

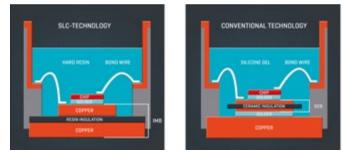


Figure 5: Comparison of SLC technology and standard package technology with base plate; cross section comparison on the top and explosion image comparison on the bottom

The IMB replaces the conventionally used ceramic isolation DCB and combines an electrically insulating resin layer with a directly bonded top- and bottom-side copper layer. Careful selection of the insulation material and resin layer thickness ensures the required insulation and heat dissipation properties. The insulating resin layer has the same coefficient thermal expansion (CTE) value of about 17x10-6/K as the copper layer. As a result, the thermo mechanical stress caused by any mismatch between two different CTEs has been reduced. Furthermore, the baseplate solder layer is completely eliminated as the top and bottom copper layers are directly bonded to the insulating resin layer. As a result the thermal cycling capability of the SLC technology is superior and ongoing results show a significant improvement in thermal cycling capability when compared to standard package technology. Finally, as mechanical stress in the solder layer increases with substrate size, the maximum size of standard packaging technology DCBs is limited. As shown in Figure 5, two or three substrates are therefore necessary to ensure thermal cycling capability of standard packaging technology. These multiple substrates have to be electrically connected with wires which increases the internal parasitic inductance. SLC Technology does not suffer from these limitations thanks to the use of the common IMB. It also increases the effective area available for dies and gives more flexibility for optimal layouts.

The second key element of the SLC technology is the use of hard DP-resin compared with the soft silicone gel of the standard package technology. The DP-resin distributes the mechanical stress on the wire bonds more homogeneously and helps support the wire bond solder joint which improves the power cycling capability. In addition, the CTE value of the DP-resin is similar to that of the IMB and the case. This eliminates the "pumping-out" failure phenomenon where the thermal interface material is "pumped out" from the module-heat-sink interface during temperature cycling.

With the combination of the IMB and the hard DP-resin encapsulation, VINco E3 offers a high reliability mid-power package for the industrial market.

Application Benchmark

The key features of the new M7 chip technology and the new SLC packaging technology have been described above. Every new tech-

nology should be compared with the established standard technologies and demonstrate its performance and benefits for the customer. This has been done with an application benchmark between the VINco E3 and a standard industry package from the best competition on the market. Both modules have been measured and simulation models have been created. VincotechISE[1], the simulation software used for the benchmark, provides a fast and accurate way of comparing power losses and temperatures at various operating points. The flowSIM tool simulates Vincotech power modules for industrial drive applications. It features parameter setup and function blocks tailored for industrial drive applications.



Figure 6: VINcoDUAL E3

The application benchmark compares the 1200 V/600 A VINco E3 (A0-VS122PA600M7-L759F70) module with a similar module from competition. A typical motor drive operation point has been selected for the comparison: lout 300 A, Vout 380 V, cosPhi 0,8, Theatsink 80°C and the benchmark simulations use the same gate resistance value of 2 Ohm for both modules. These conditions model a typical 2nd source strategy where a customer uses a single application board design on a production line, but can select between different supplier power modules during manufacture depending on availability etc.

Figure 7 shows the total power loss simulation results for different switching frequencies. The new M7 chip technology in the VINco E3 package reduces the power losses by up to 13% compared with the competitor module. The superior dynamic performance of the M7 diodes is a major contributor to the loss reduction, but also the dynamic and static characteristics of the IGBT M7 contribute to the loss reduction. This loss reduction results in higher efficiency and contributes to the energy savings and eco-friendly operation of the inverter.

VINco E3 Line-up Plan

The initial VINco E3 modules available support blocking voltages up to 1200 V in a half bridge configuration and cover current ratings from 300 A to 690 A. Sixpack and PIM topologies are under development as well as blocking voltage classes 650 V and 1700 V. To support higher current ratings and higher blocking voltages, a new IMB is in the qualification phase with an improved insulating resin layer. Figure 8 shows the comprehensive VINco E3 line up currently in development featuring the new M7 chip technology and the new SLC package technology to support a wide range of application. Following a multiple source strategy to provide customers with the highest supply chain security, the new VINco E3 will also be available with additional chip technologies such as the IGBT4 Trench field. VINco E3 will also be available with press-fit terminals and pre-applied phase change material for a cost efficient assembly process.

Topology	Housing	V _{cts} 650 V	V _{css} 1200 V	V _{crs} 1700 V	Chip Technology
Half-Bridge	VINcoDUAL E3	300 A	300 A	300 A	IGBT M7 / Trench IGBT4
Half-Bridge	VINcoDUAL E3	450 A	450 A	450 A	IGBT M7 / Trench IGBT4
Half-Bridge	VINcoDUAL E3	600 A	600 A	600 A	IGBT M7 / Trench IGBT4
Half-Bridge	VINcoDUAL E3		690 A		IGBT M7
Stopack	VINCOPACK E3	100 A	100 A	100 A	IGBT M7 / Trench IGBT4
Stypack	VINcoPACK E3	150 A	150 A	150 A	IGBT M7 / Trench IGBT4
Skpack	VINcoPACK E3	200 A	200 A		IGBT M7 / Trench IGBT4
PIM	VINcoPIM E3		150 A		IGBT M7 / Trench IGBT4
PIM	VINcoPIM E3	150 A	100 A		IGBT M7 / Trench IGBT4
PIM	VINcoPIM E3	100 A	75 A		IGBT M7 / Trench IGBT4

Figure 8: Planned line up of the new VINco E3 product line

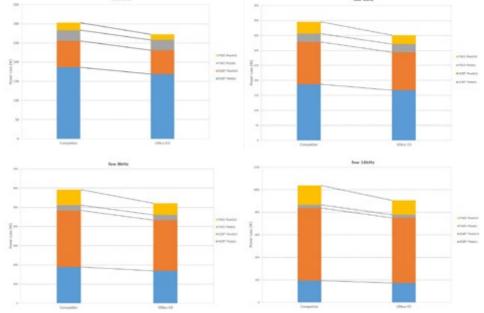


Figure 7: Total power loss simulation comparison between VINco E3 (1200 V/450 A) and appropriate competitor for a typical motor drive operation point lout 300 A, Vout 380 V, cosPhi 0,8 and switching frequencies from 4 kHz up to 16 kHz.

Summary

The new VINco E3 product line offers an efficient and reliable mid-power package by utilizing the new M7 chip technology and the SLC package technology. The new IGBT M7 offers superior performance for industrial drive applications and helps meet development goals for lower power losses, higher efficiency and eco-friendly operation inverters. The new SLC package technology with the IMB and the hard DP-resin encapsulation provides a high reliability package with a superior thermal cycling capability. The combination of these two features utilized in VINco E3 ensures flexible and cost optimized inverter designs.

Literatur

[1] http://www.vincotech.com/en/support/ simulation-software.html

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Designing a 15ns Gate Drive Transformer

ICE Components Inc. was asked to design a gate drive transformer capable of driving two MOSFETs at 1MHz with a 15ns pulse width. The customer's existing design was unable to deliver enough power to the load. This article explains the technical difficulties we faced and describes our solution.

By George Stokes, President, Ice Components Inc.

The specification

When Robin Benas, the ICE Components engineer, saw the specification of the new gate drive transformer (GT) he knew the project was unusual. The transformer had to be able to switch 12V at 1MHz with a pulse width of 15ns. Switching frequencies of 1 MHz are rare in gate drive topologies. The transformer would "drive" two MOSFETs with one primary and two secondary windings, a 1:1:1 turns ratio design, and had to maintain a voltage isolation of at least 3kV between the primary circuit and both secondaries.

The challenges

If you mention 1MHz switching to a magnetics engineer, the first things that come to mind are self-resonant frequency (SRF) and core loss. Adding to the challenge, the quantities needed by the customer would not justify any tooling expense and the customer preferred SMD. In this application, Robin needed to consider using only available materials, providing SMD mounting and ensuring easy manufacturability.

As you can see in the SRF formula, Robin needed to keep both capacitance and inductance as low as possible.

$$Fo = \frac{1}{2\pi f \sqrt{L_P C_D}}$$

Here LP, the primary inductance, is affected by the number of turns among other factors. CD is the distributed capacitance and is affected by wire proximity, insulation thickness and the dielectric constant of the insulation. The final challenge was to find a suitable core material for operation at 1Mhz that was available in the needed geometry.

The design

Based on past experience and taking into account all the challenges, Robin knew he must minimize the turns. The final design would

Gate Drive Transformers

Gate drive transformers (GTs) are a key component in many modern electronic systems.

These simple devices are used to drive the gate of metal oxide field effect transformers (MOSFETs) while providing galvanic isolation between the gate and the control circuitry. GT's also allow the drive of several MOSFETs while utilizing a single control circuit.

be greatly simplified if he could meet the requirements using single turn windings. Based on a single turn, he calculated the core area needed and then went looking for a core.

$$A_e = \frac{E_p x 10^8}{4.0 N_p f \beta}$$

$$0.3 \ cm^2 = \frac{12x10^6}{4.0(1 \times 10^6)(1,000)}$$

He felt his best bet would be to use a planar core as they offer a large core area to core length ratio compared to other geometries. Robin chose a PLT18/10/2 core with an AE of 0.4 cm2. The next step was to check if a material suitable for the switching frequency was available. He was happy to find that Ferroxcube had 3F36, a good high frequency low loss material available and in stock in the core geometry.

When picking the wire type and size Robin needed to balance the design requirements against the manufacturability of the part. Two factors influenced his wire type choice. First, he needed an isolation voltage of at least 3kV between primary and secondary windings. Second, he would prefer a thicker insulation to help reduce the distributed capacitance. If you remember from the design challenges, reducing the distributed capacitance was important to ensure the minimum SRF is exceeded. He chose TPA3 triple insulated wire (TIW) from Rubadue. It meets the insulation requirements and provides the thickness of insulation needed. For the wire size, ideally, he would have liked to use 38AWG wire to reduce skin effects at the 1MHz switching frequency but it is hard to strip TIW this small. He settled on 25AWG as a good compromise.

Since the application was unipolar, Robin had to make sure that the core would not continually build residual flux until saturation. Conveniently, the two halves of the core don't quite mate perfectly which automatically leaves a small air gap. Robin's calculations had already shown this was sufficient to prevent saturation of the core.

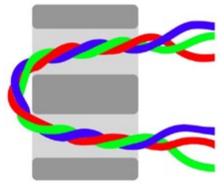


Figure 1: A Trifilar winding

The final detail was how to wind the transformer. Robin decided a trifilar winding would ensure optimal coupling and minimal leakage inductance. In a trifilar winding, the wires are wound onto the core in parallel (see figure 1). The coupling was further increased by twisting the windings together.

Magnetics design is an iterative process. Once you have a preliminary design you need to check it and adjust as necessary. Robin checked the operating flux density, the core losses and the wire losses due to DCR and ACR. He found that all were well within reasonable limits and decided to move forward with the next step of assembling a sample for testing.

Assembling the GT



Figure 2: Prototype with top of core removed to show the trifilar windings

The first step in assembly was to pick the base. The customer preferred SMD and Robin needed a base that would be easy for hand assembly. The base also must maintain the needed distance from the two primary pins to the 4 secondary pins to assure hi-pot. He found a suitable base from Lodestone that had 4 pins on each side.

To create the transformer, the twisted trifilar wires are bent into a U-shape and inserted through the windows of the core (see figure 2). The top of the core is then epoxied in place.

The wire is then untwisted at each end. The secondary windings are taken straight to the terminals, whilst the wires of the primary winding are bent back and routed down the outsides of the core.

Running the primary windings outside the core like this allows us to maintain the minimum creepage and clearance requirements while using the trifilar winding.

Finally, the ends of all the wires are cut to length, stripped and soldered to their respective terminals.

Testing the prototypes



Figure 3: The input and output match

Robin constructed 10 prototype GTs for testing in our lab. To test the transformers, their secondary circuits were loaded with a resistive load designed to simulate a dual MOSFET gate drive topology. The test rig was able to drive the transformer with a 12v, 30ns pulse, with the pulse repeating at up to 1MHz. The input and output waveforms were monitored to check for any distortion (figure 3).

Under load, the output showed no signs of distortion or core saturation when driven between 200kHz and 1MHz .

The self-resonant frequency was found to be greater than 3MHz (meaning that there is no risk of this causing waveform distortions). The primary inductance measured approximately 2μ H. The leakage inductance across the primary with the secondary windings shorted was measured at 79nH. Such a low value indicates good coupling between the windings.

The DCR measured 0.030Ω per winding. Finally, Robin checked that the GT passed dielectric withstand tests (Hipot). Throughout the testing, there was no measurable temperature rise and no sign of core saturation.

Conclusions



Designing gate-drive transformers takes skill, especially when they must meet such demanding specifications. Robin's final GT design met or exceeded all the customer's specifications and resulted in an SMD package that is small and easy to manufacture. ICE Components Inc. specializes in such custom component designs. If you would like to know more, please reach out to us.

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Why to Use Power Stage Designer[™] to Start a Power Supply Design

Many electrical engineers have been using Texas Instruments' free JAVA based Power Stage DesignerTM Tool since 2011 to aid them picking the right components for their switch-mode power-supplies. With the brand new version, Power Stage Designer 4.0 takes the next step in making power supply designers' life easier. The tool now not only calculates current and voltage information for a total of 20 different topologies, but also includes a very helpful toolbox, that enables the designer to start a power supply design very easily and also to finalize the power supply design more quickly.

By Markus Zehendner, Texas Instruments

The main purpose of Power Stage Designer is still to assist the user with calculating and visualizing general voltage and current information for the supported topologies in real-time. By clicking on the yellow highlighted components in the schematic, like in Figure 1, a window appears which displays the voltage and current waveforms for this component and some additional information like minimum and maximum voltage and current values (see Figure 2).

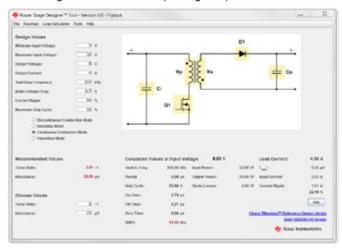


Figure 1: Topology window of Power Stage Designer

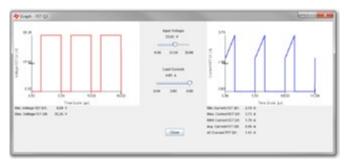


Figure 2: Graph window for the FET Q1 in a flyback converter displaying waveforms for voltage and current

The new version 4.0 adds three more topologies:

Series Capacitor Buck Converter

This topology represents a special two-phase buck converter for high output current point-of-load applications, which also need a very tiny form factor. It is possible to operate this kind of converter at very high switching frequencies with reasonable efficiency levels.[1]

Quasi-resonant Flyback Converter Low output power AC/DC converters are required to be more and more efficient. By having the flyback converter switching in a quasiresonant mode of operation, it is possible to reduce the switching losses significantly.

LLC-Half-Bridge Converter

Inductor-inductor-capacitor (LLC) resonant topologies become more and more popular with the demands for higher power and best possible efficiency levels. With the first harmonic approximation, which is implemented in Power Stage Designer, the user can quickly assess and design the power stage of a LLC-half-bridge converter without the need to run a complex simulation. However, the design needs to be evaluated and verified afterwards with simulation and a prototype.

After assessing the voltages and currents for the chosen topology, the user can now proceed with the power supply design without the need to use additional tools. The new toolbox of Power Stage Designer contains the following items to finalize the design of the power converter more quickly:

FET Losses Calculator

The FET Losses Calculator assists the design engineer with comparing and assessing the losses of different FETs. Calculations can be made for the main FET or the synchronous rectifier in a switchmode power-supply circuit. Conductive, switching and COSS losses will be summed up for the total losses of the main FET. For the synchronous rectifier the switching losses equal zero due to soft-switching, but additional body diode losses contribute to the total losses. Losses due to reverse recovery effects are neglected, but could become significant for very high switching frequencies. An estimation of the driver losses is also displayed.

Current Sharing between parallel capacitors

Often designers do not pay much attention to the current rating of input and output capacitors in their power supply design. When different kinds of capacitors, such as ceramic and electrolytic, are used in parallel, they experienced different amounts of RMS current. If this fact is overlooked, some capacitors can experience huge stress, significantly shortening their lifetime. This tool calculates the first harmonic approximation of the RMS current for three parallel capacitors based on the impedances at the switching frequency, and helps designers to choose capacitors with appropriate current rating.

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Figure 3: Power Stage Designer FET Losses Calculator window

 Bulk capacitor calculation for AC/DC power supplies AC/DC power supplies typically incorporate a bulk capacitor behind the input rectifier to provide the power stage with a quasi-constant input voltage. Power Stage Designer provides designers with a tool to quickly calculate the required bulk capacitance for their AC/ DC power supply design. The recommendation depends on the minimum acceptable bulk voltage, the maximum acceptable voltage ripple, the input power and the minimum line frequency.

RC snubber calculator for rectifiers

Meeting electromagnetic interference requirements can be challenging. When the PCB layout is already final, implementing an RC-snubber network parallel to the rectifier is an option to reduce ringing in the circuit. With the RC-snubber calculator for rectifiers, designers have an easy option to get starting values for the snubber network to minimize emissions. It only requires the user to measure the ringing frequency with and without a snubber capacitor. The frequency shift caused by the capacitance gives an indication about the parasitic circuit elements, which are used to calculate the starting values for the snubber resistor and capacitor.

RCD snubber calculator for Flyback converters

In flyback converters it can happen that a lot of stress is put on the FET. Especially when the PCB layout is not optimal, the board's parasitic effects in combination with the leakage inductance of the flyback transformer can cause a huge voltage spike every time the FET is turned off, thus increasing the voltage level the FET needs to be able to withstand. To avoid fatal damage to the FET caused by the leftover energy stored in the leakage inductance, it is common practice to clamp the primary winding with an RCD-snubber network to the input. Power Stage Designer offers the possibility to calculate starting values for the resistance and capacitance of the RCD-snubber network.

Output voltage resistor divider

It is usually an easy task to calculate the resistor divider for setting the output voltage of a power converter. However, it can still be time-consuming to rearrange the equation from the datasheet and







try different values. The output voltage resistor divider tool in Power Stage Designer lets the user select one of the feedback resistances. It then calculates the other one and the resulting output voltage. A worst case assessment is also displayed considering component and reference voltage tolerances. Effects caused by the feedback pin's biasing current are neglected.

Dynamic analog and digital output voltage scaling

Sometimes power supplies need to have an adjustable output voltage. This can be achieved by feeding a current signal into the feedback resistor divider or by paralleling different resistors with the low-side resistor of the feedback resistor divider. Power Stage Designer offers two tools, which calculate the output voltage resistor divider plus the additional components for analog and digital output voltage scaling.

Unit Converter

Commonly used power supply parameters can be easily converted with this small tool, e.g. imperial to metric units and vice versa.



Figure 4: Power Stage Designer Loop Calculator window

Loop Calculator

The Loop Calculator tool in Power Stage Designer offers users the possibility to visualize the frequency response of different power converter topologies and their compensation networks. The graphs of the bode plot are calculated with simplified transfer functions, but will still give a good indication how the frequency response will look like in reality. After having chosen a topology and the compensation network, the user needs to fill in some more general information about the power supply circuit and the power management controller. The effect of the chosen compensation network can be directly seen in the Bode plot of the tool. For some topologies Power Stage Designer is able to suggest values for the compensation network based on general rules of thumb.

By the Loop Calculator supported control schemes are:

- Voltage Mode Control (VMC) Buck
- · Current Mode Control (CMC) Buck
- · CMC Boost
- CMC Inverting Buck-Boost
- CMC Flyback
- CMC Forward

By the Loop Calculator supported compensation networks are:

- Type II
- Type II transconductance
- Isolated Type II with Zener clamp
- Isolated Type II without Zener clamp
- Type III

In summary Power Stage Designer is a tool that lets the user quickly assess important values and waveforms for the most commonly used power-supply topologies. The new toolbox provides additional design utilities to finalize the power-supply schematic. However, it is highly recommended to use simulation and bench testing of the prototype to verify and evaluate the power supply's proper functionality.

The equations behind the topology calculations in Power Stage Designer can be found in the Power Topologies Handbook, the assumptions and equations behind the toolbox in the Power Stage Designer User's Guide

www.ti.com/powerstagedesigner



Markus Zehendner is a Systems Applications Engineer in TI's EMEA Power Supply Design Services Group since 2014. He holds a Bachelor in Electrical Engineering and a Master in Electrical and Microsystems Engineering from the Technical University of Applied Sciences in Regensburg. His design activity includes reference designs of isolated and non-isolated DC/DC converters with focus on automotive applications."

To meet Markus and see the Power Stage Designer 4.0 in action register at: ti.com/psds2018 EMEA to join a Power Supply Design Seminar at a location near you

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March 6, 2018
March 13, 2018
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Accelerating Adoption of SiC Power

Practical, Ready-to-Use SiC Devices and Circuit Solutions for Better, More Efficient Power Systems

The market has heard for many years about wide bandgap product roadmaps and concepts, touting that many possibilities could be available. However, you can't design in a PowerPoint presentation or a preliminary datasheet, so this article will reinforce that Wolfspeed SiC power has moved way beyond any hype, talk, and fake news and has pioneered the widespread adoption of silicon carbide power devices in the customer base - today.

By Guy Moxey, Wolfspeed, A Cree Company

We showcase SiC devices that are widely used, and how they solve real issues: system-level examples adopted and working in the market -- today.

The practical, real, and ready-to-use circuit solutions discussed will span watts to hundreds of kW. Each solution will highlight our commercially available, fully qualified SiC devices, proven within the market to enable significant value to systems with regards to efficiency, power density, and cost.

SiC is not in the future tense, it's not just tomorrow's possibility – with Wolfspeed SiC is all around, proven and here today.

Example 1: 2kW Totem pole PFC

The advantage of SiC diodes in traditional server power PFC boost circuits are well known and understood with full market adoption for many years. Recently though, akin to the increased pressure to achieve new higher efficiency energy star and 80+ power supply regulations, power supply designers are faced with yet more challenges to increase system efficiency & increase power density whilst working with ever reducing BOM budgets.

The tried and tested single or interleaved PFC boost, a main stay of any standard PFC circuit, works hard to achieve the 80+ bronze, silver or gold server power supply standards but falls well shy of the more stringent efficiency regulations set to obtain the 80+ Titanium efficiency challenge, so more creative topologies and wide band gap device technologies are now more than simply "interesting studies".

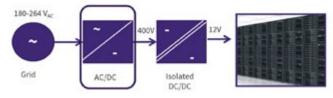


Figure 1: Functional block diagram of a typical Server power supply system

With regards to server power system architecture, Figure 1 shows a power block diagram of a typical single-phase server or Netcom switch mode power supply, breaking out by specific circuit function. The circuit function in debate during this article is the AC-DC boost, also known as the PFC. An incumbent design approach would contain the bridge rectifier, single switch or interleaved boost circuit followed by an isolated dc-dc stage.

Design Challenge

Higher efficiency power regulation in server systems is a very well know requirement as server farms are functioning 24/7 and are subject to energy regulations and legislation. The 80+ standard is a voluntary certification program intended to promote efficient energy use in computer power supply units. Despite being voluntary it is widely adopted and industry accepted. The 80+ standard comes now in 6 levels of efficiency achievement from 80+ as the basic to 80+ Titanium – being the most stringent. Titanium standard is the latest requirement that server power supply makers strive to reach. For Titanium, efficiency points are 94% at half load and 90% at full load for 115V input and 96% at half load and 91% at full load for 230V input - for a combined PFC plus dc-dc stage so just addressing the PFC alone then the efficiency targets or budget need to be 96.4% at half load and 93.8% at full load for 115V input and 98.5% at half load and 94.8% at full load for 230V input

Achieving this PFC efficiency budget with conventional silicon boost topologies is beyond reach with most silicon MOSFET devices and, although achievable, with enhanced performance devices the cost budget increases to such a level that it becomes impractical to implement.

So, the design challenge is how to achieve the required Titanium efficiency budget whilst increasing power density and maintain a cost neutral power system to typical lower performance silicon approaches.

Design Specification

System requirements for single phase PFC boost circuits are reasonably generic with regards to voltages, currents, harmonics and EMI considerations, so Figure 2 shows a typical PFC parameter specification.

2kW was chosen as typically the higher power systems require the higher efficiency standards. In addition, as increasing circuit power density is also a strong consideration, a surface mount power device adoption was taken as part of the design challenge. Bridgeless power factor correction topologies are not necessarily new concepts, whether single or 3-phase in approach, and the advantages of higher efficiency, higher power density and lower component count are compelling; however often the inadequate performance of the silicon incumbent technology for power switch combined with unusual control implementation have limited any practical adoption.

Now, with a business as usual approach a designer would construct a 4-switch totem pole circuit based off the simulation results with the best performing SiC MOSFET's available, however with the price neutral budget criteria also in place it was evaluated to approach the totem pole with two SiC MOSFETs in the high frequency leg and two low Vf silicon diodes in the low frequency leg to significantly reduce the BOM cost. This approach significantly reduces the semiconductor content and cost plus also significantly simplifies the circuit control and associated IC costs. The C3M0065090J was chosen specifically for its surface mount capability – hence reducing overall board size thus increasing circuit power density plus the fact that the device

Parameter	Specification	
Pout	2 kW	
V _{in}	90-264 V	
Switching Frequency	85 KHz	
THD	< 5 %	
MOSFET Package	Surface Mount	
Vour	400 V _{DC}	

offers the user a separate kelvin source connection which when utilized correctly significantly reduces device switching loss verses conventional D2PAK or 3 lead TO type devices.

Two-Switch Totem Pole Results

Operating at 85kHz, the two-switch totem pole PFC circuit designed to the specification shown in figure 2 achieved exemplary results. At 230V input the to-

Figure 2: PFC design specification

tem pole 50% load efficiency was 98.61% and the full load efficiency was 98.54%, both of which were above the target efficiency budgets of 98.5% and 95% respectively. This efficiency includes the losses generated from the auxiliary power supply and fan. Figure 3 shows the hardware board

Board size is 213mm x 112mm showcasing the totem pole power density. Single fan and surface mount MOSFET's and Diodes. This board is equal to or smaller than existing off the shelf silicon based 80+ gold solutions but achieves titanium level efficiency. The twoswitch circuit is practical to implement and therefore commercialize. The entire design is based off power devices that are fully released, fully qualified and manufactured in substantial volumes.



Figure 3: Hardware board and entire efficiency plot against output power

Example 2: 20kW Bi-Directional 3 phase AC-DC converter

Grid-connected three-phase AC/DC (or DC/AC) power conversion is required in a wide range of industrial applications – from power electronic interfaces of renewable energy systems (solar, wind, and batteries), industrial and mass transport vehicle charging, to regenerative motor drives (elevators, mills, etc.). A practical example of such a 3-phase grid-tied AC-DC system would be fast charging stations for electric vehicles. Figure 1 shows a functional block diagram of a 3-phase fast off-board charger for battery electric vehicles (BEVs). With Bidirectional functionality of the converter, it is possible to deliver power from vehicle to grid (V2G).

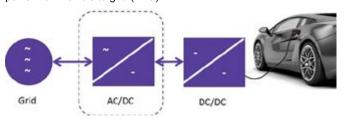


Figure 4: Functional block diagram of 3-phase AC/DC system.

Design Challenge

For PFC bidirectional applications, two-level topologies using 1200V IGBTs or three-level topologies using SJ FETs are typically used. Two-level topologies with 1200V IGBTs offer simplicity, low semiconductor cost, and high-power capability (>20kW) but switching frequency limited to <20kHz – yielding systems with lower power density, lower efficiency, and expensive inductors. Multi-level IGBT topologies such as the neutral point clamped (NPC) rectifier offer higher power density and efficiency (lower switching losses) at the expense of higher circuit complexity. For unidirectional power flow complex approaches are also seen with 650V silicon MOSFET's. The Vienna or

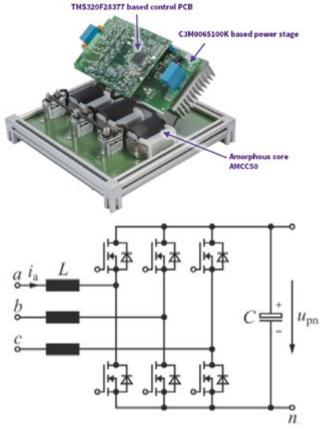


Figure 5: 20kW Active Front End Circuit and Hardware

modified Vienna circuit can achieve reasonable unidirectional power efficiency but lacks acceptable power density, is complex in design and component count and lacks any bidirectional capability.

An alternative approach designers today, utilizing SiC MOSFETs, are drastically reducing switching losses and significantly extending the usable switching frequency range of the two-level six-switch converter, while maintaining higher full-load and part-load efficiency. With SiC MOSFETs, power density of the system is significantly increased by shrinking the size of magnetic components and reducing the size of the heatsink. Additionally, when utilizing SiC MOSFETs, the device's body diode can be used as the anti-parallel diode, reducing circuit complexity and cost.

Figure 5 shows the two-level SiC MOSFET converter power stage. This example showcases a cost-effective, highly efficient design alternative for an industrial PFC application with the entire design based on SiC power MOSFET devices that are fully-qualified, and in volume production. Challenging the traditional 1200V Si-IGBT twolevel system, this approach meets the same system-level specifications but offers higher efficiency, significant increase in power density and reduction in system cost. For this power level, the $1000V/65m\Omega$ SiC MOSFET was selected. This part delivers extremely low switching losses thanks to a 4-lead TO-247 package with dedicated Kelvin source connection. In addition, the optimized 1000V blocking and rugged body diode capability allows for minimum die cost while supporting up to 800VDC link operation. This example again shows a real solution using Wolfspeed's commercially available SiC MOSFETs (C3M0065100K) which meets new market requirements for bi-directional functionality, in a simple two-level topology - switching at 48Khz. The design at full power shows measured results ~1% efficiency improvement over Si IGBT systems.

Example 3: 250kW 3 phase inverter

It is without question that electric vehicles provide one of the largest opportunities for power semiconductors for the next decade and beyond and whilst silicon has proved itself to be adequate in the early Hybrids and BEV's, the power conversion circuits that charge the vehicles battery and drive the vehicles motor need significant improvements in relation to efficiency and power density to meet the market demands of increasing mileage range, lighter vehicles and cost effective end products.

The automotive industry itself has evaluated and proven the value of incorporating SiC into On Board Chargers (OBC) and drivetrain inverters. It is an incredible result to see that replacing a 250kW EV drive inverter from silicon IGBT to Wolfspeed SiC MOSFET's reduces the inverter losses by ~80% across the combined driving cycle! Details

% inverter loss comparison



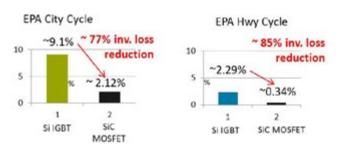


Figure 6: Inverter loss reduction by implementing Wolfspeed 900V 10mO SiC MOSFETs shown in figure 6. For the OBC, using SiC can increase system level efficiency by >1.5% whilst increasing power density by over 30% when compared to traditional silicon approaches.

To shorted customers design cycles and quantify the SiC value proposition Wolfspeed developed a high performance 250kW three-phase evaluation kit targeted at the EV drive train. The kit is designed to enable customers to prove the real-world benefits of SiC devices, in an optimized inverter stack-up, in their own laboratory environment with a minimal amount of resource investment in proof-of-concept system design. Wolfspeed's 250 kW Evaluation Units weigh in at just under 16 kg with a volume of 26.3 L (44 mm long, 39.8 mm wide, and 15 cm tall) as shown in Figure 7.

Utilizing the CAS module optimized packaging Wolfspeed has focused on developing high gravimetric- and volumetric- density solutions, which also maintain incredibly low parasitic inductance - boasting just 7.5 nH of inductance, while weighing in at only 180 grams and occupying nearly the same space as your average smart phone. The inverter design can deliver up to 250 kW continuous power at 850-900 VDC bus at 20 kHz PWM switching – with ~ 80% reduction in inverter loss (over the combined operation cycle) than an equivalent Silicon IGBT inverter.



Figure 7: The Wolfspeed 250kW EV drive train inverter

Conclusions

The tipping point for SiC availability and adoption has occurred and in many markets today the customer base is harvesting the advantages SiC gives. Wolfspeed has been pioneering the SiC revolution and with the largest most proven product portfolio in the industry – by far, the design community has real SiC solution – today that increase system level efficiency, reduce overall system board size, increasing system power density and last, but by no means least, lower power BOM cost verses conventional inefficient silicon based topology approaches.

Say adieu to preliminary datasheets, power point roadmaps, and fake news as through leveraging its 30 years of experience in SiC design, optimization and high volume manufacturing Wolfspeed has developed high performance reference designs, built around their SiCoptimized power discrete and module product line, which are targeted at ensuring that end-system designers invest minimal effort in learning the best-practices associated with achieving optimized performance for SiC-based system design.

www.wolfspeed.com

Taking Advantage of SiC's High Switching Speeds

Optimizations in measurement, layout, and design is requested

For several years, silicon carbide (SiC) has created a lot of buzz in the power electronics community. At the risk of oversimplifying, the hype comes down to one simple advantage that SiC offers over incumbent silicon power devices: the simultaneous ability to switch at high speeds and block thousands of volts. The result is smaller, lighter systems that are more efficient and often less expensive.

> *By Kevin M. Speer, Ph.D. Littelfuse Inc. and Xuning Zhang, Ph.D. Monolith Semiconductor Inc.*

Introduction

For several years, silicon carbide (SiC) has created a lot of buzz in the power electronics community. At the risk of oversimplifying, the hype comes down to one simple advantage that SiC offers over incumbent silicon power devices: the simultaneous ability to switch at high speeds and block thousands of volts. The result is smaller, lighter systems that are more efficient and often less expensive.

However, nothing comes for free. Higher switching speeds present new problems that must not be underestimated, including: difficulty in accurate test and measurement; circuit parasitics that create excessive voltage spikes, EMI non-compliance, and switching losses; and finally, highly sensitive design and integration schemes of the driving and power stages. In this work, we describe some common challenges and illustrate a few best practices that, when properly incorporated, can help users clear these barriers and unleash the myriad benefits of SiC's high switching speeds.

1. Accurate Test & Measurement

Challenges

To obtain device performance and establish expectations for how the device should behave in an end application, the importance of proper measurement cannot be overstated. When combined with circuit and

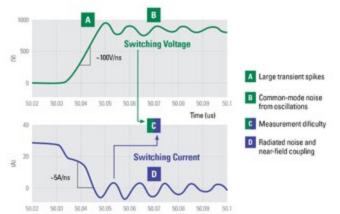


Fig. 1. Turn-off waveforms illustrating four typical problems associated with high-speed switching and their measurement.

package parasitics, SiC's ability to switch at very high rates of voltage change (dv/dt) and current change (di/dt) can give rise to four common problems that are illustrated in Fig. 1. High dv/dt can produce large transient voltage spikes, as well as common-mode noise seen as damped oscillations. High di/dt generates noise that can couple with current fields in the vicinity. Further, each of these effects can be difficult to measure and diagnose. For this reason, precision measurement tools and accurate test methodologies must be used to uncover problems before they manifest during the prototype stage, product qualification, or worst of all, in the field!

Best Practices

Measurement of power devices switching high levels of power at high speeds requires exceptional bandwidth, dynamic range, and minimum stray inductance and capacitance the probes themselves. Tables 1 and 2 show the advantages and disadvantages of various voltage and current measurement methods.

	Method	Pros	Cons
3	Differential probes	Galvanic isolation	Limited bandwidth
v v	Voltage divider	High bandwidth (with good design)	Requires high resistive load
0	Passive probes	High bandwidth	Non-galvanic isolation; requires a common ground

Table 1. Voltage measurement methods.

For the measurement of voltage, differential probes are commonly used and offer built-in galvanic isolation, but they suffer from limited bandwidth. On the other hand, passive probes and a conventional voltage divider circuit offer suitable bandwidth, but the passive probes require a common measurement reference and lack galvanic isolation, and a voltage divider requires substantial resistor size. Our recommendation is a passive voltage probe because its bandwidth allows the capture of high dv/dt transients.

	Method		Cons
65	Current probe	Galvanic isolation	Limited bandwidth
	Current transformer	High bandwidth; galvanic isolation	Saturation for large current; not suitable for DC
	Rogowski coil	Galvanic isolation; flexible tip	Limited bandwidth; not suitable for DC
	Coaxial shunt	High bandwidth; high accuracy	Non-galvanic isolation

Table 2. Current measurement methods.

There are four commonly used methods for measuring current, none of which is without a drawback. A standard current probe and Rogowski coil may not have adequate bandwidth for resolving current ringing effects, and the Rogowski coil and current transformer are incapable of capturing dc information. For designs intended only for characterization, the coaxial shunt is recommended due to its large bandwidth and high accuracy, which inherently resolves issues with non-galvanic isolation. Once problems are resolved through design optimization in the prototype, current shunts may be eliminated from the final system.

2. Power Loop Layout

Challenges

We can treat the power electronics system as consisting of two main circuits: the driver loop (also called the gate-source loop) and the power loop. The power loop contains the load and power semiconductor components. Because this loop switches hundreds of volts and many amperes, the speeds at which voltage and current change (dv/ dt and di/dt, respectively) combine with circuit parasitics to produce problems that must be mitigated:

- Voltage spikes at switch turn-off events. Due to the multiplication
 of di/dt and parasitic circuit inductance, these spikes can exceed
 the maximum voltage rating of the device, leading to catastrophic
 failure. Due to these limitations, the benefits of SiC may be undermined, as the user must either limit how quickly the devices may be
 switched, select higher-voltage (i.e., more expensive) components,
 or resort to multi-level topologies that increase complexity and
 component count.
- Electromagnetic interference. Due to ringing in the current waveforms during switching events, induced noise can then couple with other circuit elements. that can lead to inadvertent turn-on and shoot-through, malfunction of nearby circuits, or non-compliance with mandated electromagnetic compatibility regulations. this

ultimately necessitates bulkier, heavier – and more costly! – filter components.

Using a SPICE model for the Littelfuse LSIC1MO120E0080 (1200 V, 80 mOhm SiC MOSFET), the effects of parasitic inductance in a standard double-pulse test circuit were simulated with V_{DC} = 600 V, I_D = 20 A, R_g = 5 Ω , driving voltage of +20 V / -5 V, and a di/dt of 2.5 A/ns (see Fig. 2). It is seen that the parasitic inductance of the power loop has the most dramatic influence on the voltage spike at turn-off, shooting to more than 120% of the DC bus value, even for these modest values of di/dt and L_{pwr} . Figure 3 further illustrates the effect of power loop inductance on voltage overshoot. An increase of only 8 nH – as much as just the source pin of a TO-247 – can lead to a spike across the device nearly 20 percent higher than the bus.

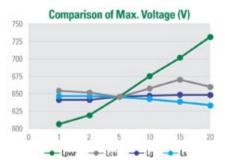


Fig. 2. Simulation of maximum voltage seen from drain to source of the MOSFET in the double-pulse test circuit as a function of parasitic inductance. Note the effect of power loop inductance, Lpwr, giving a spike of more than 100 V above 15 nH at only 2.5 A/ns.

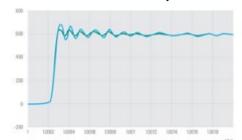


Fig. 3. Simulated VDS waveform at turn-off with a parasitic power loop inductance, L_{pwr} , of 2 nH (green) and 10 nH (blue). A much larger voltage spike is observed, even at modest values of di/dt (2.5 A/ns) and L_{pwr} .

Best Practices

The most general guideline for optimizing power loop layout is to emphasize board compactness and simplicity, with a focus on minimizing the overall loop area. This can dramatically reduce stray inductance, allowing users to utilize the high switching speed made possible by SiC power devices. the next best scenario in real application is a loop with an outgoing path that overlaps with the return path – a practice known as "lamination." As seen in the example board layout illustrated in Fig. 4, the dc+ and dc- paths are laminated. Finally, in portions of the loop where lamination is not possible (such as the pins of a through-hole component, for example), power paths should be wide, numerous, and/or cover as little of the two-dimensional space of the board as possible.

Another good practice is the use of decoupling capacitors. In the frequency domain, the process of switching at high speeds not only creates higher-order harmonics of the switching frequency, $f_{\rm s}$, but also peaks related to the transient speeds that extend well into the MHz range. Typically, the dc link capacitor acts as a notch filter, eliminating oscillations corresponding to $f_{\rm s}$ and its harmonics of appreciable

amplitude; however, it does not suppress the megahertz-scale transient-related frequencies, f_{trans} , which can be highly problematic for coupling into neighboring traces and circuits. To suppress peaks associated with f_{trans} , one can use relatively high-farad film capacitors connected across the dc link and placed as close as possible to the power transistors' drain and source terminals to minimize the associated loop inductance.

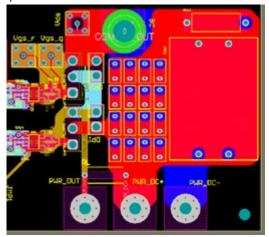


Fig. 4. An example power board layout, illustrating compactness and optimal lamination of positive (red layer) and negative (blue layer) dc power paths to reduce stray power loop inductance. Sixteen decoupling capacitors are also shown in the center.

3. Gate Driver Design and Integration

Challenges

The gate drive has two prevailing purposes: to turn on/off the power switches in a stable, well-controlled manner and to incorporate intelligent power system protection. Without proper design layout and integration of the gate drive with the power stage, these objectives can be difficult to achieve. Two of the most common challenges include:

- Gate voltage overshoot and ringing. As indicated in Fig. 5, in the presence of high gate and source loop inductance, L_G and L_S, high values of di/dt can lead to overshoots in the voltage seen at the device gate. Oscillations in the gate voltage waveform can indicate inadvertent turn-on and, thus, potentially catastrophic shoot-through events (not to mention potential device reliability/lifetime concerns).
- Unnecessary increase of switching losses. Even a modest level of common-source inductance, L_{CSI}, will resist fast changes in current and increase switching losses, as shown in Fig. 6.

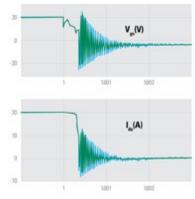


Figure 5: An example power board layout, illustrating compactness and optimal lamination of positive (blue layer) and negative (red layer) dc power paths to reduce stray power loop inductance. Sixteen decoupling capacitors are also shown in the center.

Best Practices

First, to reduce the effect of inductive coupling between the gate and power loops, one should place these two loops in orthogonal planes where possible. Second, as with optimization of the power loop, the total gate loop area should be minimized through a combination of lamination and shortening path lengths. Finally, to reduce common-source inductance, the gate loop and power loop should be decoupled; this is most easily achieved using packages with a dedicated Kelvin source, such as the four-lead TO-247 or the seven-lead TO-263.

4. Summary

This article highlights some of the prevailing challenges associated with the use of SiC and describes several best practices that can help design engineers justify its use in their systems. However, the benefits of this technology can be difficult to realize due to the problems associ-



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ated with the high switching speeds that high-voltage, majority carrier power devices make possible. Design engineers need measurement instrumentation optimized for observing the high-speed dynamics that slower silicon IGBTs do not exhibit. Once this capability is in place, the layout and integration of the gate drive and power stage circuits must also be optimized to exploit the high switching speed that SiC power devices allow.

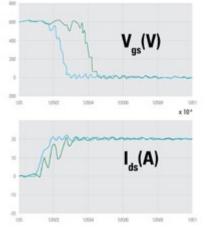


Fig. 6. Simulated drain voltage (top) and drain current (bottom) waveforms with LCSI = 5 nH (blue) and LG = 20 nH (green). As LCSI increases, there is a delay in the fall of VDS and a simultaneous decrease in di/dt; this results in an increase of switching losses from 266 μ J to 545 μ J.

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Wide Band Gap is no Mystery

In recent years GaN power semiconductors and GaN power electronics are mentioned in the news with revolutionary comments:

"High switching speed, small size, competitive cost and high reliability give the GaN transistor the positive trajectory to broadly displace the silicon MOSFET in power conversion applications."^[1]

"GaN will take over the power transistor business." ^[2] *"GaN delivers nearly double power density at total cost on par with silicon."* ^[3]

By Dr.-Ing. Marvin Tannhäuser, Siemens AG "Software Defined Inverter - Digital Power Electronics Group"

If one considers all these promising properties of GaN power semiconductors, we should think about the question: "Why there are not more products with GaN semiconductors on the market?" Of course there are always innovation barriers which make it complicated to use novel materials and technologies like GaN in real products. And the discussions about device reliability and higher cost for new technologies will come up in every case. If we categorize the young GaN power semiconductor technology as a disruptive technology we need to solve even greater challenges which are well known as the Innovator's Dilemma.[4]

But let's assume that these obstacles can be overcome. Then we need to answer the following question: "What are the major challenges using GaN power semiconductors?", but in this case from the power electronics system and application view.

Power Electronics Systems

In power electronics we have to master a wide range of different engineering disciplines like the power semiconductor itself but also the auxiliary electronic design, the control of the power circuit, the EMC management, the power inductor design and the whole mechanical and thermal design.



Figure 1: Engineering disciplines for the design of Power Electronics Systems

If we bring GaN power semiconductor technology in the power electronics system design, new challenges needs to be solved if we want to use the ultra fast switching speed of over 100V/ns. Figure 1 gives an overview of the different major engineering disciplines for a power electronics system design and some of the new challenges which come up when using fast switching GaN power semiconductors.

Due to the absence of reverse recovery charge and low parasitic capacitances, GaN devices switch faster and more efficient than clas-

sical power MOSFETs. Therefore the switching frequency of power converters can be increased which reduces the size of the passive components such as the power inductor. From a control viewpoint, reduced inductance lowers the damping of the power circuit. This needs to be handled by the control algorithm. The classical PI-control approach often reaches its limits, therefore requiring new concepts to be developed.

Obviously for a high transient in the switching current (> 10 A/ns) a power semiconductor package with very low parasitic inductance in the power-circuit is needed. Classical packages or modules with a parasitic inductance in a range of 10 to 20 nH will cause increased ringing and reduced switching efficiency. The high switching speed causes higher EMC emission and therefore all the electronic circuits in the system need higher dV/dt and EMC immunity. To handle the high dV/dt, parasitic capacitances should be taken into account from the beginning of the system design. It is also important to consider the thermal design and the cooling concept for SMD packages.

Thermal management of a GaN SMD power semiconductor

SMD (surface mount) packages enable the design of power semiconductor circuits with low parasitic inductance as well as gate drive circuits with fast and precise control of the gate voltage. Furthermore the discrete SMD package allows easy and automated manufacturing of multilevel power converter PCBs. On the other hand, the SMD device has a lower thermal performance in comparison to a TO-package or a power module. Since the PCB is a major part in the thermal path for a SMD power semiconductor, we have to take a closer look at the PCB design for both thermal dissipation and electrical interconnections.

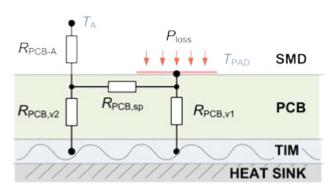


Figure 2: Thermal paths for a PCB and the steady state equivalent circuit

Figure 2 shows a steady state thermal equivalent circuit of a printed circuit board (PCB). Two different thermal path of the PCB are considered: first the local thermal path under the SMD device vertical trough the PCB $R_{PCB,v1},$ second the spreading resistance into the PCB $\mathsf{R}_{\mathsf{PCB},\mathsf{sp}}$ in combination with both a distributed vertical resistance $\mathsf{R}_{\mathsf{PCB},\mathsf{v2}}$, and the convection resistance to ambient $\mathsf{R}_{\mathsf{PCB-A}}$. All these thermal resistances can be influenced by the layout geometry as well as by different design parameters like PCB thickness, amount of copper on the surface, copper thickness of the layers, thermal VIA density and substrate material. The thermal spreading within the PCB is as important as the use of local thermal VIAs under the power semiconductor device. Thermal spreading decreases the negative influence of the thermal interface material (TIM) and the board thickness. The copper thickness of the layers is a major design parameter to improve the thermal spreading within the PCB. To analyze this influence, a simple 50x50mm² PCB with 4 copper layers has been investigated. Even with standard copper layer thickness of 70 µm or 105 µm, good thermal performance of 4 to 5 K/W for thermal resistance of the PCB could be reached. Furthermore an optimized PCB design allows less local VIAs, which allows a degree of freedom for the electrical design of the power cell. This helps to design a very efficient power cell with a small loop inductance for high transients in the switching current.

The influence and the relevance of an optimized thermal PCB design are also dependent on whether the chosen cooling method is active or passive. For applications with low power losses per SMD device (approx. 4 W for the mentioned above device and setup), passive cooling without heat sink and fan is possible. This allows for easy and cheap manufacturing of the power converter. Furthermore, passive cooling is always an advantage for applications where a closed enclosure and long lifetime with high reliability are needed. To demonstrate this cheap and easy cooling method, a GaN converter prototype was built, which shows the feasibility of such a thermal concept. The PCB was made of standard FR4 material with 4 layers of standard 70 µm copper. The target application for this case was a three phase bidirectional DC/AC converter with a power range of up to 5 kW. A GaN power semiconductor from Transphorm local thermal path under the SMD device vertical with 110 m Ω in a PQFN package was used. The nominal DC voltage of the design is 700 V and the line-to-line AC voltage is 400 V. The prototype was tested with a switching frequency of up to 175 kHz.



Figure 3: PCB and thermal measurement of the PCB based multilevel converter at 1 kW per Phase

The pictures in Figure 3 show the design of a halfbridge of the three phase PCB based multilevel converter. The thermal image shows the result of a measurement at 1 kW per phase, with 175 kHz switching frequency and an ambient temperature of 25 °C. The passive cooling of the SMD power semiconductor was realized by the thermal design of the PCB. Therefore no additional heat sink or fan was used. The Transistor T1 reaches a maximum case temperature of 57 °C, which is a good value if we consider the system power and the chosen thermal concept. This value also confirm the high converter efficiency of 98,5 %, which was measured with a Yokogawa WT1800 power analyzer. For a hard switching topology, this is a good example, of the performance of the GaN technology. The board has also an LC-filter included and therefore it could generate a sinusoidal output voltage, which is shown in Figure 4.

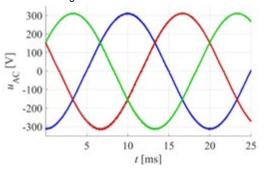


Figure 4: Measured sinusoidal AC voltages at the output of a three phase PCB based multilevel converter with a switching frequency of 150 kHz

Outlook

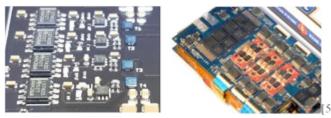


Figure 5: Examples of PCB based multilevel power converter

It is well known, that GaN technology enables power semiconductors with high switching speed. GaN power electronics can work at higher switching frequencies and GaN power semiconductors in SMD packages enable PCB based multilevel converter systems with higher efficiency than comparable existing solutions. This allows the design of power converters with smaller passive components, smaller heat sinks and higher energy density. All these advantages will lead to power electronics with a much higher level of integration (Integrated Power Electronics). It will enable PCB based power electronics designed for an automated high volume manufacturing. On the other Hand, new challenges of GaN power electronics need to be handled like: the thermal management of GaN power semiconductors; power inductors for higher switching frequencies; auxiliary electronics with higher EMC-immunity; control concepts for power circuits with a very low system damping; and concepts to handle or even to avoid the higher EMC emissions.

The increasing demand of power electronics in the growing markets for renewable energy, electro-mobility or factory automation could be addressed in the future with smaller, lighter and cheaper power converter systems, which are ready for an automated and high volume manufacturing.

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SiC and GaN Systems Design Engineers no Longer "flying blind"

By Andrea Vinci and Tom Neville, Tektronix

The advent of SiC and GaN MOSFET technologies is driving as a disruptive revolution in the power electronics industry. These new materials permits efficiency percentages, for the entire conversion system, that were simply unimaginable a few years ago.

There is no such thing in the real world as an ideal switching characteristic, but several classes of wideband gap devices based on the new materials are emerging with extremely low switching losses. The combination of low switching losses and the ability to deal with very high dv/dt slew rates and support for very fast switching frequencies, make the new technologies the dream – and the nightmare – of the DC/DC converter design engineer all at the same time.

Let's consider a design engineer working on a power conversion application, such as an inverter or a motor drive controller, or one who is taking on the challenge of designing a power factor correction (PFC) circuit that pushes power supply efficiency above the 99 percent limit. What challenges do they face?

Using a low loss transistor is just the beginning of the steep mountain they must climb. A fully isolated gate driver circuit must be able to properly drive and control the power stage which in turns leads to several issues that must be solved, ranging from isolation to the need for circuit protection techniques to avoid the potential catastrophe of the so-called "feed-through" problem.

When designing high frequency converters, a large portion of design time is spent on simulation and verification to confirm that any and all possible causes of failure have been considered and addressed.

A talented PCB designer can perform magic with the layout, but the parasitics are still there, lurking around corner. This alone can keep design teams busy and as they accumulate experience with new device packages, new system layouts and new topologies. Indeed, the move to new SiC and GaN devices involves a range of complications. Common threads

This scenario is quite common across power systems design projects. It's the fil rouge or common thread that associates the PFC/power supply market with the PV inverters market and the xEV automotive market with consumer wireless charging applications – the desire to get the most out of SiC and GaN technologies.

Certainly the requirements between these various application systems differ considerably. What a designer requires from a semiconductor device in terms of electric field magnitude, on-resistance or blocking voltage can force the move into a very specific and narrow swim lane. But there are common issues facing both a 20kW electric car battery charger designer using SiC at 250kHz and resonant topology designers of GaN-based wireless power designs working at 6.78MHz.

In both cases, the designers have a need to clearly characterize static and switching losses with high accuracy. They all need to clearly deal

with and properly manage heat dissipation and to quantify the cooling medium. They both likely have new generation transformers, inductors and capacitors catalogs on their desk that they may have never used before. They also are worried that the soldered in probe access wire could act as a mini antenna when EMC characteristics must be verified.

They also are starting to recognize that the instrumentation toolkit they used in the past may not be sufficient for what they need to do now.

Devices need to be tested for breakdown up to thousands of volts and at the same time vetted for leakage currents that can be as low as femto-amps. Are the power sources, the multimeters and the oscilloscopes still up to the task?

With all these MOSFET Vgs and Vds and currents that have to be simultaneously measured, with precise skew characterization, can they still use their four channel scopes with some external signal trick to achieve synchronization? How much time should they invest in post processing the waveforms and putting it all together offline to form decisions over the circuit behavior? Do they have enough sensitivity for the gate threshold voltage measurement on their old scope, and the oscillations they keep tracking on the scope screen, are they real or coming from the probe leads?

Invariably, SiC and GaN, designers almost universally tick off several pain points and measurement challenges including:

- High dv/dt, high di/dt and high switching frequencies that create issues related to EMI
- Measuring low voltages in the presence of high common mode current
- High voltage overshoot
- Cross-talk and other headaches in PCB layout designDetermining what percentage of the errors are coming from the measurement system

The Vgs measurement problem

Another area where designers struggle involves measuring Vgs in topologies called phase-leg or half-bridge configurations, as shown in Figure 1.

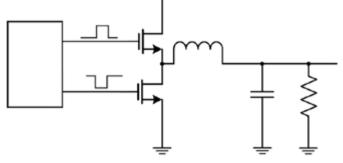


Figure 1: Typical phase-leg or half-bridge configuration

In this configuration, when one SiC MOSFET turns on, the very high dv/dt induces spurious voltage on the gate to source voltage (Vgs) of the complementary MOSFET as shown in Figure 2.

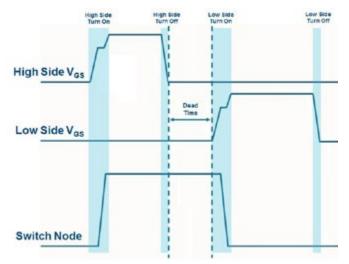
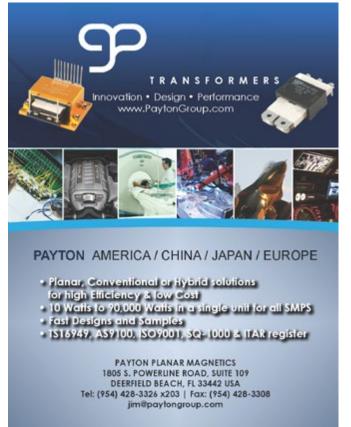


Figure 2: This illustrates the challenge involved with Vgs measurements.

Of course, you do not want to lower dv/dt, since this high slew rate is what allows these devices to achieve such minimal switching losses. Therefore, the problem must be solved differently, for example, by working on the gate driver side to actively control gate resistance of the two stages in the switching process.

In addition, an extremely talented PCB designer must make sure that the bus and connecting lanes have minimal inductive effect so as to not contribute too much to voltage and overshoot ringing caused by inductive loops. All these elements must be validated with real circuit simultaneous measurements of high side and low side stages Vgs to characterize pulse width modulation (PWM) delay time and minimize dead time to increase performances. You then need to measure the currents, and the two Vds for complete loss characterization.

Four channels scopes are insufficient for this job, and typical 8-bit ADCs do not provide sufficient vertical resolution. Also, the common probes in most lab drawers have now proven to be inadequate, even



good differential probes that have traditionally proved to be sufficient for making floating measurements on the high side stage.

Traditional differential probes are based on differential amplifiers which are connected to earth ground. This ground connection limits the common mode voltage range, causes common mode voltage frequency derating, creates ground loops, and limits the common mode rejection.

Fortunately, just as there's a disruptive revolution with the emergence of wideband gap devices there's also a disruptive revolution going on among power efficiency measurement solutions.

New measurements solutions

A typical measurement system in this space is based on oscilloscopes and differential probes that provide the connection between the device under test (DUT) and the oscilloscope. Scope selection is criti-



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cal in terms of appropriate bandwidth, noise floor, vertical resolution, number of channels and application software versatility. Probe selection is critical because probe performance can be the limiting factor in the measurement system.

When a differential measurement is needed, conventional differential probes as mentioned earlier often fail to provide a good representation of the actual signal due to limitations in their common mode rejection ratio, derating over frequency, frequency response, and the parasitics introduced by probe's input leads. These limitations become more pronounced when testing SiC and GaN power devices with very fast switching rates and high nominal common mode voltage.



Figure 3: The IsoVu measurement system

Since the problem of capturing these signals stems from the need for earth ground, it follows that a workable solution would be probe technology that does not depend on earth ground, and therefore would be more or less immune to the effects of high-common mode voltage. Such a system now exists in the form of the patented IsoVu measurement system from Tektronix, which operates entirely through fiber optics.

The IsoVu measurement system is a leap forward for Vgs measurements and is the only solution with the required combination of high bandwidth, high common mode voltage, and high common mode rejection to enable the differential measurements required for new applications involving wide bandgap MOSFETs. IsoVu offers complete galvanic isolation from the DUT and uses an electro-optic sensor to convert the input signal to optical modulation, which electrically isolates the DUT from the oscilloscope.

The sensor head, which connects to the test point, has complete electrical isolation and is powered over one of the optical fibers. The probe tips are designed to be shielded all the way to the tip and minimize parasitics. The probe is not only offers significant advantages for power conversion testing, but is also well suited for stringent EMI and ESD test requirements. Unlike electrical probes that should be kept as short as possible, cable length is not an issue for measurement systems based on fiber optics. Remote measurement capability can be very useful when the DUT and the oscilloscope must be (or should be) kept some distance apart from each other.



Figure 4: Tektronix scope

The IsoVu system works with most Tektronix scopes, but the best combination comes when it is used in combination with the 12-bit vertical resolution of the new 5 Series MSO oscilloscopes that offer up to 8 analog channels in a single unit and advanced power application software. This combination enables designers to finally take advantage of everything the wide bandgap materials have to offer for DC to DC power converters, but also represents a significant advance for 3-phase power electronics, power supply design, automotive electronics and much more.

About the Authors

Andrea Vinci is a Business Development Manager at Tektronix – Keithley in EMEA. He has an M.Sc.from Università di Padova – Italy.in Electronic Engineering.

Tom Neville is a Product Planner and Product Marketing Manager in Tektronix Time Domain Business Unit. He has an MSEE from Portland State University and a BS degree from the United States Military Academy. Andrea and Tom focus on measurement solutions for power applications.

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A team around Dr. Farid Medjdoub from IEMN research institute in France has made devices and conducted measurements on two different GaN-on-Si epiwafer products supplied by ALLOS Semiconductors of Germany. One is a prototype of ALLOS' upcoming product specifically designed for 1200 V device applications. With this epiwafer IEMN achieved over 1400 V for vertical and 1600 V for lateral (grounded) breakdown. The other epiwafer is ALLOS' established product for 600 V applications which equally showed very high breakdown voltages of 1200 V and more for both lateral and vertical measurements. The new epiwafer product for 1200 V device applications is from an ongoing internal development program at ALLOS. Its strong performance results from an innovative structure combining ALLOS' unique strain-engineering and high crystal quality approach with additional measures to suppress leakage and enhance breakdown voltage further. This was achieved without compromising on other essential parameters like crystal quality or wafer bow and without introducing carbon-doping. Epi growth was conducted on a standard Aixtron G5 MOCVD reactor. Already at the International Forum on Wide Bandgap Semiconductors (IFWS) in Beijing in November 2017 AL-LOS showed device results from an industry partner using ALLOS' 600 V epiwafer.

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Control Vout of Any DC/DC Regulator with a Serial PMBus Interface

Analog Devices announces the Power by Linear™ LTC7106, a PMBus I2C controlled precision bidirectional current DAC designed to



adjust the output voltage of virtually any DC/DC regulator. Through its PMBus compatible interface, the LTC7106 receives a 7-bit serial code and converts it to a bidirectional (source, sink) output current. When the current is fed into the feedback network of a regulator, its output voltage can be programmed dynamically for load power/performance optimization or margining in response to serial VID commands. Available in a 2mm x 3mm DFN-10 package, the LTC7106 enables small and simple solution for a wide range of discrete and modular DC/DC voltage regulators. Its internal power-on reset circuitry keeps the DAC output current at zero until a valid write takes place. Other features include a range bit for easy interfacing to almost any impedance resistor divider, and an open-drain output for controlling the Run or Enable pin of the regulator. To prevent abrupt changes in the DAC output current and subsequently the output voltage of the regulator, an internal digital programmable slew rate can be programmed from 500ns/step to 3.5ms/step.

www.linear.com/product/LTC7106

BCR430U Improves Efficiency for LED Strips

Infineon Technologies AG releases BCR430U, a constant current linear LED driver IC. The BCR430U provides industry-leading drop performance for regulating LED current in standalone operation. No external power transistor is needed. Typical applications for the



BCR430U include LED strips, architectural LED lighting, LED displays as well as retail, appliance and emergency lighting. The voltage drop at the integrated driver IC can go down to 135 mV at 50 mA. This improves overall efficiency and provides the voltage headroom required to compensate for LED forward voltage toler-

ances and variances in the supply voltage. Thus, more flexibility in the lighting design is possible. With the BRCU430U, additional LEDs can be added to lighting designs without changing the supply voltage. The LED driver current ranges between 5 mA and 100 mA and can be easily adjusted via high ohmic resistor on a dedicated pin. The supply voltage ranges between 6 V and 42 V. For safe and reliable operation and to extend the LED lifetime, a smart over-temperature controlling circuit reduces the LED current when the junction temperature is very high.

www.infineon.com/bcr430u

March 2018

DC-DC Converter Family Powers Modern Railway Applications

Vicor has released its next generation of DCMs with a family of wide input range (43 – 154V input) 3623 (36 x 23mm) ChiPs with power levels up to 240W and 93% efficiency, targeted at new rail transportation and infrastructure applications.

home. Freight rail systems require monitoring and control capabilities to assure the safe and timely delivery of all goods onboard. While both commuter and freight systems demand reliable and high-performance power systems for the necessary safety and



Modern rail infrastructure requires a wide range of DC-DC converters to power a variety of new services for both freight and commuter markets. Commuter rail systems require mobile office communication capabilities with the infotainment capabilities of board and at station). The DCM is an isolated, regulated DC-DC converter module that can operate from an unregulated, wide range input to generate an isolated DC output. These new ChiP DCMs simplify power system designs by supporting multiple input voltage

security measures (on-

ranges in a single ChiP. With efficiencies up to 93% in a ChiP package less than 1.5in2, these DCMs offer engineers leading density and efficiency.

www.vicorpower.com

High Throughput Processing for 3D and Wafer-level Package Assembly

Nordson MARCH, a Nordson company, introduces the MesoSPHERE[™] Plasma System for very-high throughput processing of 3D and wafer-level packaging processes such plasma chamber ensures that all areas of the wafer are treated equally and uniformly. Tight control over all process parameters gives highly repeatable results.



as fan-in, fan-out, wafer-level, and panellevel -handling wafers up to 450mm and panels up to 480mm. The MesoSPHERE's new, patented W3 three-axis symmetrical For wafer cleaning, the Meso-SPHERE plasma system removes contamination prior to wafer bumping, organic contamination, fluorine and other halogen contamination, and metal and metal oxides. Plasma improves spun-on film adhesion and cleans metallic bond pads. For wafer etching, the Meso-SPHERE plasma system descums wafers of residual photoresist and BCB, pattern dielectric layers for redistribution, strip/etch photoresist, enhances adhesion of wafer applied materials, removes excess wafer applied mold /epoxy, enhances adhesion of gold solder bumps, destresses wafer to reduce breakage, improves spun-on film adhesion, and cleans aluminum bond pads.

www.nordsonmarch.com

LINEAR DC Power Supply

The PMX-A is a compact, low ripple noise, linear DC power supply optimized for comfort and efficiency in any lab application. With digital interface support, clean output and high display resolution, the PMX-A provides unrivaled quality and convenience at an affordable price.

 Up to 500V output with 3U height
 True linear regulation with low output noise and fast transient response
 Programmable with LAN(LXI)/USB/R\$232C

standard interfaces High Display Resolution (1mV, 0.1mA) Remote Sensing Function



March 2018

XSPairFET™ in DFN 3.3x3.3 Package

Alpha and Omega Semiconductor Limited (AOS) introduced AONE36132, a 25V N-Channel MOSFET in a dual DFN 3.3x3.3 pack-

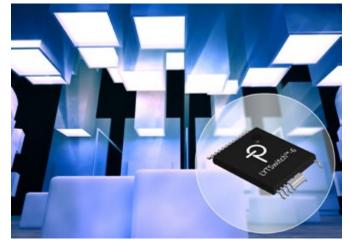


age which is ideal for synchronous buck converters. The AONE36132 is an extension to the XSPairFET™ lineup. Designed with the latest bottom source packaging technology, the AONE36132 has lower switch node ringing due to lower parasitic inductance. This new XSPairFET™ offers a higher power density compared to existing solutions and is ideally suited for computing, server and telecommunication markets. AONE36132 has an integrated high-side and low-side MOSFETs (7mOhms and 2mOhms maximum on-resistance, respectively) within a DFN 3.3x3.3 XSPairFET™ package. The low-side MOSFET source is connected directly to the exposed pad on PCB to enhance thermal dissipation. Using an existing notebook design under typical conditions, 19V input Voltage, with 1.05V output Voltage, and a 21A output load condition, the AONE36132 had more than a two percent efficiency improvement when compared to a single DFN 5x6 high side and single DFN 5x6 low side configuration. "The AONE36132 is the latest addition to the XSPairFET™ family which incorporates innovative technology to increase power density and improve efficiency for today's demanding applications," said Peter H. Wilson, Marketing Director of MOSFET product line at AOS.

www.aosmd.com

LYTSwitch-6 LED Drivers Feature High Efficiency and Low Standby Power

Power Integrations announced the LYTSwitch[™]-6 family of safetyisolated LED-driver ICs for smart lighting applications. The ICs deliver flicker-free output up to 65 W, and feature up to 94% efficiency and as little as 15 mW standby power, with configuration options for two-



stage or single-stage PFC support. Targeting smart residential and commercial fixtures and low-profile ceiling troffers, LYTSwitch-6 ICs also exhibit fast transient response, which facilitates excellent cross regulation performance of parallel LED strings without additional regulator hardware, and allows easy-implementation of a pulse-widthmodulation (PWM) dimming interface. LYTSwitch-6 ICs include both constant-voltage (CV) and constant-current (CC) operation, enabling lighting manufacturers to reduce the number of product variants, resulting in manufacturing and logistics savings. The new ICs are protected by an advanced thermal foldback system which prevents overheating while delivering as much light as thermally possible in any circumstance or installation. LYTSwitch-6 ICs feature a built-in 650 V or 725 V MOSFET and secondary-side FluxLink™ control which eliminates the need for an optocoupler and provides highly accurate output with better than 3% CV and CC over line, load and temperature. Power conversion for the flyback stage is more than 94% efficient, achieved by using synchronous rectification and quasi-resonant switching which enables high power output without a heatsink.

www.power.com/lytswitch-6

Powerful Protection for the Internet of Things

The Internet of Things is changing the world as we know it – in industry and in the home. Smart industrial robots, refrigerators and washing machines already communicate with each other. Yet devices that are online can be attacked. That's why Infineon Technologies AG is adding the OPTIGA™ Trust X to its OPTIGA™ Trust family. This hardware-based security solution provides robust security to the diverse applications in the Internet of Things, ranging from smart homes to drones.

Hardware-based complete solution for the IoT

The OPTIGA Trust X offers secured communication and software updates, mutual authentication and much more. Device manufacturers save time and costs thanks to the plug-and-play concept enabling even companies without specialist know-how in the field of security. "In the Internet of Things we have to think about security from the very beginning," says Thomas Rosteck, Division President Chip Card & Security at



Infineon. "Hardware-based security provides the necessary protection against attackers, as critical data can be separated from operations. Thanks to OPTIGA Trust X, we make it easy for manufacturers to integrate robust security into their IoT devices."

www.infineon.com

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PSR Series with Ultra-Low Ohmic Shunt Resistors

With its PSR100 series, Rohm offers a significantly more compact version of its proven PSR series. The PSR100 series ultra-low ohmic shunt resistors have a high-power capability and are suited to current measurement in automotive and industrial applications. The new shunt resistors, which are based on a high-performance metal alloy as the resistive element, feature superior temperature coefficients (TCR) from ±50ppm to ±150ppm. Thanks to Rohm's innovative



precision welding technology, they deliver a high rated power of 3W coupled with an ultra-compact form factor of 6.35mm x 3.05mm. Their resistance range covers $0.3m\Omega$ to $3.0m\Omega$. The resistance tolerance is specified with F (±1%). The operating temperature range is -55°C to +170°C. The PSR100 series is the ideal solution for automotive and industrial applications as well as many other areas with high requirements in terms of performance and size. These include for example on-board chargers, electronic compressors and EPS in motor vehicles in addition to UPS and base stations.

www.rohm.com/eu

TMC5160 Controller/Driver IC

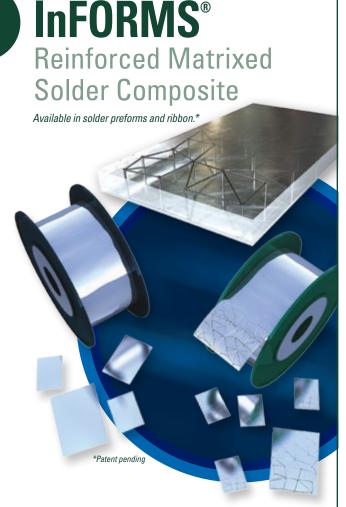
TRINAMIC Motion Control, leading global developer of motor and motion control technologies, announces the TMC5160. This new, single-



axis stepper motor driver IC with serial communication interfaces is developed for 2-phase bipolar stepper motors with external MOS-FETs for up to 20A motor current per coil. "It successfully combines our technological innovations into a single device that achieves

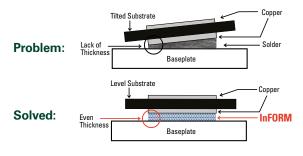
a new maximum for motor voltage and current specs with external N-channel MOSFETs," explains Michael Randt, Founder and CEO of Trinamic. "Ease-of-use was the guideline for our designers, as well as cost efficiency. By integrating a powerful stepper motor driver and a dedicated motion controller in one single chip, the TMC5160 directly transforms digital information into physical motion that's smooth, precise and reliable. In fact, it's so easy to use that you only need the target positions. All stepper motor logic takes place within the TMC5160 itself – there's no need for software when driving NEMA17 up to NEMA34 and bigger motors. Connected to a host microcontroller through an industry standard SPI or step/direction interface, the TMC5160 performs all real-time position and velocity stepper motion calculations.

www.trinamic.com



Uneven bondline thickness causes concentrated stress, which impacts reliability.

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Common InFORM stand-offs:

Solder Preform Requirements				
Description	Stand-Off (Microns)	Part Dimensions (x and y) (Millimeters)	Part Dimensions (z) (Microns)	
LM04	100	>10 per side	>150	
LM06	150	>10 per side	>200	
LM08	200	>10 per side	>250	
SM04	100	2.5–10 per side	>150	
ESM03	75	.75–2.5 per side	>125	

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NPC Modules with IGBT Chip Technology for up to 120 kVA

Vincotech announced the launch of new neutral-point-clamped power modules featuring the latest IGBT technology for three-phase solar, UPS and ESS applications. Engineered to address the key challenges of high efficiency, low weight and small size, these flowNPC 2



modules outperform standard products. Rated for 650 V / 200 A & 300 A, they are able to deliver switching frequencies up to 50 kHz even without SiC technology. When Si components are used, the best performance starts above 8 to 10 kHz. As cost comparisons show, these NPC modules offer 10% savings over MNPC modules rated for the same current. They are packaged in the low-inductive, 13 mm flow 2 housing and available with Press-fit and solder pins, without adding any non-recurring engineering costs to the bottom line. Samples of these ultra-efficient flowNPC 2s may be sourced on demand from our usual channels.

www.vincotech.com/flowNPC_2-S5

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abb.com/semiconductors



iMOTION™ IMC100 High performance motor control IC series

iMOTION[™] IMC100 is a series of highly integrated ICs for the control of variable speed drives. By integrating both the required hardware and algorithm to perform control of a Permanent Magnet Synchronous Motor (PMSM) they provide the shortest time to market for any motor system at the lowest system and development cost. Using space vector PWM IMC100 devices achieve highest energy efficiency for any high and low voltage drive.

Outstanding customer benefits

> Fastest time to market

- No software development required
- Easy motor parametrization and tuning
- > Lowest BOM cost
 - Integrated ADC and comparators
 - Sensorless FOC algorithm
 - Internal oscillator
- > Integrated protection features
- > Flexible package options

- > Next generation of field proven
 - Motion Control Engine (MCE 2.0)
 - Single or leg shunt current measurement
 - Optional hall sensor support
 - Optional boost or totem pole PFC
 - Flexible host interface options
- > Support for IEC 60335 (Class B)
- > Scripting engine for application flexibility



