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Electronics in Motion and Conversion

March 2020

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New Orleans and APEC

A few years ago, APEC was planned for New Orleans. However, Hurricane Katrina had other ideas and so it was moved to Houston. Now in March 2020 we will be in New Orleans for the conference and show.

Power Conversion and Motion Control are the basics of the conference - the highlights will be the usage of wide band gap devices. Both SIC and GaN will be game players. Passives need to show how they are adapting to wide band gap semiconductors in their performance. Hopefully we will see improvements at elevated frequencies in magnetic materials and also in capacitors.

Final system solutions are what we will look for. Reduction of losses is the key measurement of progress. The IGBT in the mid 80's contributed substantially to reducing losses in variable speed three phase motion control designs. Two decades later, GaN and SiC switching devices are available with lower conduction and lower switching loss. As a result, higher switching frequency is possible, with the benefit of smaller magnetics, other passives, and smaller heatsinks. This will be great for power conversion applications.

So, engineers will make the world better. Politicians, in some cases missed the right education or are too old for physics. Global warming is ramping up worldwide, which has been proven and accepted by the scientific community. We must preserve the future for our young generation. We need to work harder to stop global warming - efficiency is a key topic.

You will find an APEC floorplan printed in the centerfold of the March issue. The floorplan



will feature the logos of our supporters and if you are exhibiting or attending the conference, this will provide easy navigation to their booths.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving North America efficiently. If you are using any kind of tablet or smart phone, you will find all of our content optimized for mobile devices on the updated website www.bodospower.com.

If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com

My Green Power Tip for the Month:

If you have cold feet at night just wear woolen socks. This is better than heating the bedroom and has been proven by an old friend. I have tried it too and it works!

Best regards



Satellite 2020 Washington, DC, USA March 9-12 www.satshow.com

APEC 2020 New Orleans, LA, USA March 15-19 www.apec-conf.org

EMV 2020 Cologne, Germany March 17-19 https://emv.mesago.com

Events

AMPER 2020 Brno, Czech Republic March 17-20 www.amper.cz/en.html

CIPS 2020 Berlin, Germany March 24-26 www.cips.eu/en

Power Electronics Expo 2020 Silverstone, UK March 26-28 www.powerelectronicsexpo.co.uk ExpoElectronica 2020 Moscow, Russia April 14-16 www.expoelectronica.ru/home

PEMD 2020 Nottingham, UK April 21-23 www.theiet.org/pemd

EV Tech Expo Europe 2020 Stuttgart, Germany April 28-30 www.evtechexpo.eu

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Competence for System Solutions of Universal Chargers

Infineon Technologies expands with Rompower its expertise for the development of universal chargers with high efficiency and compact design. These USB-PD chargers (Power Delivery) with the universal USB-C connector enable the power supply of e.g. monitors or smart speakers and charge the batteries of mobile devices such as smartphones or tablets. Today, these plugs already perform other functions, such as fast charging smartphones. Using the USB-PD technology, smartphones can be fully charged in less than an hour. USB-PD is made possible by the universal USB-C connector, which allows for higher data transfer and higher power transfer compared to widely established micro-USB and USB-A/B connectors. The next development stage for all these functions will be permanently installed USB-PD wall outlets. With a maximum power output of 100 W made possible by the USB-PD standard, they not only support fast charging of mobile devices, but also function as permanently installed adapters. In the medium term, USB-PD charging sockets will be used in public buildings, such as airports and hotels, as well as in private households and



will reduce the need for adapters and chargers. Within the partnership, Infineon will contribute its semiconductor expertise, Rompower will offer its technologies and international know-how in the system area as well as in the construction of compact, small and highly efficient charging solutions. The first step is the development of system solutions for compact fast chargers for smartphones and USB-PD wall outlets.

www.infineon.com

The Lighting Industry Comes Together

The focus for the workshops and panel discussions at LpS/TiL in Bregenz will be centred around the third industrial revolution and what this really means for lighting designers, technologists, manufacturers and regulators. All parties can inspire, contribute and influence the next steps companies must make in order to satisfy end-users and harness IoT capabilities. A new industrial revolution is characterized by three major technological advances occurring almost simultaneously; new energy sources, new communication channels and new transport options. Renewable energy sources, the world of the Internet, IoT and self-propelled traffic on land and in the air show these developments in concrete terms. After 200 years of industrial activity, resource depletion and climate change, the lighting industry is navigating future technologies, infrastructure and investment decisions. There is a palpable biosphere consciousness and drive to protect nature and the environment, to guard our habitat for future generations as well as for ourselves.

LpS/TiL 2020 will explore how and with what the light sector, including Photonics, can contribute. The new world for architects is dominated by smart retro-fit programmes and data-driven optimization. The new



world for manufacturers is designing for a circular economy including interoperability and standardization. Eminent speakers from these fields will come together to help share perspectives and understand the necessary collaborations and obstacles ahead.

www.led-professional-symposium.com

Transistor Technology Reaches Record Frequencies

Scientists at the Fraunhofer Institute for Applied Solid State Physics IAF have succeeded in developing a novel type of transistor with extremely high cut-off frequencies: metal oxide semiconductor HEMTs, in short MOSHEMTs. To achieve this, they have replaced the Schottky barrier of a conventional HEMT with an oxide. The result is a transistor that enables even smaller and more powerful devices. It has already reached record frequencies of 640 GHz. This technology is expected to advance next generation electronics.

The high frequency characteristics of high eElectron mobility transistors (HEMTs) have been steadily improved in the past years. The transistors have become increasingly faster by downscaling the gate length to 20 nm. However, a HEMT encounters a problem at such small structure sizes: The thinner the barrier material of InAIAs (indium aluminum arsenide) becomes, the more electrons leak from the current carrying channel through the gate. These unwanted gate leakage currents have a negative impact on the efficiency and durability of the transistor, which renders further downscaling attempts impossible.



The current transistor geometry of a conventional HEMT has reached its scaling limit. Silicon MOSFETs (metal oxide semiconductor field effect transistors) are no stranger to this problem, either. However, they possess an oxide layer that can prevent unwanted leakage currents for longer than it is the case with HEMTs.

www.iaf.fraunhofer.de

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SMALLER inverter designs reducing volume and weight

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FASTER charging and efficient power conversion





A New Solar Era in Spain Begins

By adding an estimated 4.7 GW in 2019, Spain returns to the continent's top solar markets and is the clear market leader in Europe. The forecasts for the future development remain promising. According to Solar Power Europe's "European Market Outlook 2019-2023", Spain is expected to have a compound annual growth rate of 34% by 2023 in the medium scenario. A total installed solar PV capacity of 25.6



GW will then be reached. What role corporate sourcing of renewables and PPAs (Power Purchase Agreements) will play in this process and what obstacles still have to be overcome will be discussed on May 19, 2020 at Intersolar Summit Spain in Barcelona. After a successful start in 2019, Intersolar Summit Spain is taking place for the second time and will welcome more than 250 attendees. At the beginning of 2019, the Spanish government approved the submission of the draft Integrated National Energy and Climate Plan 2021-2030 (NECP/ PNIEC). It defines caps on national greenhouse gas emissions, taking into account renewable energy and energy efficiency measures. The main goals are, to reduce greenhouse gas emissions by 21% with respect to 1990, to achieve 42% renewable energy in the country's final energy use, and to achieve 74% renewable energy in electricity generation by 2030.

www.thesmartere.com

Symposium on Reliability for Semiconductor Devices, Microelectronic Systems, and Advanced Technologies

The 2020 IEEE International Reliability Physics Symposium (IRPS), a technical conference for engineers and scientists to present the latest original research in microelectronics reliability, will be held in Dallas, TX from March 29 – April 2, 2020 at the Hilton DFW Lakes Executive Conference Center. The Symposium will feature a number of special



focus sessions highlighting novel and emerging areas of electronic reliability, as well as topics relating to conventional semiconductor, integrated circuit, and microelectronic assembly reliability. The 58th annual IRPS will feature a technical program of more than 100 invited and accepted papers delivered by leading reliability scientists and engineers from around the world. It will be preceded by 24 90-minute tutorial sessions on Sunday & Monday, March 29 & 30, and by interactive evening workshops covering 10 different reliability topics on Tuesday, March 31.

"The Symposium program is expanding beyond the traditional areas of CMOS device, circuit, and systems reliability to include emerging microelectronics reliability topics, including circuit reliability & aging, wide bandgap semiconductors, neuromorphic computing reliability, and RF/mmW/5G device reliability, reflecting major trends in the industry," said Charles Slayman, IRPS 2020 technical program chair & Cisco Systems technology leader. "In addition, this year IRPS is privileged to have five outstanding keynote speakers for the plenary sessions from both industry and academia."

www.irps.org

Adding Resistors to Passive Components Portfolio

Exxelia announced that it has completed the acquisition of Micropen Technologies Corporation. Micropen is a designer and manufacturer of high technology resistors, known under the Ohmcraft® brand, serving the medical, defense, space and industrial markets. Micropen also manufactures with the same technology unique special sensors dedicated to the medical and security markets.

Established in 1982 in Honeoye Falls, NY, Micropen Technologies has developed a unique process to print critical functional materials, such as conductive electrodes, precious metals, on various planar or 3D substrates, such as ceramic, plastic and others. This patented system is the core technology for the design and manufacture of Ohmcraft® complete line of resistors as well as some of the world's most innovative monitoring & stimulating medical sensors. "We are very excited to welcome Micropen's talented, engaged and committed team, and very proud to add Micropen's unique technology under our already



extensive portfolio of highly-engineered passive components and sensors. Thanks to this unrivaled process, Exxelia gains a foothold in the high-rel resistors world and enhances its ability to serve as a key product solution provider to customers with mission-critical applications", said Paul Maisonnier, Chief Executive Officer of Exxelia.

www.exxelia.com

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Low Power Drives SEMITOP E1/E2: 0.37 - 30kW



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Medium to High Power Drives SEMiX 3 Press-Fit: 55kW - 250kW

Coalition Dedicated to Corporate Social Responsibility

Microchip Technology announced it has joined the Responsible Business Alliance (RBA), a nonprofit coalition of companies dedicated to the improvement of social, environmental and ethical conditions in their global supply chains. The RBA Code of Conduct is a set of social, environmental and ethical industry standards. The standards set out in the Code of Conduct reference international norms and standards including but not limited to the Universal Declaration of Human Rights, ILO International Labor Standards, OECD Guidelines for Multinational Enterprises plus ISO and SA standards.

"With the principles of corporate social responsibility as a fundamental part of Microchip's DNA, we remain committed in every aspect of our business and operations to advancing human rights, ethics and health and safety worldwide," said Ganesh Moorthy, president and chief operating officer. "Along with RBA member companies, we align under a set of common values that send a clear message of commitment to the global supply base and to our customers." Microchip's values and operating principles including its Code of Business Conduct and Ethics, certifications, sustainability reporting and other standards are reflected in the company's practices and actions of employees worldwide. Microchip is committed to aligning with



organizations and companies worldwide to advocate for principals regarding workforce and labor standards, human rights, sustainability and anti-corruption.

www.microchip.com

Introduction to Engineering

"Our aim was to inspire children's interest in the technical world," explains Peter Fenkl. The Door-Opener Day of the "Show with the Mouse" is held every year when hundreds of German institutions and companies open their doors to children. "As a specialist in quiet and efficient fans and electric motors, Ziehl-Abegg was putting the focus



of the 2019 Door-Opener Day on its core area of expertise, the electric motor", says the CEO.

The "Show with the Mouse" doesn't aim to be just an "Open Day" – the intention instead is to provide children with glimpses behind the scenes and – as far as possible – enable them to make something themselves. Roughly 100 children between 9 and 12 year came to Ziehl-Abegg in Derrimut (Australia), Singapore (Asia), Johannesburg (South Africa), Cajamar (Brazil), Greensboro (USA) and Kupferzell (Germany). They all built an electric motor. Project manager Sophie Grill emphasises that this international action goes hand in hand with the company's development: "We started selling our products on the international markets in 1972, then 'internationalised' our production and subsequently brought the successful model of dual training to France, Hungary, Brazil and the USA – making an international Door-Opener Day for the "Show with the Mouse" the next logical step."

www.ziehl-abegg.com

Reduce System Costs for Inverters

The installed photovoltaic capacity is growing rapidly worldwide. Photovoltaic systems with a total output of around 600 GW now supply clean and cost-effective electricity - replacing around 600 mediumsized coal-fired power plants. SMA Solar Technology AG (SMA) and Infineon Technologies support this growth trend with the latest generation of innovative silicon carbide (SiC)-based solar inverters. The semiconductor material reduces the system costs for inverters and increases their efficiency. The production costs for solar power are thus further reduced. With the Sunny Highpower PEAK3 from SMA, available since 2019, decentralized photovoltaic power plants can be planned flexibly and efficiently up to the megawatt range. The basis for this is the compact design designed for 1500 VDC, which delivers an output of 150 kW per unit. This is made possible by SiC technology from Infineon: Six power modules of the type CoolSiC™ EasyPACK[™] 2B and 36 gate drivers of the EiceDRIVER[™] family 1ED20 convert the direct current generated by the solar cells into grid-compatible alternating current - with an efficiency of over 99 percent. "Silicon carbide enables us to build the inverters compact, powerful and reliable," said Sven Bremicker, Head of Technology Development Center at SMA. "In the Sunny Highpower PEAK3, the CoolSiC modules almost double the specific output from 0.97 to 1.76



kW/kg. Due to the compact design, the inverters are much easier to transport and much faster to install."

www.sma.de



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The World of Power Semiconductor Devices Meets in Vienna

The 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD) will be held in Vienna, Austria, May 17–21, 2020. It is the premier forum for technical discussion in all areas of power semiconductor devices, power integrated circuits, their hybrid technologies, and applications. With an attendance of about 500 experts it is firmly established as the must-attend conference for the power semiconductor industry reflecting the growing importance of power electronics and power semiconductors for a sustainable world. It is technical co-sponsored by IEEE and its societies EDS, PELS and IAS, as well as by ECPE and IEEJ.

The ISPSD captures all areas of power semiconductor devices and power integrated circuits (low and high voltage power devices & circuits, all semiconductor materials including Si, SiC, GaN and Ga2O3, as well as power semiconductor packaging). The conference offers an attractive short course program on Sunday covering important topics like modelling of package parasitics for fast switching devices, system



level optimization of power converters, bipolar and super junction device concepts for SiC, GaN integrated circuit design, processes and devices with materials beyond SiC & GaN (like AIN, Ga2O3), and last but not least silicon high power devices (IGBTs and Fast Recovery Diodes).

www.ispsd2020.com

Battery Electric Vehicle Architectures Congress

To realise the transition towards zero-emission high-efficiency vehicles, battery weight reduction and design of lightweight structures become the main challenge for the automotive industry. To realise the transition, OEMs need to identify the right strategies in selecting and utilising lightweight materials; taking safety, performance, production volume and manufacturability into consideration, for longer range, with lower cost.

Optimisation in design, engineering and manufacturing are key issues for all OEMs. In order to directly address these, and identify solutions, LBCG is delighted to announce the Battery Electric Vehicle Architectures & Lightweight Materials 2020 Congress, May 5 & 6, 2020, Munich, Germany, a combination of our successful BEVA series and GALM series on BEV lightweight structures and material utilisation. Bettery Battery Electric Vehicle Architectures & Advanced Lightweight Materials 2020

Strategies & Solutions For Design, Engineering, Material Selection & Manufacturing For Optimal Integration Of Battery & Systems Within The Car Body

MAY 5-6, 2020 | MUNICH

Highlights of the 2020 agenda include:

- Platform strategies evaluate dedicated
- BEV platforms vs. conversion platforms
 Engineering solutions to protect the battery enclosure from side & under vehicle impacts to optimise stiffness, NVH, and safety

- Battery packaging, thermal management, and systems integration for weight reduction and efficiency optimisation
- Innovative battery design and engineering technologies for battery weight reduction
- Flexible platform to accommodate a diversified mix of powertrains and integration in one production line
- Optimised design of new components for battery systems, motors and powertrain
- Case studies and cost-effective engineering solutions in advanced joining between dissimilar materials
- Future technologies for structural composites, adhesives, additive manufacturing and enhanced crashworthiness

www.beva-alm-europe.com

PCIM Europe 2020's Trending Topics and Highlights

Every year the power electronics industry from all over the world meets at the PCIM Europe in Nuremberg. In 2020, trade visitors of the leading international exhibition and conference for power electronics can, once again, look forward to highly specialized highlight topics



and an attractive program of lectures. From 5 - 7 May 2020, Nuremberg will revolve around power electronics and its applications. Some 500 exhibiting companies from 30 countries are expected to present a broad range of products and solutions to trade visitors - from components to intelligent systems along the entire value chain. New trends and developments will be presented to the public for the first time at the meeting point for experts from industry and science. Trade visitors will receive a deeper insight into product innovations and enjoy a personal exchange with manufacturers - whether they come from the field of power electronic converter systems, sensors, semiconductors, passive components or power quality and energy storage. For those interested in power electronics for electric mobility, the E-mobility Area is the first place to go. Here, numerous suppliers will provide information on relevant products and components from this application area. In addition, there is a special E-mobility Forum with exciting technical presentations to be discovered on all three days of the exhibition.

https://pcim.mesago.com



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Meet us at APEC 2020 Booth # 1760



Shining the Spotlight on Intelligent Charging Systems



The expansion of charging infrastructure is one of the most important factors that will determine the success of the transportation transition. With this in mind, many European countries are stepping up investments in this infrastructure. Smart charging is resulting in e-mobility becoming increasingly intelligent by, for example, charging electric cars when it makes economic sense to do so or by allowing car batteries to temporarily store electricity for use in the car owner's home or the power grid. A new white paper produced by the European business association SmartEN (Smart Energy Europe) in cooperation with Power2Drive Europe, the international exhibition for charging infrastructure and e-mobility, sheds light on the latest trends. The topic will also be a key feature of the exhibition itself, which will take place in Munich from June 17 to 19, 2020. One highlight of the event will be the introduction of new smart charging and vehicle-to-grid concepts (V2G).

www.powertodrive.de

Iso 13485:2016 Certification Achieved



EOS Power is proud to announce that it has received certification for ISO 13485:2016, Quality management system for Medical devices. The certification

was granted by LL-C Certification, Czech Republic. EOS Power is engaged in design, manufacturing and selling of Medical grade power supplies. EOS Provides standard, modified and custom design power solutions to customer needs. All Medical grade power supplies are approved to latest medical certifications required globally and now in addition EOS Power design process, manufacturing and quality systems are certified to ISO13485 standards. This allows EOS Power to become a "one stop" solution for medical device manufacturers for their power supply and any EMS/PCBA requirements required in their medical application. ISO 13485:2016 standard is recognized by the Global Harmonization Task Force (GHTF) and has become the model QMS standard for the medical industry. "EOS Power's manufacturing facility obtaining ISO 13485:2016 certification is an advantage when working with Medical customers, allows us to add potential opportunities in the medical device markets we have being missing where this certification was required." says Mr. Paul Scholz, VP-Sales. This certification provides additional leverage with customers, added Ms. Teresa Fernandez, EMEA Sales Manager. "Successfully achieving ISO 13485:2016 certification is a huge milestone for EOS Power in its journey of becoming a world class organization. This will certainly help to position EOS Power as a global leader in the medical device industry" says Mr. Vijay Gujarathi, COO and Director.

www.eospower.com

North Carolina State University to Host EnerHarv

The Power Sources Manufacturers Association (PSMA) and North Carolina StateUniversity (NCSU) are pleased to announce the EnerHarv 2020 International Workshop on Energy Harvesting and Micro-Power Management will be held from June 16-18. 2020 in Raleigh, North Carolina and hosted by North Carolina State University. The event will be managed by the Center for Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST) at NCSU. EnerHarv 2020 will build upon the inaugural event held in 2018 at the Tyndall National Institute in Cork, Ireland. The mission remains the same - to create a focal point for a community of experts and users of energy harvesting & related technologies to share knowledge, best practices, roadmaps, experiences and to create opportunities for collaboration primarily in the wireless IoT edge device sector. "EnerHarv



was set up as a key biennial event to help solve the 'trillion sensor challenge' of 2025, recognizing that most of the world's IoT devices will require a portable power source such as a battery needing to outlive the device that it powers," commented Brian Zahnstecher, PSMA Energy Harvesting Committee and EnerHarv Co-Chair.

www.enerharv.com

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BETTER the total ble



Designers seeking to strike the right balance between cost and performance need real alternatives. Combining flying-capacitor topology with full SiC or hybrid Si/SiC components, Vincotech's latest three flowBOOST 1 dual modules provide the real alternative for the right cost/performance balance.

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Boost: hybrid

a common footprint for greater flexibility in design and leading cost/performance metrics

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Boost: full SiC

Boost: full SiC



/ Optimized IGBT- and SiC-based solutions with

An Intelligent Power Module for High Switching Frequency Applications



To enable washing machines and various small-capacity motor drives to achieve reduced motor noise and consume less power, Mitsubishi Electric has recently announced the coming launch of its SLIMDIP-W, a new high-performance intelligent power module (IPM).

Mitsubishi Electric pioneered the DIPIPM[™] concept and introduced in 1997 the first transfer-molded IPM, integrating IGBTs for a three phase inverter and low side and high side gate drivers with additional protection functions to offer an optimized and consistent reliable performance while addressing the module's low-cost requirements.

The SLIMDIP[™] family is the newest through-hole IPM, which offers reduced space and an optimized pin layout. The newly developed SLIMDIP-W module is a high-speed switching optimized version of the SLIMDIP-L module to fulfil the market demand of low audible noise inverters, which require high switching speeds above the audible range of a human. Especially for home appliance products located in the living space, a low noise level is mandatory. For white goods sold in the EU, the EU energy label gives, beside the energy efficiency, the information about the noise level, allowing the customer the easy choice for a silent model.

Developing the SLIMDIP-W module for high-speed switching required adaption on the chip level. In the tradeoff curve of V_{CE,sat} vs E_{off}, a different point is chosen to achieve an optimal loss performance at switching speeds higher than for the SLIMDIP-L with the same current rating and RC-IGBT technology. Additionally, the gate driver was optimized, resulting in faster switching times. Switching power loss is reduced by approx. 35% (Tj=125°C, Io=5Arms, fc=15kHz). Usually, faster switching speeds of the IGBT modules will increase also electromagnetic noise emissions. In this case, due to advanced gate driver adjustments, the EMI could be even improved.

Important for platform inverters and new design-ins is the fact, that the SLIMDIP-L and SLIMDIP-W are fully pin-compatible. This allows a use of the SLIMDIP-W in existing PCBs for the SLIMDIP-L without any modifications, if going to higher switching frequencies. Moreover, the thermal impedance of the package for SLIMDIP-W is the same as for SLIMDIP-L.



The new SLIMDIP-W module is the answer to the market demand for compact and price sensitive inverters in home appliances and small industrial applications with high switching speeds. Built with Mitsubishi Electric's long term experience in producing transfer-molded IPMs, a high reliability can be achieved.

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Making ADAS Technology More Accessible in Vehicles

by Curt Moore, General Manager Texas Instruments

Advanced driver assistance system (ADAS) features have been proven to reduce accidents and save lives. As ADAS continues to evolve toward the Society of Automotive Engineers-defined L4 and L5 autonomous vehicles, there's an opportunity to make a greater impact on the road by creating ADAS technology that can be used in a wider range of cars.

The need for smart and diverse sensing

Maintaining consistent ADAS operations in all situations is challenging. Unanticipated scenarios like the sudden onset of inclement weather or unsafe road conditions require vehicles to adapt in real-time. These are not scenarios you can code for, but by developing a dynamic system that can help the car sense, interpret and react quickly to the world around it, cars can act more like a co-pilot for the driver. Such a system requires data and the ability to process that data in real-time using a combination of computer vision and efficient deep learning neural networks.

ADAS solutions need to extract data from a diverse sensor set and convert the data to actionable intelligence for the vehicle. At a minimum, these sensors include different types of cameras and associated optics, radars and ultrasonic technology. More complex cases will also include LiDAR and thermal night vision. Further, the system may perform vehicle localization by comparing features extracted from sensor data with high-definition map data. Assimilating and analyzing this multimodal sensor data must happen in real-time – new data arrives 60 times per second – without replacing the backseat of a car with a data-center server.

Any solution must be road-ready

In the same way that a driver receives multiple inputs concurrently and must make a safe driving decision guickly, any ADAS application - no matter what the level of autonomy - must do the same. A high-performance system on chip (SoC) that can handle concurrent processing without blowing the budget in terms of power, heat, component and integration costs is highly desirable. An SoC solution can scale from more simple cases (fewer sensors, lower resolutions) to the most complex cases without compromising basic ADAS features or requiring a lower-end system. Meeting application performance across a vehicle lineup is only one requirement. For wide deployment, these systems must be developed cost-effectively. Software complexity is increasing exponentially in vehicles - it is already 150 million lines of code - which is exploding development and maintenance costs. As systems become more situationally aware, safety requirements will evolve and grow, and all of these systems must meet strict automotive quality and reliability targets. These are the exacting demands and realities of supporting the automotive electronics market. The right SoC can accommodate an open software development methodology, making it possible to reuse the resulting code and

preserve efforts made in development and testing. An SoC can also be built from the beginning with functional safety as an imperative and with the reliability and product longevity necessary to keep vehicle lines viable in the market for years. Done well, the vision of enabling more cars with robust ADAS features (like those shown in Figure 1) is within reach.



Figure 1: Examples of ADAS applications

How TI is helping democratize ADAS technology

TI worked to address sensing, concurrent operation and system-level challenges by leveraging our decades of automotive and functional safety expertise to design our Jacinto 7 processor platform.

We focused on what matters to the entire system: combining outstanding sensing capabilities that monitor a car's surroundings in multiple directions, and using an automotive-centric design methodology for optimized power and system cost.

The Jacinto 7 processor family, including the TDA4VM and DRA829V, integrates key functional safety features on-chip that enable both safety-critical and non-safety-critical functions on one device; they also improve data management by incorporating high-speed and automotive interfaces. Jacinto 7 processors bring real-world performance to automotive ADAS and gateway systems and help lower system costs to help democratize ADAS technology and make it more accessible.

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Materials Science Changes the World of Electronics

VIP-Interview with Dr. Andy Mackie, Senior Product Manager, Semiconductor and Advanced Assembly Materials at Indium Corporation, about the company as a premier supplier of materials for a wide variety of different applications.

By Henning Wriedt, US-Correspondent Bodo's Power Systems

Your company was founded in 1934. What were the major milestones of Indium Corporation?

It should come as no surprise that the early history of Indium Corporation is tightly linked with the element indium. Indium as an element was discovered in 1863, but Indium Corporation's history really begins with the work of William S. Murray (Figure 1) and Daniel Gray, who independently began experimenting with indium as a coating to prevent silver from tarnishing. Indium Corporation was founded to explore other uses of indium. One of the first applications of indium was as a coating for ball bearings in airplanes: indium is a soft metal, but forms very hard, and hard wearing, intermetallics. In 1982, we expanded our manufacturing capabilities for our solder paste program in the fledgling surface mount technology (SMT) industry. In 1990, our first non-USA facility opened; we have since become a major global manufacturer and supplier of materials for the electronics and semiconductor assembly, thermal management, and thin-film markets.



Figure 1: Indium Corporation founder Dr. William S. Murray dedicated his life to investigating and developing the uses of indium metal.

In general: What role does your company play in the worldwide electronics market? What are your challenges?

We are a premier supplier of materials into a wide variety of different industries. Although we mostly serve the electronics and semiconductor assembly markets, we are also involved in medical devices and renewable energy, for example. The challenges are multifarious, and we have strong competitors. It is a daily challenge to develop and promote materials that differentiate us from our competition. We have a strong emphasis on collaboration:

- in consortia focused on growing markets and technology;
- with equipment partners (such as Mycronic), who provide deep process insights and opportunities for collaboration;
- · with universities working on promising new technologies.

Your Solder Alloy Directory has over 220 alloys. Does that mean that the corresponding applications are very complex? Correct: complex and broad! Our complete solder and brazing alloy metallurgy directory has over 250 Indalloy entries, of which we

annually ship around 150 in different forms: powder, paste, wire, microspheres, and a variety of shapes, sizes, thicknesses and even specialty surface treatments of engineered solders for specific applications, including those in power electronics.

Components and systems are getting smaller and smaller. How do you keep your soldering products and materials expertise ahead of this curve?

In digital electronics Moore's law has been the force for transistor shrinkage, but the economies of scaledown are no longer the main driver. The power semi world has also seen a revolution in shrinking die, alongside increasing current and power density. Not everything is getting smaller: for example in artificial intelligence (AI), we are seeing some die that are now as large as the wafer itself.

This general "decrease" trend has resulted in not just smaller device feature sizes, but thinner die - a common theme across most semiconductors. In power devices, silicon is slowly being replaced by wide band gap materials, and thinner die are reducing RDSON. However, thinned gate oxides are now impacting the longevity of SiC devices, so there are clearly some tradeoffs.

Package shrink in mobile devices is growing the heterogeneous integration and assembly (HIA [SIP]) market, which now bridges the 3-way gap between contract electronics manufacturers (CEMs); out-sourced assembly and test (OSATs); and major wafer fabs. The last are simply extending their post-back-end-of-line (BEOL) processes a little further, with the advantage of upstream supply chain control only dreamed of by the OSATs and CEMs.

Shrinkage impacts the pitch (I/O center-center distance), so Indium Corporation focuses on two aspects of materials: 1) The physical size of, for example, the printed or jetted solder paste deposit; and 2) Increasing quality expectations: for example, a material that works well for one specific application will exhibit increasing sensitivity to foreign matter as the package size shrinks to meet market needs. We have had to adopt a whiteroom approach to manufacturing some of our more advanced materials as a result.

There is a clear move from water soluble to low residue no-clean fluxes in flip-chip for two different reasons:

- As flip-chip pitches shrink (60µm pitch and below for copper pillar applications), water soluble fluxes become very difficult to clean out, as clearances are very tight
- The proliferation of flip-chip on (increasingly delicate) leadframe (FCOL) is only feasible if you eliminate the damaging water wash process.

You fabricate and package materials with unique shapes and physical properties. What kind of market requirements are behind this?

For solder preforms, we customize shapes to best meet customer needs, including extending into the z-axis. Each component or package has differing requirements for reliability, utility, and assembly process. For example, the small laser diodes used in an active optical cables assembly would need a die-attach to the submount of gold-tin (280°C melting point), while the submount attach to the PCB would be SAC305 (218°C MP), and final board attach would use a BiSnAg solder (238°C MP).

For SMT soldering, SAC305 (96.5Sn/3.0Ag/0.5Cu) can be used in many applications. Indium Corporation offers lead-free solder paste for a variety of melting points: Durafuse TM LT (<200°C) for lower melting points, Indalloy[®] 292 (>235°C) for moderate MPs, and BiAgX[®] technology (>262°C) for higher MPs.



Figure 2: Indium Corporation has a long research and development history regarding the unique applications of indium metal.

Indium, Germanium, Gallium, and Tin Metals. Which properties make them unique for which applications?

Indium (In): The importance of indium and its oxide can be seen in ubiquitous LED lighting, TVs, and displays. It is also used in cryogenic sealing and soldering applications in quantum computers. Indium's softness and low melting point make it ideal for some soldering and other applications where its moderately high cost is countered by its unique properties. In electronics assembly, it can be found as a component in solder alloys, and is also important in conductive thin-film indium-tin oxide as well as in III/V CVD deposited layers in LEDs and VCSELs. We would be remiss not to mention the concerns about the availability of indium. We have written several papers (available for download from our website) that prove that indium metal will continue to be available for many years to come.

Germanium (Ge): Germanium has historically been used for transistors, but it has a very low bandgap (0.7eV), so it is much more heat sensitive than silicon MOSFETs. There are emerging applications in spintronics and 3nm gate-all-around contact metals, such as SiGe. SiGe is also used in LIDAR and some low wattage power amplifiers.

Gallium (Ga): Its low melting point (29.8°C) and relatively low toxicity makes gallium and its lower melting alloys an ideal replacement for mercury (Hg). In electronics, Gallium is most often used in III/V semiconductors, but can increasingly be found as GaAs and even GaN and InGaN in power RF amplifiers and LEDs. Gallium and its

alloys have also been used as liquid metal thermal interface materials (TIMs) in new and emerging applications.

Tin (*Sn*): Tin is ubiquitous in solders as it reacts to form intermetallics (Cu and Ni are the metallizations of choice). It can also easily be recycled.

What is your expertise in Compound Semiconductors and what are the dominant applications?

We manufacture many materials for CS. High-purity (6N and higher) indium ingots are used for making crystal substrates, such as InP, InAs, and so on. InP laser devices are crucial for data communications as the InP bandgap results in a photonic wavelength within the transmission window of optical fibers.

The epitaxial layers on compound semiconductor wafers are grown by metal oxide chemical vapor deposition (MOCVD). The organometallic CVD chemicals are made from indium trichloride and gallium trichloride; both of which are manufactured at our facilities in the USA. Because CVD chemical manufacturing is challenging, we concentrate on the high purity and physical aspects of these materials, such as density and pourability. For example, gallium trichloride at room temperature is a difficult-to-handle waxy, sticky material that will corrode stainless steel, so we developed a granulated form that makes it pourable and much easier to handle.

"Indium Corporation is enabling the 5G Lifestyle". Can you explain your headline in more details?

5G is a major driver of growth for the electronics industry, although we have recently seen signs that it may not be as reliable for automated driving as we had thought. Our products can be found at almost every place in the electronics supply chain: from no-clean solder pastes using high reliability solder alloys, water-soluble flip-chip fluxes used in advanced logic and FPGA chips to gold-tin solder preforms for "coin" RF amplifier attachment.

What are 'Thermal Interface Materials' and in which applications do they have unique advantages?

Thermal interface material (TIM) is a general term for a heat-conducting material placed between two adjacent surfaces. The TIM ensures a reliable path for heat energy to flow out of an object to facilitate cooling. An ideal TIM will be thin and highly thermally conductive, and will reliably ensure perfect thermal contact between the TIM and both the heat source and the underlying cooler/heatsink contact surface.

Solder as a TIM melts, but even under the best conditions voiding is seen. A soft non-melting laminar thermal interface material, such as a thin, flat piece of indium may appear to be an ideal TIM, but even under the best conditions, there is some non-planarity which leads to poor mechanical contact. So, we developed the Heat-Spring[®] TIM which is a soft, highly thermally-conductive metal that under pressure forms a strong interfacial bond that, unlike other TIMs, continues to improve over time.

Increased current density, such as in WBG, has also led to a focus on inconsistent bondline thickness. As you can imagine, low concentrations of widely distributed small voids will not lead to local increases in current, while a small difference in the bondline thickness, will cause an increase in the current flow at the die edge or die corner.

This has repeatedly been shown to create local stress that leads to die cracking. Maintaining absolute flatness of the bondline is therefore critical. Our InFORMS[®] preform technology uses a solid solderable

metal framework embedded within solid solder to ensure that, after the solder melts, the bondline is consistent across the interface.

Is NanoFoil[®] your entrance into Nanotechnology?

I believe so, from a product perspective. We also supply materials such as very high-purity indium to be used in vapor deposition processes, so nano is not new in applications! NanoFoil[®] was certainly the first Indium Corporation material to feature true 1D (one dimensional) nanotechnology. It is a unique product for many of our customers, as it can instantaneously bond solderable surfaces together without warpage, and withstands extremely high usage temperatures, as the end product is essentially an intermetallic.

More recent nanoparticle-containing materials include our small-die pressureless QuickSinter™ silver sintering materials to replace some high-lead (Pb) and gold alloy solder pastes in die-attach. Nanocopper pastes are also under development and scale-up.

You have a solid presence in Asia: Are your main markets there?

Yes. More than 50 percent of our business is in Asia. That is why we have a major tech service and R&D focus there, as well as manufacturing capabilities. Our Asian customers range from mobile device manufacturers and subcontractors to wafer fabs for AI chips. We manufacture products in Suzhou, China, and we are further expanding capabilities in our main semiconductor and advanced materials hub in Singapore. Our recent addition of a new manufacturing facility in Chennai, India, is the start of a new wave of expansion.

What is your role in Space?

In 1989 we were honored to be part of NASA experiments in zero gravity alloy purification, led by our engineering team, so our technology has been in space a long time.

The military/aerospace (mil/aero) industry is notoriously conservative, and it is one of the last bastions of legacy eutectic tin-lead solder usage. Our long term association with the automotive electronics council (AEC) is also bearing fruit in mil/aero, as the latter increasingly looks to the automotive industry to learn how low cost, high volume and high reliability can exist together.



Figure 3: A 3D profilometric view of a jetting solder paste bump of Indium Corporation's PicoShot™ solder paste.

Our high reliability assembly products developed for the automotive industry have already found their way into both federal and private space ventures.

Looking to the further future, we have been monitoring space mining to ensure longevity of supply of non-indium rare elements. Asteroid or comet mining is fraught with difficulty. The ability to rapidly launch a vehicle capable of mining and retrieving minerals from a near-earth body is not there yet. Water can be split into H₂ and O₂, and is considered the "oil" of the solar system. As the race to mine water from the lunar polar ice caps heats up, we will be watching to see how we can supply materials to meet customer needs here.

What can our readers expect from your company in the near future?

One constant with Indium Corporation is our ability to innovate to meet customer needs: both in the near term to meet more speculative needs further down the line.

In early 2020, we are commercializing a new jetting paste (PicoShot[™], Figure 3), a lower melting high-reliability solder paste (Durafuse[™] LT), and a new high-reliability automotive solder alloy (Indalloy[®]292). Additionally, we have a type 6/7 (SiPaste[™]) solder paste for system-in-package set for release later this year. For new TIMs, the recently developed m2TIM[™] is a unique solid/liquid hybrid thermal interface material that combines liquid metal with a solid metal preform to provide reliable thermal conductivity while eliminating the need for die backside metallization.

Many thanks for the interesting questions!



Dr. Andy Mackie, Senior Product Manager, Semiconductor and Advanced Assembly Materials, Indium Corporation

Andy is an electronics industry expert in physical chemistry, surface chemistry, rheology, and semiconductor assembly materials and processes. He has more than 25 years

of experience in new product and process development and materials marketing in aspects of electronics manufacturing from wafer fabrication to semiconductor packaging and electronics assembly. He is an award-winning industry leadership and technical contributor. He is also an IMAPS Fellow and Life Member, Chair of the Editorial Advisory Board for Chip Scale Review magazine, and Surface Mount Technology Association (SMTA) member and keynote speaker.

Andy has written papers and lectured internationally on subjects ranging from sub-ppb metals analysis in supercritical carbon dioxide to solder paste rheology. Additionally, he holds patents in novel polymers, gas analysis, and solder paste formulation. Andy earned his PhD in Physical Chemistry from the University of Nottingham, UK, and a Master's of Science (MSc) in Colloid and Interface Science from the University of Bristol, UK. He is an alumnus of the UC Berkeley Product Management program.

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Value Enhancement of Full SiC 3.3 kV Power Module in nHPD2 Package

By Praneet Bhatnagar, Hitachi Europe and Katsuaki Saito, Hitachi Power Semiconductor Devices

Abstract

Hitachi has been at the forefront of introducing new packaging technology for high power semiconductors. Implementing the nextgeneration package platform, nHPD2, the product line-up of full SiC 3.3 kV modules is being expanded. By providing SiC Schottky barrier diode (SBD) co-packaged with SiC MOSFETs and full SiC chopper modules applicable circuit configurations such as 3 level converters, brake chopper circuit and boost converter can be implemented. Hitachi are introducing Copper sintering technology to the full SiC nHPD2, which replaces the conventional soldering thus elevating the maximum operating junction temperature Tvj(op). This drastically improves the power cycle durability. We have shown the maximum available output current which has been estimated using the mission profile of a METRO traction motor inverter. The performance of the full SiC 3.3 kV power module without SBD is revealed to enhance power cycling by 6 times that of a conventional Silicon counterpart in the same package platform. Presented here are the performance benefits obtained from these technology introductions.

Introduction

For traction converter systems, high power density is a key parameter for driving towards reducing size and weight. Silicon carbide (SiC) power modules are inherently suited to achieve the above goals due to low loss, faster switching speed and high temperature characteristics as compared to their Silicon (Si) counterpart. However, the advantage of high switching speeds can be compromised by the switching oscillations leading to lower switching speeds in real time applications. Apart from reducing the switching speeds which negates the inherent advantage of SiC we can also aim to reduce stray inductances at power module level. This can have a significant impact on reducing switching oscillations for the motor control systems thus enabling systems to avail the advantages of SiC technology. Young's modulus characteristics of SiC also stifle the appetite to transition to WBG technologies in high reliability applications.

Package platform for SiC

In 2015, Hitachi presented a next-generation low-inductance package for high-voltage and high-current/power devices named "next High Power Density Dual (nHPD2)" [1]. This package was developed to extract the best performance from high-voltage wide band-gap semiconductor devices, which have significantly faster switching speeds than that of their Si devices. To achieve this goal, the first step required is to reduce the total loop inductance by significant magnitude. This can be realised by aligning the conduction paths inside and outside of the package as anti-parallel and securing sufficient insulation distances. This enables us to estimate the product of the total inductance, including the filter capacitance and the rated current product, which is as low as 40 nH * 450 A (18 μ A·H). The inductance was verified as being low enough for SiC devices in high-voltage, high-power applications

to provide superior switching characteristics without generating oscillations [2, 3]. Figure 1 shows a comparison between the conventional high-voltage package platform and nHPD2 and between the Si-IGBT + SFD (soft and fast recovery diode) and Si + SiC-SBD. In this example, by using the SiC-SBD for Si SFD, reverse recovery energy became one-hundredth of the original value, and the turn-off oscillations were completely reduced. In addition to these effects, the turn-on and turn-off energy could be reduced significantly.



Figure 1: Comparison between the conventional high-voltage package platform and nHPD2 for different semiconductor configuration

Based on the above presented research the scope of this study was expanded to SiC-MOSFETs. To enable characterisation, we populated 3.3 kV SiC MOSFETs and anti-parallel SiC-SBDs in a nHPD2 package. Results exhibiting low switching energy and smooth switching waveforms were presented here earlier [4]. Figure 2 shows the simulated dependence of the maximum output current on the carrier frequency for the PWM inverter operation under similar cooling conditions for 3 variants of nHPD2 package. The 3 variants under discussion include the latest Si-IGBT + Si-SFD (Si+Si), latest Si-IGBT + SiC-SBD (Hybrid), and SiC-MOSFET + SiC-SBD (Full-SiCwSBD). The operation of a traction motor inverter for both acceleration and deceleration with power factors of +98 % (solid line) and -98 % (dotted line) corresponding to each state, respectively, was assumed. In the case of Si+Si, the maximum available output current decreases considerably with increasing carrier frequency due to the comparably larger switching energy loss. In contrast, Hybrid and Full-SiCwSBD have a moderate decrease in maximum available output current. However, when Hybrid operates at low frequency and with a negative power factor (PF = -98 %, fc < 500 Hz) and when Full-SiCwSBD operates at low frequency with a positive power factor (PF = 98 %, fc < 200 Hz), the maximum available output currents are even lower than those of Si+Si power module configuration. It was also observed that Hybrid exhibits almost negligible reverse recovery energy (Err), and conversely, the V_F of SiC SBD is much higher, especially at a high current density. In case of Full-SiCwSBD, the reverse current is



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Hitachi Europe Limited, Power Device Division email pdd@hitachi-eu.com +44 1628 585151 shared between the SiC SBD and the positive-gate-biased MOSFET. It is expected that the voltage drop, $V_{DS(on)}$ of a MOS structure is higher than that of an IGBT at higher current densities which will have an impact on higher conduction losses. Furthermore, except for unidirectional converters, such as an auxiliary inverter, most of the traction inverters are bidirectional, and they are expected to have the same output current in both directions. Therefore, the rated outputs are limited by the lower output of the plotted curve for the *Full-SiCwSBD*.



Figure 2: Comparison of the dependence of maximum output current on the carrier frequency.

Full SiC without SiC SBD

In the 1st-generation nHPD2 full-SiC module, the SBD was used to remove the risk of bipolar degradation in the MOS structure. Hitachi have been actively involved in analysing and demonstrating the mechanism for bipolar degradation caused by stacking faults (SFs) generating from basal plane dislocations (BPDs). Subsequently we have successfully proposed solutions to overcome these phenomena [5, 6]. The adoption of this technology solution enables the realization of high-voltage full SiC without SBD (Full-SiCw/oD), which does not show bipolar degradation and possesses sufficiently high gate oxide reliability [7, 8]. Figure 3 details the mechanism for bipolar degradation and an example of a degraded SiC-MOS. Triangle-shaped SFs are observed, and the electron current paths are supposed to be blocked by SFs. This behaviour causes an increase in $\mathsf{V}_{\mathsf{DS}(\mathsf{on})}$ from its initial value as the device ages. Figure 4 provides a test flowchart to eliminate the chips that have the potential to reveal bipolar degradation during field operation. The degradation quantity is evaluated by Δ Von, which is the difference in the forward on-voltage before and after the current conduction through the body diode over time [8]. Using this methodology, Hitachi have realized a 3.3 kV full SiC by eliminating the SBD, and thus enabling us to expand the active area of SiC MOSFETs. Increasing the active area has a direct correlation with the rated current which can be increased to as high as 800 A, versus the 1st-generation 450 A, using the same package platform of nHPD2 [7].

However, the presence of SiC SBD represents great advantages in other circuit configurations. Hitachi have added two chopper configurations: P-type (MSL800FS33PLT), with the MOSFET at the top arm and the SBD at the bottom arm, and N-type (MSL800FS33NLT) with the opposite arrangement [9], in addition to the dual configuration. These full-SiC chopper modules are aimed to apply in several circuit topologies such as a 3-level converter, break chopper and boost converter as detailed in Figure 5. Just to clarify it should be mentioned that the red part in Figure 5 represents MSL800FS33PLT, and the blue part shows MSL800FS33NLT. In this article we intend to focus on the 2-level inverter and use this topology to exhibit the results.



(a) Mechanism of bipolar degredation SF: Stacking faults, BPD: Basal plane dislocation

Figure 3:

(b) An example of degraded SiC-MOS

Bipolar operation in SiC may cause SF expansion from BPDs [7].



Figure 4: Sequence of bipolar degradation screening process for SiC MOSFETs.



Figure 5: Example applications of the full SiC chopper module. Red: MSL800FS33PLT, Blue: MSL800FS33NLT. (a) one phase of a 3-level converter, (b) a break chopper in a 2-level traction converter, and (c) a boost converter.

Introduction of Copper sintering enhances output current Copper (Cu) possesses a substantially higher melting point than that of conventional solder materials. By introducing Cu as a bonding material, the T_{vi}(op) of 3.3 kV devices can be enhanced, from the current 150°C, to 175°C, and this enhancement enables a 25 % higher maximum available current (rated 1000 A) [10]. As shown in Table 1, the material properties of conventional solder, Silver (Ag), and Cu are compared. Ag and Cu are used as sintering materials, not only for their melting points but also the values of their thermal conductivity and yield stress, which are considerably greater than those of conventional solder. From a cost perspective Cu sintering is more viable than Ag sintering. For semiconductor metallization purposes, we get more effective bonding from Cu sintering. Moreover, the pressure force required for Cu sintering is significantly less than that for Ag sintering. Taking all these advantages into account Cu sintering is expected to enhance the product value substantially more than the corresponding increase in product cost with Ag sintering. Figure 6 shows cross-sectional scanning electron microscopy (SEM) images for different layers. The data confirm that metalized SiC and the Cu electrode on the insulating substrate are bonded properly by Cu sintering. Figure 7 shows switching waveforms rated at 1000 A, 175°C for the nHPD2 package platform, which is named MSM1000GS33ALT-where "S" indicates

full SiC, and "G" indicates Cu sintering. Despite more than double the rated current as shown in Figure 7 (d) for the rated package platform, smooth waveforms and low switching losses are confirmed.

	Conventional Solder	Sintered Silver	Sintered Copper
Thermal conductivity (W/(m.k))	24	427	398
Melting point (°C)	280	1085	
CTE (ppm/K)	17	19.7	16.6
Yield stress (MPa)	59	262	310
Electrode material to be bonded	Cu,Ni	Ag,Au	Cu,Ni
Material cost	Low	High	Low

Table 1: Comparison of material properties of conventional solder, Ag sintering, and Cu sintering.



Figure 6: Cross-sectional SEM images of the Cu sintering layer.



Figure 7: Switching waveforms of MSM1000GS33ALT. (a) turn-on, (b) turn-off, (c) reverse recovery, (d) RBSOA, (e) Short circuit (Type 1).

In order to evaluate the output current from the inverter operation environment, we repeated the simulation as shown in Figure 2 for Full-SiCw/oD with conventional solder (MSM800FS33ALT) and Cu-sintered Full-SiCw/oD (MSM1000GS33ALT). The results are overlayed on the same plot as shown in Figure 2 in order to have a direct comparison as seen in Figure 8. Unlike Hybrid or *Full-SiCwSBD*, the maximum available output current for positive and negative are overlapped, and the simulated output currents can be fully achieved in the rated current. The maximum available output current of MSM1000G-S33ALT is 2.3 times that of Si+Si configuration at a carrier frequency of 1000 Hz, which increases to about **4 times** at 2000 Hz. These increased performance gains are considerably higher than the ones we achieve using the state of art standard product.



Figure 8: Full SiC w/o SBD with conventional solder and with Cu sintering added on Figure 2.

Product value in considering product lifetime for a traction converter

The discussion up to now has assumed that the maximum available current is defined at the maximum junction temperature while including a reasonable safety margin (here, 15K was used). However, when the actual maximum current is defined in the field operation, the temperature cycling during actual operation must be taken into consideration. SiC is a hard material, which exhibits a Young's modulus thrice that of Si. Therefore, for the power cycle test under same ΔTj and Tj(max) conditions, it was reported that SiC devices show only



Figure 9: Lifetime estimation flowchart for the mission profile analysis.

one-third the durability of Si devices [11, 12]. On the other hand, SiC devices with Cu sintering present a power cycle durability 20 times that of the same semiconductor devices with conventional solder [12]. Considering these effects in addition to the effects of total loss reduction by using SiC, the following discussion will reveal the real values of each technology in an actual inverter operation. Herein, as an example, we used the mission profile of METRO, and the output current at which the estimated product lifetime reaches the defined period (30 years, F=1 %).

Figure 9 shows a flowchart of the mission profile analysis. Input data are (a) the inverter operation pattern (output current, voltage of the filter capacitor, and carrier frequency), and (b) the loss curve with temperature dependence (from the product data sheet). Based on the input data we arrive at (c) The transient power dissipation. From (c) and (d), the thermal impedance curve, junction temperature and case temperature can be estimated as shown in (e). Then, (e) is feedbacked into (c) the power dissipation calculation. The temperature swing for the whole mission profile can be calculated (e). Using the Rainflow method, the parameters used in the lifetime calculation such as ΔT j, Tj(max), and ton can be derived. Based on the parameters derived we use the linear damage rule and modified Coffin-Manson rule, to estimate the lifetime.



Figure 10: Dependence of the estimated lifetimes of the METRO mission profile on the maximum output current.

Si-IGBT (MBM450FS33F), Full-SiCw/oD (MSM800FS33ALT), Full SiC w/o SBD with Cu sintered (MSM1000GS33ALT).

Figure 10 shows the dependence of the estimated lifetime for the METRO mission profile on the maximum output current for Si+Si (MBM450FS33F), Full-SiCw/oD (MSM800FS33ALT), Full-SiCw/oD Cu-sintered (MSM1000GS33ALT). As there is an increase in output current, the power dissipation from the power module increases (ΔT_{j} , Δ Tc, Tj(max), and Tc(max) increase). Consequently, the estimated lifetime decreases. Therefore, the relations become as shown by the lower-right curves. In the case of Si+Si (MBM450FS33F) at 660Hz maximum, increasing the output current by 1.33 times, the estimated lifetime decreases to one-fourth the value as highlighted by label (1). From another perspective we can safely assume that if by increasing the lifetime 4 times, the product value enhances to 1.33 times. Replacing Si with SiC, we can increase the maximum output current from 300 A rms to 480 Arms for a lifetime of 10 years at 1 % failure as pointed by label (2). This increase (approx. 1.6) achieved in maximum output current values represent the same ratio as that of the rated current increase achieved (450 A to 800 A which 1.7). Furthermore, by adopting Cu sintering, the power cycle test results show a durability 20 times that achieved with conventional solder. According to the mission profile analysis, the lower Tj(max) dependence and ton dependence result in a significantly higher operation lifetime of 40 times marked by label 3. Comparing SiC with conventional solder and with Cu sintering for 10 years with a 1 % failure rate, the maximum output current increases from 480 Arms to 680 Arms as shown by label \circledast . This increased ratio is 1.4, which is substantially higher than the ratio of the rated currents determined from the results of the output current estimation limited by the Tj(max) which was observed to be about 1.3.

Increasing the carrier frequency makes it possible to reduce the motor current ripple, which results in a reduction in the total loss from the motor and inverter [13]. Case studies increasing the carrier frequency by 3 times are shown with dotted curves in Figure 10 (a), and the dependences of the maximum available output current fulfilling 10 years at 1% failure on carrier frequency are shown in Figure 10 (b). It can be clearly seen that Si+Si configuration shows a drastic decrease of 60% at a 3 times-higher carrier frequency for maximum output current; however, Full-SiCw/oD decreases by only 25%. The current rating capability for the same product at a 3 times-higher carrier frequency is as high as factor of 6 times. We aim to have the samples available soon for the SiC version of nHPD2 with Cu sintering.

Summary

Enabling lifetime enhancement has been a lifetime's challenge for rail traction inverters. HITACHI's development in this application area has always been to be at the forefront to challenge existing boundaries. Keeping the vision alive we have presented our next generation of low inductance package with SiC technology. In order to take full advantage of wide bandgap technology ensuring a low inductance power module package is essential. We have highlighted the benefits of this package in SiC technology. While demonstrating the power rating enhancement of nHPD2 package in SiC technology we have also exhibited significant lifetime improvements by introducing Cu sintering. Results presented here showed an improved lifetime of 40 times for the same output current with Cu sintering.

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Why are Ultra-Low On-Resistance SiC FETs Hot? So Your Systems Can Run Cool!

Power semiconductor switches are typically used in circuits where reducing losses during current conduction without aggravating switching losses is of great benefit. In various circuit protection applications where the devices must carry current continuously, lower losses in the conduction state are beneficial for keeping system efficiencies high and waste heat generation at a minimum.

By Anup Bhalla, V.P. Engineering, UnitedSiC

Various types of robustness criteria must also be met for power switches to be used with confidence in these applications. In this article, we will examine state of the art low resistance power semiconductor switches, their key characteristics and application benefits. These switches were developed by United-SiC, using a stacked cascode technology, where a specially designed Si low voltage (LV) MOSFET with under 1mohm resistance, is stacked atop a 650-1200V normally-on SiC JFET with under 10mohm resistance. The composite device is referred to as a SiC FET and can be driven like standard silicon devices, but offers many advantages when compared to Silicon IGBTs, Si MOSFETs and SIC MOSFETs.

What is a stacked cascode?

Normally-on SiC JFETs have lower on-resistances per unit chip area than other available power transistors including SiC MOSFETs, Silicon MOSFETs and GaN HEMTs. When a low voltage (LV) MOSFET is stacked on the JFET as shown in figure 1a, to implement the cascode structure of figure 1b, a low resistance normally-off switch is formed. This is referred to as the stack cascode. Its resistance is the sum of the LV MOSFET and SiC JFET resistance, which can be 5-20% higher than the JFET resistance depending on the choice of MOSFET and JFET being combined.



Figure 1: (a) Stack cascode using a low voltage Silicon MOSFET stacked on top of the source pad of a high voltage Normally-on SiC JFET. (b) The final circuit configuration of the cascaded SiC FET.

Figure 2 shows the dimensions of the 8.6mohm, 1200V chip stack UF3SC120009. Since the LV MOSFET is pre-stacked on the JFET before assembly, the composite device is compatible with standard assembly die attach and wire-bonding equipment. It therefore makes sense that this device is suitable for use in power modules and is also available in the TO247-4L package (part name UF3SC120009K4S).

Table 1 shows a listing of parameters of the low $R_{DS(ON)}$ series of SiC FETs recently launched by UnitedSiC. Note that in the TO247 package, the current rating of the two lowest resistance devices are bond wire and lead limited.

On-State and thermal characteristics

While details of the device characteristics are available in the product datasheets, it

is instructive to review a few key features. The gate of the device has protection ESD diodes, that breakdown at +/-26V. The Si MOSFET provides a +/-20V rating, a 5V Vth, and does not suffer from any hysteresis or instabilities encountered with a traditional SiC MOSFET. It can be driven with gate voltages compatible with existing SiC MOSFETs, Si MOSFETs or IGBTs. There are no restrictions on use of negative gate bias, although given the 5V Vth, most applications can be accomplished with a simple 0 to 12V gate drive. The SiC FET $R_{DS(ON)}$ has a positive temperature coefficient, as shown in Table 1 and Figure 3a, which is useful given that many applications require paralleling of these devices.

Figure 3a shows that the ${\sf R}_{DS(ON)}$ increase of the 650V UF3SC065007K4S is far below that

Device Packag	Package	VDB(MAX)	6(100C)	RTHUC(max)	Rosion (25C)	Rosion (125C)	Rosion (175C)	Coss(ER) 800V	Eon	Eorr	Switching
	I denage	(V)	(A)	(C/W)	mohm	mohm	mohm	pF	mJ	mJ	Conditions
UF3SC120009K4S	T0247-4L	1200	120	0.19	8.6	13.3	18.2	395	3.5	0.7	100A, 800V HB 150C
UF3SC120016K4S	TO247-4L	1200	77	0.29	16	24.8	33	243	2.82	0.15	80A, 800V HB 150C
UF3SC120016K3S	TO247-3L	1200	77	0.29	16	24.8	33	243	3.35	0.67	80A, 800V* HB 150C
LE3SC065007K4S	TO247-41	650	120	0.19	67	87	11	856	1.08	0.1	80A 400V HB 150C

Table 1: Performance parameters of the low R_{DS} SiC FETs added to the TO247 portfolio. The 120A limit for the lowest RDS devices are wire limited. *Includes a 50hm 680pF snubber.

seen with Silicon Superjunction MOSFETs. It is clear that conduction loss at 125-150C can be 2.5X to 4X lower than even the best available Superjunction Silicon MOSFETs. When comparing 1200V devices to SiC MOSFETs, the rate of $R_{DS(ON)}$ increase with temperature is quite comparable up to 125-150C for parts with similar $R_{DS(ON)}$ (at 25C). It is also clear from figure 3 (right side chart) that the UF3SC120009K4S is the lowest $R_{DS(ON)}$ FET available in TO-247 at all temperatures by a wide margin.

The third quadrant characteristics in the conduction state of SiC FETs is better than SiC MOSFETs, since the drop amounts to the Si junction drop of 0.7V with the JFET $R_{DS(ON)}$ in series. Typical third quadrant characteristics are shown in figure 3b below.

The low V_F is accompanied by excellent low Q_{RR} values (e.g. 1200-1300nC for UF3SC120009K4S and 850nC for UF3SC065007K4S).



The low R_{DS(ON)} series all employ Ag sinter technology to provide the best thermal performance, as shown in Table 1 (max R_{THJC} column). In addition, it helps that both the MOSFET and SiC JFET are thinned, and that SiC has a thermal conductivity (3.7W/ cm-K) comparable to Copper (3.85W/cm-K). The T_{JMAX} rating of these devices is 175C, but they can be operated without thermal runaway at T_J >200C, since the MOSFET V_{TH} stays over 3V and its leakage is low as shown by the characteristics in figure 2.

On-resistance vs. temperature comparison 650V 45 40 35 30 25 20 15 8 UF3SC065007K4S 6.7 8.8 9.7 11 34 Superjunction A Superjunction B 40 23.4

in both hard and soft-switched circuits, and in particular, quite well suited for use in EV inverters. The body diode recovery characteristics of the SiC FET are excellent, which can be seen from the half-bridge switching waveforms in figure 4a.

Table 1 shows the low switching losses for

larger than $\mathsf{E}_{\mathsf{OFF}}$, which is true of most WBG

devices. These switches are therefore useful

the SiC FETs taken from the datasheets.

 $\rm E_{ON}$ and $\rm E_{OFF}$ are nearly temperature independent and quite low. $\rm E_{ON}$ is generally

Switching behavior









Figure 3b: The third quadrant (freewheeling mode) on-state characteristics (left), and Q_{RR} (right) vs temperature for the UF3SC120009K4S. Note the low conduction drop at V_{GS} =0,-5V of 1.65V at 100A along with a low Q_{RR} of 1200-1300nC nearly independent of temperature.



Figure 2: Dimensions of the 8.6m, 1200V SiC FET. The device in yellow is the SiC JFET, and the LV MOSFET in blue stacked on it. The devices are rated at 175C for continuous operation but the on-state and blocking characteristics of this device show that operation at 200C is possible to handle overstress conditions safely without thermal runaway.

Here a small RC snubber is included to reduce the turn-off voltage overshoot, which is necessary when driving 100A through a single TO247-4L device. The low voltage MOSFET contributes about 100nC, largely from its $\mathrm{C}_{\mathrm{OSS}},$ and the rest of the observed $\mathsf{Q}_{\mathsf{R}\mathsf{R}}$ comes from the $\mathsf{Q}_{\mathsf{OSS}}$ of the SiC JFET output capacitance. The measured Q_{RR} changes very little with temperature (figure 3b) because the LV MOSFET has very little stored charge, with most of the observed \mathbf{Q}_{RR} relating to the charging of device capacitances. At 650V, this value is 850nC for UF3SC065007K4S, which is a key advantage over any Superjunction MOSFET. Superjunction MOSFETs have >10-50X higher Q_{RR}, and have dV/dt limitations under hard recovery.

Since the normal switching dV/dts of 20-50V/ ns may be too fast for some inverter applications, Figure 4b shows one of several techniques used to achieve a low dV/dt during both turn-on and turn-off (90%/10% dV/dt_on =5.7V/ns, dV/dt_off= 4.1V/ns shown). Just using R_G values to achieve these low dV/dts can result in excessive delay time, therefore, one can use an external C_{GD} capacitor in addition to the R_G to achieve the target dV/dt.

Behavior in avalanche and short circuit

Figure 5 shows the typical avalanche behavior of the UF3SC120009K4S in two regimes. In the low current, high inductance regime the devices can handle >5.5J and are rated at 550mJ. Interestingly, under shorter inductive spikes, the peak avalanche current handling of the UF3SC120009K4S exceeds 200A. This is due to the unique operation of the SiC FET, where the JFET gets self-biased into the active mode to sink the avalanche current safely.



Figure 6: Typical Short Circuit test waveform for the UF3SC120009K4S. The peak current of 1200A is set by the SiC JFET, and current drops rapidly due to self-heating. The data is taken with V_{DS} =600V, T_{START} =25C.



Figure 4a: Half-bridge switching waveforms on the UnitedSiC double-pulse demo board. $R_{GON}=R_{GOFF}=5$ ohm, and a 680pF, 50hm RC snubber across each device is applied.



Figure 4b: A method to achieve low dV/dt waveforms for motor drive applications. Switching at 75A/800V, with 33 Ω RG and 68pF external CGD capacitor. Half-bridge switching waveforms measured on the UnitedSiC double-pulse demo board.



Figure 5: Typical avalanche behavior of the UF3SC120009K4S at low current, high inductance (left), and high current, low inductance (right).



Figure 7: Two UF3SC120009K4S devices switched in parallel at 60A each (total 120A) with VGS=+15/-5V, using a 15ohm RG on each gate and 1ohm in the gate return path. Excellent sharing is achieved under high speed switching conditions.


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Figure 6 shows a typical short circuit test waveform. The peak short circuit current is 1200A, and the current drops rapidly due to self-heating of the JFET, given that the JFET sets this peak short circuit current. SiC FETs do not degrade under repetitive short circuits, which is a strength derived from the intrinsic robustness of the SiC JFET. The electrothermal stress on the LV MOSFET during such a short circuit event is negligible.

Parallel operation of SiC FETs

Figure 7 shows the typical behavior of SiC FETs when paralleled. The on-state currents balance due to the positive temperature coefficient of $R_{DS(ON)}$. The main reason for the current balancing during switching is that the switching behavior is actually controlled by the SiC JFET, and not the LV MOSFET. Since the SiC JFET V_{TH} does not decrease with temperature, there is no tendency for a V_{TH} imbalance to lead to one switch turning on faster and turning off slower. It also helps that the body diode has a positive V_{SD} temperature coefficient for most of its operating currents, and little or no temperature dependence to its Q_{RR} . It is important to note that as with all Kelvin source devices, it is important to add a resistance in each gate return path.

Applications: Low R_{DS(ON)} SiC FETs in EV inverters

Given these desirable characteristics, EV inverters are a natural fit for these low $R_{DS(ON)}$ switches. While power modules are often preferred for EV inverter modules, these devices facilitate fairly low cost constructions of EV inverters. Table 2 shows the estimated losses using UF3SC120009K4S versus a state of the art IGBT module-based solution for an EV inverter. The solution using 6x paralleled units per switch can drop the operating losses at 200KW output by a factor of 3, which is very beneficial both for vehicle range, battery capacity, and for reducing the cooling burden for the inverter. Alternatively, these switches can be used to increase the switching frequency, which can help reduce the inverter current ripple, and improve motor efficiency and life. It also makes these switches a great choice for inverters targeted at high RPM motors.

Applications: Fast chargers

Fast chargers for EVs operating at 350KW have to deliver a current of 875A into 400V battery, or half that at 800V. A typical charger circuit may use SiC diodes on the secondary of a high frequency transformer to rectify the voltage being delivered to the batteries. Using SiC FETs as synchronous rectifiers can cut these losses by at least a factor of 2. Figure 8 shows the conduction characteristics if a 100A SiC JBS diode compared to the UF3SC065007K4S. If each device in a highpowered module were being used at 100A, at say a 50% duty cycle, the diode would have a 2V drop at 125C and loss of 100W, while the SiC Fet could be used to get down to a 0.9V drop at 125C, leading to just 45W loss per FET, representing a 2X improvement.



Figure 8: Synchronous rectification at high currents with UF-3SC065007K4S. One can save a lot of wasted heat compared to the use of SiC JBS diodes. Now the converter can also be bi-directional.

Given the excellent conduction and switching losses, these devices offer peak efficiency in the standard Active front end (PFC stage) and DC-DC (Phase shift full bridge/LLC) primary stage as well. Users can reduce the number of parallel switches, simplify assembly, and even push individual charger sections to go from 15KW to 30-50KW. The UF3SC065007K4S can allow users to push the Vienna rectifier to new power levels with discrete devices, or the 1200V devices can provide a path to an equally efficient simplified two-level architecture.

Applications: PV Inverters, Welding and UPS circuits

Given the excellent combination of conduction and switching losses, these devices can be used quite effectively in high performance 2-level, NPC and TNPC circuits to maximize inverter efficiency, and push the limits of the power levels that can be handled with power discretes. The simplicity of the SiC FET gate drive is another important factor in containing costs.

Figure 9 compares the calculated efficiency as limited by semiconductor power losses in a 60kVA, 480 VAC inverter at frequencies of 12.5kHz, 25kHz and 50kHz, operating with a bus voltage of 800V. The 2-level solution uses just 1x UF3SC120009K4S per switch position, and therefor needs just 6 transistors and gate drives. The TNPC uses 2X UF3SC120009K4S and 2X UF3SC065007K4S per phase, while the NPC case uses 4X UF3SC065007K4S per phase. The TNPC and NPC options use 12 transistors and 12 gate drives but deliver >99% efficiency even at 50kHz. Considerable cost savings can be achieved compared to module-based approaches.

Voltage	Dealer Date	China (Dasha)	Bus			Power Output					
Class Device Type	Chips/Switch	Voltage	Frequency	Loss Type	50KW	100KW	150KW	200KW	250KW	300KW	
	A REAL PROPERTY AND A REAL		and the start start		Pconduction (W)	193	440	742	1097		
1200	ICOT Diada	100 A VA analy	800 V	8kHz	Pswitching (W)	823	1191	1559	1927		
1200	IGB1+Diode	100A X4 each			Ptotal (W)	1016	1631	2301	3024		
					Semi Efficiency	97.97%	98.37%	98.47%	98.49%		
		UF3SC120009K4S X 4			Pconduction (W)	67	270	608	1080		
1200	CIC LET		800V	01411-	Pswitching (W)	185	218	261 313	313		
1200	SICFEI			SkHz	Ptotal (W)	252	488	869	1393	-	
					Semi Efficiency	99.50%	99.51%	99.42%	99.30%		
Q		UF3SC120009K4S X 6 80		8kHz	Pconduction (W)	45	180	405	720	1127	1621
					Pswitching (W)	265	293	327	368	415	469
1200	SIC PET		800 V		Ptotal (W)	310	473	732	1088	1542	2090
					Semi Efficiency	99.38%	99.53%	99.51%	99.46%	99.23%	98.96%
					Pconduction (W)	67	270	608	1080		
					Pswitching (W)	370	436	521	625		
1200	SICFET	UF35C120009K4S X 4	800V	TOKHZ	Ptotal (W)	437	706	1129	1705		
				Semi Efficiency	99.13%	99.29%	99.25%	99.15%			

Table 2: Power loss comparison of a state-of-the-art IGBT based 2-level EV inverter with various Low R_{DS(ON)} SiC FET options. At 200KW output, loss reduction by nearly 3X is possible.

Applications: Solid state circuit breakers

UnitedSiC as demonstrated a 2mohm, 1200V SOT227 switch using six of the UF3SC120009 chips in parallel, targeted at high current solid-state power controllers and circuit breaker applications. However, at lower currents, these low $\mathsf{R}_{\mathsf{DS}(\mathsf{ON})}\,$ FETs can be used in single or paralleled form to perform these functions. While a simple load switch requires nothing other than low conduction resistance and good thermal properties, some applications may require more. Consider the use of this device in linear mode, to form and electronic load. In this mode, especially at high voltages like 600-1200V, the JFET handles most of the power loss. Since its V_{TH} does not drop with temperature, it does not have a tendency to form hot spots within the die and can therefore be used stably in these conditions. Figure 10 shows very slow turn-off transitions stably performed using UF3SC120009K4S with large Rgoff resistors. Slow turn-on and turn-off transitions are needed in solid state power controllers to minimize voltage spikes when switching into highly inductive lines





Figure 9: Loss evaluation for a 60KVA, 480VAC Solar inverter with 800V DC link at 3 operating frequencies for a 2-level, NPC and TNPC topology. The efficiency only accounts for power semiconductor losses. This power level is usually accomplished with power modules but can now be done with UnitedSiC discrete devices.



Figure 10: Managing slow switching transitions with the UF-3SC120009K4S for power controllers/ load switches. Resistive load RL = 9.4W, VDD = 800V, Tj = 25° C, DUT switch with: VGS = -5V/15V.

Conclusion

Designers will find the availability of such extremely low $R_{DS(ON)}$ devices in the familiar TO247-4L package with excellent switching losses of great value in building higher powered inverters, charger units and solid-state circuit breakers. Design is further simplified by the high V_{TH} and compatibility with Silicon and SiC gate drive voltage levels. The devices are all inherently robust and capable of parallel operation, which allows the designer to use these devices instead of power modules.

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Solving the Power Density Challenge

How innovation in power management enable artificial intelligence in hyperscale datacenters

Artificial intelligence (AI), smart cities, and autonomous driving are only a couple of megatrends that impact mankind and transform our way of living. They also pose some tough challenges to current state-of-the-art technologies in many related disciplines.

By Bastian Lang, Product Marketing Manager, Dr. Roberto Rizzolatti, System Innovation Engineer and Christian Rainer, System Innovation Engineer at Infineon Technologies

The Challenge

One of the biggest bottlenecks in enabling AI and keeping up with the calculation and storage needs in the cloud is power management. More specifically, the power density of the power converters used to fuel the processors and ASICs in the system.

The "Open Compute Project" (OCP) attempts to address these challenges by defining new standards in the power architecture, moving from the traditional 12 V intermediate bus voltage up to 48 V. This significantly reduces transmission losses and enables a more efficient way to transfer power to the payload (i.e., AI ASIC / GPU / CPU or SOC). The power levels of AI accelerator modules are already exceeding 750 W with currents as high as 1000 A (@ 0.75 V core voltage). When looking at as many as eight of those modules on one mainboard, the power ratings and thermal management efforts become mind-boggling.

Current state-of-the-art

With the introduction of the 48 V power-delivery architecture, efficiency improvements in the power conversion process are becoming vital. A two-stage conversion is commonly adopted to satisfy the requirements for high voltage ratios with challenging transient requirements. LLC resonant converters are widely used as intermediate bus converters (IBCs) because of zero-voltage switching (ZVS) at the primary 48 V side and zero-current switching (ZCS) on the secondary 12 V side. If isolation is not required, a conversion based



Figure 1: A general OAM board from Infineon

on switched-capacitor converters (ZSCs) can be adapted to further improve performance and increase power density.

For the new open compute accelerator module (OAM), depicted in Figure 1, power density is a key parameter and the main challenge for the new 48 V power-delivery architecture. The available footprint area for the IBC and multiphase buck system is visualized in Figure 2.

To meet the footprint requirements, high switching frequency operation is needed both in the first and second stages. However, highfrequency operation, especially on the VRM stage (i.e., 1.5...2 MHz), leads to higher losses (i.e., switching, gate-driving, and conduction losses).

Reducing the input voltage on the VRM stage down to 6 V enables a reduction of the footprint size while maintaining high efficiency. For higher conversion ratios, an IBC based on a switched capacitor topology becomes too complex and bulky in terms of floating driver requirements and the number of switches and ceramic capacitors.



Figure 2: The OAM dimensions and footprint requirements for a 48 V power-delivery system

To implement a high step-down ratio IBC, a transformer-based topology such as a full-bridge LLC resonant converter is widely used regardless of galvanic isolation requirement. While there are many advantages to using a transformer-based topology, there are also some drawbacks.

For example, the step-down ratio is determined by the turn winding ratio between the primary side and secondary side and in an LLC centertapped resonant converter the utilization of the copper is not optimized. To overcome the limitations of I²R losses in the transformer, Infineon has introduced a hybrid switched-capacitor (HSC) converter that combines the benefits of switched capacitor converters and the high step down ratio capability of a magnetic device. By transferring the energy through capacitors and a magnetic device, the efficiency and power density can be improved significantly. This enables the required power density for the OAM.

HSC converter

In resonant converters like the LLC, the switching frequency needs to be close to the LC resonance for soft switching. Moreover, the entire energy is transferred through the transformer, increasing the overall losses. A converter topology whose efficiency varies heavily with the component mismatch is not viable for mass production without extra compensation efforts. To overcome these issues a novel approach based on the HSC topology dual-phase resonant converter is proposed by Infineon. As illustrated in Figure 3 the HSC is formed by 6 MOSFETs divided into two legs, connected through two flying capacitors and a magnetic device called a multi-tapped autotransformer (MTA). The MTA is formed out of 4 windings connected in series sharing the same magnetic core. High-frequency operation is enabled by ZVS operation with the magnetizing inductance of the MTA.



Figure 3: HSC converter topology

The HSC provides an unregulated voltage rail which depends on the turn ratio between N_1 and N_2 . The topology is driven by two symmetrical PWMs: H (i.e., Q_1 , Q_3 and Q_5 are ON with Q_2 , Q_4 and Q_6 OFF) and *L* (i.e., Q_1 , Q_3 and Q_5 are OFF with Q_2 , Q_4 and Q_6 ON). An introduced dead-time between the states enables load-independent ZVS operation. The HSC can run above- and below-resonant frequency without influencing the ZVS operation. Therefore, the overall system performance can be kept at a high level regardless of component tolerances.

One of the key enablers for high efficiency and high power density of the HSC is the use of low-voltage rated MOSFETs with better figureof-merits (FOMs). For example, in an 8:1 configuration running from a 48 V rail, 25 V-rated MOSFETs for Q_3 and Q_6 can be used.

The Source-Down concept, pushing the envelope in power density

Addressing the power density challenges requires innovation at the component level with advancements in resonant topologies. With the introduction of Infineon's Source-Down package technology, the IQE006NE2LM5 further enhances electrical and thermal performance, enabling the power density needed in modern datacenter applications. The main benefits of the innovative package include:

- 30 percent lower RDS(on), decreasing I²R losses
- Lower package-related parasitics, reducing the FOM and leading to lower switching losses

- Lower Rthjc, optimizing the distribution of the generated heat from the package
- The thermal pad is located on the source pin, thus enables optimized layouts where the large GND area can be utilized as a heatsink



Figure 4: The thermal behavior of the HSC at 450 W from 48 V input at T_{amb} = 24°C and v = 3.3 m/s:

a) with BSZ011NE2LS5I, b) with IQE006NE2LM5

To compare the performance benefits, two versions of an 8:1 HSC was built, using today's standard Drain-Down device (BSZ011NE2LS5I) on one board and the new Source-Down device (IQE006NE2LM5) on the other. Figure 4 compares the thermal performance of the devices. The traditional package shows a hot-spot (Figure 4 a) that is eliminated with the use of the new source-down package (Figure 4 b). The surface temperature of the MOSFET is significantly improved, showing a 9°C difference compared to the Drain-Down device. Figure 5 illustrates the efficiency comparison (including auxiliary losses). The higher efficiency of the system featuring the new source-down device leads to a significant increase in power density as well.



Figure 5: The HSC converter efficiency from 48 V to 6 V, including auxiliary losses, with BSZ011NE2LS5I (in blue) and with IQE006NE2LM5 (in red) at $T_{amb} = 24^{\circ}$ C and v = 3.3 m/s

From all of the above-mentioned benefits and performance measures, one can easily conclude that this novel solution, the Source-Down packaging technology, is a key enabler for delivering the required power density to feed the power-hungry megatrends like artificial intelligence.

www.infineon.com/PQFN-3-Source-Down

Getting the Most Out of a DC/DC Converter

Small isolated DC/DC converter modules have been used for decades to efficiently match the supply voltage requirement of a load to the available power rail, to provide low-power auxiliary voltages such as a negative rail for an analog interface, for safety isolation or just to break ground loops for a particularly sensitive area of circuitry.

By Steve Roberts, Innovations Manager, RECOM and Axel Stangl, Product Sales Manager, RUTRONIK

Modular DC/DC converters have evolved for higher power density Small isolated DC/DC converter modules have been used for decades to efficiently match the supply voltage requirement of a load to the available power rail, to provide low-power auxiliary voltages such as a negative rail for an analog interface, for safety isolation or just to break ground loops for a particularly sensitive area of circuitry. As modules, through-hole single in-line pins (SIP) versions have been popular and the earliest boasted around a Watt of unregulated power output in a compact SIP-7 format, plenty enough power for many of the applications mentioned. Over the years, power density has steadily increased with unregulated 3W now available in the even smaller SIP-4 format (Figure 1).



Figure 1: Unregulated and regulated DC/DC power density increase from 1990s (left) to today

Fully regulated parts soon appeared, initially using a self-oscillating, variable frequency flyback circuit for minimal component count, but the latest versions are typically fixed frequency IC-based for optimum efficiency over a wider load range, giving high power density, 4:1 input range and features such as output trim and ON/OFF control. 2W in a DIP24 package was the initial benchmark, but soon SIP7 and SIP8 2W, 3W and 6W versions appeared and now the 12W benchmark has been reached (Figure 1). As power levels have increased, the modules are increasingly used for powering entire sub-systems and even whole products, rather than being used as just an auxiliary power supply. As the main power conversion stage, agency-rated isolation becomes more important and as SIP7 or SIP8 packages allow meaningful creepage and clearance between input and output pins, so a trend has been to increase power from these packages rather than to shrink module size keeping the same power.

New construction techniques enable higher power density without derating

As vendors have introduced more SIP8 DC/DC modules with improved power density, some have resorted to optimistic claims just to appear to keep up with the industry leaders. The headline power may only be available with heavy derating – for example, a nominal 9W part may well be able to deliver full power if case temperature is held to an impractically low temperature, if the load duty cycle is low or if significant forced air cooling is applied, but the useful power may be much less. For example, the 6W part from RECOM delivers more power at +75°C ambient with convection cooling than the nominal 9W part from the competition.

Such discrepancies, where a nominal lower power part delivers more useful power than a nominal higher power part in real-life situations, is an indication that the existing design topology has reached its limits. It may be possible to further increase the power density by using more expensive components, but a radical redesign is necessary to jump up to the next power level, for example abandoning the inefficient bobbin transformer construction and using a fully planar design. This is the approach used in the new RS12-Z series from RECOM [1]. Planar transformers use PCB tracks for the windings which is technically challenging with multilayer PCBs necessary, often with blind and buried vias. Additionally, achieving guaranteed isolation (3kVDC in the case of the RS12-Z) requires careful design of the PCB stack-up. Finally, for every input out voltage combination, a different PCB layout is required with different turns ratios, so the manufacturing process is more complex. Planar transformers do however take labour out of the assembly process and give very repeatable performance compared with traditional wire-wound transformers. Along with the improvements in efficiency, the advanced thermal management enables the full 12W output at 75°C ambient across the 4:1 input range. In this product, the heat generated in the converter is efficiently transferred to the metal case with a low thermal resistance. Tinned case tabs are used to additionally lead heat away into the host PCB.

Latest designs have added functionality

A bonus that appears with advanced IC-based converter circuits is the extra functionality available, solving some important problems. For example, as a main sub system or product power source, the converter should operate in a well-behaved way when the input supply drops, typically from a discharging battery. Regulated switched-mode converters take constant power from their input for a constant load so if the input voltage drops, current increases. If the converter continues to operate below the minimum rated input voltage, the increased Home Appliances

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current can be damaging, so an under-voltage lockout function is necessary which is built-in to many control ICs. The function also ensures that the converter output switches off cleanly at a set minimum input voltage.

Another feature available from circuits such as used in the RS12-Z product is a 'control' pin or ON/OFF function. This can be used to put the converter into a 'sleep' mode for minimum power consumption and extended battery life if used as an input supply. The function can also be used to delay or 'sequence' the converter output with other power rails. Control can be purely 'primary-side' or derived from isolated outputs via optocouplers. Figure 2, as an example, shows an arrangement of converters where DC/DC 2 is enabled after DC/DC 1 is powered with a fixed delay set by R1/C1 but DC/DC 3 is enabled only when DC/DC 2 output is within tolerance.



Figure 2: Example DC/DC converter sequencing scheme

Trim pins can have multi-functions

A trim feature is also useful to adjust a DC/DC output to compensate for external voltage drops. A typical use would be with converters paralleled for redundancy where output series diodes are inserted to prevent failure of one DC/DC affecting the other, Figure 3 for example. In this case, with Schottky diodes, each output may be trimmed up by about 0.3V via R1 and R2 so that the 'gated' supply is the correct nominal, 3.3V in this case. Note that converters are typically rated for a maximum power output so if the output is trimmed up, rated current should be reduced.



Figure 3: DC/DC outputs trimmed up to compensate for diode drops in redundant configuration

A trim pin can also typically be controlled by an external voltage allowing other functions; one example is where a power rail is needed in a production ATE system which cycles between its allowed tolerances to achieve a 'margining' function, to test resilience to power supply variations. The circuit of Figure 4 achieves this and comprises a sinewave oscillator IC1 which couples to the trim pin of a RECOM RS12-Z DC/DC converter with a set DC-offset to match the trim pin nominal voltage. VR1 controls the amplitude of the variation, IC2 sums this with a negative fixed offset producing a positive offset on the trim pin with a sinusoid superimposed.



Figure 4: Trim pin used for power rail cycling for 'margining'

With other external circuitry, the trim pin could also be used to implement a remote sense function or to control power sharing if current is sensed externally to the converters.



Figure 5: Typical DC/DC EMI filters for EN 55032 Class A and B compliance

DC/DC EMI filters should be compact

When used as the main power source for low power equipment, a DC/DC will itself be powered from an external supply and may have to meet particular EMC specifications, typically EN 55032, either Class A or Class B limits. To achieve this, particularly noisy or variable frequency converters may need additional filter components that can occupy more board space than the converter itself. Typical filter circuits are shown in Figure 5 that enable the RECOM RS12-Z converters to meet the two limits, in this case with a combination of small electrolytic and ceramic capacitors, and low value inductors.

Modular DC/DC converters have evolved significantly since their first introduction. Power density has increased dramatically but so has functionality allowing them to be used as precision power sources for modern electronic systems. The RECOM RS12-Z series is a good example, an innovative new design suitable for nominal 12, 24 or 48V DC inputs with a range of outputs delivering a full 12W at 75°C.

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Imagine a World Without Switching Losses

AI-powered architecture unleashes decades of future silicon IGBT and SiC improvements – today

Until recently, the power conversion industry's progress in efficiency, size, weight and cost have been principally driven by improvements in semiconductor transistors. To achieve these improvements, the engineering goals for new transistors were straight-forward: increase the stand-off voltage, reduce conduction and switching losses, and reduce costs.

By Bruce T. Renouard, Pre-Switch

Billions of dollars have been spent - and continue to be spent - chasing these same goals. Today's seventh generation IGBTs and MOSFETS and third generation SiC MOSFETs and GaN FETs are vastly superior to previous generations of power devices. All of these devices are true marvels of human ingenuity.

While many different types of transistor improvements have benefited our industry, it has been the relentless reduction of transistor switching losses which has had the most impact. To reduce switching losses, the semiconductor industry focused on improving device transition speeds. The faster a device can transition between On and Off states, the smaller the overlapping current and voltage waveforms - which in turn reduces switching losses Etot (total turn-on and turn-off energy wasted across a switching cycle).

Reduced switching losses means designers can use higher switching frequencies for the same or lower loss budget. Higher switching frequencies have the follow-on benefit of reducing the amount of energy needing to be stored in the passive devices between switching cycles -thereby shrinking power converter size and costs. Reducing switching losses also reduces wasted energy and the size of the heatsink needed to dissipate the waste heat. The net results of reducing switching losses is the further improvement in power converter efficiency, size, weight and cost.

A barrier to further progress

Unfortunately, many of today's high-performance semiconductor transistor technologies are bumping into a physical barrier, limiting further switching frequencies gains and power conversion effectiveness. Faraday's law of induction is expressed as V=L di/dt. This means that the total Voltage across the power switch (the addition of the conduction voltage drop (VSAT or Id x RDS -depending on switch type) plus the transient voltage = Inductance (package parasitic and system parasitic inductance) multiplied by the Change in Current (through the device) divided by the Time duration of that change. In simple terms, what this means is that the faster a switch transitions between On and Off states, the higher the transient Voltage is generated across the device. The transition speed of today's faster switches is enough such that the internal inductance causes the devices to experience an overshoot across the device. Hence an infinitely fast turn-on time would produce an infinite voltage across the device, which would blow up the device. Additionally, since some of the parasitic inductance is

in the Emitter or Source connection, this can cause severe ringing in the gate drive circuit and cause a plethora of control problems.

Switching Results of UF3C120040K3S at 800V-39A with an RC snubber (RS = 4.7 Ω , CS = 220pF) for both high-side and low side switches



Figure 1: Switching results of fast SiC Cascode with snubber circuit to limit overshoot.

Designers need to limit the transient voltage overshoot to protect transistors. In practice, many engineers buy 'fast' transistors only to slow them down by adding large gate drive resistors (or snubbers) -which negates some or most of the efficiency gains they desired in the first place. Additionally, the fast dV/dt of these devices degrades insulation and causes differential bearing currents in electric motors and limits the distance motors can be placed from their drives. In short, transistors with fast di/dt or dV/dt are problematic and require special attention.

Elimination of switching losses

So how does our power community continue to increase efficiency, while reducing size, weight and cost despite the insurmountable Faraday challenge (V=L di/dt)? The answer, once again, is driven by human ingenuity - but this time it's focused on power architectures.

The concept of soft-switching has been around since the 70's when Deepak Divan (now with Georgia Tech) introduced temporarily separating the current and voltage wave forms to eliminate switching losses. Since then, resonant architectures have been designed to reduce switching losses for many applications - but have been limited to markets with stable loads/inputs in either DC to DC or AC to DC converters. This neglects the giant DC to AC market which is needed for e-mobility, industrial motor drive, solar and wind applications.

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DC to AC could not be soft-switched because of the challenge and complexity needed to vary the timing of a forced resonant circuit while generating a constant sine wave with varying load, input voltage, temperature and device degradation. The result has been an absence of commercial soft-switching architectures for DC to AC applications until Pre-Switch (Figure 2).

Pre-Switch, Inc. took an unconventional approach by incorporating Al into the previously developed ARCP (Auxiliary Resonant Commutated Pole) architecture (Figure 2). The ARCP (invented by R.W. De Doncker and J. P. Lyons at General Electric in 1990) was investigated by many leading power institutions only to be abandoned due to the inability to control for variabilities. Pre-Switch developed AI to sense many inputs and finely control the ARCP enabling full DC/AC and AC/ DC bi-directional soft-switching.



Figure 2: Modified ARCP showing AI sensing and control. Blue shading represents RPG (resonant power gate) additional components added. Note: Pre-Switch uses low cost IGBT's to soft-switch IGBTs, SiC MOSFETs and GaN FETs.

Pre-Switch's AI dynamically senses and adjusts the timing of a lowcost auxiliary resonant circuit called the RPG (resonant power gate) shown in figure 2. The result is a precisely timed resonant current (Figure 3) into a capacitor across the working transistor enabling zero voltage (ZVS) across the working switch. The AI processes multiple analog inputs without using an ADC IC or current sense resistors and adjusts the timing of auxiliary resonant switches on a cycle by cycle basis. The result is virtually perfect soft-switching that compensates for changes in load current, input voltage, device temperature, component degradation and manufacturing tolerances (Figures 4 and 5). Additionally, the AI adds very fast safety and protection features such as OVP, OCP and desaturation protection. The AI does not need to be trimmed in production and can be added to many other architectures.



Figure 6: IGBT value propositions of using Pre-Switching in an IGBT system.



Figure 3: Pre-Switched ARCP turn-On waveform of 1200V 35mOhm MOSFET (United SiC UJ3C120040K3s) at 800V and 40A. Resonant current (green), voltage (yellow), ARCP loss (red).



Figure 4: Pre-Switched turn-On wave form of 1200V 35mOhm MOS-FET (United SiC UJ3C120040K3s) at 800V and 40A. Note lack of overlapping current (blue) and voltage (purple) wave forms resulting in virtually no switching losses (red).



Figure 5: Pre-Switched turn-Off wave form of 1200V 35mOhm MOSFET (United SiC UJ3C120040K3s) at 800V and 40A. Note the non-overlapping current (blue) and voltage (purple) wave forms and virtually no switching losses (red).

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Pre-Switch enables multiple new design paradigms resulting from the elimination of efficiency-robbing switching losses and device overshoot. With no switching losses, the complete switching loss budget can be allocated to conduction losses – thereby reducing the size and cost of the transistors needed (Figure 6). Alternatively, the switching loss budget can be reallocated to let transistors switch at ultra-high switching frequencies -thereby reducing inverter output ripple and hence their system filter size and cost. Additionally, any combination of these new options can be used for system optimization and the architecture adjusts dV/dt to any value required at the system level.

Pre-Switch has enabled customers to build systems with switching frequencies 4X-5X faster than their hard-switched IGBT systems and 10-20X faster than their hard-switched SiC and GaN systems. In the case of a SiC-based EV inverter, increasing the Fsw from the ubiquitous 10kHz up to 100kHz or 300kHz creates a near perfect sine wave without any output filter. The result is elimination of unnecessary motor iron losses and an increased motor efficiency at low torque and low RPM. Higher switching frequencies also enable higher RPM motors that are lighter and lower cost.

In a world without switching losses, the best optimization is achieved by looking at the WHOLE SYSTEM for efficiency and cost. As an example, many EV companies have separate inverter, motor and battery teams. If Pre-Switch technology is siloed in the inverter team, they will likely want to eliminate their switching losses to save on their transistor and heat sink costs - all while producing a higher efficiency inverter (Figure 6 vertical axis). Who could fault them? But the real goal is 'battery to wheel efficiency', measured in EV range. In this case, the motor team should be asked how much more EV range could be achieved across the full drive profile if their motor was fed a pure sine wave from the inverter. To achieve a pure sine wave, design freedoms should be optimized with ultra-fast switching frequencies (Figure 6 horizontal axis) which significantly improves low torque efficiency, and hence increases EV range.



Figure 7: CleanWave200 evaluation system (200kW inverter power block, 800Vdc, 99% efficiency at 100kHz).

SiC test results explained:

The hard-switching and Pre-Switching comparisons in Table 1A were obtained by Double Pulse Tests (DPT) on Pre-Switch's Clean-Wave200 Evaluation system (figure 7) using United Silicon Carbide's UJ3C120040K3S in a 3 pin TO247 discrete package. To measure the hard-switched DPT data, all ARCP soft-switching components were removed from the same CleanWave board for the same devices. The measured hard-switched results were in excess of the manufacturers data sheet specifications so further effort was made to reduce the hard-switched results. In the process, it was discovered that the UJ3C series parts used in the CleanWave200 were optimized for soft-switching applications but not hard-switching applications. For transparency purposes, Pre-Switch added section B and C to Table 1 showing measured gains compared to other devices based on their data sheet specifications.

Additionally, the ARCP losses shown in Table 1 are conservative. This is because Pre-Switch sized the ARCP components used in the CleanWave200 for the current capability of three switches in parallel per switch location and only one switch was used in the DPT. This means that the measured ARCP losses in Table 1 (which were measured on a single switch) are over representative of the total losses and engineer would expect to see in an optimized system.

A) UJ3	Measured doub C120040K3S vs	le pulse test same device	data on Clean	Wave200. Hard (mJ) 800V, 40	switched amps, 25C
	Hard-Switched Device loss	Device loss	Pre-Switched ARCP losses	i Total losses	Measured Savings
Tum-On	2.513	0	0.218	0.218	91%
Tum-Off	1.246	0	0	0	100%
Etotal	3.759	0	0.218	0.218	94%

	Hard-Switched	Device loss	ARCP losses	Total losses	Savings vs data sheet same device
Tum-On	1.945	0	0.218	0.218	89%
Tum-Off	0.55	0	0	0	100%
Etotal	2.495	0	0.218	0.218	91%
C) Com	parison of differe	nt switch opt	imized for hard	switching (UF	3C120040K4S)
C) Com dat	parison of differe ta sheet secs to n Clea	nt switch opt neasured Pro nWave200 ()	imized for hard s-Switched dat mJ) 800V, 40 a	switching (UF a on UJ3C120 mps, 25C	3C120040K4S) 0040K3S on
C) Com dal	parison of differe a sheet secs to n Clea Hard-Switched Data sheet spec	nt switch opt neasured Pro nWave200 () Device loss	imized for hard e-Switched dat mJ) 800V, 40 a Pre-Switched ARCP losses	switching (UF a on UJ3C12(imps, 25C I Total losses	3C120040K4S) 0040K3S on Savings vs. different device data sheet
C) Com dal	parison of differe ta sheet secs to n Clea Hard-Switched Data sheet spec 1.306	nt switch opt neasured Pro nWave200 () Device loss 0	imized for hard s-Switched dat mJ) 800V, 40 a Pre-Switched ARCP losses 0.218	switching (UF a on UJ3C120 imps, 25C I Total losses 0.218	53C120040K4S) 0040K3S on Savings vs. different device data sheet 83%
C) Com dal Tum-On Tum-Off	parison of differe ta sheet secs to n Ciea Hard-Switched Data sheet spec 1.306 0.21	nt switch opt neasured Pro nWave200 (r Device loss 0 0	imized for hard s-Switched dat mJ) 800V, 40 a Pre-Switched ARCP losses 0.218 0	switching (UF a on UJ3C120 Imps, 25C I Total losses 0.218 0	53C120040K4S) 0040K3S on Savings vs. different device data sheet 83% 100%

Table 1: CleanWave200 Double Pulse Test data: A) Measured hardswitched to Pre-Switched on the same device, B) Data sheet data compared to measured Pre-Switched and C) Data sheet data on a different device compared to Pre-Switch measured data.

How to design with Pre-Switch technology

Pre-Switch is focused on supporting applications requiring >350V and power ranges >50kW. While the technology scales to smaller power converters, the company is intentionally delaying these markets.

Pre-Switch is selling the CleanWave200 evaluation system to allow customers to assess the cycle by cycle adaption of Pre-Switches Al based soft-switching and explore the benefits of higher switching frequencies in their application. The CleanWave200 represents the power block of an inverter with a PWM interface. The system bi-directionally converts 800VDC to three phase AC at power up to 200kW with a Fsw of 100kHz and 99% efficiency.

Now in its 4th year of business, Pre-Switch is also providing design services to customize the RPG (Resonant Power Gate) board needed to complement the company's 3-phase soft switching controller board called the Pre-Drive3. For customers with >100K units of the same design, Pre-Switch will bundle design services with the sale of its Pre-Flex IC.

The future is now

The power conversion world has never been more exciting -and the real power revolution is just starting. Electric cars, busses, tractors, planes, trains, boats, motorcycles, robotics, drones and many more

are barely penetrating our lives. The revolution unleashed with Pre-Switch's AI-controlled architectures, capable of soft-switching DC/ AC and AC/DC, is delivering decades of future incremental transistor innovations - today. A world without switching losses changes everything. System level benefits now extend past the lonely inverter sub system. The pure sine wave inverter output offering EVs 5-12% more range is no longer "the future". Second order benefits from dramatically higher switching frequencies are now within reach. It's time to increase motor pole counts, drive them with higher speed fundamentals, and increase their RPMs thereby increasing power density while shrinking size and cost. It's time to shrink solar inverters, wind turbines, VFD, OBCs and fast DC chargers while eliminating their cooling fans.

Think about it. A world with no switching losses is finally here. I can't wait each month for my next issue of Bodo's Power Systems to report on it all.



About the Author

Bruce Renouard is the CEO of Pre-Switch, Inc. and was the former SVP of Cree and Power Integrations. He is a world traveler, surfer, solar home geek, electric motorcycle enthusiast, land conservationist and dog-lover.

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What Makes a Good Magnetic Design?

The story of magnetics in Europe has many important characters including some who have been in the industry since the 80's. It is impossible to analyze what makes a good design without these people. I'm not referring to the researchers or the brilliant engineers, but rather the individuals who have been looking for the materials, winding the coils and repairing the winding machines.

By Dr. Jose Molina, Frenetic

People of Magnetics

A few weeks ago, I visited Josep Llano and his son, Raimon Llano, who are the owners of Prodin, a Barcelona-based company who distribute "everything" related to magnetics at high and low frequencies.

Mr. Llano worked in a winding house called Avisor for more than 20 years. After that, he left the company and founded Prodin, which provides electrical steel, ferrites and coil formers.

They started attending small manufacturing conferences in 1990 such as Matelec, where they found their first customers from different markets. During this period, the manufacturing conferences had a much greater impact than they have in the modern-day, internet era, since customers would actively look for their suppliers at these events. During the 90's, every week suppliers were delivering trucks with tons of ferrites to their European customers like Alcatel or big winding houses. They supplied more than 1 million transformer cores every month for the power supply of TVs.

As time went on, they started to include more products in their portfolio, including powder and nanocrystalline cores, varnish and even winding machines. This converted suppliers into a one-stop shop for magnetics customers. However, the story of manufacturers in Spain took a turn when relevant companies in the industry decided to move their factories to China and India. This created uncertainty within the industry, and other small manufacturers and competitors began to follow suit by moving their factories to Asia.

Due to the manufacturing process migrating to China, the minimum quantities of projects increased considerably. Josep Llano recalls that "clients who typically had orders of around 1,000 transformers per year were being rejected by these Asian manufacturers since the minimum order quantity was now 50,000 units" which left a gap in the market for small, custom companies who could now focus on low volume production. With very tight profit margins, these companies had survived due to their national clients from the Basque, Catalan and Madrid industries. For example, companies such as Indra continue to support national manufacturers which allows them to carefully control the IP rights of their designs along with delivery periods. It is worth noting that deliveries relating to a large order from a Chinese manufacturer not only have to take duties into account, which can increase the cost of a magnetic by up to 25%, but also require a delivery period of several months in some cases.

In this tough economic climate, many companies started to close down. The reduction in national orders, the specialization of the sector and the increase in complexity and competition caused hundreds of factories in Europe to shut down their operations. Josep saw this happen to dozens of his clients and in some cases he bought part of their machinery to repair it. However, not all of the sector within Europe suffered. The enormous technological capacity of Europe and it's engineers paved the way for the creation of companies with a high level of specialization in custom magnetics. For instance, in Játiva in Valencia, the company Jesiva manufactures transformers weighing hundreds of kilos. Also, magnetics from certain markets such as solar and space along with high-quality products continue to be manufactured in Europe.

Nowadays, Mr. Llano is very well-known within Spain since he and his son are not just simple distributors, they solve all problems relating to magnetics on a national scale for small and medium production levels.

Magnetic design process

In order to figure out what makes a good magnetic, let's define the magnetic design process which is divided into four main steps:

- 1. Design
- 2. Build a sample
- 3. Test
- 4. Manufacture

Classic Magnetics Process



Figure 1: Classic magnetic design process

Since each of these steps are closely correlated, it is impossible to work on any one individually. The design must consider the stock of materials and, even more importantly, it should consider the manufacturing stage. For example, you could create a highly efficient design that is impossible to manufacture. Also, the tests should consider potential risks to the manufacturing process. The curious point here is that in the classical process the manufacturing step is the only phase for which the customer pays.

However, manufacturing is the result of a large amount of complex work which involves many talented people along the way.

In the design stage we find that designers are unable to consider the majority of the existing options in the market since they don't have access to them, or because they don't have the necessary data to consider them. In this area (self-promotion warning), Frenetic has a great advantage and we have succeeded in having an enormous stock of materials and shapes, but we also have a great capacity to help those who need rapid assistance. Given that Frenetic uses AI technology, it continues learning to use new core shapes and materials and the technology is enriched by the supply of ferrites that we receive from manufacturers such as Ferroxcube. There are other names here such as Ferroxcube, or better, Óscar Perez, David Castillo, Mauro Marchesi, Marcin Krolak, etc. They have more than 100 years of experience in manufacturing and selling the ferrites created by Philips and remain one of the main players in the market today.



Figure 2: Design imposible to be manufactured

When we move from the design phase to building the sample, we realise that 50% of the problems during the construction of magnetics arise from the design phase. For example, if we take an optimistic estimation of the window and the complexity of the bobbin strategy, this may make us discard the initial design and have to return to the beginning of the process.

Once we have built the sample, next comes the step where the majority of magnetics die: the testing phase. In my opinion, this is where a good magnetic makes all the difference. Until now, the problems have been related to stock and the manufacturing instructions included in the design for an appropriate construction, which you can learn. But when you connect a magnetic to the power supply and the temperature starts to rise, it is as if it were connected to the hell itself. Who are you going to call then? Óscar Pérez from Ferroxcube? Or your managers to ask them if you can include a superfan in the OBC?

The only solution here, apart from writing a question on Ridley's Facebook group, is to use technology. That is exactly why we created Frenetic.

Even after these issues have been resolved, the process is not over. Next, we move onto the manufacturing stage, which means creating all of the necessary documents so the magnetic can be manufactured, whether for just one unit or for one million.

These instructions are key for manufacturing companies to be able to prepare a production line, which is an area I will not cover in greater detail here.

The considerations above have led me to ask myself again: 'What makes a good design?' And more importantly: 'Who can provide a good design?'

Whilst the answer to the question is highly complex, a good design should: reach the expected efficiency; have a logical price; be the specified size and comply with the expected timeline. The crucial aspects to achieve this are the engineer who defines the specs, the design process itself and the winding houses.

I believe that there is a need to work more closely with the client in order to define the right specifications and to comply with timelines. However, the most important area is to be precise in the design and to be able to manufacture samples and test them in real conditions, finally giving the specific instructions to the winding houses, and completing the whole process in days. To return to my previous question about what makes a good design, we are likely to see many different opinions about this during this year's PSMA Workshop. Some will discuss the importance of using complex mathematical models or customized core shapes. We will also learn about the direction in which the industry is heading. In this topic, Alex Gerfer from WE, has a lot of interesting points.

At Frenetic, we believe that the solution is the appliance of AI to magnetics, and we are traveling along this path. Lastly, and related to the topic of my next article, I would like to pose the following questions: Which features does a winding house need to be considered optimal? Which winding houses have the same status in the magnetics industry as Rafael Nadal in the world of tennis?

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Design Considerations for a GaN-Based High Frequency LLC Resonant Converter

This article evaluates the performance of Gallium Nitride (GaN) power transistors in comparison to Silicon Superjunction MOSFETs (Si SJMOS) and Silicon Carbide MOSFETs (SiC MOS) for the high frequency LLC resonant topology.

By Jimmy Liu, GaN Systems Inc, Canada

Introduction

With the clear trends towards higher power, smaller size, and higher efficiency, a high frequency LLC resonant converter is an attractive solution for an isolated DC/DC topology in the industry, such as a laptop adapter (>75W), 1KW-3KW datacenter Power Supply Unit (PSU), and a multi-kilowatt On Board Charger (OBC) for electric vehicles. Figure 1 shows a topology for a half bridge LLC resonant converter with switching frequency at 100KHz and 500KHz. At the higher frequency, it is obvious that the size of the passive resonant tank (e.g. transformer, resonant inductor, and resonant capacitor) are dramatically reduced, thus the power density is improved. Additionally, the selection of the power transistors (Q1 and Q2) need to be considered to trade off the efficiency and power density. GaN power transistors have established themselves in the market as a proven transistor technology, but are often not considered in soft switching applications. While using GaN in hard switching applications shows a significant improvement in efficiency, improvements on efficiency and frequency in soft-switching converters (such as LLC) can also be equally dramatic.

In this article, the benefits of commercial GaN power transistors in comparison to Si SJMOS and SiC MOS transistors are discussed for a soft-switching LLC resonant converter. The analytical approach for the transistor selection and comparison are conducted. The transistor parameters such as time related output effective capacitance (C_{o(tr)}) and turn-off energy (E_{off}), etc., are taken into consideration, which



influence the high performance achievements of an LLC converter. A 3KW 48V output LLC converter, based on GaN, Si, and SiC MOS, is also analyzed for efficiency and power density comparison.

Figure 1: The Half bridge LLC resonant converter at 100KHz and 500KHz

Primary Transistor Selection

The LLC has several benefits due to its full resonant behavior allowing soft switching turn-on over the entire range which intrinsically helps to minimize losses in both power transistors and magnetic components. In Figure 2, the LLC primary side current, ${\rm I}_{\rm Lr}$, consists of a superposition of the secondary side current, divided by the transformer turns ratio n, and the magnetizing current $\mathbf{I}_{\text{Lm}}.$ The magnetizing current does not transfer to the output but is required to discharge the parasitic output capacitance of the transistors as well as a combination of the transformer intra-winding and inter-winding capacitance, hence to achieve Zero Voltage Switching (ZVS) for transistor turn-on without switching turn-on loss. On the one hand, in order to achieve the ZVS for turn-on, the parasitic output capacitance of the transistor should be fully discharged by using this magnetizing current during each dead time. On the other hand, the magnetizing current will contribute an additional circulating loss on the primary during the dead time. Minimizing magnetizing current is thus a goal for improving an LLC converter.

The minimum dead time $t_{deadmin}$ for a half bridge LLC's ZVS achievement condition can be derived from equation (1). Here, L_m is the magnetizing inductance of the main transformer and f_s is the switching frequency. From equation (1), The transistor parameter $C_{o(tr)}$, which describes the output capacitance needed to transition the drain to source voltage passively, is a key parameter for high efficiency and high density LLC converters. The lower the value of the effective $C_{o(tr)}$, the less magnetizing current is required for a given drain to source transition time, and this allows a higher value of magnetizing inductance for the transformer and a shorter dead time, which in turn lowers the circulating losses on the primary side. Meanwhile, for a given L_m and t_{dead} , the lower value of effective $C_{o(tr)}$, the higher switching frequency f_s can be used with ZVS condition to make a higher density.

This effective capacitance $C_{o(tr)}$ can be derived from the output capacitance C_{oss} through output charge Q_{oss} , which has the relation equations of $Q_{OSS} = \int_0^{Vds} C_{OSS}(v) dv$ and $C_{o(tr)} = C_{o(tr)}/V$. Figure 3 plots the Q_{oss} with the voltage of V_{ds} . For a V_{ds} voltage transition from 400V to 0V, Si SJMOS has typically 10 times higher $C_{o(tr)}$ than GaN, and SiC has 50% higher $C_{o(tr)}$ than GaN.

Another important transistor parameter for LLC is Q_{gd} , which describes the charge required for gate to drain switching and the switching turn-off time t_{off} . These two parameters give an indication of turn-off capability and losses, and thus the maximum operating frequency and efficiency. The turn-off time t_{off} is normally not shown in a transistor datasheet, but can be estimated according to the reference book [1] with the given switching voltage and current conditions.



Figure 2: The primary current and voltage waveform for the half bridge LLC resonant converter



Figure 3: \mathbf{Q}_{oss} Vs \mathbf{V}_{ds} curves with different transistors (GaN, Si, and SiC)

One of the challenges for Si and SiC MOSFETs is incomplete body diode reverse recovery. With the exception of the capacitive load results from overload or during the startup, there is a potential system reliability issue caused by the incomplete body diode reverse recovery of the power MOSFET for the LLC [2]. The existing reverse recovery charge Qrr of the body diode will generate high dv/dt and a large shoot-through current will flow through the bridged transistors, which may result in a MOSFET breakdown. So, the Q_{rr} parameter is a key parameter to verify the risk for the hard commutation failure mode, and therefore the lower Q_{rr} , the better, to avoid the failure.

Table 1 summarizes three transistor type parameters with the physical material of GaN, Si, and SiC. For Si SJ MOS, the most recent Si-based MOSFET with an intrinsic fast body diode was chosen. GaN and SiC are the latest generation wide bandgap transistors which are more suitable for high efficiency and high density power conversions. As shown in the table, compared to Si and SiC, GaN power transistors with the similar $R_{DS(on)}$ have great benefits for the LLC key parameters. The lower values of $C_{o(tr)}$, Q_{gd} , toff, and Q_g , the better performance of the LLC converter designed for efficiency and power density. Additionally, GaN power transistors have a lateral two-dimensional electron gas (2DEG) channel formed on an AlGaN/GaN heterojunction which has no intrinsic bipolar body diode. No body diode means no Q_{rr} which means no hard avalanche operation as mentioned above due to the existence of the body diode for MOSFET.

Operation and Loss Analysis

Figure 4 gives a steady state cycle for a half bridge LLC resonant converter. The following are the main five states, each with its accompanying loss analysis:

- At state 1, when the high side driving signal V_{GSH} goes low, the primary side magnetizing current I_{LM} begins to discharge the output capacitance of the low-side transistor during the dead time.
- 2. At state 2, the parasitic output capacitance is completely discharged and the GaN power transistor is operating at its 3rd quadrant operation through the 2DEG channel from source to drain. As for the Si and SiC MOSFETs, there is an intrinsic bipolar body diode; the body diode will conduct the current from source to drain with the gate's channel turning off. At this state, there is a circulating reverse conduction loss on the primary side due to the existing of magnetizing current. This reverse conduction loss highly depends on the value of $C_{o(tr)}$. Lower $C_{o(tr)}$ results in shorter dead time and the lower magnetizing current results in lower reverse conduction loss.
- At state 3, when the driving signal V_{GSL} is high, the ZVS is achieved for the transistor and there is no switching turn-on loss.
- At state 4, the transistor is turned on with a forward current from drain to source. There is a conduction loss during this state which is related to the on-state resistance R_{DS(on)} of the transistor.
- 5. At state 5, the driving signal V_{GSL} goes low and the channel of the transistor is turned off with hard switching. Due to a peak magnetizing current I_{Im_pk} , there is a current and voltage crossover switching loss. This loss depends on the transistor's characteristic for gate to drain charge Q_{qd} and turn off time t_{off} .

Parameters Blocking voltage V _{ds} ; V		GS66508B	Superjunction MOSFET			Another loss not
		œ	Si	SiC	Gan's value	mentioned above in Figure 4 is gate
		650	600	650		drive loss, which is relative to the
On resistance	$R_{DS(on),}$ typ; m Ω	50	48	55	Almost same typical R _{DS(on)}	transistor's gate
Time related effective output capacitance	C _{o(tr)} ; pF	142	1171	210	Shorter dead time for LLC, low circulating loss	Q_g results in lower
Gate to drain charge	Q _{gd} ; nC	1.8	28	27	Lower switching turn-off loss	especially for high
Turn-off time @5A 400V	t _{off} ; ns	2.52	15.1	11.0	Lower switching turn-off loss	switching frequency. This gate drive loss
Total gate charge	Q _g ; nC	5.8	79	73	Lower switching and gate drive loss	may not be ignored.
Reverse Recovery charge	Q _{rr} ; nC	0	720	85	No hard commutation failure	

Table 1: Key primary side transitor's parameters for LLC resonant converter

A 3KW LLC Resonant Converter

According to the above loss analysis, comparisons can be done with different primary transistors and different switching frequencies to evaluate the performance of efficiency and power density. A 3KW half bridge LLC resonant converter with 48V output are designed, comparing the performance with two comparable scenarios: the first one is all three transistor types are operating at 500KHz resonant frequency and the second one is 500KHz GaN-based LLC versus 100KHz Si-based LLC. The primary transistors are GaN, Si, or SiC. Each switch on the primary implements two transistor devices in parallel from table 1. Figure 5 illustrates the efficiency and loss data for a 3KW Half bridge LLC with all transistors at 500KHz. With 500KHz, the loss breakdown for other components such as transformer, inductor, and SR transistors are supposed to the same, the key loss differences are from the primary side transistors. Although the LLC converter can achieve ZVS for turn-on, the switching turn-off loss still exists with magnetizing current on the primary, especially when the switching frequency is increased to 500KHz. These turn-off losses cannot be neglected. Compared to GaN, the most dominate losses for Si and SiC are the switching turn-off losses, and Si has six times higher switching turn-off loss than GaN, while SiC has four times higher



Figure 4: The LLC resonant converter's operation and loss breakdown for a steady state cycle



Figure 5:

The loss and efficiency of a 3KW 500kHz LLC resonant converter with GaN versus Si and SiC



Parameters	GaN @500KHz	Si @100Hz
Peak Efficiency	97.9%	97.9%
Resonant tank parameters	Lm=10uH, Lr=2uH, Cr=50nF	Lm=50uH, Lr=9uH, Cr=280nF
Transformer; Tr Size	PQ3535 17300mm ³	PQ5050 37200mm ³
Inductor; Lr Size	PQ2016 8T 2310mm ³	PQ3535 12T 17300mm ³
Capacitor; Cr Size	9x5.6nF 32mm ³	6x47nF 82mm ³
Total volume	19642mm ³	54582mm ³
Normalized total resonant tank volume	1x	3x
Normalized DC/DC power density	2.2x	1x

Figure 6:

The 3KW loss and efficiency of a 500kHz GaN-based LLC and a 100KHz Si-based LLC

switching turn-off loss than GaN. Also, the GaN-based LLC has much smaller drive loss compared to Si and SiC. The overall results show that the GaN-based LLC has around 20% lower total losses than SiC and 37% lower total losses than Si. Ultimately, high efficiency is achieved with GaN-based LLC, and this improvement in efficiency provides the incremental performance desired to meet or exceed the latest industrial system requirements, for example, 80Plus titanium for a telecom AC/DC PSU.

Figure 6 shows the other 3KW comparison between 500kHz GaN-based LLC and 100kHz Si-based LLC. In this example, efficiency was held constant with 97.9% to investigate the impact on power density.As shown in Figure 6, with GaN-based LLC at 500KHz, the volume of the resonant tank can be relatively reduced by 64% comparing to a Si-based LLC at 100KHz. Overall, the GaNbased solution with 500kHz can achieve 2.2 times smaller volume than Si-based for the 3KW LLC converter.

Conclusion

This case study of the LLC resonant converter shows a clear performance advantage with GaN power transistors. From the viewpoint of efficiency and power density, GaN power transistors, with the lowest $Co_{(tr)}$, Q_{gd} , t_{off} and Q_g , are the best selection for LLC topology. Furthermore, the absence of the body diode with GaN and zero Q_{rr} makes the system more reliable, avoiding hard commutation failure damage. In summary, GaN provides much higher value in both efficiency and power density compared to Si and SiC transistors for LLC topology applications.

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About the Author

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The Power of Dowell's Equations and Curves

The standardized curves of Dowell's equations are a superb tool for designing better high-frequency magnetics. It is not sufficient to simply use a wire or foil of one skin depth or less. Excessive losses can continue at high frequencies. A careful balance of layer count and wire or foil count is needed to reach an optimum design. Using the numerical curves, instead of the original equations, provides a shortcut path to better understanding of winding design.

By Dr. Ray Ridley, Ridley Engineering Inc.

Dowell's Equations

In 1966, Dowell published his famous paper about high frequency losses in multilayer magnetics windings. Despite this happening so long ago, very few engineers working in power electronics today use them in their work. From surveying our thousands of workshop [3] attendees over the years, we estimate the number of engineers using Dowell's equations to be about 1% of working engineers.

Why is this number so low? When you look at the form of the equation in Figure 2, you get a good idea. The functions in the equation are neither familiar nor intuitive. It takes a lot studying and dedication to learn exactly how to apply the equation to a given situation to find out what losses are going to be.



Figure 1: Cross-section of a two-layer winding in a bobbin

$$P_{d} = b_{w} \sum_{i=1}^{n} l_{i} \frac{1}{h_{i} \eta_{i} \sigma} H_{i}^{2} \left[(1 + \alpha_{i}^{2}) G_{1}(\Delta_{i}) - 4\alpha_{i} G_{2}(\Delta_{i}) \right]$$

$$G(\Delta) = \Delta \frac{\sinh 2\Delta + \sin 2\Delta}{\sin^{2} \Delta + \sin^{2} \Delta}$$

$$\cosh 2\Delta - \cos 2\Delta$$

$$G_2(\Delta_i) = \Delta \frac{\sinh \Delta \cos \Delta + \cosh \Delta \sin \Delta}{\cosh 2\Delta - \cos 2\Delta}$$

I, Mean turn length of layer

7, Ratio of fields on either side of layer

 $\sqrt{\frac{2}{\omega \mu_s \sigma \eta}}$ Skin depth of layer including porosi

 $H_i = \frac{n_i I_i}{2}$ H field at boundary of la



Dowell's Curves

Fortunately for working engineers, it is not necessary to wrap your head around these equations and fully understand them. We can take a lesson from the past days of engineering where it was recognized that the best way to deal with complex expressions was to visually examine them, and see the major effects from a picture, or a series of graphs. Hence the creation of the set of curves shown in Figure 3.

This set of curves is a beautiful example of applied engineering. The family of curves completely encapsulates the complicated mathematics of Dowell's equation. We can apply the curves to analyze different arrangements of windings to optimize design. We will frequently come up with very surprising and illuminating results. Several examples are shown in this article.



Figure 3: These curves completely represent the solution to Dowell's equations for every design

Although the curves are an elegant and very compact representation of Dowell's equation, it can be quite complex for newcomers to magnetics design to understand how to use them. The unexpected consequences of these curves cannot immediately be seen. We must apply the curves to specific situations to realize their full potential.

The first thing that you will notice about the curves is that the x axis does not plot frequency as a variable. Instead, it plots the height of the wire divided by the skin depth. Frequency is an implicit variable, not explicit, since the skin depth given in Figure 1 is a function of frequency. Hence there is a double normalization in the x axis – the size of the wire chosen, and the skin depth at a given frequency. Observant engineers will also notice that the final slope of each of the curves is unity.

It is useful and instructional to take a more specific case and plot the curves as an explicit function of frequency. To do this, we have to select a layer height (in this case the thickness of a #29 wire) and center



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the curves around the frequency where h/δ is one. The example in figure 4 shows this to be 100 kHz. This is the frequency where the wire is equal to one skin depth.



Figure 4: Plotting Dowell's equation versus frequency

The range of frequencies that you can see in this form of the curves spans 4 decades, not just the two decades that you see with standard Dowell's curves. 1 kHz to 10 MHz is a wide enough range to cover just about any need for modern power electronics. You can also see that the final slope is now 0.5, not unity as it is for the previous curves. Both of these effects are due to the fact that the skin depth is proportional to the reciprocal of the square root of the operating frequency.

If the wire gauge changes in your design, simply find the frequency at which one skin depth is equal to the new wire height. This becomes the central frequency of the set of curves. Notice that the underlying data of the curves does not change – only the x axis changes. There is no need to resolve the original equation. A fixed data set is sufficient.

Single Versus Multiple Layers

The curves for Dowell's equation clearly show the penalty in using multiple layers of windings. They don't reveal the whole story by inspection, however, since the y axis is normalized with respect to the dc resistance. When the winding layer count increases, the dc resistance will drop, and there is a vertical shift to the curve. This is best illustrated with a design example.

Consider the current waveform, and the two different winding designs in Figure 5.



Figure 5: Primary current waveform and two different winding choices

In the upper winding arrangement of Figure 5, 2 layers of wire are used. Seven turns of 2x20 awg wire are used to make a 14-turn primary. In the lower winding arrangement, all of the turns are kept on a single layer. In order to fit the wire on the single layer, 2x26 awg wire are used. This means that the wire has only ¼ of the cross-sectional area of the two-layer winding.

As you can see in figure 6, the two-layer winding starts out with four times less resistance than the single-layer winding. However, at the switching frequency, the two-layer winding has a higher resistance. When we consider both the dc and ac components of the current flowing in the winding, the losses in these two different designs are just about the same. The one-layer design will be lower cost with lower capacitance. It provides a better engineering solution, although it conflicts with our natural intuition on design performance.



Figure 6: Un-normalizing the y axis for a specific design shows the power of Dowell's analysis applied to different winding arrangements. In this example we have 4x less copper in the single layer winding, but the same dissipation.

Foil Windings with Different Thicknesses

Even more dramatic effects can be seen if a winding is constructed of copper foil rather than wire. As the turns count drops, it becomes impractical to wind heavy gauge wire to fill the layer of a bobbin. Copper foil has been available to optimize this situation for over 100 years, and you will see this in old transformers with lower output voltages.

In Figure 7 you can see a foil winding on the left where the gauge of the copper has been chosen to completely fill the available bobbin area. The winding on the right has selected a thickness of foil to minimize the loss of the winding for the given waveform.



Figure 7: Two different foil windings. 50 mil foil is used on the left, and 6 mil foil is used on the right.

As we can see from Figure 8, the thicker foil winding has about 8 times less resistance than the thin foil, as we would expect. However, at the switching frequency, the thick foil has almost 15 times more resistance than the thin foil. The net result, when we take the currents at dc and the switching frequency and above, is more than a 10:1 reduction in loss with thin foil.



Figure 8: Dowell's curves applied to the foil windings. The thin foil winding has over 15 times less dissipation than the winding, which is more than 8 times larger

This is powerful knowledge to have when designing transformers and inductors. Once you realize that using less copper is often much more efficient, there are many opportunities for improving your magnetics design. For this foil case, we now have the option of increasing the spacing between the layers, resulting in a lower capacitance design. The thinner foil will also result in lower leakage inductance to other windings of the transformer.

Every winding design provides a different case to for analysis with Dowell's curves. There is no standard solution. In every case, it is necessary to analyze the parameters and optimize the layers and gauges accordingly to minimize losses.

Summary

Published long ago, Dowell's equations provided a powerful analytical tool for magnetics engineers. Without this type of analysis, the dissipation in windings can be grossly wrong. However, the equations are not widely used in the modern day since it is not reasonable to expect most working engineers to solve them. Today's design schedules do not allow the time to properly understand and apply the theory. Fortunately, the numerical curves of Dowell's equations contain all the results needed. Taking the time to learn how to read and apply the curves can make a tremendous difference to magnetics performance.

For interested engineers who want to speed up their learning and application further, the software used to generate the curves and waveforms in this article is available to the design community.[2]

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- [2] RidleyWorks[™] design software contains complete magnetics design and advanced analysis. A free Buck Designer is available to download.
- [3] Learn about proximity losses and magnetics design in our handson workshops for power supply design www.ridleyengineering. com/workshops.html

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Internal Faraday Shield and Small Ci-o Enhance Optocoupler Galvanic Isolation Performance

High voltage isolation in today's context involves integrating subsystems with large voltage differences and systems ground potentials. This enables isolation applications ranging from power supply, motor control circuit of servo automation systems and industrial robots, battery management systems, photovoltaic (PV) inverters, electric vehicle (eV) inverters, ultra-fast charging and wireless charging stations to data communication and digital logic interface circuits.

By Lim Shiun Pin, Technical Marketing Engineer, Isolation Products Division, Broadcom Incorporated

Basically the most important components that provide electrical isolation that allows integration of different subsystems by breaking direct conduction paths are called the isolators or couplers. Integrated circuits (IC) can be combined into the isolators for various electrical functions like driving power electronic devices, high accuracy current and voltage measurements, analog and digital communications and logic interfaces, and isolated power supply conversions.

Isolation Technology

There are three main types of isolator technologies, namely, optocoupler, magnetic coupler and capacitive coupler. Table 1 below shows the key differences between the different isolation techniques, component safety certifications and lifetime reliability failure mechanisms.

The optocoupler transmits electrical signal through the isolation barrier by converting electrical signal to optical signal using an LED and on the other side of the isolation barrier of thickness 0.08mm to 2mm, converts the optical signal back to electrical signal through the photodiodes. In terms of lifetime reliability, the integrity of an optocoupler insulation material can be predicted by partial discharge measurement.

Theoretical dielectric strength values of insulation materials would always apply if optocoupler manufacturers could produce consistently pure insulation barriers. Often, however, high voltage dielectrics contain defects like voids and inclusions of air or other impurities. These voids will have lower breakdown strength than the surrounding dielectric and will discharge or arc when their breakdown strength is reached. The discharge, however, is limited to the length of the void, and after discharging, will slowly recharge with the limited current available through the good dielectric. The void eventually recharges to the breakdown voltage and discharges again, as the process continues as long as the applied electric field remains high enough. These

Isolator / Coupler Types	Broadcom Opto Coupler	Magnetic Coupler	Capacitive Coupler
Isolation Construction	Land Hecking Entitle Chip Epory Duer Mod Input Land Have Opp Patter Definition Protection Definition Protection Definition Protection Definition Protection Definition Protection Definition Protection Definition Protectio	Folyman + Top Coll Folyman + Top Coll Folyman + Top Coll Folyman Coll	Lastrane Mod.Aler Mod.Aler Dig
Insulation Material	3 layers Silicone / Kapton Tape / Silicone	1 layer Polyimide	1 layer Silicon Dioxide
Insulation Thickness	0.08mm to 2mm	 Up to ~ 0.02mm for single coil Double coil (~0.04mm) 	 Up to ~ 0.014mm for single cap Double cap (~ 0.028mm)
Component Certification / Lifetime Test Method	IEC60747-5-5 For Optocoupler Only Partial Discharge (PD) Reinforced Isolation	VDE 0884-10 Alternative Isolator Partial Discharge (PD)	VDE 0884-11 Alternative Isolator Partial Discharge (PD)
Lifetime and Reliability Failure Mechanism	Partial Discharge	Space Charge Degradation	TDDB-Time Dependant Dielectric Breakdown (oxide film degrade over time)

Table 1: Key difference between different isolation techniques, component safety certifications and lifetime reliability failure mechanisms.

discharges are considered "partial" because they occur across the void in a limited portion of the length of the dielectric barrier. Partial discharges, which cannot be detected by leakage current measurements, can over time spread in the insulation that eventually lead to complete insulation breakdown. The problem then, is to detect the presence of partial discharge during manufacturing test in order to prevent this phenomenon from degrading devices in the field.

Broadcom optocouplers high voltage insulation strength is further enhanced with three key design methods. The first is by inserting a clear polyimide called Kapton tape in between the LED and photodiode. The second method is the use of a proprietary, low-cost Faraday shield which decouples the optocoupler input side from the output side. Figure 1 illustrates the isolation construction of Broadcom optocouplers. The third method is by unique package design which is optimized to minimize input-to-output capacitance, Ci-o. The importance of the three design methods will be discussed in detail in this technical paper with an accompanying high voltage surge test as proof.



Figure 1: Broadcom optocouplers isolation construction which incorporates Kapton tape and Faraday shield for enhance insulation strength.

Magnetic coupler uses two coils that are stacked on top of each other with a separating polyimide material of about 0.02mm in between. The application of an AC signal creates a magnetic field, which in turn induces an electric field in the secondary coil. Since the transmission is by magnetic field coupling, the magnetic coupler is also susceptible to nearby magnetic interference. Figure 2 shows an example of magnetic coupler isolation construction with a single pair of top and bottom coils with polyimide insulation material in between the coils. To double the insulation strength, two sets of magnetic coils are used for one isolation path achieving an insulation thickness of about 0.04mm. The failure mode of the magnetic coupler insulation material is space charge degradation.



Figure 2: Magnetic coupler isolation construction with a single pair of top and bottom coils with polyimide insulation material in between.

The construction of a capacitive coupler, as the name implies, is quite similar to a ceramic capacitor, whereby silicon dioxide (SiO2) dielectric of thickness of about 0.015mm is sandwiched in between

two metal plates, usually aluminium (AI), in close proximity. The SiO2 crystal is grown on top of the Al plate. Transmission of signal through the capacitive isolation barrier is usually AC electrical signal. One of the factors that may affect the insulation strength of the capacitive coupler is how well the SiO2 crystal is grown. Defects in the crystal will weaken the insulation material. The lifetime reliability failure mode for the capacitive coupler is time dependent dielectric breakdown (TDDB). Similar to magnetic coupler, to double the insulation strength, two sets of capacitors are used for one isolation path and the insulation thickness is doubled to about 0.03mm. Figure 3 shows a typical double capacitor isolation construction.

Optocouplers are certified to components safety certification of IEC 60747-5-5 for reinforced isolation. This international certification recognizes partial discharge as the failure mechanism for insulation material breakdown. As such, the certification only applies to optocouplers. The alternative isolation technologies like the magnetic and capacitive are certified German standard VDE 0884-10/11. Though the insulation material strength is determined by partial discharge test, this may not be suitable to predict the lifetime reliability of the magnetic (space charge degradation) and capacitive couplers (TDDB).



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High Voltage Surge Test

A quick bench test setup can be easily assembled to compare the insulation strength of various isolators. Figure 4 below shows the test setup where the high voltage surge is applied using an ESD gun. The voltage profile of the ESD gun has a very fast rise time of about 1ns and slow fall time of 30ms. This surge profile is different from the IEC 60060-1 standard surge profile of 1.2μ s / 50μ s, but it is sufficient for the purpose of comparisons of high voltage strength of different isolation technologies.

Three random samples each from two optocoupler manufacturers, Broadcom and Isolator A, one magnetic coupler (Isolator B) and one capacitive coupler (Isolator C) were selected for this high voltage surge test. These isolators are high precision current sensing sigmadelta modulators with internal clock generator built into 8-pin stretched surface mount package outline (SSO8). The isolation withstand voltage, Viso of this type of SSO8 package is rated

5kVrms per minute and with creepage and clearance distance of minimum 8mm. Figure 5 below shows the schematic diagram of the PCB used to hold the device under test (DUT).

Both isolated side power supplies were provided from 9V batteries separately and regulated down to 5V through an LDO voltage regulator on each side of the isolation. The test was carried out by applying high voltage level starting from 14kV between Gnd1-Gnd2 of the sigma-delta modulators. The output clock and data signal were observed for any anomalies. If the outputs resumed normal functionality

after the high voltage surge, the voltage level were increased by 1kV and the test continued up to 25kV test limit. If the output clock and/or data signal latched, the test would be stopped.

i) Faraday Shield

The high voltage surge will induce high density displacement current from Gnd1 to the input circuitry of the isolator and then transmit over to output circuitry and Gnd2 via capacitive structures or parasitic capacitance formed throughout the isolation barrier. Figure 6 below shows the various parasitic capacitance paths formed between the wirebonds of the input circuitry / input leadframe to the Faraday shield of Broadcom optocoupler. The Faraday shield is grounded to Gnd2 and provides an electric and magnetic shielding to remove the displace-



Figure 3: Capacitive coupler isolation construction with two series caps where SiO2 dielectric is sandwiched in between by two Alu metal layers.







Figure 6: Various parasitic capacitance paths formed between the wirebonds of the input circuitry / input leadframe to the Faraday shield of Broadcom optocoupler. The Faraday shield is grounded to Gnd2 and helps to remove the displacement current.



Figure 5: Schematic diagram of PCB board used of high voltage surge test.

ment current. In capacitive or magnetic couplers, the Faraday shield is not a viable solution. A Faraday shield would block the electric or magnetic fields used for data transmission in addition to transients.

ii) Input-Output Capacitance, Ci-o

In addition to the Faraday shield, Broadcom optocoupler leadframe and package design is optimized for smaller combined input to output capacitance, Ci-o. Table 2 shows the comparisons of Ci-o of various isolators. Displacement current follows the relation of $i=c^*dv/dt$. With a smaller Ci-o, smaller displacement current is induced during occurrence of high voltage surge.

Sigma-Delta Modulator SSO8 Package	Isolation Technology	Internal Faraday Shield	Typical Ci-o
Broadcom	Opto Coupler	Yes	0.5 pF
Isolator A	Opto Coupler	Yes	1.0 pF
Isolator B	Magnetic Coupler	No	2.2 pF
Isolator C	Capacitive Coupler	No	1.0 pF

Table 2: Input to output capacitance comparisons between various isolators.

Table 3 shows the results of high voltage surge test on the isolators with different technologies. As evident from the test, Broadcom optocouplers are the most robust against high voltage surge whereby no failure is observed for all the units under test up to 25kV test limit. Isolator A (optocoupler) outputs permanently latched starting from 16kV upwards, while Isolator B (magnetic coupler) from 14kV upwards

Sigma-Delta Modulator	High Voltage Transient across Gnd1-Gnd2 before failure occurs	Failure Mode
Broadcom (optocoupler)	DUT 1: No failure up to 25 kV test limit DUT 2: No failure up to 25 kV test limit DUT 3: No failure up to 25 kV test limit	No failure observed
Isolator A (optcocoupler)	DUT 1: 16 kV DUT 2: 18 kV DUT 3: 17 kV	Output clock and / or data latch permanently low / high
Isolator B (magnetic)	DUT 1: 15 kV DUT 2: 18 kV DUT 3: 14 kV	Output clock and data latch per- manently low / high
Isolator C (capacitive)	DUT 1: 21 kV DUT 2: 15 kV DUT 3: 17 kV	Output clock and data latch per- manently low / high

Table 3: Results of high voltage surge test on different isolators.

and Isolator C (capacitive coupler) from 15kV upwards respectively. Although Isolator A, B and C started to fail at about the same level, Isolator C recorded the widest range of the high voltage surge levels at which the test units failed.

Being one of the advocates for the highly reliable optocouplers galvanic isolation technology, Broadcom's portfolio covers some of the industrials highly adopted internally clocked sigma-delta modulators for precision shunt-based current and voltage sensing solutions. Table 4 shows Broadcom product offerings of internally clocked sigma-delta modulators housed in the SSO8 package format.

^ Automotive AEC-Q100 qualified and Ta, max.=125°C.

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Broadcom Author



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since 2011 and has been instrumental in the area of application development of high precision isolated sigma-delta modulator and optocoupler SPICE modeling. Before that he was doing product development for RF SAW and BAW filters. He has an MSc degree in RF and Microwave Engineering from Nanyang Technological University of Singapore.

Lim Shiun Pin

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Broadcom Part Number	Input Linear Range	Input Full Scale Range	Clock Frequency	Typical Signal to Noise Ratio (SNR)	Typical Offset Temp. Drift (TCVos)
ACPL-C740	±200 mV	±320 mV	20 MHz	86 dB	0.3 μV/°C
ACPL-C797	±200 mV	±320 mV	10 MHz	78 dB	1.0 μV/°C
ACPL-C797T ^	±200 mV	±320 mV	10 MHz	79 dB	-
ACPL-C799	±50 mV	±80 mV	10 MHz	77 dB	0.3 μV/°C
ACPL-C799T ^	±50 mV	±80 mV	10 MHz	77 dB	0.1 μV/°C

Table 4: Broadcom internally clocked, optically isolated, CMOS output, high precision sigma-delta modulators housed in SSO8 package format.

Improving Vacuum Solder Reflow for Challenging Power Module Packaging

The Power Module Packaging Market is projected by some analysts to have a CAGR of nearly 10% from 2019 through 2025, driven by the competing demands for more global energy consumption and the push to reduce the impact of fossil fuels on our environment. Sustainable energy and savings through improved efficiencies will drive improvements in the chip and packaging technologies used in power electronics.

By Matt Vorona, SST Vacuum Reflow Systems, a Palomar Technologies Solution

Increased energy consumption worldwide means an increased need for power electronics devices to meet the requirements along the electrical energy supply chain, from generation to consumption. These devices are required to be more efficient and to operate under more stressful conditions, such as higher temperatures and more power cycles. This is particularly true for the automotive industry, as it transitions from fossil-fuel-powered engines to hybrid electric and battery electric vehicles.

Power Modules for the Electric Vehicle Market

Provided the drivers for the growth of the HEV/EV market remain in place, there are tremendous opportunities ahead for power modules and the necessary vehicle charging infrastructure. This growth should continue to be rapid, as evidenced by the investment into EV technologies by many the top car-producing nations. To meet the requirements of the automotive industry, the semiconductors which populate these modules will need to endure higher operating temperatures and have extended service lives.

The rising demand for power modules does not depend strictly on the conversion of passenger vehicles to the electric power train. There are also abundant opportunities in other areas such as elevators, motor converters, solar energy, welding, industrial frequency converters, pumps, large scale medical devices and so on. All benefit from increased efficiency.



Figure 1: Typical power module construction

Power Modules: Typical failure modes

For a conventional IGBT module consisting of a stack-up of materials and interconnects, the interconnects within the package are the source of mechanical failures due to the thermal expansion mismatches that exist between the materials and components in the assembly. Typical failure modes can include wire bond lift-off due to rapid power cycling or cracks in the solder due to temperature changes.

Application Study: Developing a lead-free, flux-free, extremely low void solder attach process

The Baseplate-to-DBC solder attach was selected, as the increased surface areas for this interconnect pose challenges within the assembly operation and are a source of yield loss for conventional reflow systems, often due to high void rates. Achievement of low cumulative voiding over the entire solder joint is difficult due to the large solder joint surface area and the baseplate bowing found in the most module designs. If flux is used, this can exacerbate the voiding issue. Plus, there is the added challenge and expense to ensure the flux residue has been cleaned from the product after reflow. The power electronics industry is actively seeking a reliable flux-free solder reflow process that achieves low void rates over increased surface areas. With decades of experience operating in high-reliability microelectronics markets that demand a flux-free, void-free solder reflow process, Palomar Technologies is prepared to deliver similar solutions to the power module industry with its SST Vacuum Reflow Systems.

For this application work, a lead-free alloy, SAC305, 0.100 mm thick, was chosen to comply with the European Union and Japan legislation restricting the use of hazardous materials. This E.U. mandate is known as the RoHS (Restriction on Hazardous Substances) Directive and restricts the use of hazardous substances, including lead, in electrical and electronic equipment.

Sulfamate nickel plating for the 44 mm X 104 mm X 3 mm thick baseplate was selected as it provides a more solder-friendly surface vs. electroless nickel plating, as the increasing phosphorous content used in different varieties can hinder the wetting process. The 24 mm X 28 mm DBC was bare Cu.

There are three commonly used metal oxide reduction techniques for electronics assembly.

- **100% or a very high concentration of a hydrogen atmosphere:** Effective, but there are safety concerns about using this highly combustible material in the assembly facility.
- Forming Gas: A Nitrogen/Hydrogen mix, usually in the 95/5 or 97/3 ratio, is safe to use but is not effective unless operating at 350° or

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higher. If the temperature range is compatible with your materials, then it does effectively reduce the oxide layer on metals such as copper and nickel.

Formic Acid: A "low-temp" method to remove the metal oxide layer from surfaces, such as copper or nickel. The power module industry has become very interested in this method. The industry is looking to eliminate the use of flux, but requires an oxide reduction method that is compatible with their materials, that is environmentally friendly, and that is easy to integrate into their existing production process. Formic acid fulfills these requirements.



Images 2 & 3: Fixture with three Cu Alumina DBC on top of SAC305 preforms and baseplate; reflowed assembly.

An SST Model 5100 Vacuum-Pressure Reflow System was selected to conduct the application. The SST QuikCoolTM Option was not used for this evaluation. However, it is recommended it be included on a system used for the production of power modules for the following reasons:

- Productivity improvement: It will increase the throughput by reducing the cool down portion of the profile.
- It will reduce the TAL, or time-above-liquidus, which is a factor for intermetallic compound growth at the interface areas.

Description of the Process Profile Used During Evaluation

The profile review: The SST Model 5100 with 12" x 12" thermal work zone can include up to six monitoring thermocouples on the assembly to track the temperature during the profile. The vacuum and pressure are monitored at all times. This evaluation profile included:

- 1. An initial vacuum followed by a nitrogen purge as the means to evacuate the chamber, fixture and components of the atmosphere, moisture, oxides and other forms of contamination that hinder the reflow operation.
- 2. Temperature is ramped up to 160°C to start the formic acid process.
- 3. The formic acid concentration is adjustable. A 6% level was used. Chamber exhaust remains open during the formic acid portion of the profile.
- 4. The chamber is purged of any remaining fumes by a brief increase in pressure; then a small amount of nitrogen is added to aid the



Images 4 & 5: CSAM images showing voiding (in red) of sample B55 at T0 and T50 temperature cycles.

heat transfer as the temperature is ramped up to the reflow peak.

- 5. At the end of the temperature peak, when the solder is molten, the chamber pressure is increased to 40 PSIG (3.8 Bar) to collapse any remaining voids (air bubbles) trapped in the solder.
- 6. The chamber remains pressurized during cool down till solder returns to solidus.

Sample #	Sample ID	T0 Void Rate	T25 Void Rate	T50 Void Rate	Comments
1	B48	0.5%	0.6%	0.8%	
2	B49	0.5%	0.5%	0.5%	
3	B50	0.5%	0.5%	0.5%	
4	B51	1.1%	1.1%	1.2%	
5	B52	1.6%	1.6%	1.7%	Probably due to undercut preform shift
6	B53	1.1%	1.3%	1.3%	
7	B54	0.9%	1.0%	1.0%	
8	B55	0.3%	0.3%	0.3%	
9	B56	0.4%	0.4%	0.4%	
10	B57	1.6%	-	-	Used for x-section at T0
11	B58	0.3%	-	-	Used for x-section at T0
12	B59	3.1%	-	-	Probably due to undercut preform shift; used for x-section at T0.
	Average	0.99%	0.81%	0.86%	

Void Results: Less than 1% void ratio

The assembled samples were sent to a 3rd party for void rate calculation through the use of a scanning acoustic microscope (CSAM) and subject to -40° to 125°C. temperature cycling. Table 1 below shows the calculated void rates through the first 50 cycles. The average void rate remains at just below 1% at T0, T25 and after T50 cycles

(-40°/+125°C).

Conclusions

The purpose of this study was to evaluate the flux-free soldering process for bare copper DBC substrate to Nickel-plated copper base plate soldering. Using SST's unique void reduction reflow soldering technology and with the use of formic acid, as a means for surface oxide removal, the low voiding results of less than 1% were demonstrated. The same technique can be applied for soldering of power dies (IGBTs, MOSFETs, and Diodes) to DBC substrates with similar results. Future tests by SST will be conducted using 95Sn/5Sb solder alloy with bond line control features. This should be 64 x 34 mm DBC substrate and a similar base plate to demonstrate similar low-void capabilities.

Table 1: CSAM Void Rate Calculations

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Proper Validation of Output Choke: Same Shaped Ferrite vs. Dust Core

Output chokes for Switched Mode Power Supplies (SMPSs) normally operate for a DC load, where a bias magnetic field (H_{DC}) is generated under operation of the magnetic cores. For the emerging mega-watt applications with SiC power devices, the proper validation of output chokes is of great challenge. Basically, there are two criteria for magnetic component design, which are from thermic aspect or from the magnetic nature.

By JC Sun and K. Seitenbecher, Bs&T Frankfurt am Main GmbH and Yi Dou, Technical University of Denmark

Introduction

These two criteria couple, and the difficulty of proper validation is enhanced by ever increasing requirement of high efficiency, high-power density, as well as additionally by the system reliability.

Standards for magnetic materials validation do exist but only specified by voltage levels, whereas the standards by power levels are still lack. However, the increasing requirement for proper validation comes up with developing applications, including the shipboard medium voltage distribution and propulsion, chargers for electric vehicles, medium voltage grid tied interface for datas centre and hybrid propulsion for future aircrafts. In these applications, power levels can range from hundreds of watts to hundreds of mega-watts [1].

Since no micro-magnetic model for magnetic material exists, which is able to lead an analytic reveal of the nonlinearity for magnetic components, measurement is now regarded as the only way to address the challenge. The impulse technique, with its transient high current amplitude to characterize the saturation behaviour, and elimination of the thermal effect during the measuring period, becomes the only option. The damped oscillation with full reversal current, enabling power loss evaluation, is very promising, to be established as validation standard.

Using this concept, a measurement configuration with a bipolar thyristor (SCR silicon-controlled rectifier), which can endure high voltage stress and high dU/dt, has been reported and it is able to provide an accurate validation and loss measurement for critical applications [2]. In this article, a comparative study for a high-saturation material D9BTM vs. dustcore design with same design and nominal parameters is made and validated for its advanced performance for higher power applications.

Design challenges for output chokes

The saturation is an intrinsic phenomenon of magnetic materials, magnetic cores and components, and it is a main concern for designing the output chokes in SMPSs. Typically the power ferrite materials start to saturate when the magnetic field strength achieves 50 A/m and also the permeability of the materials drops sharply. The saturation can be directly observed by measurement and can be qualified by derived differential inductance, amplitude inductance and energy

equivalent inductance [2]. Need to highlight is that all the features can be measured by the pulse method, which can also avoid the thermal interference by heat dissipation during the measurement.

Conventionally there are two remedies against the saturation effect in the magnetic design:

- The use of gapped ferrite cores
- · The use of metal alloy powdered cores

In the case study, we tested both configurations with the gapped ferrite cores in D9BTM material and the alloyed powered cores (super sendust powdered core) in the same shape. The new high B_s ferrite materials, which feature a higher saturation level as well as a high Curie temperature, especially at elevated temperatures, have been reported by [3] [4]. The D9BTM material owns a high saturation feature, whose saturation flux density is higher than 600 mT at room temperature and higher than 500 mT at 100 °C. Besides, its Curie temperature is over 320 °C (i.e. 600 Kelvin), which makes it highly adaptable for higher power applications. The physical configuration for two cases was designed identical to provide a fair comparison: the core shapes are standard E65/ 32/ 27 and the effective permeability of the $\mathsf{D9B}^\mathsf{TM}$ cores were controlled same as well by gapping properly; and the winding configuration were also built identically. Thus, the only difference between two cases is the materials and the gapping configuration.

Materials performance evaluation with outerdiameter 1 inch ring cores

As to the evaluation of magnetic components, where the current standard IEC 62024 is only valid till rated current of 22 A [2], standards for magnetic component for high current application is still missing. The ferrite material evaluation has been standardised by IEC 62044. In more detail, the description of nonlinearity is distinguished in two categories: the small signal measurement is specified in IEC 62044-2, in which the initial permeability, temperature coefficient, discommendation factor etc. are defined; and the large signal measurement is specified in IEC 62044-3, which includes amplitude permeability and its corresponding loss.

In this study, we aim to qualify both the performance of the materi-
als and of the components for the reluctance-level-modelling. For example, the amplitude permeability of the material and its temperature dependence can be measured for evaluation and circuit-level simulation.

The large signal parameters (i.e. amplitude permeability and core loss) for D9BTM and super sendust material are listed in table 1 and 2, where the measurement is performed according to IEC62044-3 by BsT-Analyze. Those data are performed at different temperature level, and only the flux density dependence for particular frequency and temperature is shown:

Test B (mT)	Pcv (mW/cm3)	ua	Bmax (mT)	Hm (A/m)
10	1,644	586,0	8,7	11,8
20	3,240	570,4	20,0	28,0
30	7,095	619,2	30,2	38,8
40	12,534	669,2	40,2	47,9
50	19,373	714,9	50,2	55,9

	Table 1: Tested	parameters	for D9B TM	ferrite	material	at 25	°C/	16	kHz
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Test B (mT)	Pcv (mW/cm3)	ua	Bmax (mT)	Hm (A/m)
10	15,932	85,2	10,0	93,6
20	62,081	79,6	20,1	201,5
30	139,347	80,1	30,2	300,2
40	247,288	80,8	40,7	401,1
50	386,354	81,3	50,3	492,1

Table 2: Tested parameters for super sendust powder material at 25°C/ 16 kHz









It can be noticed from the measurement that the super sendust material shows a higher thermal stability by the large signal parameters: the amplitude permeability and the power loss are significantly less depended on the temperature (Figures 3 and 4). In addition, the power loss measurement results reflect that the magnetization current would be higher than that in ferrite materials by an order, thus giving a low permeability at constant frequency and flux density. Compared to previous power ferrite materials, such as N92, 3C92 and PE90, D9BTM provides obviously more accessible flux linkage at 100°C as inductor for energy storage during magnetization, because it has higher saturation flux density Bs, which can be over 600 mT in room temperature and over 500 mT at 100°C [4].



Figure 3: Amplitude permeability vs. flux density for super sendust material



Figure 4: Power loss density vs. flux density for super sendust material

Evaluate the component with gapped ferrite core design vs. dust core: During the operation of the output chokes, the magnetizing and de-magnetizing process by large energy excitation would repeat continuously thus a fair evaluation must be conducted by large-signal measurement. In this case the small-signal testing would lose the accuracy while the pulse method shows its benefit of enough power excitation and no thermal interference, because of very short term excitation.

Firstly, the devices are tested by the small-signal method: the series inductance is measured as 36 μ H and the equivalent series resistance is measured as 450 m Ω . The measurement equipment is Agilent 4284A and the excitation is 1 kHz/ 20 mA. The photo of the tested component with super sendust material is shown in Figure 5.



Figure 5: Photo of tested compoment with super sendust material

The large signal measurement is conducted by BsT-Pulse, whose operation is illustrated in Figure 6. In the first subinterval, the capacitor C is charged to a specific voltage, which is depended on the value of pulse energy and on the second subinterval, the energy is damped by the Device under Test (DUT) in temperature chamber, together

with capacitor, during which the voltage and current of the damping circuit should be sampled for further evaluation. In the case study, the capacitor was charged to 100V and then damped by the tested components with E65/32/27 cores. The damping voltage and current for both the D9BTM ferrite core (left) and super sendust core (right), as in Figure 7. Compared with other measurement set-ups, such as continuous sinusoidal excitation, the major advance of the pulse method is that the thermal interference during the testing can be eliminated maximally. Thus, as illustrated the performance of the materials or the components can be depicted as a function of temperature.



Figure 6: Illustration of pulse method testing for BsT-Pulse



Figure 7: Damping record for pulse testing in BsT-Pulse (100 °C; voltage in blue, current in red)

The magnetizing and de-magnetizing can also be depicted by the pulse method because the pulse process consists of two sections: Section 1: Magnetizing process of the measuring object from

$$I = 0 A to I = I_{max}$$

Section 2: Demagnetizing process of the measuring object from $I = I_{max}$ to I = 0 A.

The amplitude inductance, which is defined as

$$L_{\mathcal{S}}(i) = \frac{1}{i} \int_{0}^{l} L_{\mathcal{S}}(i) di$$

which is able to depict the key performance for an output choke, including the saturation phenomenon and the nonlinearity under different excitation. In Figure 8 and Figure 9, the amplitude inductance during magnetizing and de-magnetizing process for the component with ferrite D9BTM core is illustrated. Correspondingly the amplitude inductance of the component with the dust core is illustrated in Figure 9 and Figure 10. It can be noticed in the component with D9BTM core that when the excitation current increases higher than 65A, the saturation phenomenon comes up, thus the corresponding amplitude inductance starts to decrease during the magnetizing process. As a comparison, during the de-magnetizing process, the saturation disappeared also at 65A excitation but the performance shapely shift under low excitation, which is more obvious at 20 °C environment. This detailed depiction of the performance advances other measurement method and is capable of expand at mega-watt applications, which cannot be conducted by the conventional method.

The enveloped area through magnetization and demagnetization equals energy loss of choke in half cycle, and this can be calculated by the bipolar impulse method. The flux linkage vs. magnetization current at different temperature is illustrated, here again, the accessible working flux linkage of ferrite design is significantly dependent on temperature compared to powder core design in Figure 12. The core loss of the D9BTM and the dust core can be calculated by integral of the enveloped area.



Figure 8: Amplitude inductance of the component with D9B[™] material v.s. current during magnetizing process



Figure 9: Amplitude inductance of the component with D9B™ material vs. current during de-magnetizing process







Figure 11: Amplitude inductance of the component with dust material vs. current during de-magnetizing process

The conventional design approach for output chokes is to calculate effective permeability through ratio of air gap length to the effective magnetic path length due to the air-gap actually dominates the energy storage inside of the magnetic circuit. The reluctance of air gap needs to be controlled and overcome to reach desired current amplitude. Under these circumstances, the analysis of the fringing effect become more challenging because both the geometry and the flux distribution need to be understood thoroughly [3]. However, the detailed comprehension of the loss mechanism is still missing thus the important of measurement should be truly valued.



Figure 12: flux linkage vs. magnetization current comparison with D9B[™] (on left) and dust core (right) material for 22°C and 100°C

Nowadays the specification of magnetic component with defined shape, air gap length and winding topology is unique assigned to manage the procurement, but it still does not deliver necessary magnetic property, which urgently needed by application engineers. The performance uncertainty becomes increasingly critical for wide acceptance for energy transformation, especially for emerging power range.

Conclusion

The design of gapped ferrite core E62/32/27 are studied along with super sendust powdered core and a complete inductance analysis by the pulse method at different operation temperatures is presented. This study provides insight magnetic properties under pulsation condition, which is able to decouple the self-heating disturbance. Comparing conventional small AC signal measurement with the unipolar impulse technique, the bipolar impulse technique, with damped oscillation approach is able to provide the full picture of nonlinearity of inductor performance, and loss evaluation, decoupled with thermal interference. The bipolar damped oscillation method shows great potential, especially the new configuration; equipped with thyristor stack for medium voltage level (tens of Kilovolt), with repetition rate of some kHz, is target for 3 phase power reactor of future emerging megawatt power applications.

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Gaining 2.5%+ in PFC Efficiency at Low Cost

For low-cost and simple implementation, power factor correction (PFC) has historically been achieved by simple diode bridge rectification and a single-switch boost converter. This arrangement however has significantly reduced efficiency at low line, requires bulky magnetics, large heatsink and fans with high airflow. ICERGi PFC solutions can offer 2.5%+ improvement in efficiency at a cost comparable with the conventional approach.

By Dr. Trong Tue Vu and Edgaras Mickus, ICERGi Limited

Search for High Performance Low-cost PFC Solution

Power factor correction (PFC) is a universal requirement for AC/DC switched mode power supplies with input power above 75W. PFC can be implemented using a wide variety of architectures and topologies. Mandatory performance is defined in IEC 61000-3-2. The industry-standard approach as illustrated in Figure 1 involves usage of a Diode bridge rectifier followed by a Boost converter composed of an Inductor, a high voltage Super-junction MOSFET, and a SiC Diode [1]. The Boost converter steps up the AC voltage, typically from 90Vrms to 264Vrms, to a nominal DC level of 400V and stores energy in an output capacitor. For ease of control implementation and EMI noise filtering, the converter is designed to operate in continuous conduction mode (CCM) with hard switching. This limits the switching frequency of the high voltage MOSFET to around 65kHz, and imposes significant volt-seconds stress on the inductor as a result.



Figure 1: Conventional CCM Boost PFC – Industry standard approach

Another drawback of the conventional PFC implementation is very high conduction loss at low line because the input current at any given time will flow through two diodes in the rectifier bridge and through either an active switch or diode within the boost stage.

A bridgeless totem-pole structure as shown in Figure 2 has been widely used as a technique for conduction-loss reduction [2], in which half-bridge rectification is replaced with full-bridge rectification. This replacement allows removal of one rectifier diode in the power path. Removing conduction losses associated with a diode voltage drop typically translates into approximately 1% efficiency gain at low line. The conduction loss in the boost stage is also lower because the switching leg consists of active devices only.

The totem-pole PFC operating in CCM faces several challenges in practice. Particularly, hard switching transitions rule out usage of Super Junction MOSFETs due to their long reverse recovery time trr and high reverse recovery charge Qrr. Therefore, the only option left for implementation here is Wide-bandgap (WBG) devices, e.g. GaN, SiC. For designers, these are currently not standardized making second source challenging, and they don't have the same economies of scale as with MOSFET devices due to low volume. A challenging engineering issue with WBG devices is high hard-switching loss confining the operating frequency to less than 100kHz, which once again results in high volt-seconds applied across the inductor.



Figure 2: Conventional (2-level) Bridgeless Totem-pole CCM Boost PFC



Figure 3: ICERGi 3-level Bridgeless Totem-pole CCM Boost PFC

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Topology	Conventional CCM Boost PFC	Conventional (2-level) bridgeless totem-pole PFC	ICERGi 3-Level bridgeless totem-pole PFC
Schematic	AD Carrier Redain Constant Dode	BOW Dode Dixtge Rectifier & Invash Dixde	BOV Dode Bridge Richtler & Ivrait Dode
Advantages	 Low cost commodity 650V SJ MOSFETs and SiC diode Simple current sensing and control circuitry 	 Low conduction loss Simple current sensing and control circuitry 	 Low cost commodity 150V MOSFETs Simple current sensing and control circuitry 4 x reduction in magnetics size, low noise No interleaving required for high power
Disadvantages	 Low switching frequency and bulky magnetics High conduction loss Interleaving required for high power, e.g. > 1.5kW 	 Low switching frequency and bulky magnetics Non-standardized GaN/SiC FETs with no economy of scale in short terms Interleaving required for high power, e.g. > 1.5kW 	 Multiple floating drivers (addressed by ICERGi self-powering drive technologies) Extra components, e.g. flying capacitor & balance enforcement circuits

Table I: Co	mparison of Three	e Different Approaches to	b Low-cost High-performance PFC

Тороlоду	Conventional CCM Boost PFC	Conventional (2-level) bridgeless totem-pole PFC	ICERGi 3-Level bridgeless totem-pole PFC
Schematic	AC Francisco Production Control Contro	ACTIVE A trank Dode	Box Clash Bridge Rectifier & Innah Clash Rectifier & I
Full load efficiency	97% @ 230Vac	98.7% @ 230Vac	98.7% @ 230Vac
	94% @ 115Vac	96.8% @ 115Vac	96.8% @ 115Vac
Input Protection	Similar		
EMI Filter	Similar		
Inrush current Man- agement	Similar		
Rectification &	Similar		
Inrush diodes			
Power switches	600V SJ MOSFET & 650V SiC Di- ode (Proven & Lowest cost)	2 x 650V GaNFET (High cost)	8 x 150V MOSFET (Proven & Low cost)
Flying capacitor	No	No	1 x 3.3uF 450V Film capacitor
			(Small added cost)
PFC inductor	Bulky	Bulky	4 x size reduction
			(Cost saving)
Drive and control	Digital PFC controller & Drive cir- cuitry	Digital controller & Drive circuitry	ICERGi Proprietary Digital controller & Self-powering gate drive
	(Simplest & Lowest Cost)	(Medium to high cost)	(Low-cost)
Heatsink	Large	Small (cost saving)	Small (cost saving)
Fan	High air flow	Less demanding (cost saving)	Less demanding (cost saving)
PCB & Enclosure Size	Large	Medium	Small (cost saving)

Table 2: BOM Cost and Performance Comparison

The ICERGi goal is to address two issues associated with WBGbased 2-level totem-pole PFC implementation:

- · Non-standard component without economy of scale
- High volt-seconds stress on the main PFC inductor. It should be noticed that volt-second product indicates how much differential EMI noise will be generated by the boost stage. Low volt-seconds product is always desired.

Figure 3 shows an ICERGi topology which is similar to the conventional bridgeless totem-pole PFC except that the 2-level boost converter is replaced by a 3-level boost converter with a flying capacitor for voltage division [3]. This innovation enables 4 x reduction in voltseconds product and 2 x reduction in operating voltage of switching devices. Those features can be translated into:

- 4 x lower differential EMI noise. The PFC inductor could be 4 x smaller.
- Enable the usage of 300V Silicon switching devices instead of 600V GaN/SiC FETs. For performance and cost optimisation, two 150 MOSFETs are connected in series in order to form a composite switch with an equivalent voltage rating of 300V. This explains why there are 8 x 150V MOSFETs deployed in Figure 3.

Scalable PFC Platform with Digital Control Features

The ICERGi innovative PFC solution boasts a very high peak efficiency of 98.7% at 230Vac and 97.5% at 115Vac as demonstrated in Figure 4. The efficiency data are measured with input EMI filters and a bias supply. The hardware prototype as shown in Figure 5 is implemented by proven and standard Silicon components with a compact PFC inductor. The platform can be easily scaled up in power.

The main difficulty that has inhibited adoption of the 3-level topology is the provision of isolated gate drive for 8 x low voltage (LV) MOSFETs and lack of an off-the-shelf digital controller at low cost.



Figure 4: ICERGi 3-level PFC stage efficiency including EMI filters and bias supply



Figure 5: 1kW Industrial/Medical 3-level Totem-pole PFC Platform

A key ICERGi mission is to make the 3-level solution practical and very cost-effective for usage in high volume single-phase PFC applications. ICERGi have developed self-powering drive and control technologies that can be readily implemented by proprietary ICs and planar-based magnetic coupling, and a low-cost digital controller.

Cost and Performance Comparison

Table I summarises the benefits and drawbacks of each approach as discussed.

Table II compares BOM cost and performance of the three solutions. For a fair comparison, the switching frequency is assumed to be the same and the amount of EMI noise injected back to the AC source is similar for three implementations under study.

Summary

The historical CCM boost PFC has marginally lower cost for power switches, drive, and control as compared to that of the ICERGi PFC solution. However, if one looks at total system cost, the two solutions would be running neck and neck. The cost differences can be bridged by the benefits of the 4x inductor size reduction, smaller heatsink, smaller enclosure, less demand on fans for cooling air, and advanced digital control functionalities. Higher efficiencies also bring long-term benefits of energy saving, e.g. lower utility bills, and the benefits of compatibility with increasing demand for green practice and standards.

The ICERGi 3-level PFC solution is easily capable of scaling-up in power. In other words, no interleaving is required for power up to 3.3kW, which would allow further system cost reduction for power above 1.5kW. The ICERGi PFC design is expected to have lower system cost than a conventional PFC implementation with interleaving.

Moving from the conventional boost PFC to the GaN-based totempole PFC enables power saving with direct benefits of smaller heatsink and less demanding cooling requirements. However, such benefits would not be great enough to compensate for the high cost of GaN devices which do not have the same economies of scale and experience curve and where single sourced components pose a significant risk in terms of single source component vulnerabilities.

ICERGi will present the multilevel Si power conversion technologies at APEC 2020. If you would like to talk to us, please email ttrongvu@icergi.com or edgarasmickus@icergi.com

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A Low loss and Low Forward Voltage Drop SIPOS Passivated Fast Recovery Diode

This article introduces a new family of 1700V 25A to 300A Fast Recovery Diodes (FRDs). The experimental findings are consistent with numerical modelling results and demonstrate that using Variation in Lateral Doping (VLD) employing SIPOS, SIN and polyimide passivation, it is possible to achieve a stable 1700V diode. The devices show low switching losses and low forward voltage drop with positive temperature coefficient.

By J.V. Subhas Chandra Bose, Hua Shen, Fu Yong and Bruce Chen, StarPower Europe AG

Introduction

To increase the avalanche breakdown voltage, to improve the switching power losses for example in windmills, induction heating, motor drive or inverter applications, there have been many efforts concerning the development of optimized diodes called first, second, third and fourth generation FRDs. The main development of these new generation diodes using bulk wafer, Thin wafer technology, n+ back surface contact, laser annealing and multiple proton implantations were all employed for diode fabrication [1-5].

In this article a 1700V soft recovery diode with different current ratings are introduced. The fast and soft recovery diodes with tail current were developed using a combination of deep diffused phosphorous wafers from the backside of a wafer and controlled axial lifetime killers. The proposed diodes give stable performance throughout their operating temperature range and maintain positive forward voltage drop with respect to temperature. These diodes are designed for medium to high frequency applications where low and high switching performance is required. The switching losses at RT and hot compared with respect to competitor devices. Furthermore, to our knowledge we have found out that an economical approach to fabricate power diodes is using commercially available 6-inch 600V to 1700V deep diffused phosphorus wafers instead of using multiple proton implantation to get N buffer region. If one needs thin wafers for example like 600V to 1200V, thin wafer technology can be implemented using final Phosphorus implantation and laser annealing to activate Phosphorus prior to backside metallisation.

Structure

Figure 1 shows the simplified cross-section of the proposed VLD design. The structure is fully compatible to a 1700V to 4500V IGBT process technology. To provide consistency with the process conditions, the structure has been derived directly from DIOS and subsequently analysed using TCAD simulation software[6]. Great care has been taken to ensure a close fit between measured spreading resistance profile and that of the simulated profile. Since SIPOS is a semi resistive layer and difficult to implement in a breakdown voltage simulation tool, therefore zero charge is assumed. Deep P- region incorporated to reduce leakage current from axial lifetime killer such as Helium or Proton and to make the device robust during hard switching conditions.



Figure 1: Cross section of a Planar junction VLD termination for 1700V device.



Figure 2: Conventional spreading resistance profile of a 1700V soft recovery diode.

In an effort to obtain soft recovery diodes at all conditions StarPower has developed a 1700V diode by using phosphorus deep diffused wafers and axial lifetime killers as shown in Figure 2. The controlled axial lifetime killer inside the main boron is used to control the injection efficiency of holes from P region. P- region used to reduce leakage current with respect to Anode boron junction depth and Metal thickness tolerances. The same P region also reduces curvature effect so that during hard switching test conditions, current crowding does not occur. The soft N as shown provides extra charge for the soft recovery. The low injection efficiency of holes makes the device Vf positive temperature coefficient with an increase in temperature which is good for parallel operation of diodes in modules where several IGBTs and Diodes are connected in parallel, and during high temperature switching losses are minimised. Diode softness Trr is controlled using additional uniform lifetime killing by electron irradiation.

Discussion

The requirements of FRDs are (a) Area efficient termination (b) Reliability (c) switching performance.

Area efficient termination

The Anode active area can be increased when the area of a termination is reduced for a given die size. As the active area increases the current capability of a device increases, Vf decreases and surge current increases. Premature edge breakdown is a very common effect in power devices. The breakdown takes place at the surface of the P/N- base junction due to curvature and a lower surface critical electric field. To avoid edge breakdown, the most commonly used techniques are floating ring termination [7-11]. This technique is based on P floating rings placed at the edge of the device to release the depletion width or share potential drop between the rings. However,

this structure is passivation charge sensitive. To reduce charge sensitive spacing between rings should be reduced and more rings should be added. To reduce surface charge effect, the field plate technique can also be used in combination with the floating ring termination [12-15]. However, in both cases P rings do not completely deplete and do not share potential with N- and not area efficient. Therefore, VLD technique is used.

The VLD technique is based on implantation through small openings in the oxide using photoresist mask and subsequent drive in, leading to a controlled doping profile [156-17]. The slope in the lightly doped region and concentration of the doping profile as shown in the proposed structure Figure 1. VLD structures are sensitive to the doping concentration boundary between the main junction and the junction termination. Therefore, ISE software is used to optimise the boron dose with Si thickness of 290um with effective N- thickness of 155um. 1700V VLD designed such that with 10% variation in doping concentration, breakdown voltage varies between 1900V to 2000V. Modern implanter dose variation is also within the range of 2% therefore it is possible to get minimum 1900V. Total width of a VLD design is 300u with redundant area between edge of VLD to channel stopper is 100um.

Reliability

When the device is in avalanche breakdown voltage VLD completely depletes to the surface. If proper choice of passivation is not made, reduced breakdown voltage or unstable blocking characteristics or increase in leakage current occurs. Therefore, SIPOS passivation is made to deposit directly on the silicon surface. This is because SIPOS has got limited conductivity, any undesired charge such as ionic contamination, interface charge or trapped charge which may disturb the electric field distribution is compensated by mobile carriers within the SIPOS. LPCVD machine is used to deposit 0.2um of SIPOS with SIN passivation. Conductivity of SIPOS is carefully adjusted by oxygen content



Figure 3: VLD breakdown voltage with respect to Boron dose.

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during deposition. Furthermore, we have observed that reverse leakage current increased at higher temperature because of thermally activated conductivity of SIPOS. However, this leakage current at 150°C is negligible or below our chip/module limit. Prior to the official release for mass production 75A and 200A went through full qualification testing. The most important reliability tests for the electrical stability of the chip are high Temperature Reverse Bias (HTRB) and humidity test. The HTRB test checks the ability of the samples to withstand a reverse bias while being subjected to the maximum ambient temperature that the parts are rated to withstand. The condition used for the HTRB test is 80% of rated voltage at 150°C. The breakdown voltage and leakage current were measured before starting the test. 1700V chips (78+78 =156 chips) were assembled into the C6 package. The test was conducted for up to 1000Hr and readings were taken once every 8H. Pre and post measurement results show 10uA and there is no increase in leakage current. Humidity test checks the ability of the package and chip to resist moisture penetration. The sample is loaded into an environmental chamber. The relative humidity is then increased to 85% and the temperature is elevated to 85°C. The device characteristics are measured before starting the test. The devices are re measured after cooling down for 3hr. Pre and post measurement results show there is no increase in leakage current.



Figure 4(a): Forward voltage drop at 25° C and 150° C Figure 4(b) Switching performance at 25 and 150° C

The maximum leakage current at room temperature is 10uA and at 150°C 1mA.

(c) Switching performance

In order to verify the performance of the StarPower FRD diode in comparison to two competitor FRDs at 25 and 150°C were carried out using an inductive load circuit. The forward voltage drop of all diodes are within +/. 0.15V. After axial life time killer and electron irradiation devices were tailored to Vf 1.8V using vacuum annealing furnace. Figure 4(a) On state characteristics show that at rated current and above Vf increase with increase in temperature. This makes a better choice for parallel operation. Typical switching results are as shown in Figure 4(b) at RT and 150°C for 75A Vr at 900V and di/dt 1500A/ us. The switching results show that there is no over shoot voltage. Therefore, devices can be stressed to higher blocking voltage. Table-1 shows comparison results of competitor devices for identical chip sizes. The reverse recovery waveforms and Table-1 results show that the diode does not ring and therefore produce low EMI, results in removal of parallel RC snubbers across the diode. Comparing RT to 150°C maximum reverse recovery current (Irm) value increase is 25% therefore IGBTs will be less stressed across the temperature range in real application.

Conditions	Competitor-1	Competitor-2	StarPower
Vf(@75A),V	1.7	1.83	1.85
lrm@25°C	87	103	85
Trr, ns@25°C	333	301	268
lrm@150°C	112	129	104

Table-1: Switching condition at 75A, Vr-900V Rg 10ohm and di/dt-1500A/us.

Conclusion

Simulation analysis and practical results show that by using VLD structure it is possible to obtain breakdown voltage 1900V with thin N- thickness of 155um. The experimental results demonstrate that the use of a semi insulating material such as SIPOS, for the passivation of a planar junction termination results in stable blocking voltage characteristics. Without using wafer grinding, backside phosphorous implantation, laser annealing and using deep diffused phosphorus wafers demonstrated that it is possible to get low Vf 1.8V with low Irm and smooth reverse recovery with no ringing. Using deep diffused phosphorus wafers, optimising N- thickness and lifetime killers it is possible to get more economical and highly reliable FRDs. The same technology and fabrication procedures are potentially suitable for medium voltage 1700V to 6500V by adjusting the VLD design. Optimal solution for the area efficient VLD design can be obtained within several days of simulation.

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Hybrid Converter Simplifies 48 V/54 V Step-Down Conversion in Data Centers and Telecom Systems

There has been a shift in data center and telecom power system design. Key applications manufacturers are replacing complex, expensive isolated 48 V/54 V step-down converters with more efficient, nonisolated, high density step-down regulators (Figure 1). Isolation is not necessary in the regulators' bus converter since the upstream 48 V or 54 V input is already isolated from hazardous ac mains.

By Ya Liu, Jian Li, San-Hwa Chee and Marvin Macairan, Analog Devices, Inc.

For a high input/output voltage application (48 V to 12 V), a conventional buck converter is not an ideal solution because component size tends to be larger. That is, a buck converter must run at a low switching frequency (for example, 100 kHz to 200 kHz) to achieve high efficiency at high input/output voltage. The power density of a buck converter is limited by the size of passive components, especially the bulky inductor. The inductor size can be reduced by increasing the switching frequency, but this reduces converter efficiency because of switching-related losses and leads to unacceptable thermal stress.



Figure 1: A traditional telecom board power system architecture with an isolated bus converter. The isolated bus converter is not necessary in systems where 48 V is already isolated from the ac mains. Replacing the isolated converter with a nonisolated hybrid converter significantly reduces complexity, cost, and board space requirements.

Switched capacitor converters (charge pumps) significantly improve efficiency and reduce solution size over conventional inductor-based buck converters. In a charge pump, instead of an inductor, a flying capacitor is used to store and transfer the energy from input to output. The energy density of capacitors is much higher than inductors—improving power density by a factor of 10 over a buck regulator. However, charge pumps are fractional converters—they do not regulate the output voltage—and are not scalable for high current applications.

An LTC7821-based hybrid converter has the benefits of both conventional buck converters and charge pumps: output voltage regulation, scalability, high efficiency, and high density. A hybrid converter regulates its output voltage with closed-loop control just like a buck converter. With peak current-mode control, it is easy to scale the hybrid converter up for higher current levels (for example, a single-phase design for 48 V to 12 V/25 A to a 4-phase design for 48 V to 12 V/100 A).

All switches in a hybrid converter see half of the input voltage in steady state operation, enabling the use of low voltage rating MOS-FETs to achieve good efficiency. The switching-related losses in a hybrid converter are lower than a conventional buck converter, enabling high frequency switching.

In a typical 48 V to 12 V/25 A application, efficiency above 97% at full load is attainable with the LTC7821 switching at 500 kHz. To achieve similar efficiency using a traditional buck controller, the LTC7821 would have to operate at a third of the frequency, which results in a much larger solution size. Higher switching frequencies allow the use of smaller inductances, which yield faster transient response and smaller solution size (Figure 2).



Figure 2: Size comparison of a nonisolated buck converter and equivalent 48 V to 12 V/20 A hybrid converter.

The LTC7821 is a peak current-mode hybrid converter controller with the features required for a complete solution of a nonisolated, high efficiency, high density step-down converter for an intermediate bus converter in data centers and telecom systems. The LTC7821's key features include:

- Wide VIN range: 10 V to 72 V (80 V abs max)
- Phase-lockable fixed frequency: 200 kHz to 1.5 MHz
- Integrated quad ~5 V N-channel MOSFET drivers
- RSENSE or DCR current sensing
- · Programmable CCM, DCM, or Burst Mode® operation

- CLKOUT pin for multiphase operation
- Short-circuit protection
- EXTVCC input for improved efficiency
- Monotonic output voltage start-up
- 32-lead (5 mm × 5 mm) QFN package

48 V to 12 V at 25 A Hybrid Converter Featuring 640 W/IN3 Power Density

Figure 3 shows a 300 W hybrid converter using the LTC7821, switching at 400 kHz. The input voltage range is 40 V to 60 V and the output is 12 V at loads up to 25 A. Twelve 10 μ F (1210 size) ceramic capacitors are used for each flying capacitor, CFLY and CMID. The relatively small size 2 μ H inductor (SER2011-202ML, 0.75 in × 0.73 in) can be used because of the high switching frequency and the fact that the inductor only sees half of VIN at the switching node (small volt-second).

The approximate solution size is 1.45 in × 0.77 in, as shown in Figure 4, resulting in a power density of about 640 W/in3.

As the bottom three switches always see half the input voltage, 40 V rated FETs are used. An 80 V rating FET is used for the very top switch because it sees the input voltage at the beginning of the precharge of CFLY and CMID during startup (no switching). During steady state operation, all four switches see half of the input voltage. Therefore, the switching losses in a hybrid converter are much smaller compared to a buck converter in which all switches see the full input voltage. Figure 5 shows the efficiency of the design. The peak efficiency is 97.6% and the full load efficiency is 97.2%. With high efficiency (low power loss), the thermal performance is very good, as shown in the Figure 6 thermograph. The hot spot is 92°C at an ambient temperature of 23°C with no forced airflow.







The LTC7821 implements a unique CFLY and CMID prebalancing technique, which prevents input inrush current during startup. During initial power-up, the voltage across the flying capacitor CFLY and CMID are measured. If either of these voltages are not at VIN/2, the TIMER capacitor is allowed to charge up. When the TIMER capacitor voltage reaches 0.5 V, internal current sources are turned on to bring the CFLY voltage to VIN/2. After the CFLY voltage has reached VIN/2, CMID is charged to VIN/2. The TRACK/SS pin is pulled low during this duration and all external MOSFETs are shut off. If the voltages across CFLY and CMID reach VIN/2 before the TIMER capacitor voltage reaches 1.2 V, TRACK/SS is released, and a normal soft start begins. Figure 7 shows this prebalancing period and Figure 8 shows the VOUT soft start at 48 V input, 12 V output at 25 A.

Top Side



1.45 in × 0.77 in × 0.42 in

Bottom Side



Figure 4: Possible layout for a complete bus converter uses the top and bottom sides of the board, requiring only 2.7 cm2 of the topside of the board.



Figure 5: Efficiency at 48 V input, 12 V output, and 400 kHz fSW.

1.2 kW Multiphase Hybrid Converter

The easy scalability of the LTC7821 makes it a good fit for high current applications, such as those found in telecom and data centers. Figure 9 shows the key signal connections for a 2-phase hybrid converter using multiple LTC7821s. The PLLIN pin of one LTC7821 and the CLKOUT pin of another LTC7821 are tied together to synchronize the PWM signals.



Figure 6: Thermograph of the hybrid converter solution in Figure 2.







Figure 8: LTC7821 startup at 48 V input, 12 V output at 25 A (no high inrush current).







Figure 10: A 4-phase, 1.2 kW hybrid converter using four LTC7821s.



Figure 12: Thermograph of the multiphase converter shown in Figure 9.

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Figure 9: Connection of key signals of LTC7821 for a 2-phase design.



Figure 11: Efficiency for a 4-phase, 1.2 kW design.



Figure 13: Current sharing for the multiphase converter shown in Figure 9.

For a design with more than two phases, the PLLIN pin and CLKOUT pin are connected in a daisy chain. Since the clock output on the CLKOUT pin is 180° out of phase with respect to the main clock of LTC7821, even numbered phases are in phase with each other, while those with odd numbers are antiphase to the evens. A 4-phase, 1.2 kW hybrid converter is shown in Figure 10. The power stage of each phase is identical to the single-phase design in Figure 3. The input voltage range is 40 V to 60 V and the output is 12 V at load up to 100 A. The peak efficiency is 97.5% and the full load efficiency is 97.1% as shown in Figure 11. The thermal performance is shown in Figure 12. The hot spot is 81°C at an ambient temperature of 23°C with 200 LFM forced airflow. Inductor DCR sensing is used in this design. As shown in Figure 13, current sharing is well balanced among the four phases.

Conclusion

The LTC7821 is a peak current-mode hybrid converter controller that enables an innovative, simplified approach to intermediate bus converter implementation in data centers and telecom systems. All switches in a hybrid converter see half of the input voltage, significantly reducing the switching related losses in high input/output voltage applications. Because of this, a hybrid converter can run at 2× to 3× higher switching frequency than a buck converter without compromising efficiency. A hybrid converter can be easily scaled for higher current applications. Lower overall cost and easy scalability differentiate hybrid converters from traditional isolated bus converters.

About the Authors

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Thermal Endurance Estimation of Magnetic Components Used in Embedded Automotive Applications

Over the years, there has been considerable debate on how to determine and classify the thermal performance of insulation materials used in electrical power systems equipment and their related applications.

By Patrick Fouassier & Abdelkader Birch, PREMO FRANCE Inductive Components R&D

'Unfortunately, there is a tremendous amount of confusion in the marketplace regarding the thermal performance of insulation materials. There are many terms used to describe thermal performance, including: Relative Temperature Index, Thermal Classification, Continuous Operating Temperature, and other. However, as a customer of a branded material or a supplier which must provide reliability guarantees, it is important to ask and understand what is being supplied! This is of even more importance for power electronic equipment embedded in new hybrid or electrical vehicles, such as onboard battery chargers, DCDC converters, inverters, electrical motors, and the like. As a matter of fact, the constant target of a higher power density at a lower weight, lower volume, and at a lower cost, really pushes the components to their limits in regard to their operating temperature versus the thermal resistance of any polymer material from their structure.



Figure 1: Excess of heat can lead to electrical breakdown of power components

In this article we will present and discuss the common possible definitions of the temperature limits given for any relevant material part of the insulation system. We will present the description of certified test methods, as well as how the results can be used for thermal endurance estimation of a device. One example related to an inductive component will be presented considering some real mission profiles that can be found in automotive applications. A tool to estimate the "lifetime consumption" of the insulation during the mission profile will be shown and commented.

Definitions

Without question, there are many terms used to describe the thermal performance of materials. Unfortunately, some of these terms have no technical meaning established by industry standards or specification. For example, there is no industry definition or standard for "Continuous Operating Temperature". What does that term mean? How is it tested? How does it apply to design considerations for electrical equipment? A property value for Continuous Operating Temperature really has no meaning unless there is a very specific test method indicated to help determine how that property value was determined.

It is safe to say that each industry may have its own terms and its own test methods for determining the thermal performance of various materials used in its designs. However, the electrical industry has established very specific terms and test methods pertaining to rigid electrical insulation laminates.

In the electrical industry, the terminology referring to the thermal characteristics of insulation materials can sometimes be confusing because several terms are used interchangeably. The following most common definitions today should help clarify this:

a) Thermal Endurance

Defined as the relationship between temperature and the time spent at that temperature required to produce such degradation of an electrical insulation that it fails under specified conditions of stress, electric or mechanical, in service or under test (IEEE Standard Dictionary of Electrical and Electronic Terms). The point of failure, also referred to as the "thermal life", is typically considered as the time at which the measured property falls below 50% of its original untreated value.

b) Relative Temperature Index (RTI)

IEEE Definition:

An index that allows relative comparisons of the temperature capability of insulating materials or insulation systems based on specified controlled test conditions (IEEE Standard Dictionary of Electrical and Electronic Terms).

UL Definition:

The temperature above which the material is likely to degrade prematurely. This temperature can be determined by performing a thermal aging comparison against a material known to have accept-

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- Protection against overload, overvoltage and short circuit
- 3-year product warranty



Series	Power	Package	Temperature	Isolation	Working voltage
TRI 3	3 W	DIP-24	-40 °C to +90 °C w/o derating	5000 VAC	1000 VACrms
TRI 6	6 W	DIP-24	-40 °C to +85 °C w/o derating	5000 VAC	1000 VACrms
TRI 10	10 W	DIP-24	-40 °C to +65 °C w/o derating	5000 VAC	1000 VACrms
TRI 15	15 W	2"×1"	-40 °C to +65 °C w/o derating	4200 VAC	1000 VACrms
TRI 20	20 W	2"×1"	-40 °C to +55 °C w/o derating	4200 VAC	1000 VACrms



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able performance at a known temperature. The RTI can also be simply assigned based on the known performance of the generic class of the material.

One of the most important tests to determine a given plastic's fitness for long-term ambient heat is the UL Standard 746B, "Polymeric Materials - Long-Term Property Evaluation". Underwriters Laboratories Inc. (UL) developed RTI to test the deterioration of insulating materials in electrical devices over time. Maximum service temperature for a material where a class of critical property will not be unacceptably compromised through chemical thermal degradation. This spans over the reasonable life of an electrical product, relative to a reference material having a confirmed, acceptable corresponding performance defined RTI.

- RTI electrical: The electrical RTI is associated with critical electrical insulating properties by measuring dielectric strength.
- RTI mechanical impact: The mechanical impact RTI is associated with critical impact resistance, resilience and flexibility properties by measuring tensile impact strength.
- RTI mechanical strength: The mechanical strength (mechanical without impact) RTI is associated with critical mechanical strength where impact resistance, resilience and flexibility are not essential by measuring tensile strength.

Where to find the RTI for a material? Underwriters Laboratory has tested many materials for RTI and they report these numbers on what they call the UL "Yellow Card" of the material (Exxxxx number). You can find these on the UL Prospector website. Here is an example of one for a well-known PA66 plastic:



Figure 2: Example of the UL "Yellow Card" for FR50 PA66 plastic material

The RTI values are listed under the thermal section of the card, usually under columns. The RTI numbers are divided into RTI Elec (electrical properties), RTI Imp (impact strength), and RTI Str (tensile strength). You might have to decide what the most important property is. If all three are critical, then use the lowest RTI figure.

You will also notice that many materials have different thicknesses listed under each category such as 0.35, 0.75, 1.5mm... This represents the thickness of the tested plaques. Usually, thicker sections can take more heat. Look at the RTI that corresponds to the thinnest section of your part.

Such a value for RTI will be also specific to a particular grade of a polymer, sometimes even to a specific color. The difference between grades of a particular species of polymer can be substantial, depending both on the variation in the inherent stability of a material between differing manufacturing methods and also on the type and amount of additives used. It is possible to obtain from the laboratory a Generic

Temperature Index to cover a species of material, but this will usually be considerably lower for many of the individual grades within that species.

Today, the Relative Temperature Index is widely accepted by the electrical industry when determining the thermal performance of a material. As seen in the previous definitions, the RTI value can be determined by methods ranging from long-term thermal aging studies to simply assigning values based on the generic class of the material (after chemical analysis to confirm a material belongs to a certain class).

c) Temperature Index (TI)

ASTM Standard D2304:

A number which permits comparison of the temperature/time characteristics of an electrical insulation material, or a simple combination of materials, based on the temperature in degrees Celsius which is obtained by extrapolating the Arrhenius plot of life versus temperature to a specified time, usually 20.000 hours. The international standard IEC 60085 gives the table as below for reference where an added column shows examples of corresponding materials per thermal index.

Temp. (°C)	mp. Therm. C) class	Related materials			
90	Y	organic materials e.g. paper, wood, cotton, silk together with conventional impregnating compounds (shellac, asphalts, oils), from the group of polymers PVC			
105 A		organic materials e.g. paper, wood, cotton, silk, fabric together with a suitable impregnant or enamel, cellulose based synthetic materials, press boards for electrical purposes, paper-based adhesive tapes, acrylate combine with paper, PET foil with caoutchouc, PES fabric or tape, hardened cotton fabric with phenolic resin			
120	E	organic materials e.g. cellulose or hardened paper, hardned fabric, cellular tissue in combination with impregnants or phenol-formaldehyde or phenolic resin, hardened paper and fabric with phenol formaldehyde, pressed phenol- melamine laminate, PET foil with electrical press boards			
130	в	inorganic materials e.g. glass fibers, glass laminate with epoxy binder, mica based inuslation, PES resin with glass mat, PET/caoutchouc and PET/acrylate based adhesive tapes			
155	F	components of these materials are glass fibers, mica paper, PET, PEN foils, aramid and its modifications (nomex, kevlar twaron), aramid paper, epoxy and novolac resins			
180	н	silicone and modificated epoxy resin is used as a binder, aramids, polyimids, PES, mica, mica paper and its modification (remca, samica, calmica) and its composites			
200	N	glass, asbestos (banned), aramid papers with silicone binders, teflon, polyester-alkyd based impregnating enamel			
220	R	same as class N materials, glass fibers, asbestos (banned), aramid papers mostly with silicone bindings, aromatic polyamide			
250	250	polyimides (kapton), aramids (nomex), PTFE, class R materials with new binding materials, polyimid foils			

Figure 3: Table of thermal index according to IEC 60085

d) Other temperature characteristics of polymers

Additional temperature parameters can be under the scope for plastic materials selection for use in one application.

Melting temperature (Tm):

The temperature at which a substance changes from solid to liquid state.

Glass Transition Temperature (Tg):

The glass-liquid transition, or glass transition, is the gradual and reversible transition in amorphous materials (or in amorphous regions within semi-crystalline materials) from a hard and relatively brittle "glassy" state into a viscous or rubbery state as the temperature is increased. An amorphous solid that exhibits a glass transition is called a glass. The reverse transition, achieved by supercooling a viscous liquid into the glass state, is called vitrification. So, the glass-transition temperature Tg of a material characterizes the range of temperatures over which this glass transition occurs. It is always lower than the melting temperature, Tm, of the crystalline state of the material, if one exists.

Temperature of Degradation (Td):

The temperature at which the material weight changes by 5%. This parameter determines the thermal survivability of the resin material. Issue: material decomposition can result in adhesion loss and delamination. The chemical bonds break upon exceeding Td resulting in permanent degradation and damage to the material.

Heat Deflection Temperature (HDT):

The temperature at which a polymer or plastic sample deforms under a specified load. This property of a given plastic material is applied in many aspects of product design, engineering and manufacture of products using thermoplastic components.

Vicat Softening Temperature (VST):

Is the determination of the softening point for materials that have no definite melting point, such as plastics. It is taken as the temperature at which the specimen is penetrated to a depth of 1mm by a flat-ended needle with a 1mm² circular or square cross-section. For the Vicat A test, a load of 10N is used. For the Vicat B test, the load is 50N.

Even if all those physical properties may have some meaning, they do not provide for any reasonable estimation of the life of an electrical insulation material based on mechanical or electrical property retention at a certain temperature over a period of time.

That's why these tests are not referenced in any IEEE, UL, NEMA or ASTM test method for electrical insulation materials. However other standards describe their testing method, like for example the IPC-TM-650. In the electrical industry, there are no other widely accepted terms that define the thermal performance of a material based on an accepted test method for electrical insulation materials. Remember that other industries may have their own standards for defining terms such as "Continuous Operating Temperature", but unless a specific test method is referenced, such terminology has no real technical meaning.

Test Methods

Today, the Relative Temperature Index is widely accepted by the electrical industry when determining the thermal performance of a material. As seen in the previous definitions, the RTI value can be determined by methods ranging from long-term thermal aging studies

(for up to 60.000 or 100.000 hours) to simply assigning values based on the generic class of the material (after chemical analysis to confirm a material belongs in a certain class).

The test programs and methods for the determination of thermal performance of insulation materials were developed based on the assumption that heat is the chief cause of insulation degradation. Other factors being equal, thermal degradation is accelerated as the temperature is increased and other mechanical and electrical properties deteriorate with increasing temperature over time.

To simulate the thermal response and determine the RTI of a material, the test specimens are aged in a load-free state at different temperatures in forced-ventilated hot-air cabinets. The change in specific properties in relation to the aging period can subsequently be calculated at room temperature.

These property changes are generally investigated by means of a mechanical shock test, quasi-static and electrical measurements. The test ends when the property value in question falls below the minimum threshold (50% of the original value).



Figure 4: Determination of the time to reach the end-point at each temperature – Property variation

The time until the property limit is reached is calculated for each individual property (temperature/time pairs) based on the results obtained. Those pairs are then used to generate a thermal resistance diagram for the material being tested. By extrapolating the results over time, a temperature index (TI), normally after 20.000 hours, can be determined according to (IEC) DIN EN 60216-1.



Figure 5: Long-term thermal resistance diagram for different physical properties

For a full aging study, thermal performance at a minimum of three and preferably four temperatures would be tested. ASTM recommends choosing the lowest temperature test to be less than 25°C above the hottest-spot temperature expected in use so that the thermal life is at least 5.000 hours. Select the highest temperature so that the thermal life is at least 100 hours. If possible, the aging temperatures should differ from each other by at least 20°C, but 10°C increments remain acceptable.

The linear regression of the plot gives the Halving-Interval Coefficient (HIC) corresponding to the numerical value of the temperature interval (in Kelvins) which expresses the halving of the time to end-point taken at the temperature equal to TI. In the below example we can deduce TI # 130°C and HIC # 5 to 6K.



Figure 6: Lifetime characteristic under long-term thermal stress – Thermal endurance graph (Arrhenius plot) according to IEC 60216-1

From experiment and data from suppliers, we find HIC values around 5-15K for most of the insulating materials. According to ASTM D2304, "Experience has shown that the thermal life is approximately halved for a 10°C increase in exposure temperature".

Composites - Example of enameled wires

Many insulators are composites using adhesives and varnish. They are used as test samples following a simple varnish treatment. For example, the helical-coil method is a life testing method for impregnated varnish. By winding a bare copper wire densely to form a cylinder, impregnating and coating the varnish and drying/sintering it to make a test sample, its bending breakage stress after heating can be determined and the thermal degradation rate can be checked simply.

Another example is the method in which varnish is impregnated in a glass cloth and dried to make a varnish glass cloth for use as a test sample, and the breakdown voltage is then determined following thermal degradation. Another is the twisted-pair method, in which a test sample made of two twisted enamel wires is used to determine the dielectric strength by applying a high voltage (DC or AC 50Hz) between both wires. Meanwhile, the heat resistance of laminated materials can be examined easily by using a test sample of an appropriate size to conduct a bending test or tensile strength test.

Thermal endurance estimation for Inductive Components

The above paragraphs discuss about the thermal resistance of insulators fully used in power electronic systems. At component level like transformers or inductors we have now to consider the assembling of those in a common structure. Electrical Insulation Systems (EIS) certified by the UL exist and must be mentioned. These are systems in which the designer can choose the plastic parts to be in accordance with a given thermal class of the end-product (B, F or H). If the selection can be out of such a list, the lowest insulating plastic material must be considered as the weak point.



Figure 7: Arrhenius plot for different enamel wires (UEW/130°C, UEW-F/155°C, UEW-H/180°C... AIW/220°C)

The question is then to know if the temperature reached by the insulating elements might reduce the expected lifetime of the product (if temperature will be higher than its thermal class) or, on the opposite, increase its reliability (case of lower temperature than the thermal class).

For the following study, let us consider an isolated flyback transformer designed for a 35W/100kHz switch mode power supply used in an inverter module of an electrical motor (xEV application). Its primary will be connected to the high voltage battery side (200-450Vdc) whereas the secondary low output of 17V/2Adc must be fully isolated at basic level according to IEC 61558-1/-2-16. To provide such an isolation, a creepage distance of no less than 8mm must exist. It is done by using triple-insulated wire (TIW) in all windings and a special coil-former to provide enough distance between pins and core.



Figure 8: Isolated flyback transformer construction

The constitutive elements can be described as in the below table including thermal information like TI and HIC values. The TI number comes from the UL "Yellow Card" of the material (thermal RTI data) or classification according to the IEC 85. The HIC is given as a typical value for the material. The user normally needs to contact the supplier of the plastic to get such a data not so often described in standard specifications. From this table we determine that the weak point can be the wire insulation which is of the lowest thermal class (F/155°C). The coil-former is at same level but might suffer less from the heat than the wire carrying the current and therefore subjected to frequency effects.

Parts	Material	Property	Thermal Class	TI	нтс
Core					
- Core	Ferrite	None	None	None	None
- Air gap	Air	None	None	None	None
Winding Section					
- Wire	Copper Cu-ETP	None	None	None	None
- Wire insulation	ETFE TIW	Electrical	F	155	11
- Layer insulation	Polymide tape	Electrical	Н	180	11
Other materials					
-Coil former	Bobbin made of Phenolic PM9630	Electrical	F	155	11

Figure 9: Constitutive parts and thermal properties of the transformer's elements

As predicted by theory and experience, the transformer hotspot is located at the middle of the winding and close to the air-gap due to both proximity effect between winding layers and fringing flux out from the gap. The below result shows the heating at different location and under worst case operating conditions in the equipment. The component is originally placed in an oven set at 90°C and cooled by forced convection by an oven fan. After approx. 30min of stabilization, the oven and fan are switched off and the temperatures increase as there is no forced convection anymore. After another 30min we can read the reached temperature, in a context like the real case in the inverter



Figure 10: Thermal behavior of the transformer under test at different locations

power supply unit. The plotted Eq Temp are from the correction: Eq Temp(t) = Measured Temp(t) – Ambient Temp(t) + 90° C.

As far as we can see, the hotspot inside the winding (curve no. 2.) can reach up to 160-165°C at the end of the test. Does it mean that the isolation of the wire stated at F/155°C class is not enough? The only way to properly answer to this question is to have an idea of how long this worst-case condition will apply during the whole life of the product. That's why it is often better to know a mission profile related to the application. The (automotive) customer can normally share this information in a chart as below at least as an estimation level of the mission.

From this example related to the studied transformer, we can notice that finally the exposure to high temperature over the thermal class of the system is only a few hundreds of hours (800 hours) in contrast to the total mission of approx. 53.000 hours.



Figure 11: Example of mission profile (utilization vs. estimated maximum temperature)

Max Power Operation

	-15°C	4,9%
Winding hotspot distribution in time acc. to given mission profile	47°C	38,8%
	60°C	34,4%
	70°C	7,7%
	108°C	1,5%
(worst case)	135°C	11,3%
	155°C	1,4%
	160°C	0,2%
		100,0%

Figure 12: Distribution of temperature vs. estimated utilization

Additionally, since the reference time for the TI is 20.000 hours, the total duration of 53.000 hours must also be considered as a possible failure mode. The method proposed here refers to the IEC 60216 standard to estimate the global Consumed Endurance Potential (CEP). The CEP is firstly calculated at every temperature step of the mission profile according to the Arrhenius law. Only the TI and HIC values are needed to deduce the A and B coefficients. The thermal Endurance in Continuous Operation (ECO) can then be deduced from them.

		Operating temperatures						· · · · · · · · · · · · · · · · · · ·				
		Une in the application	Reteast (*C)	п	ню	Log A	•	800	AOT	œ		
1	ETFE TOW #/355*C		-15%	155,0°C	\$1,8°C	-1.32	5145	1 641 441 280 168 %	2 601 fvr	0.00%		
			42%	155,0°C	\$1,0°C	17,72	5145	240-062-300 hr	20.603 hr	0.01%		
8.1			60%	155,0°C	BL/P/C	1,32	3145	53 459 796 hr	18 253 hr	0,03%		
			70°C	155,0°C	11,0°C	1.12	5145	18.964 197 hr	4 0.14 te	0.02%		
			308°C	155,0°C	11,0°C	-9,32	5145	606-705 W	BOD Nr	0,13%		
			3354C	155,0°C	11,0°C	-2,32	5145	77 642 Nr	6-000 hr	7,72%		
No.			155°C	155.0°C	11,010	7,32	5145	20 000 hr	720 hr	3,60%		
			39940	155,0°C	11,0°C	-7,22	5145	14 501 34	80 hr	0,55%		
1		Lifetime overview										
	Total CEP	12%										
1	Lifetime expectatory ¹¹	1	439 921 la									

Figure 13: CEP calculation from the known mission profile and (TI,HIC) data from the material

This calculation is based on Arrhenius equation of each material (refer to IEC 60216).

$$Log E(hr) = Log A + \frac{B}{T_{HS}(K)}$$

TI (Temperature Index) :

Numerical value of the temperature (in degrees Celsius) derived from the thermal endurance relationship at a time of 20000 h (or other specified time).

HIC (Halving interval) :

: Numerical value of the temperature interval (in Kelvins) which expresses the halving of the time to end-point taken at the temperature equal to TI.

ECO (Thermal endurance in continuous operation) or E(hr) : Thermal endurance in hours.

AOT (Actual Operating Time) : This is the actual time (in hours) the insulating system will operate at the given hotspot temperature.

CEP (Consumed Endurance Potential in %) :

$$CEP(\%) = \frac{AOT}{ECO} * 100$$

Figure 14: Applied formulas and definitions in the proposed method

The global CEP is calculated at the end as the sum-up of the contributions at all temperature and from it we can calculate back what would be the lifetime expectancy for the material under study. The results for the insulation of our flyback transformer is 12%, so, approx. 440.000 hours of operation for the given mission profile. With a total expected operation of 53.000 hours only we can easily conclude that there is definitively no danger for the product made of a F class insulation system even if it can reach higher temperatures than 155°C for a certain period of time and runs for more than 20.000 hours during the total lifetime. As a safety rule it is considered that a total CEP of no more than 10-20% is fully safe for the insulating system not to suffer from degradation during the mission.

Conclusion

This article reviews the common definitions of temperature stated for an insulating material to have an idea of its resistance to heat versus time. The Thermal Index (TI) or Relative Temperature Index (RTI) values are the most used as a reference at 20.000 hours. The given lifetime expectancy almost always considers a drop of 50% of the characteristics under study (electrical or mechanical properties). UL 746B, IEC 60085 and ISO 60216 are the identified standards to deal with this approach.

For magnetic components, the mix of different insulators must be considered, always relying on the lowest thermal class index of each of them. A method based on the Arrhenius law was presented to be able to perform calculations of the lifetime expectancy for a given mission profile. The Halving-Interval Coefficient (HIC) must be known from plastic suppliers as a given, in its role as an independent variable. According to the result as total Consumed Endurance Potential (CEP), a conclusion about the compliance of the insulating system regarding the mission profile can be drawn.

This approach is even more useful when developing electrical power components for the automotive sector (xEVs) for which heating and lifetime are the main parameters for design optimization in terms of sizing and level of loss acceptance.

About PREMO - Perspectives

PREMO is a Spain-based company engaged in the development, manufacture and sales of electronic components with a special focus on the growing market of xEV, smart metering and market segments including automotive, telecommunications and industrial electronics. Our product portfolio includes NFC and RFID antennas, power transformers, inductors and chokes, current sensors, EMC filters, PLC components and accessories. In addition to our broad range of standard components, off-the-shelf products, PREMO designs custom solutions to fit customer requirements

For power magnetics embedded in OBC or DCDC converters, the size reduction is a must which leads to more heat generated by more losses in a smaller volume. To guarantee the reliability of the parts over the lifetime, the cooling efficiency of the solution has become a key factor.

For the recent years PREMO has been testing many thermal conductive resins and compounds (more than 30 different formulations in fact) to try to optimize the performance-to-cost compromise. Of course, such additives will also help in the mechanical fixing and isolation of the part in the application. The goal was to find the best mixing to offer the most competitive solution.



Figure 15: Fully finished unit with integrated CoolMagTM compound encapsulation

TPICAL PROPERTIES			
	COOLMAG 28 Resin	COOLMAG 28 Hardener	COOLMAG 28 mixed
Appearance	Beige Liquid	Beige Liquid	Beige Liquid
Viscosity, cps@ 25%C	32000	32000	24000
Rotio	1	1	
Pot Life (min)			60
Cured time (min)(125RC)			40

*Property volues represent typical results only and are not to be considered specifications.

TYPICAL CURED PROPERTIES**

Thermal Conductivity, W/mk (Hot Disc Transient Method)	1,5
Hardness (shore A, UNE-ISO 7639-1:20111)	42
Tensile Strength, N (ISO 37:2011)	11.25
Elongation at Break, % (ISO 37-2015)	50
Water Absorption % (ASTM DS70 - 98.2018)	0.04

**Property values represent typical results only and are not to be considered specifications. Cure schedule of 60 minutes at 125PC.

Figure 16: CoolMag28TM characteristics from KADION (1.5W/mK)

After massive investment and research in the field, today PREMO uses and recommends the CoolMagTM resin references developed in collaboration with KADION Spanish company which show the best compromise between thermal as well as mechanical performances and cost.

www.grupopremo.com

www.kadion.com

About the Authors



Patrick Fouassier, R&D Manager Inductive Components PREMO FRANCE

Patrick, Engineer degree and PhD. in electrical engineering, has more than 20 years of experience in magnetic components related to signal and power electronics. He studied at Grenoble INPG/ENSE3 engineering school and did his thesis in G2ELab close to the existing as PSP Managare at MICROSPIRE

Alps. After his prior position as R&D Manager at MICROSPIRE (now part of EXXELIA Group), a French company oriented towards professional markets like defense, avionics and space, he joined the Spanish PREMO Group in 2008 when participating in the creation of the PREMO FRANCE office located in Grenoble area.

Now his activity within his team is fully focused on the development and project management of innovative solutions for the automotive sector with components for battery chargers and DCDC converters from some kW to tens of kW used in new electrical and hybrid cars. His R&D expertise is on a worldwide scale and in a fully multicultural context from customer technical support to internal training.



Abdelkader Birch, R&D Engineer Inductive Components PREMO FRANCE

Abdelkader, Engineer degree in electrical engineering, has more than 11 years of experience in magnetic components related to power electronics.

He studied at Grenoble INPG/ENSE3 engineering school from where he got his electri-

cal engineer degree. Previous position: 8 years of experience in design of magnetic components for railways applications in the company TRANSRAIL BOIGE & VIGNAL

He joined PREMO Group in 2016 to develop magnetics within the R&D team of PREMO FFRANCE. His activity is focused on the development and project management of innovative solutions for the automotive sector with components for battery chargers and DCDC converters from some kW to tens of kW used in new electrical and hybrid cars. His expertise in thermal endurance approach and lifetime calculation is fully thanked here for application to the presented flyback transformer case.

DrMOS Power Modules



DrMOS

▶ (30A - 65A)

- Industry leading Trench MOSFETs with 20m Ω^*nC FOM
- Wide range of package solutions from QFN3.5x4.5 to QFN5x5
- Compatible with many common VR controllers for various CPU and GPU platforms
- High peak current capability to handle challenging transient response

Our latest generation of DrMOS power stage products provides flexible, high efficiency, and easy-to-use solutions for computing CPU and graphic card GPU applications.



ALPHA & OMEGA SEMICONDUCTOR

Automotive Display Power Management IC

Designers of automotive electronic systems can now increase the number of displays per vehicle while reducing design complexity by using the MAX16923 4-output display power IC with watchdog timer from Maxim Integrated Products. By replacing four or five discrete ICs with a single power management solution, the MAX16923 significantly



shrinks solution size and makes it easier for automotive designers to increase the number of displays from two to five per vehicle, or even more. The number of automotive displays per vehicle continues to grow as OEMs seek to make cars more attractive with advanced instrument clusters, infotainment, heads-up displays, center displays, rear-seat entertainment and smart mirror applications. Designers struggle with the complexity of adding these screens because the required power supply circuitry competes for space with a myriad of other electronic systems inside the car. The MAX16923 offers high integration with four power rails, featuring both a high-voltage and low-voltage buck converter, a high-voltage and low-voltage low-dropout (LDO) regulator, electromagnetic interference (EMI) mitigation and a watchdog timer in a single IC. Its high level of integration can reduce an automotive power solution from four or five ICs down to one chip, without making the temperature rise significantly.

www.maximintegrated.com

Programmable DC Load Product Series

Vitrek introduces the DL Series of Digital, Programmable DC Loads, designed to support the testing requirements for the latest generation of off-line power supplies, dc-dc converters and LED drivers. The DL Series is also equipped to handle a wide range of battery testing requirements. The devices are offered in three power ratings (125W,



250W and 500W), each with input voltages of 0-150V or 0-500 VDC. Unlike comparable programmable DC loads, the DL Series is capable of supporting loading sequences utilizing constant voltage (CV), constant resistance (CR), constant current (CC) and constant power (CW) in any combination in single or arbitrary sequences of up to 100 steps.

The DL Series provides high-current transient loading capability twenty times higher than other units in this class while also being capable of generating μ A loads. Measurement accuracy is typically an order of magnitude better at lower loading levels and double that of competing devices at higher loads. The instruments allow for a current or power sweep of up to 500 steps in each direction to and from set values and a voltage dependent current loading mode for complex variable output supplies. Standard OCP/OPP/OTP/OVP features and battery test modes are among other loading modes also included.

www.vitrek.com

E Cores Solve Challenging Power Conversion Applications

Micrometals continues to expand their prototyping and custom core capabilities with the expansion of E Core variations available. Micrometals E Cores are renowned for their performance and quality by delivering exceptional part-to-part consistency. With over 20 industry standard E Core sizes, from 12.7mm to 210mm, in both Iron and Alloy materials, Micrometals leads the industry in COTS shapes and materials. One significant advantage to Micrometal's E Cores are their dis-



tributed gap materials, which do not require any gapping to improve saturation like ferrite cores. The expanded prototyping and customization capabilities allows Micrometals to customize their standard E Cores by shaping the outer legs or center post to improve the usability for customers. This customization permits the use of pre-wound coils for higher winding density compared to traditionally square shaped E Cores. Further, these custom E Cores deliver superior performance compared to similar shaped cores that are custom tooled. Jim Cox, Micrometals President commented "For decades, our customers have trusted Micrometals cores to deliver exceptional reliability, consistency and performance. With these expanded customization capabilities we deliver that same performance and consistency, but with more application friendly features that exceed our customer's expectations in terms of performance and functionality. Customer are also thrilled that they can get these as prototypes or production parts without any tooling costs, allowing them to test multiple designs without a large investment."

www.micrometals.com

SiC-Based Power Converters Using Gate Drive Evaluation Platform

Littelfuse, Inc. announced the Gate Drive Evaluation Platform (GDEV). The evaluation platform helps designers evaluate SiC MOSFETs, SiC Schottky diodes, and other peripheral components like gate driver circuitry, so that they can better understand how silicon carbide technologies will behave in converter applications under continuous operating conditions. The GDEV offers quick connect header pin terminals that allow for rapid and consistent comparison of different gate drive circuits, unlike most other SiC evaluation platforms. The GDEV supports an 800 V DC link input voltage and up to 200 kHz switching frequency. "The Gate Drive Evaluation Platform (GDEV) is a critical addition to our SiC technology portfolio because SiC is still relatively new and there are some unknowns surrounding the operating characteristics under various conditions," said Corey Deyalsingh, Director, Power Control at Littelfuse. "The GDEV helps engineers understand the operating characteristics of SiC devices. By utilizing this evaluation platform, designers will



be better informed about the incredibly energy efficient opportunities that SiC technologies present. Equipped with that knowledge, we anticipate that designers will be more likely to incorporate SiC into their future designs."

www.littelfuse.com

New PST14X DC-DC 320W Very Low Profile Conduction Cooled

160 x 50 x 25 mm Input 12 & 24V Output 3V3 to 48Vdc MIL-STD 1275, 810, 461 option Vicor DC-DC Converter Based



Aluminum Electrolytic Snap-in Capacitors

Cornell Dubilier Electronics, Inc. (CDE) introduces its 381LL series of long-life snapin aluminum electrolytic capacitors. The series, designated with an expected life of 8,000 hours at full-rated conditions, demonstrates superb stability in capacitance and DC leakage current over time on test. The snap-in series is targeted for use in critical applications where long life and reliability are paramount. Capacitance values range from 740 μ F to 100,000 μ F at working voltages of 16 to 250 WVDC with ripple current ratings up to 10 Amps @ 105 °C. The snap-in series



CORNELL DUBILIER

8,000 Hour, 105* C Aluminum Electrolytic Snap-in Capacitors is available in two pin configurations in the smaller diameters with 4 and 5 pin options in the larger diameters.

General applications include any circuit requiring high capacitance with low ESR, high ripple current and long life. This includes switch-mode power supplies, UPS systems, solar and other high-power inverters. CDE's 381LL, long-life aluminum electrolytic capacitors are available from the company's franchised distributors.

www.cde.com

Electrolytic Capacitors with Solder Lugs

Aluminium electrolytic capacitors with solder lugs are needed in applications where the capacitor is separate from the electronic circuitry and cannot be mounted directly on the printed circuit board. In this case, the solder lugs allow flexible connection by means of a soldered cable. FTCAP (part of the Mersen Group) offers different series with numerous solder lug variations in this product area. The fully welded design increases the life of the capacitors.

"There are two basic types of solder lugs or solder pins: with closed and open eyes", explains André Tausche, Managing Director of FTCAP. "The difference is that in the second version the cable can be fed through the eye. But we also offer numerous variations within these two categories. This allows us to offer customers maximum flexibility in connecting the cable." In addition to the extensive product range, solder lug capacitors from FTCAP feature a fully welded design: The life of these capacitors is much longer than that of riveted models. FTCAP electrolytic capacitors with solder lugs provide reliable solutions with high energy density, which in turn allows high discharge currents. Potential areas of application for solder lug



capacitors include switch-mode power supplies, computers, industrial electronics, and drive systems.

www.ftcap.de

Non-Isolated Converter Saves Board Area

TDK Corporation announces the addition of the TDK-Lambda brand i6A4W SIP (Single Inline Package) to the popular i6A series of 250W rated non-isolated DC-DC converters. Requiring less than 3 cm2 (0.47in2) of board area, this provides a saving of 60% over the i6A 1/16th brick package.

Offering adjustment ranges of up to 3.3V to 40V the 10 to 20A rated step-down converters can accept input voltages between 9 and 53V. The i6A4W series allows the creation of multiple, high current output voltages from a single output 12V, 24V, 36V or 48V AC-DC power supply, and is suitable for use in communications, industrial, test and measurement, broadcast and portable equipment.

With overall dimensions of 33 mm x 11.4 mm x 24.8 mm (L x W x H), these converters have ultra-high efficiencies of up to 97%. This allows operation in ambient temperatures of -40° C to $+125^{\circ}$ C with the minimised output derating, even in low airflow and high ambient temperature conditions. The product's optimised dynamic voltage response reduces the need for external capacitors, saving cost and additional board space. Standard features include a trim pin for output



voltage adjustment, + remote sense, remote on-off (positive or negative logic), input under-voltage, over-current and over-temperature protection. Power good, operating frequency synchronisation and output sequencing are available as options.

www.emea.lambda.tdk.com/i6a

Intelligent Power Devices Enabling Standalone System Protection

ROHM announced the availability of the BV2Hx045EFU-C, a family of high voltage (41V) dual channel output high side switch (Intelligent Power Devices, IPD) optimized for automotive ECUs in transmission



control, engine control, and other vehicle systems. IPDs are semiconductor devices that protect electronic circuits from breakdown (i.e. due to overcurrent during abnormalities). Unlike conventional fuses, IPD as semiconductor fuses can protect circuits without degrading or breaking down, making it possible to achieve maintenance-free systems. The BV2Hx045EFU-C are the industry's first high-side IPDs capable of providing standalone protection against overcurrent by incorporating an original overcurrent protection function. Conventional IPDs only protect against inrush current at startup, so MCUs and overcurrent detection ICs are needed for protection of steady-state currents, and there is still the possibility of an out of control situation due to compatibility issues with subsequent circuits connected to the IPD output. In contrast, this new series can protect the system against both inrush and steady state overcurrent, ensuring greater system safety by providing a high reliability solution with fewer parts compared to conventional products. In addition, the overcurrent protection range can be adjusted with external components to enable broad compatibility.

www.rohm.com/eu

Compact DC-DC Converter in Chassis Mount Format

Power System Technology announces the introduction of PST14X family on its ecommerce platform. Available March 1st, by connecting to www.powersystemtechnology. com, more than 20 different models of the PST14X family with their options and accessories can by ordered online. Thanks to optimized logistics and dedicated manufacturing process, an express delivery in 1-2 weeks for limited quantities can be achieved. PST14X is a very high power density 320W DC-DC converter in conduction cooled format. In a very small package 160*50*25mm, with input voltage ranges of 9-50Vdc, 18-36Vdc, 16-

50Vdc, PST14X incorporates EMI filtering, input active reverse polarity and transient



protection, output protections, very robust mechanical package and connection, required in most of the severe environment for industrial, railways, defense type of applications. The output can be configured in many different output voltages from 3,3V to 48Vdc, other possibilities are even possible as semistandard versions. With the -MV option, the converter is protected against surges and transients MIL-STD-704 and MIL-STD-1275, EMI filtered built to meet MIL-STD 461 and ruggedizzed according MIL-STD-810.

www.powersystemtechnology.com

Low R_{DS(on)} MOSFET

Nexperia announced the release of its lowest-ever $R_{DS(on)}$ power MOSFET. The PSMNR51-25YLH sets a new standard of 0.57 m Ω at 25 V. Utilising Nexperia's NextPowerS3 technology, this performance



is offered without compromising other important parameters such as maximum drain current ($I_{D(max)}$), Safe Operating Area (SOA) or gate charge Q_G . Very low $R_{DS(on)}$ devices are required in many applications such as ORing, hot-swap operation, synchronous rectification, motor control and battery protection, to reduce I²R losses and increase efficiency. However, some competing devices with similar $R_{DS(on)}$ values suffer from reduced SOA – a measure of the ruggedness of the MOSFET – and reduced $I_{D(max)}$) ratings due to shrinking cell-pitches. Nexperia's PSMNR51-25YLH MOSFET offers a maximum drain current rating up to 380 Amps. This parameter is especially important in motor control applications where motor-stall can result in very high current surges for short periods, which the MOSFET must withstand for safe and reliable operation. Some competitors provide only computed $I_{D(max)}$ whereas Nexperia demonstrates continu-

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ous current capability up to 380 Amps. The device is packaged in LFPAK56, Nexperia's 5mm x 6mm Power-SO8 compatible package, offering a high performance copper-clip construction which absorbs thermal stresses, increasing quality & lifetime reliability.

www.nexperia.com/nextpowers3

Gate Drivers Achieve Automotive Qualification

Power Integrations announced the launch of its automotive-qualified SID1181KQ SCALE-iDriver[™] gate driver for 750 V-rated IGBTs. The part expands the company's range of auto-qualified driver ICs, following the introduction of the 1200 V SID1182KQ driver IC. Compact, efficient and highly robust, the driver IC uses Power Integrations'



high-speed FluxLink[™] communications technology to ensure system safety even during fault conditions. FluxLink technology dramatically improves the reliability and isolation capability of the new AEC-Q100qualified gate drivers, replacing optocouplers and capacitive or silicon-based inductively coupled solutions. SCALE-iDriver devices also include critical protection features such as desaturation monitoring, primary and secondary Undervoltage Lock-out (UVLO) and Advanced Soft Shut Down (ASSD) that protect the switch during short-circuit turn-off.

Comments Michael Hornkamp, senior director of marketing for automotive gate-driver products at Power Integrations: "The SCALEiDriver family with FluxLink technology supports safe, cost-effective designs for a wide range of IGBT drivers for electric vehicle applications including powertrain, on-board chargers and charger stations, and other high reliability drivers and inverters."

SCALE-iDriver ICs minimize the number of external components required, eliminating tantalum and electrolytic capacitors and simplifying the isolated power supply, requiring only one transformer secondary winding. A simple two-layer PCB can be used, further increasing design simplicity and easing supply-chain management.

www.power.com

www.bodospower.com



CIPS 2020

11th International Conference on Integrated Power Electronics Systems

March, 24 – 26, 2020, Berlin, Germany

www.cips.eu







EEE



port an output voltage range of 0.6V to 5.5V. The devices support frequency synchronization, PolyPhase operation, selectable Burst Mode operation, 100% duty cycle and low IQ operation. Their high switching frequency and a current mode architecture enable a very fast transient changes without sacrificing stability. The

Operating over an input voltage range of 2.7V to 17V, the LTM4668 and LTM4668A sup-

response to line and load changes without sacrificing stability. The LTM4668 and LTM4668A are available today in 6.25mm x 6.25mm x 2.1mm BGA packages.

Quad-Output DC/DC

µModule Regulators

for telecom, networking and industrial applications.

ANALOG DEVICES

LTM4668A

Analog Devices, Inc. introduced the LTM4668 and LTM4668A µModule[®] regulators, quad-output DC/DC regulators with up to 4.8A output capability. The devices integrate switching controllers, power FETs, inductors and support components, easing the design process while reducing power consumption and board space. They are ideal

www.analog.com

Fuses Designed for Automotive and In-Rush Current Applications

Bel Fuse-Circuit Protection announces their 0680L Series of ceramic surface mount fuses with in-rush current withstand capability in a 2410 SMD package size. These slow blow fuses are designed for automotive and applications which require high DC voltage ratings and high DC interrupting ratings.



Bel's 0680L Series fuses are compatible with the 260°, IR Pb-free solder process and feature a current rating from 375mA to 12A and a wide operating temperature range of -55° to 125°C. These fuses are also AEC-Q200 compliant, RoHS compliant (with exemption 7(a)), halogen free (MSL = 1)

and lead free. In addition, they are packaged in tape and reel for the auto-insert SMD process and meet the Bel automotive qualification, which is based on the AEC-Q test plan. Typical application use for the 0680L Series includes notebooks, LCD/LED monitors and TVs, PC computers and office electronic equipment, industrial and medical equipment, PoE, PoE+, power supplies, storage systems, telecommunication systems, wireless base stations, white goods, game consoles and battery charging circuit protection applications which require slow blow or time delay fuses to power the 2410 chip.

The 0680L Series is in stock with Digi-Key and Mouser in up to 1,000 or 5,000 pieces in tape and reel. Product samples also available upon request.

www.belfuse.com

Signal Integrity Debugging with Jitter Decomposition

Rohde & Schwarz has developed method for analyzing the individual components of jitter, providing electronic circuit designers with previously unavailable in-depth knowledge invaluable for debugging high-speed signals. As data rates increase and voltage swings decrease, the jitter in digital interfaces becomes a significant percentage of the signaling interval, and potential source of failures. Increasingly, engineers require tools that accurately characterize the signal jitter including the break-down into its individual components.



The R&S RTO-/ RTP-K133 advanced jitter analysis option introduces an analytic approach to separating the individual components of jitter such as random jitter, and deterministic jitter components, such as data dependent and periodic jitter. This approach is based on a parametric signal model that fully characterizes the behavior of the transmission link under test. A core benefit of this Rohde & Schwarz



method is that the jitter model includes the complete waveform characteristic of the signal under test, in contrast to conventional methods that reduce the data to a set of Time Interval Error measurements. The result is consistent measurement data even for relatively short signal sequences, plus previously unavailable information such as the step response, or a distinction between vertical and horizontal periodic jitter.

www.rohde-schwarz.com

AC/DC Modules Meet ecodesign Specifications

Dengrove Electronic Components is now stocking the RECOM RAC04-K/277 AC/DC 4-Watt power modules, which meet the latest EU ErP Lot 6 ecodesign specifications for standby and off-mode that apply to industrial and consumer products. Able to supply short-term



overloads of up to 150%, the modules are a cost-effective solution for powering industry 4.0 and industrial automation, IoT and smartbuilding devices, and household appliances. With a wide operating temperature range of -40°C to +90°C with power derating, and able to operate at up to 5000 metres altitude, RAC04-K/277 modules can be deployed in stressful environments. The series offers a choice of 3.3V, 5V, 12V, 15V and 24V output voltage and the full-load output power is available from -40°C to 75°C.

Ease of use is another strength of the RAC04-K/277 series. No external components are needed to configure a fully functioning AC/DC converter with 80-305V AC input range and a wide margin to class-B emissions requirements. Fully encapsulated in a 36mm x 26.5mm x 17.4mm 6-pin case, the modules are convenient and compact for use in space-constrained applications. The RAC04-K/277 series meets high safety standards, with reinforced class II isolation rating for floating outputs and certified according to IEC/EN/UL/CSA 62368-1 for IT and AV equipment, EN 60335 for household appliances, and EN 61010 for measurement control and laboratory use.

www.dengrove.com

Current Sensors Combine Small Size and High Performance

ICE Components announces a series of current sensors for use in a wide range of pcb mount applications. The ISE current sensors measure both DC and AC current from 50A up to 200A. The sensors include an integrated core to improve accuracy and provide protection



from external stray fields. The ISE series is available in four standard current ratings of 50A, 100A, 150A and 200A. For applications of over 5k pcs the current sensors can be programmed for unique current ranges or output slopes. They are rated for an operating temperature range of -40 to +130 degrees C.

Key Features Include:

- Integrated bus bar for easy application onto your pcb
- Programmable current measurement slope
- 25.4mm x 18mm footprint and 10.8mm low profile height
- Integrated shield for EMC immunity
- 3 µ-Sec response time (200kHz bandwidth)
- High level of output accuracy
- Outstanding linearity. Predictable output vs. current measurement
- Operates off an input voltage of 5 VDC and provides a 0.5 to 4.5
- VDC output voltage that is ratiometric to the input.

www.icecomponents.com/ise-a-800-series

DC/DC Converter for Industrial & Railway Applications

TRACO POWER announces their THN 10 WIR series of 10 watt highdensity DC/DC Converters in the industry standard 1" x 1" footprint and qualified for rugged industrial and railway applications and certified to EN 50155 and EN 61373 standards. The THN 10WIR series



of ruggedized 10 Watt DC/DC converters are designed and manufactured for high reliability in harsh environments. The converters have ultra-wide wide 4:1 input ranges of 9-36, 18-78 and 36-160 VDC with single and dual outputs ranging from 3.3-24 VDC. The innovative design provides high efficiencies up to 90% and enables a full load operating temperature range from -40 to +80°C without derating and increased resistance against electromagnetic interference, shock/ vibration and thermal shock. All models are safety approved to IEC/ EN/UL 62368-1 with CB Report and EN 50155 certified qualifying them for harsh environments in industrial, railway and transportation systems and further qualified for fire behavior of components per EN 45545-2. Features include: an internal EN 55032 class A input filter; input under-voltage-lockout; short circuit protection; remote On/Off; and output voltage trim. All models offer extreme reliability with an MTBF in excess of 2.3 million hours and are supported by TRACO POWER'S 3 year warranty.

www.tracopower.us/tthn10wir

Source-Down 25 V Power MOSFET

Infineon Technologies is focusing on system innovation with enhancements on component level by addressing the challenges of modern power management designs. The Source Down is the new industry standard packaging concept. The first wave of power MOSFETs launched in this new package is the OptiMOS TM 25 V in a PQFN 3.3x3.3 mm. The device sets a new industry benchmark in MOSFET performance, reducing on-state resistance (R DS(on)) and offering superior thermal management capability to the marketplace. The product is well-suited for a wide range of applications such as drives, SMPS (including server, telecom, and OR-ing) and battery management.

The new package concept connects the source potential (instead of the drain potential) to the thermal pad. Along with the enabled new PCB layout possibilities, this helps achieving ever higher power density and performance. Two different footprint versions are released – the Source-Down Standard-Gate and the Source-Down Center-Gate in a PQFN 3.3x3.3 mm package. The Source-Down Standard-Gate



footprint is based on the current PQFN 3.3x3.3 mm pinout configuration. The location of the electrical connection remains the same, simplifying the drop-in replacement of today's standard Drain-Down packages with the new Source-Down package. For the Center-Gate version, the gate-pin is moved to the center supporting easy parallel configuration of multiple MOSFETs.

www.infineon.com/pgfn-3-source-down

Gate Drivers for Fast Switching SiC Power Modules

CISSOID delivers robust Gate Drivers for XM3 SiC MOSFET Power Modules from Wolfspeed. Aiming high power density converters, the Gate Driver board safely drives the fast switching SiC power modules to achieve low losses and operates in high temperature environments found inside space-constrained motor drives, compact power supplies or fast battery chargers.



The CMT-TIT0697 Gate Driver board has been designed to be directly mounted on CAB450M12XM3 1200V/450A SiC MOSFET Power Modules. With an on-board isolated power supply delivering up to 2.5W per channel without derating up to 125°C (Ta), the gate driver can drive XM3 modules up to 100KHz, enabling high power density. Peak gate current up to 10A and immunity to high dV/dt (>50KV/µs) make possible to drive the power module with zero gate resistance achieving minimum switching losses. The board withstands isolation voltages up to 3600V (50Hz, 1min) and offers creepage distances of 14mm. Protection functions such as undervoltage lockout (UVLO), Active Miller Clamping (AMC), Desaturation detection and Soft-shut-down (SSD) ensure the safe drive and reliable protection of the power module in case of fault events.

www.cissoid.com

Jetting Solder Paste

Indium Corporation continues to develop innovative solder paste solutions to fit customers' needs. PicoShot™ NC-5M is designed for customers needing a no-clean halogen-free SAC305 solder paste for their Mycronic jetting systems or add-on and



repair modules. PicoShot™ NC-5M jetting solder paste is the first material to come out of Indium Corporation's new partnership with Mycronic, a global leader in dispensing and jet printing equipment. PicoShot™ NC-5M is a no-clean halogen-free solder paste approved after joint Indium/Mycronic technical development with Mycronic's MY 600/700 jetting systems. PicoShot™ can be used in standalone applications, such as system-inpackage (SiP), jetting into cavities, stencilreplacement, shield attach, and microBGA. It also complements the stencil printing of Indium8.9HF. Designed as a no-clean solder paste, PicoShot™ can be cleaned easily with industry standard cleaning solutions. Indium Corporation also offers a PicoShot™ NC-5M conditioner (purging gel) designed to allow the rapid purging, cleaning, and long-term storage of jetting, dispense, and microdispense systems without the use of liquid solvents. PicoShot™ Conditioner C-1 is a chemically benign, bright blue-colored translucent, viscous gel that aids in visual endpoint detection and prevents inconsistent dispense volumes and clogging caused by solder paste dry-out.

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SMD Fuse Family Extended

The proven UMF 250 SMD fuse family is extended by a 15 A version. SCHURTER is now offering the UMF 250 in a total of 15 rated



currents between 500 mA and 15 A. It is particularly suitable for electromobility applications with higher rated currents.With its quick characteristics (small melting integral) according to IEC 60127-4, the UMF 250 is the logical addition to the successful UMT 250 range. It is sealed against potting compound to achieve a hermetic seal for use in intrinsically safe applications according to ATEX and IECEx requirements. Thanks to its high cycle stability and minimal temperature derating, it is extremely robust and resistant to ageing. Thanks to its low internal resistance, the UMF 250 is ideally suited for primary and secondary protection on SMD circuit boards. Applications of the UMF 250 include the protection of battery-powered systems with high switch-off capacities of 500 A @ 125 VDC (e.g. electromobility). The fuse is also suitable for primary protection in the AC range, for example in voltage regulator modules and charging stations. The UMF 250 can is a halogen-free and RoHS-compliant fuse for lead-free soldering processes. The solder surface compatibility with the most important competitor products allows SCHURTER to offer the UMF 250 as a replacement product. The fuse is cURus approved.

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