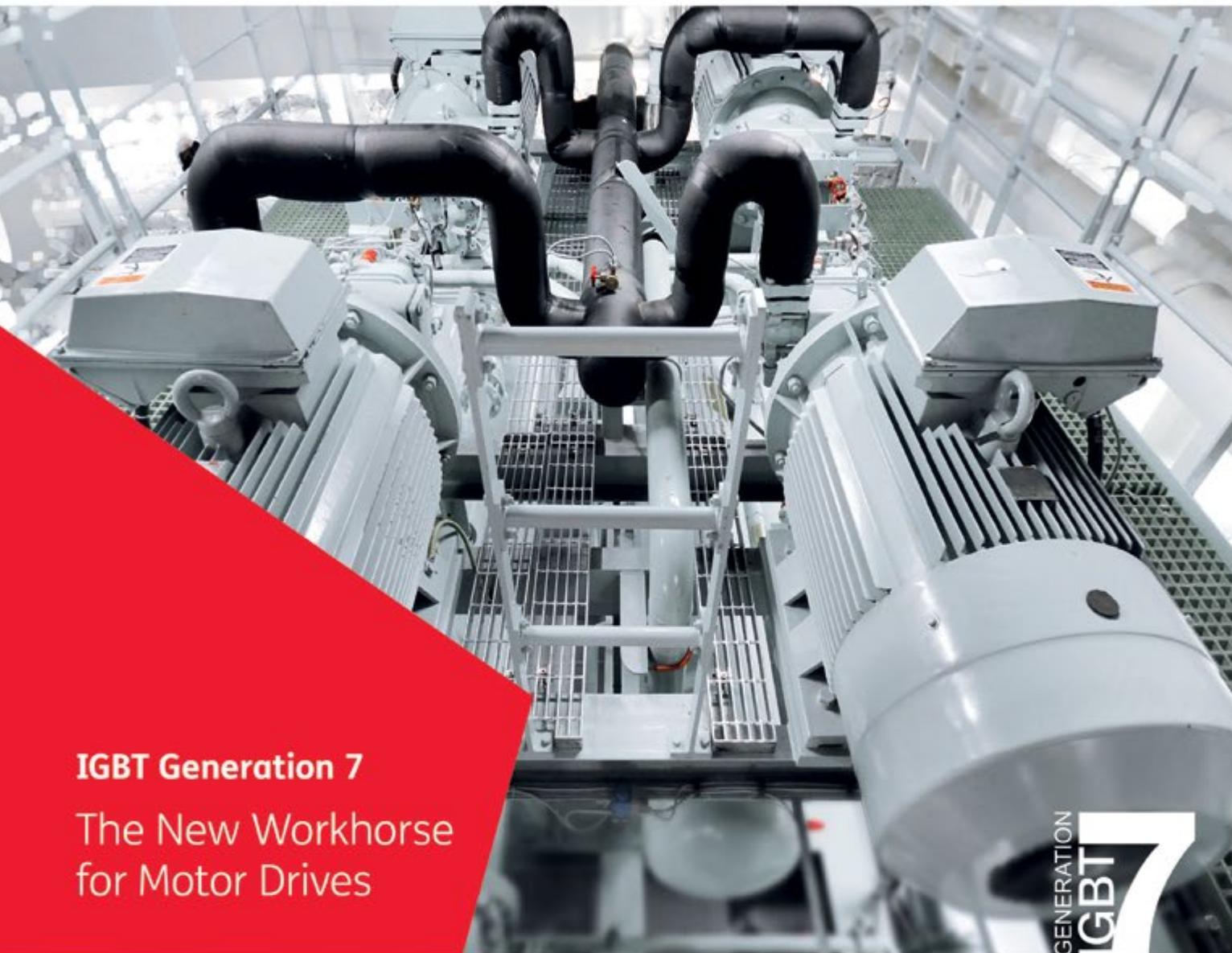


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April 2020



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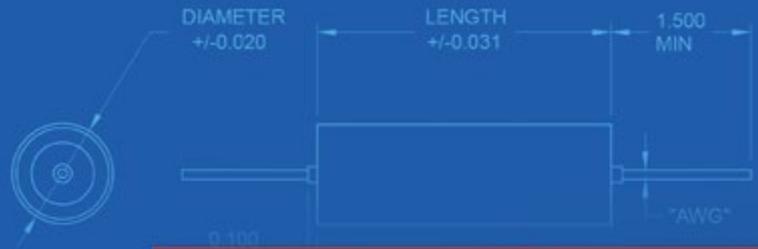
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www.bodospower.com

Challenging Times

My planned opener for the April issue is of course now obsolete. Usually, writing a viewpoint for April is one of the easiest things to do: APEC only a few days ago, lots of stories to tell about the latest products presented and interesting meetings with partners and friends. Also, PCIM Europe is normally just a few weeks away and we would be working on our preview. But now PCIM Europe is also postponed. Both cancellations, along with so many others are the right decision in my opinion – whether these decisions were made by the event organisers or the authorities. In these difficult times it is simply not appropriate to hold or attend mass events. It is up to each individual to do everything possible to help fight the spread of the corona virus. My thoughts are with all those who face this challenge every day in the medical sector.

These cancellations are a bitter loss not only for the teams of APEC and PCIM, not only economically, but also for the presenters of the conference and the exhibitors. All the preparation and the work that has been invested, all the hours in the evenings which, mostly in their free time, people worked on their presentation – all these efforts should not have been in vain. Now, more than ever, it is up to the media to deliver your message. In times when such extraordinary, external circumstances, make direct contact with your audience impossible, publications can be a reliable carrier of information. It is important to stay up to date and to keep your message alive.

No one can predict how long this situation will last. The situation is very dynamic, and you will understand that the event calendar you can find below starts in July this time. The one on our website is updated daily to keep you informed. You may find it a useful source when it comes to travel planning. We are getting very positive feedback on this feature of our new site!



Bodo's preparations for the podium discussion during PCIM later this year continue unchanged. The topic of wide-band-gap is still hot, you can find more about it on the following pages. But in parallel to this we are working on alternatives for the worst-case scenario. As I previously mentioned the media, both print and digital, must then step up. I think that companies would do well to consider alternatives as well. I visited the first virtual exhibition stand and I think that this is an interesting idea that could be pursued further.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving North America efficiently. If you are using any kind of tablet or smart phone, you will find all of our content optimized for mobile devices on the updated website www.bodospower.com. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com

My Green Power Tip for the Month:

I am not sure if a Green Power Tip is relevant at this moment. If there is one positive aspect about the virus, it might be that the world has almost stopped for a while. All the travel bans and the slow down of everyday life are at least a positive impact on the environment.

Stay healthy

Events

PCIM Asia 2020

Shanghai, China July 1-3
<https://pcimasia-expo.cn.messefrankfurt.com/>

Electronica China 2020

Shanghai, China July 3-5
www.electronica-china.com

DAC 2020

San Francisco, CA, USA July 19-23
www.dac.com

SEMICON West 2020

San Francisco, CA, USA July 21-23
www.semiconwest.org

PCIM Europe 2020

Nuremberg, Germany July 28-30
<https://pcim.mesago.com>

CIWEME Shanghai 2020

Shanghai, China July 29-31
<http://cn.coilwindingexpo.com>

Thermal Management 2020

Denver, CO, USA August 6-7
www.thermalconference.com

World Battery Expo 2020

Guangzhou, China August 16-18
www.battery-expo.com

EPE ECCE 2020

Lyon, France September 7-11
www.epe2020.com



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PCIM Europe Postponed



Due to the increasing spread of covid-19 in Europe, Mesago Messe Frankfurt GmbH has decided to postpone the PCIM Europe exhibition and conference from 5 – 7 May 2020 to 28 – 30 July 2020. The venue remains the Nuremberg Exhibition Centre.

Visitor tickets already purchased are valid for the new date. "The dynamic developments around covid-19 in Europe require all exhibition organizers to continually assess the situation. We very much hope that we have acted in the interest of all parties involved with this postponement and that we can thus make a joint contribution to delaying the spread of covid-19 in Europe," stated Petra Haarburger, Managing Director of Mesago Messe Frankfurt GmbH.

www.pcim-europe.com

Financing to Advance its GaN Power Conversion Business

Transphorm announced it raised \$21.5 million in a private placement equity financing. Prior to the financing, Transphorm Technology completed a reverse merger with Peninsula Acquisition Corporation, a public Delaware corporation, whereby Transphorm became a wholly owned subsidiary of Peninsula. Following the merger, Peninsula changed its name to Transphorm, Inc., and will continue the historical business of Transphorm. Previous members of Transphorm's Board of Directors, David Kerko, Eiji Yatagawa, Brittany Bagley, Mario Rivas and Dr. Umesh Mishra will remain as directors of the Company. "We are thrilled to announce this new equity financing which will support and accelerate our product development, manufacturing, and sales for our GaN power solutions," said Mario Rivas, CEO. Mr. Rivas continued, "We believe the success of this financing demonstrates confidence and support in Transphorm's team, technology and products by both our current partners as well as our new investors."

"Our core capabilities in GaN epitaxy, design, process and circuit applications have positioned us well to innovate and address the power conversion systems needs of our customers," said Dr. Primit Parikh, Co-founder and COO. "We have created an integrated device model and developed highly reliable, high performance GaN device technology, as well as amassed one of the largest intellectual property portfolios in the GaN power industry," Dr. Parikh added.



www.transphormusa.com

Acquisition Will Accelerate GaN Expertise

STMicroelectronics announced it has signed an agreement to acquire a majority stake in French Gallium Nitride (GaN) innovator Exagan. Exagan's expertise in epitaxy, product development and application know-how will broaden and accelerate ST's power GaN roadmap and business for automotive, industrial and consumer applications. Exagan will continue to execute its product roadmap and will be supported by ST in the deployment of its products.

Terms of the transaction were not disclosed and closing of the acquisition remains subject to customary regulatory approvals from French authorities. The signed agreement also provides for the acquisition by ST of the remaining minority stake in Exagan 24 months after the closing of the acquisition of the majority stake. The transaction is funded with available cash.

"ST has built strong momentum in silicon carbide and is now expanding in another very promising compound material, gallium nitride, to drive adoption of the power products based on GaN by customers across the automotive, industrial and consumer markets" said Jean-Marc Chery, President and CEO of STMicroelectronics. "The acquisition of a majority stake in Exagan is another step forward in strengthening our global technology leadership in power semiconductors and our long-term GaN roadmap, ecosystem and business. It comes in addition to ongoing developments with CEA-Leti in Tours, France, and the recently-announced collaboration with TSMC."



www.st.com

Battery Cell Competence Center

Keysight Technologies announced the use of Keysight's Scienlab Battery Test Solution for comprehensive battery cell test in the recently opened BMW Group Battery Cell Competence Center in Munich, Germany. Keysight's Scienlab Battery Test Solution is comprised of Keysight's Scienlab Battery Test Systems to provide precise measurement results, and PathWave Lab Operations software, which ensures an optimized test lab operation by managing resources, hardware and information. Comprehensive functions provided by the solution support the planning and execution of test procedures including schedule definition, management, control and monitoring of the battery test systems and device under test. It also analyzes test results as well as the overall efficiency of the lab to identify potential improvements. "Our long-standing partnership with the BMW Group is



based on mutual inspiration and collaboration as we work together to address the challenges associated with automotive power train electrification," stated Dr. Michael Schugt, senior manager of Keysight's Automotive and Energy Scienlab E-Mobility business. "We are proud to support the car manufacturers objectives with our innovative solutions and extensive expertise in battery test to continue driving e-mobility forward."

www.keysight.com

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SiC: FROM NICHE TO MASS MARKET

As technology driver ROHM has pioneered in SiC development. Meanwhile, SiC power semiconductors have a high acceptance in the mass market. We produce SiC components in-house in a vertically integrated manufacturing system and thus guarantee the highest quality and constant supply of the market. Together with our customers in the automotive and industrial sector, we are shaping the power solutions of the future.

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AUTOMOTIVE



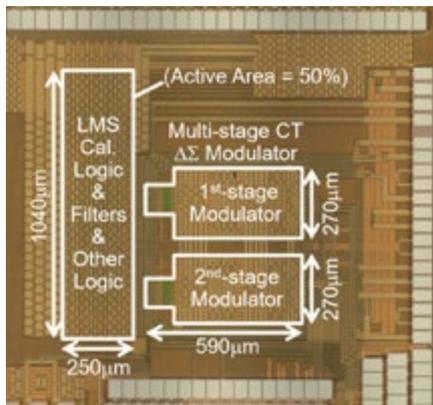
INDUSTRIAL

www.rohm.com

Developing of A/D Converter Circuit Together

Renesas Electronics and Hitachi announced a technology collaboration to enable continuous-time digital calibration of a delta-sigma ($\Delta\Sigma$) modulator and an analog-to-digital (A/D) converter circuit.

Designed to boost the performance of $\Delta\Sigma$ A/D converters for stable performance under the harsh conditions required for automotive semiconductor devices, the technology comprises enhanced precision by using a least mean square (LMS) algorithm to measure and calibrate the transfer function of a continuous-time $\Delta\Sigma$ modulator, and the world's first multi-rate LMS search algorithm, which lowers the order and operating frequency of the coefficient search circuit and FIR digital filter to reduce power consumption. The



results of this joint effort with Hitachi were presented by Renesas on February 18 at the International Solid-State Circuits Conference

(ISSCC) 2020. In recent years, as advanced driver assistance systems (ADAS) and self-driving vehicles come closer to becoming a reality, there has been an increasing need for automobiles to incorporate a variety of sensors, such as millimeter wave radar, LiDAR, and ultrasonic wave sensors, in order to detect objects and people, and to provide an awareness of the vehicle's surroundings. A/D converters used to convert analog signals from such sensors into digital signals must operate at a high speed and with high precision. However, the harsh conditions specific to automotive vehicles have made obtaining stable performance an important issue.

www.renesas.com

Partnership with Distributor in Turkey

Panasonic Factory Solutions and Ankatek, a technical distributors of high-tech capital goods for electronics manufacturing in Turkey, announce their future cooperation. Ankatek will distribute the portfolio of Panasonic Factory Solutions, especially the automation products such



as placement machines, printers and software for industry sectors like telecommunications, automotive, IT and consumer electronics. With a lot of experience in technical sales, Ankatek is a valuable partner who will bring Panasonic Industry's smart factory solutions directly to customers in Turkey.

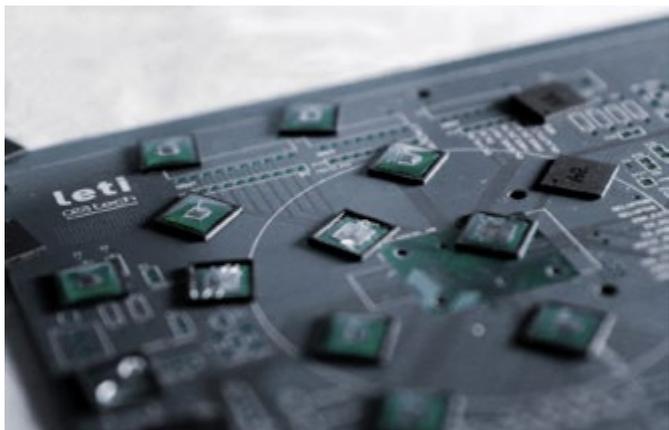
"For Panasonic Factory Solution, the partnership with Ankatek is a logical step to bring our proven hardware and software solutions closer to customers in Turkey. We are very much looking forward to an intensive cooperation," says Nils Heininger, Division Director Factory Solutions.

Selim Ergül, Managing Director of Ankatek, is looking forward to the cooperation: "We are pleased to have found an experienced partner and global player for SMD Factory Solutions. Panasonic is also an expert beyond the SMD line, especially when it comes to the important topic of Smart Factory and machine communication".

www.panasonic.com

Energy-Harvesting ICs Point the Way to Battery-Free Sensor Systems

In scientists' quest for ambient-energy sources that can power sensor nodes in remote environments or difficult-to-reach settings where batteries are impractical, CEA-Leti takes a wide view. It is investigating harvesting systems ranging from micrometer-and-millimeter scale to centimeter scale or larger. The institute presented two papers on



energy-harvesting systems for both of those size scales at ISSCC 2020: "Self-Tunable Phase-Shifted SECE Piezoelectric Energy Harvesting IC with a 30nW MPPT achieving 446% Energy-Bandwidth Improvement and 94% Efficiency", and

"Electromagnetic Mechanical Energy Harvester IC with no off-chip Component and One switching period MPPT achieving up to 95.9% end-to-end Efficiency and 460% Energy Extraction Gain".

Energy harvesting is the action of scavenging available energy in the environment from vibrations, thermal gradients, or solar radiation and turning it into storable electrical energy. The first paper presents a system in which vibration energy is converted into electrical energy by means of a piezoelectric material fixed on a beam. The second project explored converting vibration energy into electrical energy by means of an oscillating magnet in a coil. The harvesters in both approaches required specific IC interfaces to enhance the stored, harvested energy.

Systems that can be powered by surrounding energy sources allow longer lifetimes than battery-powered systems.

www.leti-cea.com

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EMEA Distribution Agreement

SCHURTER and TTI are pleased to announce the signing of an EMEA distribution agreement. This will extend the long-standing, successful cooperation in France to include the rest of Europe, Africa and the Middle East. TTI, Inc. was founded in 1971 and now has over 6700 employees across the globe. With the acquisition of Mateleco in France in 2008, TTI has become an important distributor of SCHURTER products. The SCHURTER portfolio and TTI's Specialist passive, electromechanical and discrete strategy are a perfect fit "We are delighted to now be able to offer SCHURTER high quality products to even more customers and combine our value propositions to provide the best service to our customers. We are looking forward to a successful launch and long term partnership", says Felix Corbett, Supplier Marketing Director at TTI Europe. Laurent Brühl, Managing



Director of SCHURTER S.A.S., sums up: "TTI has proven to be a reliable and competent partner who has been able to clearly exceed its ambitious goals in the past years of successful cooperation. With TTI as an EMEA wide distributor we will be able to serve various markets even better in the future". With over 133 subsidiaries in Europe, America and Asia, TTI is established as one of the largest distributors of electromechanical components.

www.schurter.com

Investment for Design Center in Dublin, Ireland

Maxim Integrated announced the opening of a design center in Dublin, Ireland. The design center will focus on product development and conducting research and development in the areas of analog semiconductor design to deliver Maxim's innovative solutions across many end markets.



To make this vision a reality, the company will recruit a strong team of mixed-signal and analog design engineers at this facility. The \$25M investment will be primarily geared towards recruiting talent, equipment and building costs, as well as research and development. Located on the south side of Dublin, this is Maxim's seventh design center located in Europe. "With our rich history and depth of talent, I'm thrilled that Maxim Integrated has chosen Dublin for this important investment," said John Kirwan, vice president of Global Customer Operations at Maxim Integrated. "We encourage collaboration between employees representing a wealth of diverse, global experiences, from recent graduates of local universities to veteran designers who have been in the industry for many years."

"Maxim's innovative IC designers create products that truly excite their design engineering customers and change everyday lives," said David Dwelley, chief technology officer at Maxim Integrated. "With this new facility, we plan to reinvent the way we develop technology and push innovation even further, giving our customers the products they need to succeed."

www.maximintegrated.com

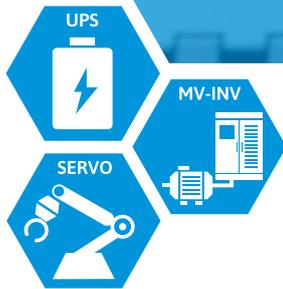
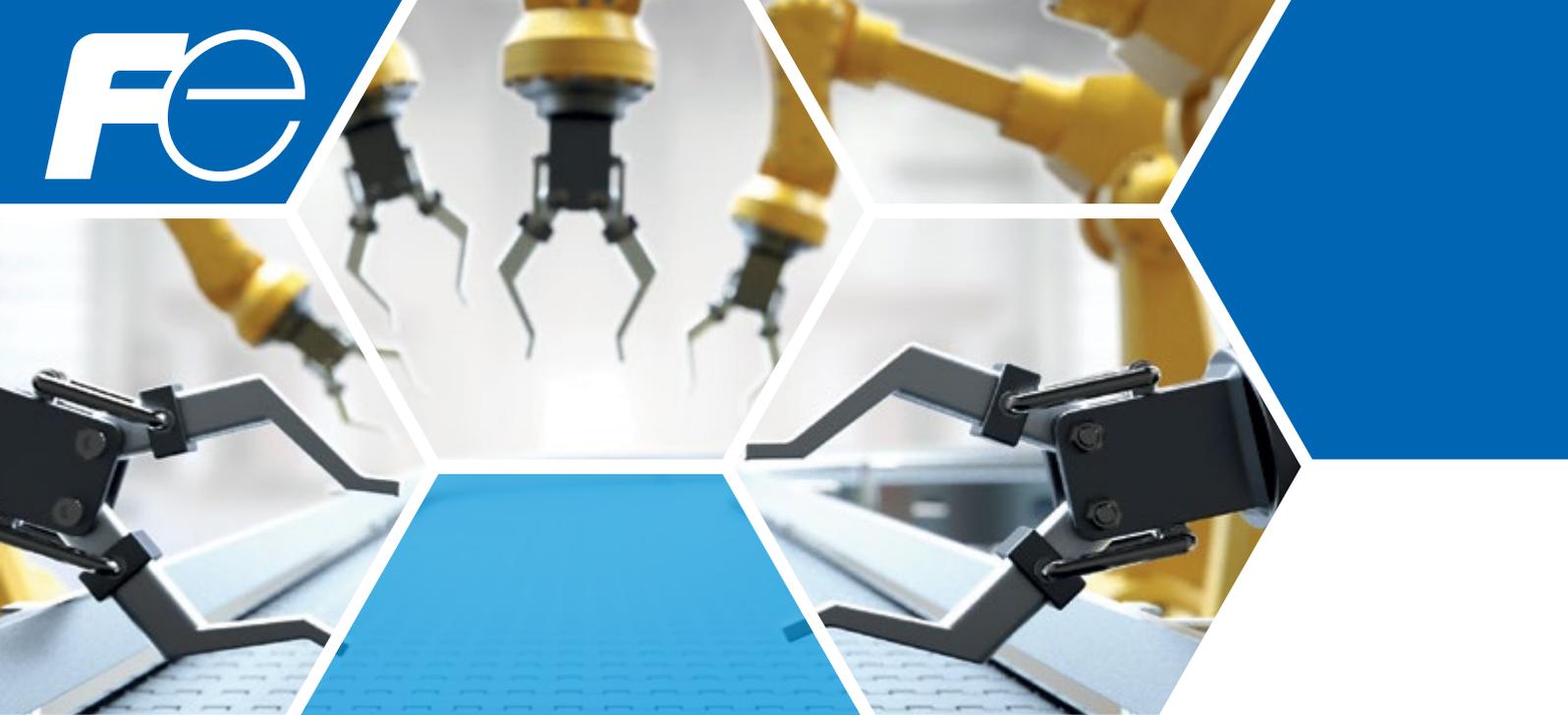
electronica China: New Date in July 2020 Has Been Set

Following the directives of the Government of Shanghai Municipality to prevent and control the virus from spreading, Messe München Shanghai was compelled at the beginning of February to postpone electronica China, productronica China and LASER World of PHOTONICS CHINA, which were planned to take place in March. The new date has been set, combined with a unique change in location. The trade fairs will be held from July 3 to 5, 2020 at the National Exhibition and Convention Center (NECC) in Shanghai. Since the outbreak of the novel coronavirus (COVID-19), more than 300 trade fairs in China have been postponed. Due to the tight schedule of the Shanghai New International Expo Centre (SNIEC) it wasn't possible to find an alternative date at the SNIEC in 2020. After examining carefully all possible dates, Messe München Shanghai has decided on a one-time postponement of electronica China, productronica China and LASER World of PHOTONICS CHINA: The trade fairs will take place from July 3 to 5, 2020, at the National Exhibition and Convention Center in Shanghai. Stephen Lu, Chief Operating Officer of Messe München Shanghai, explains: "We are taking the spread of the coronavirus very seriously and have been monitoring the local situation closely. Based on current developments, we are confident that by setting a new date we will create good conditions for staging the trade fairs."



After intense communication with the exhibitors, Stephen Lu believes that "despite the current uncertainties, the importance of our trade fairs at the Shanghai location remains intact. There is still a great demand for participating in the trade fairs."

www.electronica-china.com



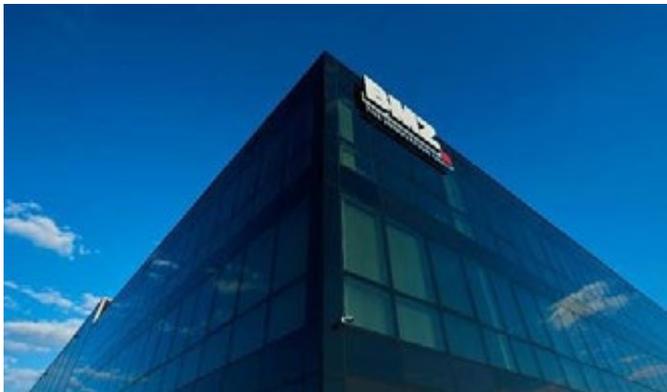
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FEATURES

- ▶ Optimized for Fuji modules
- ▶ Increased lifetime of IGBT
- ▶ Advanced IGBT power density
- ▶ Thermal – Benefits
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 - Uniform thermal resistance
 - Increased reliability and lifetime
- ▶ Process – Benefits
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 - Stable quality level
 - Computer controlled automated process
 - Increased System reliability
 - Printing according customer specification
 - TIM upon customers preference possible

Successful Business Year

BMZ Poland, second largest production site of the international BMZ Group, doubles production area and reports 10% sales growth and thereby record results for the business year 2019.



The past year 2019 led to a very positive result at the Polish subsidiary BMZ Poland, particularly in terms of operating profit growth. The economic situation has become more volatile, while global growth has slowed noticeably. Despite an increasingly difficult market environment, BMZ Poland remains on its course. This is a confirmation of the BMZ Group's continuous growth averaging 30% per year. In each month of the past year, activities were focused on sales and, in particular, results, which led to a significantly higher gross margin of 11% at the end of 2019, an increase of almost 50% over the previous year, confirming the confidence of customers in the BMZ brand.

These good performances are the result of implemented optimization and production process balancing changes. New key customers, all leading OEMs in Europe, from the e-bus and power tool sectors are opening up access to fast-growing markets such as bus electrification. These customers ensure a stable order situation throughout 2020.

www.bmz-group.com

Belgian National Company Opened

Würth Elektronik continues its international expansion course and with the opening of Würth Elektronik België BV which celebrated the 23rd sales branch. From Turnhout, to the east of Antwerp, electronics developers and manufacturers throughout Belgium and Luxembourg are supported by five technical field staffers, who in turn are supported by a three back office staff. Components and samples are supplied within 24 hours from the central warehouses in Germany and France. Würth Elektronik has been active in Belgium with local employees since 2006. This is now followed by the conversion into a separate national company. "The foundation of the new company is a logical step in the positive development of the Würth Elektronik eiSos Group in BeNeLux. This creates the basis for further growth," said Thomas Schrott, CEO of the Würth Elektronik eiSos Group, on the occasion of the foundation of the Belgian sales office. The Country Manager is Dimitri Verhaert, who has established Würth Elektronik in the Belgian market with growing success since 2006.

www.we-online.com



Becoming a Carbon-Neutral Company

Infineon Technologies AG will become carbon-neutral by 2030. The company presented its plans at its Annual General Meeting in Munich. Infineon is thus making an active contribution to reducing CO 2 world-



wide and achieving the targets defined in the Paris Climate Agreement. The objective relates to its own greenhouse gas footprint and includes not only all direct emissions, but also indirect emissions from electricity and heat production. Emissions are to be cut by 70 percent over the 2019 levels by 2025. Energy efficiency and hence reducing CO 2 emissions have long been core elements of Infineon's business model. Making life greener is part of the company's mission. Through the use of its products and solutions by the customers of Infineon, 40 times more CO 2 can currently be avoided than is generated during production. With its goal of going carbon neutral, the company is thus taking the next strategic step to fulfill its own mission. "Climate change threatens the global ecosystem and so the very existence of mankind," said Dr. Reinhard Ploss, Chief Executive Officer of Infineon. "It's an acknowledged fact that we need to act. With our goal to become carbon-neutral, we are making a pledge by which others outside the company can measure us."

www.infineon.com

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CHALLENGES WITH
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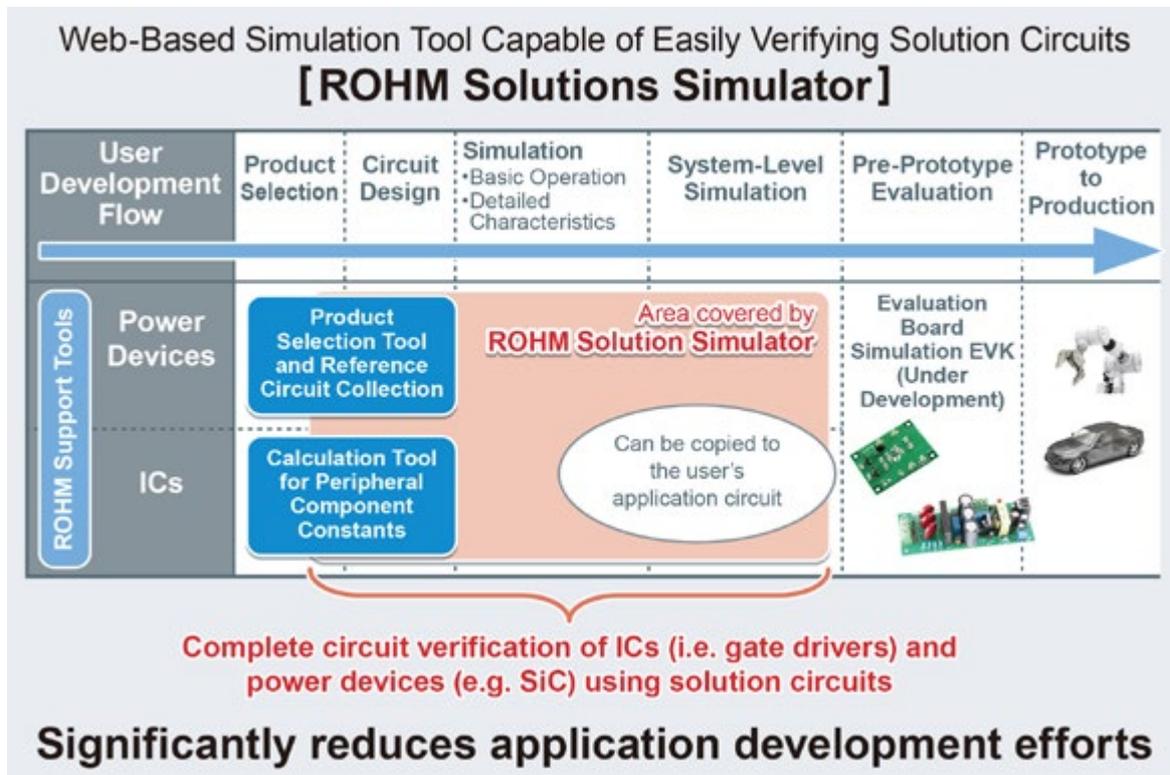
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Low inductance [Capacitor
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proprietary technique

Web Simulation Tool for Power Devices and ICs



ROHM announced to start to provide with a web simulation tool, “ROHM Solution Simulator”, that allows designers of electronic circuits and systems in the automotive and industrial markets to simultaneously verify power devices and ICs on 44 different solution circuits.

Simulations are typically conducted before the prototype design phase in order to reduce development efforts not only in the automotive and industrial equipment markets. Even when designing electronic circuit boards, simulations are used to minimize the time and effort required for component selection as well as to identify potential or fundamental issues before actual equipment validation in order to significantly decrease man-hours during board prototyping and evaluation phases.

Until now, ROHM has provided a range of solutions that contribute to solving issues for a variety of user development flows, such as SPICE models that faithfully reproduce the electrical characteristics of products through simulation along with thermal design support for validating both heat generation phenomena and dissipation results using fluid analysis. This time, in addition to focusing on developing and supporting application circuits that maximize the characteristics of driver ICs and power devices designed to supply high power in the automotive and industrial equipment markets, ROHM offers the cutting-edge simulator, ROHM Solution Simulator, that allows users to perform complete circuit verification of power devices and ICs. Among these, validation of SiC devices and gate driver ICs for driving SiC ranks among the most advanced initiatives in the industry.

ROHM Solution Simulator is a web-based electronic circuit simulation tool that can carry out a variety of simulations, from initial development that involves component selection and individual device verification to the system-level verification stage. This makes it possible to quickly and easily implement complete circuit verification of ROHM power devices (i.e. SiC) and ICs (e.g. driver and power supply ICs), in simulation circuits under close to actual conditions, significantly reducing application development efforts.

The simulator was developed to work with the SystemVision Cloud simulation platform from Mentor, a Siemens business, a leader in electronic design automation software with an extensive track record in the automotive and industrial equipment industry. As a result, users with an SVC account can also perform verification in a more realistic environment by incorporating simulation data executed by the ROHM Solution Simulator into their own SVC workspace.

“ROHM is committed to reducing customer development time and costs by providing a comprehensive online solution built using SystemVision, a multi-domain cloud-based platform,” said Darrell Teegarden, Product Manager for SystemVision Cloud at Mentor, a Siemens business. “By focusing on maintaining and enhancing device models and reference circuits that operate in the SystemVision Cloud environment, ROHM can further contribute to solving customer issues.”

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IGBT Generation 7 - A Practical View on the Benefits in Motor Drives

The 1200V Generation 7 IGBTs are the new workhorse in the power electronics world. They are specifically designed for motor drive applications and at SEMIKRON available from two different suppliers. This ensures supply chain safety paired with highest performance in four different packages.

*By Rainer Weiss, Application Manager, SEMIKRON
and Stefan Häuser, Senior Manager Product Marketing International, SEMIKRON*

IGBT Generation 7 features four main advantages compared to previous generations. Besides a) a higher reliability thanks to increased humidity robustness these are b) lower conduction losses ($V_{ce,sat}$), c) an increased overload capability, and d) a smaller physical chip size.

Thanks to the smaller size of Generation 7 IGBT chips with the same nominal chip current, it is now possible to accommodate a larger nominal chip current in the same module package. This results in two possible options to use Generation 7 IGBTs: Either in the same current rating but smaller chip area or with the same chip area and increased nominal current rating.

The conduction losses of the IGBT Generation 7 are lower while the switching losses are similar to those of Generation 4. Therefore, the total losses are also lower. In contrast, the Generation 7 IGBT chip now has a higher thermal resistance $R_{th(j-c)}$ due to its smaller size, and thus poorer cooling. Nevertheless, smaller losses result in higher efficiency and lead to lower cooling effort for the semiconductor modules.

This work dives deep into the practical examples implementing Generation 7 IGBTs and highlights the resulting benefits. It is based on two of the four SEMIKRON power modules equipped with Generation 7 IGBTs. These are SEMiX 3 Press-fit and MiniSKiiP, both the dominating packages in motor drive applications. In both packages the nominal current range can be extended by replacing IGBT 4 with IGBT Generation 7.

The maximum nominal current with IGBT 4 in SEMiX 3 Press-fit is 600A with the SEMiX603GB12E4 half-bridge. With the IGBT Generation 7, the maximum nominal current increases by 16% to 700A in SEMiX703GB12M7, while the 600A version SEMiX603GB12M7 is also available.

Within the MiniSKiiP series we will look into the biggest sixpack power modules. Based on IGBT 4, the SKiiP39AC12T4V1 is fitted with a 3-phase inverter output with a nominal IGBT current of 150A. Switching to Generation 7 IGBTs, two options become available in the same package. The first option is fitting the same nominal chip current to make a SKiiP39AC12T7V1 with 150A nominal current. Alternatively, the same IGBT chip area with higher nominal current can be embedded into SKiiP39AC12T7V10. This makes it a 200A rated power

module. Of course, the MiniSKiiP with IGBT Generation 7 is also available in other popular motor drive topologies like CIB (Converter-Inverter-Brake) and half-bridge configurations.

Motor Drive Applications

In motor drive applications the IGBT is usually the power-limiting semiconductor device. Electrical machines have a power factor $\cos\phi$ of 0.7 to 0.95. Therefore, during each switching cycle in motor drive applications, the current flows through the IGBTs longer than the antiparallel freewheeling diodes. This is where the Generation 7 IGBTs can make the most out of their advantages.

Before looking into a detailed comparison, let's have a closer look at a further advantage of the Generation 7 IGBT: the improved EMC behaviour in motor drive applications. The voltage slew rate (dv/dt) at the inverter output of modern IGBT chips is usually relatively high due to their fast switching behaviour. Together with the cable capacitance, this voltage change causes a parasitic capacitive leakage current I_{cap} . It flows through the cable capacitance of the motor cable shields and the winding capacitance of the motor towards earth potential. It is calculated as $I_{cap} = (C_{cable} + C_{motor}) * dv/dt$ and occurs as current peaks with every switching instance.

This results in conducted and radiated interference emissions from the drive. These emissions must be reduced to certain limit values due to the norms and standards to be observed. HF EMC filters are used for this purpose. Additionally a high capacitive current is added to the motor drive output current and a drive with higher nominal current might have to be selected. Moreover, the capacitive currents lead to additional power losses in the semiconductor module. Finally, a high dv/dt value might also generate motor bearing currents, resulting in pre-mature bearing failures and the use of expensive insulated bearings.

Reducing the dv/dt value will reduce the capacitive currents and with this all above mentioned risks. On the other hand, slower switching will result in an increase of switching losses, reducing the efficiency of the motor drive. A relatively slow switching IGBT with low switching losses is therefore advantageous. Here IGBT Generation 7 will greatly help to achieve low dv/dt values and acceptable switching losses at the same time.



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Turn-on behaviour

When the IGBT is turned on, the current commutates to this IGBT from the complementary freewheeling diode and vice versa when it is turned off. Therefore, the switching speed of the IGBT does not only influence the electromagnetic emission, it also affects the IGBT and diode switching losses.

As a general rule of thumb, faster IGBT turn-on reduces the IGBT losses and at the same time increases the diode losses. Since the diode losses are much lower than those of the IGBT, the resulting total losses are dominated by the IGBT. Nevertheless, the diode losses cannot be fully ignored. The gate resistance sets the switching speed of the IGBT. The junction temperature and the load current have a considerable influence on that speed. In order to find an EMC-optimized IGBT switching speed, it is useful to first define the gate resistance with which the highest switching speed can be obtained. For both IGBT 4 and IGBT Generation 7, this is the case at a) cold (room) junction temperature and b) relatively low current values.

The temperature influence of Generation 7 IGBTs is much smaller than that of its predecessor. For an example, we compare the voltage slopes of the two 600A rated SEMiX 3 Press-fit modules with IGBT 4 and IGBT Generation 7. The comparison refers to a system with 600V DC-link voltage and a load current of 300A. At a junction temperature of 150°C and with a turn-on gate resistor of 2Ω, both generations show a dv/dt value of 2.5kV/μs. At 25°C, the voltage slope of the Generation 7 IGBT rises to a moderate 4.2kV/μs, whereas the IGBT 4 exceeds 15kV/μs.

A dv/dt of 4.2kV/μs is an acceptable value for general purpose motor drive applications. As the highest voltage slope occurs at low temperatures, the lowest possible gate resistor must be determined at room temperature. In order to limit the voltage slope to 4.2kV/μs, the IGBT 4 turn-on gate resistor must increase from 2Ω to 4.8Ω. The switching losses increase with the junction temperature, so the power loss comparison should be done at an elevated temperature of 150°C. Here, the increased gate resistors results in an increase of IGBT turn-on losses for IGBT 4 from 30mJ to 48mJ (+60%). As explained above, the diode losses reduce as the IGBT turn-on losses rise, in this case from 20mJ to 17mJ (-20%).

Due to the dominance of the IGBT losses, the combined turn-on losses at turn-on of one IGBT 4 switch increase by 28% to 64mJ at 4.2kV/μs compared to 15kV/μs voltage slope. This is slightly more than the Generation 7 IGBT at 62mJ. Figure 1 shows the exact dependency of dv/dt at 25°C and switching losses at 150°C versus the turn-on gate resistor.

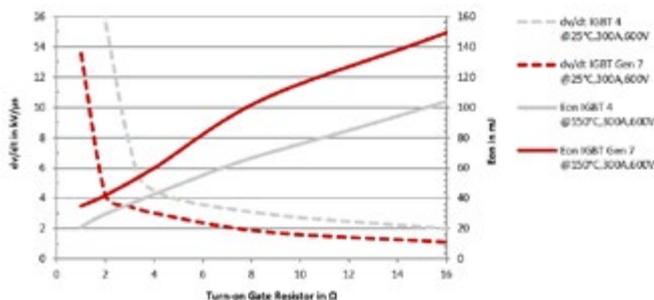


Figure 1: dv/dt and E_{on} vs. $R_{gate,on}$

Turn-off behaviour

During turn-off, the voltage slope dv/dt increases with the current. Therefore, during turn-off most of the interference emissions occur

with large load currents. With cooler junction temperatures, the voltage slope increases as it does during the turn-on of the IGBT, but the effect is much less pronounced. In general, the voltage gradients are also smaller when the IGBT is turned off than when it is turned on. However, the influence of the gate resistance on the voltage slope is also only very limited. In summary, the operating point with the highest electromagnetic noise emission is at cold temperature and high current. This applies to both IGBT generations 4 and 7.

Comparing again the 600A rated SEMiX 3 Press-fit power modules, the voltage slope at IGBT turn-off of the IGBT Generation 7 is about 20% higher than that of IGBT 4. In order to achieve the same noise emission for both IGBT generations, a higher-impedance gate resistor must be used for SEMiX603GB12M7. This will increase the turn-off losses. The target is again to limit the voltage slope to 4.2kV/μs, same as at turn-on. A turn-off gate resistor of 7.1 Ohm is required for the IGBT 4 compared to 12 Ohm for Generation 7. This results in similar turn-off losses of 41mJ for the SEMiX603GB12E4 and 42mJ for the SEMiX603GB12M7 as Figure 2 shows.

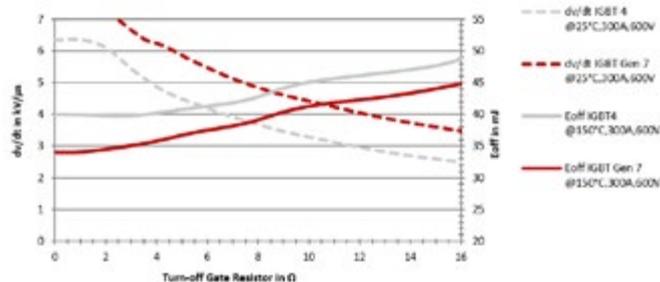


Figure 2: dv/dt and E_{off} vs. $R_{gate,on}$

Lower losses, higher power

The total switching losses are the sum of the turn-on and turn-off losses of the IGBT and the switching losses of the freewheeling diode. If the voltage slope is limited to 4.2kV/μs the total switching losses of both IGBT generations with the same nominal module current of 600A are roughly the same with 104mJ for the IGBT Generation 7 and 105mJ for IGBT 4. Nevertheless, thanks to the 20% lower saturation voltage $V_{ce,sat}$ the overall power losses of the Generation 7 IGBTs are lower. For a direct comparison, we look at the power losses with the previously selected gate resistors, a PWM frequency of 2kHz and a maximum junction temperature of 150°C.

In comparison, Generation 7 IGBTs can reduce the losses by 13% from 504W per switch to 439W per switch (SEMiX603GB12M7p) or by 19% to 409W per switch (SEMiX703GB12M7p) (Figure 3).

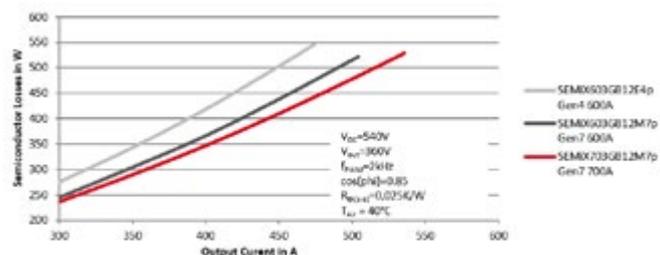


Figure 3: Semiconductor Losses vs. Output Current

These lower losses convert directly into savings on the electric power bill. In this example the loss savings are 95W per switch. Considering electricity cost of 0.10€/kWh and 4000h operation hours per year, this results in immediate cost savings of 228€ every year ($6 \times 95W \times 4000h/a \times 10ct/kWh = 228€/a$). Beside this secondary benefit, the cooling efforts can also be reduced. Losses that do not occur at all

do not heat up the semiconductors and do not need to be dissipated. Further savings can be achieved in the heat sink design or the cooling of the cabinet where the motor drive is installed. In another use case, the economic viability results from frame-size jumps and a higher power density on the system level: the same housing size can now be rated for a higher nominal inverter current, considering the recommended junction temperature of 150°C as the design limit. It can be increased from 473A SEMiX603GB12E4 to 506A (+7%) with the SEMiX603GB12M7. Choosing the SEMiX703GB12M7 it even increases to 536A (+13%). Figure 4 shows the detailed comparison for 2kHz PWM frequency.

Moving to the MiniSKiiP we do direct comparison of the above mentioned three sixpack modules based on application data shows the benefits of IGBT Generation 7: For the same load current (here

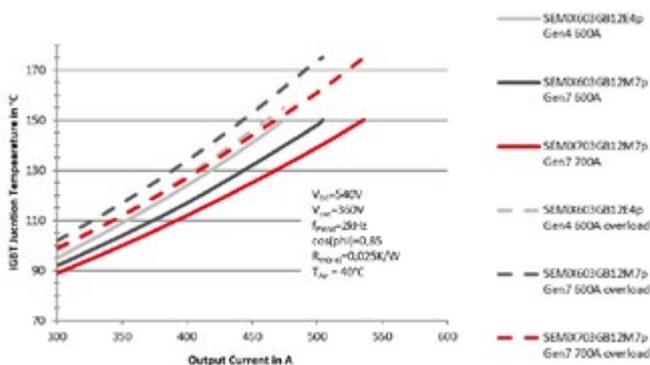


Figure 4: IGBT Junction Temperature over Output Current

100Arms) the larger 200A chip reduces the losses by 12W per switch compared to the smaller sized 150A Generation 7 chip. This equals between 5% and 10% of the total semiconductor losses, depending on the used PWM frequency (Figure 5).

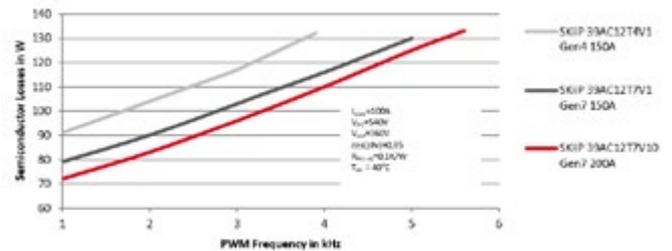


Figure 5: Semiconductor Losses vs. PWM Frequency

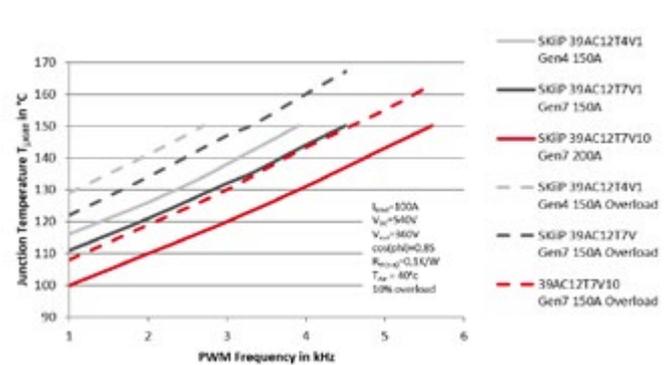


Figure 6: IGBT Junction Temperature vs PWM Frequency

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The power dissipation of Generation 7 IGBTs in MiniSKiiP is significantly lower than that of IGBT 4, e.g. 15% (12W) at 2kHz for the same chip current, increasing to even 24% (19W) for the larger chip. This results in savings of electricity cost of over 45€ per year for the user, based on electricity cost of 0,10€ per Kilowatthour and 4000h operation per year ($6 \cdot 19W \cdot 4000h/a \cdot 10ct/kWh = 45.60€/a$) compared to IGBT 4. As an alternative to the higher efficiency, the lower power dissipation enables increasing the load current or the PWM switching frequency. Thus, for a load current of 100Arms with IGBT 4, only 3.9kHz switching frequency is possible. With Generation 7 IGBTs using the same nominal chip current, 4.5kHz is possible and with the bigger chip current even 5.6kHz (Figure 6). The limiting factor is the maximum recommended junction temperature for continuous operation of 150°C permissible for the IGBT chip. The second alternative could be to increase the continuous load current from 115A to 122A (Generation 7 with 150A) or even 138A (Generation 7 with 200A) at 2kHz PWM frequency.

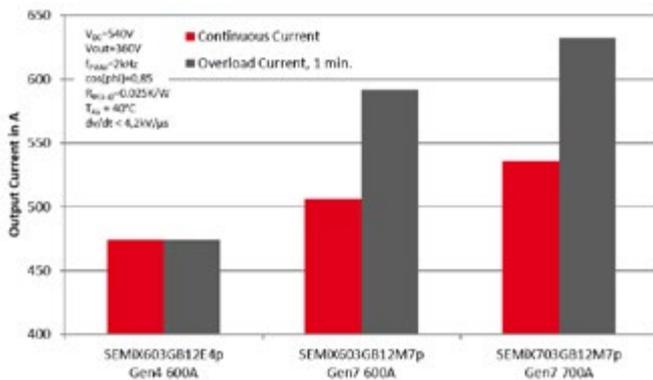


Figure 7a: SEMiX 3 Press-fit: Continuous and Overload Current at max. $T_{j,IGBT}$

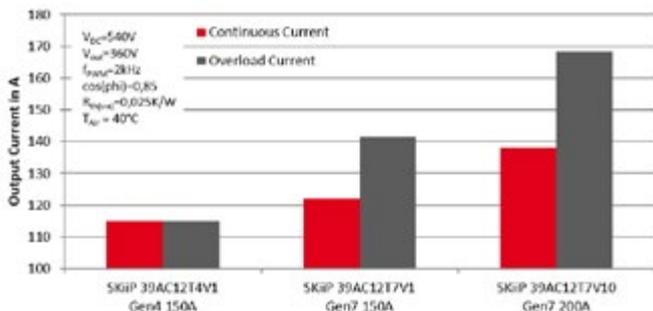


Figure 7b: MiniSKiiP: Continuous and Overload Current at max. $T_{j,IGBT}$

Additional benefit: Overload

Using IGBT 4, no additional overcurrent is possible as it is not recommended to exceed the junction temperature of 150°C for safety reasons. However, IGBT Generation 7's additional temporarily allowed junction temperature enables a chip temperature increase up to 175°C for one minute. Replacing the SEMiX603GB12E4 with Generation 7 IGBTs results in overload currents of 592A for SEMiX603GB12M7 and 632A for SEMiX703GB12M7 (Figure 7a).

For the MiniSKiiP, an additional overload current of up to 1.12 times or 1.14 times the continuous load current can be utilized for up to one minute (Figure 7b). If an overload current was necessary using IGBT 4, the continuous current must be reduced by 9%, from 115A to 105A, to allow a 10% short-term overcurrent for 1 minute.

Conclusion

Generation 7 IGBTs bring several benefits to motor drive applications when compared to previous IGBT versions. Besides the increased reliability of the new chip technology, the smaller size, lower forward losses and the optimized switching performance allow for higher power density in given power module packages.

In motor drive designs specifically, the dv/dt on the inverter output side is one of the major design restrictions. IGBTs of the 7th Generation exhibit lower power losses at a fixed dv/dt compared to IGBT4. Consequently, this efficiency increase leads to immediate savings in the Total Cost of Ownership (TCO). Alternatively, in a given design, the lower power losses can be converted into higher output power or higher PWM frequencies. Additionally, it is possible to consider the built-in overload function in the inverter specification without the need for an explicitly designed reserve, as is the case with IGBT 4.

Generation 7 IGBTs are currently available in SEMITOP E1/E2 (0.37 to 30kW), MiniSKiiP (0.37 to 110kW), SEMiX 6 Press-fit (15 to 75kW) and SEMiX 3 Press-fit (55 to 250kW and higher), see Fig. 8. The baseplate-less MiniSKiiP and SEMITOP packages include CIB and sixpack topologies, the MiniSKiiP also covers half-bridge topologies. The SEMiX 6 Press-fit is a baseplate design available as CIB and sixpack. The SEMiX 3 Press-fit is a half-bridge module, which has a baseplate as well. Rectifier modules in the MiniSKiiP and SEMiX packages complete the portfolio, to offer a full motor drive solution, made by SEMIKRON.

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Figure 8: Initial SEMIKRON product line-up using IGBT Generation 7



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Boost Your 1500 V String Inverter

Flying-Capacitor Boost Topology for Unrivaled Cost and Performance

This article investigates performance and cost of different boost topologies for 1500 V multistring solar inverters. Designers are seeking for higher level of integration, which means the mounting of the boost inductors on the printed circuit board (PCB). Beside this fact, also efficiency and cost are important aspects to be considered.

By Matthias Tauer, Technical Marketing Manager, Vincotech GmbH, Unterhaching

Introduction

This case study investigates the optimal solution to meet cost and performance requirements at the same time. It introduces a new three-level boost topology named flying-capacitor boost and shows that this topology outperforms in cost and performance.

Comparison of boost topologies

Three different types of boost topologies will be compared: two-level, three-level symmetric and three-level flying-capacitor circuit.

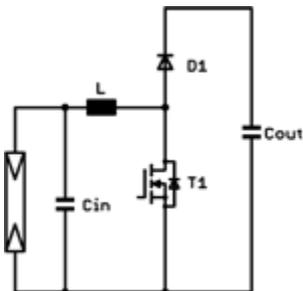


Figure 1: Two-level boost circuit

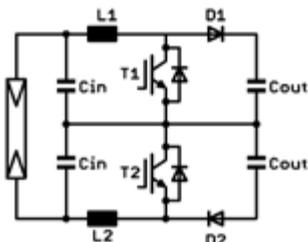


Figure 2: Three-level symmetric boost circuit

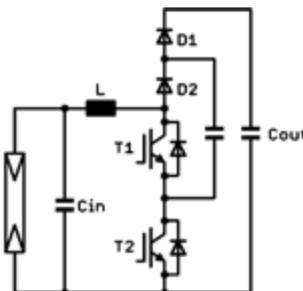


Figure 3: Three-level flying-capacitor boost circuit

The three-level topologies comprise an additional third voltage level. This third voltage level reduces the voltage across the boost inductor, boost switch and diode to half the value required for two-level topologies. Less voltage across the boost inductor has the advantage that the required inductance for a given ripple current is only half of the required inductance at two-level. In consequence the overall inductor volume, weight and cost is reduced. This benefit is not considered in the following power module cost benchmark and should therefore be kept in mind. In the symmetric boost topology the third voltage level is created by splitting the boost circuit into a positive and negative part. Input and output capacitors are split as well and connected to the neutral point, which provides the additional third voltage level. The pulse-width modulation (PWM) pattern needs to be corrected in order to ensure a symmetry of the neutral point. The flying-capacitor boost topology creates the third voltage level – as the name indicates – by a floating or flying-capacitor (C-FC). The flying-capacitor shall be charged to half of the output voltage. It is noticeable that only one boost inductor is required.

Cost and performance benchmark

In this case study the cost and performance is compared for a 21 kW boost leg of a 1500 V multistring solar inverter. Following topologies and chipsets are benchmarked:

chipset	two-level	three-level symmetric	three-level flying-capacitor
Si/SiC hybrid	not examined as efficiency doesn't meet the requirement	1200 V fast Si IGBT 1200 V SiC diode	
full SiC	1700 V SiC MOSFET 1700 V SiC diode	1200 V SiC MOSFET 1200 V SiC diode	

From the efficiency benchmark in Figure 4 it can be seen that the full SiC two-level boost stage has the lowest efficiency (red dotted line) and the highest price (Figure 5). The hybrid chipset would even have lower efficiency in this frequency range and therefore is not taken into account.

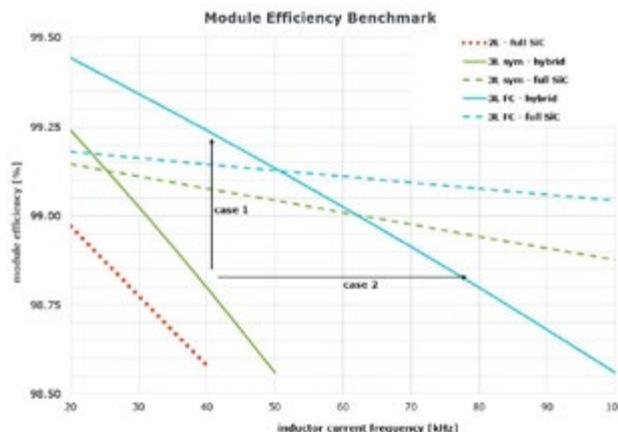


Figure 4: Module efficiency benchmark – conditions: $V_{in} = 760 V$, $V_{out} = 1200 V$, $P_{dc} = 21 kW$

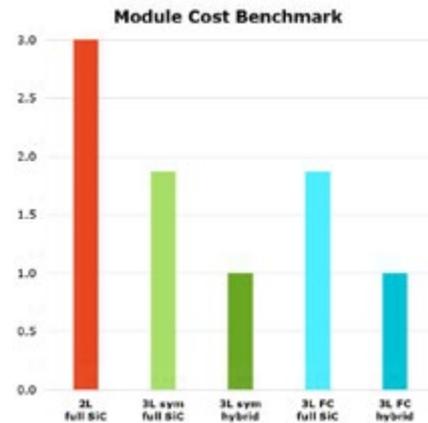


Figure 5: Module cost benchmark

The flying-capacitor (FC) boost topology (solid and dashed blue line) shows always higher efficiency as the symmetric boost (solid and dashed green line). Both use the same components and therefore have the same module price. The first conclusion to be drawn is that the flying-capacitor topol-

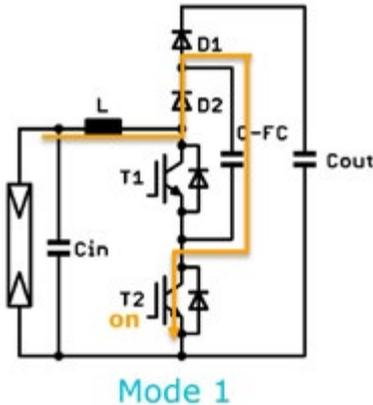


Figure 6: Operation mode 1 – excitation

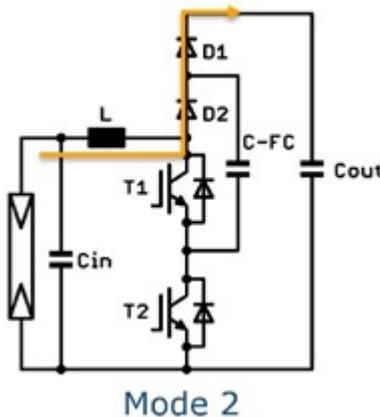


Figure 7: Operation mode 2 - free-wheeling

ogy has best price and performance ratio compared to symmetric and two-level boost topology.

Up to 50 kHz the hybrid flying-capacitor topology (solid blue line) has the highest efficiency. Above 50 kHz the full SiC flying-capacitor boost circuit (dashed blue line) has the highest efficiency, but also higher price than the hybrid circuit.

The two-level boost and three-level symmetric boost topologies are already well described in the literature and considered as state of the art. In the following section the flying-capacitor topology is discussed.

Flying-capacitor boost topology in details

The two semiconductor switches T1 and T2 in the flying-capacitor topology are controlled on phase opposition (180° phase shift), but with identical on time (duty cycle). During normal operation T1 and T2 are never turned on at the same time. In continuous conduction mode (CCM) the duty cycle (D) can be calculated to

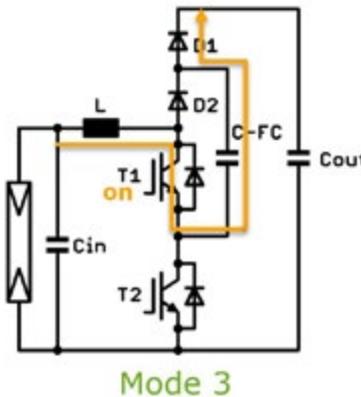


Figure 8: Operation mode 3 – excitation

$$D = 1 - \frac{V_{in}}{V_{out}}$$

The operation is divided into three modes. In mode 1 the low-side switch T2 is turned on and the inductor current is rising. The current is flowing through D2, the flying-capacitor (C-FC) and T2. Once T2 is turned off mode 2 is entered. In mode 2 the current is free-wheeling through D1, D2 and the output capacitor. In mode 3 the floating switch T1 is turned on and the inductor current is rising again. The current is flowing through T1, the flying-capacitor and D1. After turning off T1, mode 2 is entered again and the sequence starts from the beginning. The normal operation mode sequence is: 1 → 2 → 3 → 2 → 1.

Figure 9 shows for the sake of clarity the gate signals of T1 and T2 together with the boost inductor current I_L . The inductor current period is defined from one rising slope to the next rising slope. The period of the PWM fundamental switching frequency is defined from the rising edge of T1 or T2 to the next rising edge of the same gate signal. It then shows that the inductor current period is half of the PWM period or in other words the inductor current frequency is double of the PWM frequency.

The flying-capacitor boost topology allows for an existing choke design with fixed inductivity and ripple current to halve the PWM frequency (case 1 in Figure 10). In the first approximation this will also half the semiconductor switching losses and increase the power module efficiency. Figure 4 illustrates case 1 for 40 kHz inductor current frequency: The efficiency can be increased from 98.8% (symmetric boost stage) to 99.24% (flying-capacitor boost stage).

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Another potential for optimization is to keep the power module losses constant (same module efficiency), but increase the inductor current frequency (case 2 in Figure 10). Figure 4 shows for case 2 that the efficiency is not changing when the inductor current frequency is doubled from 40 kHz (symmetric boost stage) to 80 kHz (flying-capacitor boost stage).

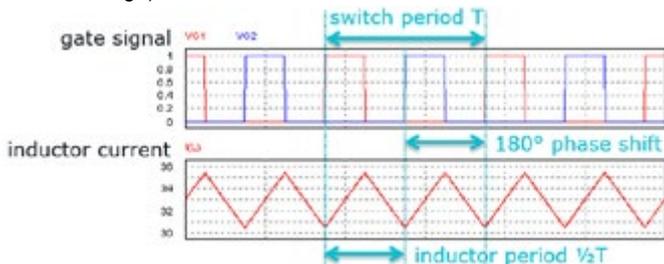


Figure 9: Gate signals of T1 (VG1), T2 (VG2) and boost inductor current I(L)

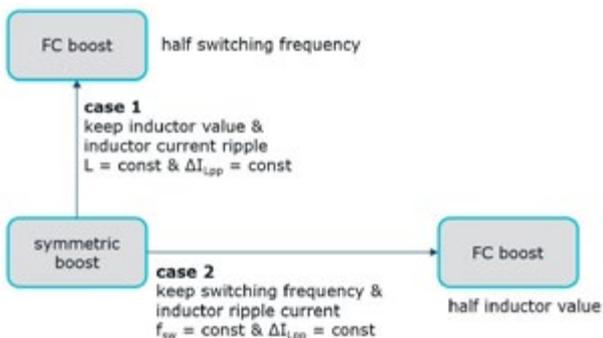


Figure 10: Potential for optimization with flying-capacitor boost topology

An investigation of the required boost inductance shows that moving from two-level to three-level cuts the inductance to half and the additional doubling of the inductor current frequency further halves the required inductance for the same ripple current.

Boost inductance of two-level can be calculated to

$$L_{2L} = \frac{u_L \cdot t_{on}}{\Delta I}$$

- L_{2L} : boost inductance of two-level boost
- u_L : voltage across boost inductor
- t_{on} : boost switch on-time
- ΔI : inductor current ripple

Moving from two-level to three-level will reduce the voltage across the inductor to half value:

$$L_{3Lsym} = \frac{\left(\frac{1}{2}u_L\right) \cdot t_{on}}{\Delta I} = \frac{1}{2}L_{2L}$$

- L_{3Lsym} : boost inductance of three-level symmetric boost
- L_{2L} : boost inductance of two-level boost

Moving from symmetric boost to flying-capacitor boost topology will double the inductor frequency or half the on-time:

$$L_{3L-FC} = \frac{\left(\frac{1}{2}u_L\right) \cdot \left(\frac{1}{2}t_{on}\right)}{\Delta I} = \frac{1}{2}L_{3Lsym} = \frac{1}{4}L_{2L}$$

- L_{3L-FC} : boost inductance of three-level flying-capacitor boost
- L_{3Lsym} : boost inductance of three-level symmetric boost
- L_{2L} : boost inductance of two-level boost

Conclusion and outlook

This article discussed the benefits of flying-capacitor boost topology in regards of cost and performance. The costs for symmetric and flying-capacitor boost topology are the same, but the flying-capacitor boost circuit comprises higher efficiency at the same inductor current frequency. Alternatively, it can even double the inductor current frequency while keeping the module efficiency. In the required frequency range the two-level full SiC boost circuit can't meet the required efficiency and cost. This article will be continued by taking a closer look into the flying-capacitor topology, discussing its challenges e.g. balancing strategy of the flying-capacitor and further highlighting the system level benefits.

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Avalanche Ruggedness of SiC MPS Diodes Under Repetitive Unclamped-Inductive -Switching Stress

Freewheeling diodes are connected antiparallel with a switch such as IGBTs or MOSFETs.

They have to be rugged enough to overcome temporary overvoltage and overcurrent conditions. SiC merged pin Schottky (MPS) diodes are one of the superior contenders. The avalanche ruggedness of discrete 1.2 kV SiC MPS diodes from Infineon was investigated far beyond the specified maximum ratings. Furthermore, repetitive avalanche was studied, including a detailed failure analysis.

By Shanmuganathan Palanisamy, Prof. Dr. Josef Lutz, Technische Universität Chemnitz, and Thomas Basler, Infineon Technologies

Introduction

Silicon carbide bipolar devices may suffer from forward voltage drift (V_F) after bipolar current stress (bipolar degradation). The energy from electron-hole recombination causes Shockley type stacking faults (SSFs) which are triggered from basal plane dislocations and converted into triangular defects and bar-shaped stacking faults (BSSFs) [1][2]. The intention of this work is to investigate the possibility of recombination induced stacking faults (SFs) and other reliability issues under very high avalanche current.

Experiment details

To perform UIS measurements, the test device was connected antiparallel to a 4.5 kV IGBT as shown in figure 1. The applied DC link voltage has been varied in the range of 50 V to 900 V for different inductances. The diode current was measured with a coaxial high-power shunt. Optional resistance was connected in parallel to the inductance to reduce the LC oscillation. When the IGBT turns off, the stored energy in the inductance will cause a high voltage across the IGBT and the antiparallel connected test device. Since the rated voltage of the IGBT is higher compared to the device under test, the diode will go into avalanche mode with a high reverse current.

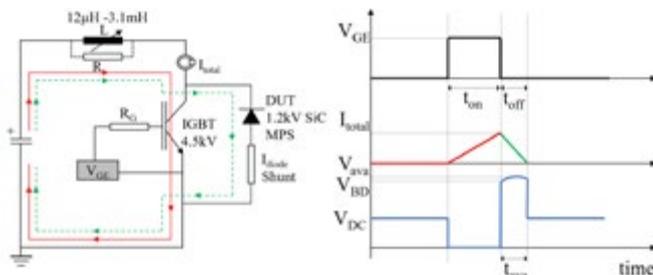


Figure 1: Test circuit (a) and typical schematics (b) of current and voltage waveforms in UIS measurements

Unclamped inductive switching

The avalanche behaviour was measured with various inductances to find the avalanche limit of the test device as shown in figure 2 (a). The used inductance was between 12 μH to 3.1 mH with maximum avalanche energy (see Equation 1) deposited for the last pass pulse of 13.6 J/cm^2 to 11.8 J/cm^2 respectively. Due to the applied inductance, the total current (I_{total}) and clamping time (t_{ava}) had changed ($di/dt=V_{\text{DC}}/L$). The clamping time is shorter for lower inductance where the dissipated energy is stored only at the SiC bulk (for 3 μs). Whereas for higher inductance, due to longer t_{ava} , the dissipated energy could be transferred to the cathode side metallization layers.

$$E_{\text{ava}} = \int_0^{t_{\text{ava}}} I_{\text{diode}}(t) \cdot V_{\text{ava}}(t) dt \quad (1)$$

The single event avalanche limit was measured for each inductance by increasing the DC link voltage until device destruction. After every UIS pulse, the forward and blocking behaviour was tested to ensure the diode has not been destroyed during the pulse. As an example, a single event avalanche limit for 3.1 mH is shown in figure 2 (b). As the overvoltage occurs and the diode reaches V_{ava} , the electric field is high and leads to avalanche multiplication [3], therefore, current flows in reverse direction through the diode. After the avalanche regime, the diode returns to standard blocking mode. This can be seen in figure 2 (b) at $V_{\text{DC}}=908$ V, the device goes into blocking after 11.5 μs . Increasing the DC link voltage to 920 V, finally leads to destruction of the device due to exceedance of the maximum avalanche energy at 11 μs . The diode lost its blocking capability and a failure current flowing through the device and discharging the DC link capacitor.

Repetitive unclamped inductive switching

An automated test bench was built for testing repetitive clamping [4]. The measurements were performed at ~30 to 40 percent below the single event failure limit and were made up to 100 k pulses with a 500 ms interval between each consecutive pulse. Every 20 k pulses, the test was interrupted to verify the forward voltage (V_F), breakdown voltage (V_{BD}) and Schottky barrier voltage (V_{bi}).



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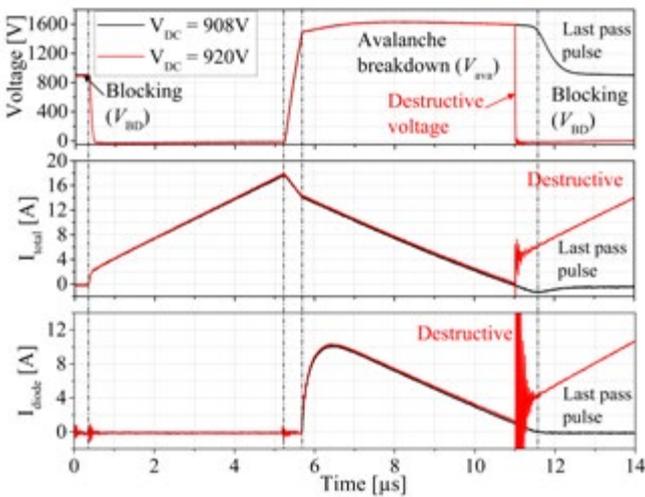
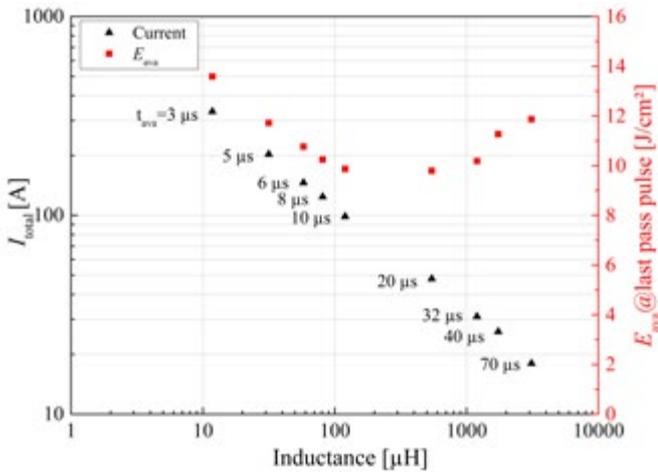


Figure 2: (a) Maximum avalanche energy (E_{ava}) during last pass pulse and maximum current (I_{total}) as a function of inductance. (b) Last pass and destructive pulse of a single event UIS measurement with a load inductance of 3.1 mH

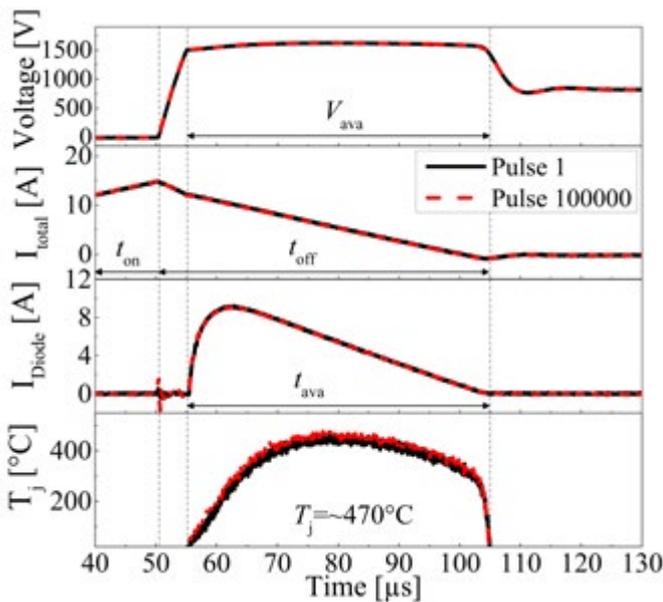


Figure 3: Repetitive avalanche stress under condition of $L=3.1$ mH; $V_{DC}=820$ V; $t_{on_IGBT}=50$ μ s; $t_{interval}=1$ s; $T_c=25^\circ$ C

A repetitive UIS measurement was performed with inductances of 12 μ H and 3.1 mH. The waveforms of the 3.1 mH condition are shown in figure 3. Since the avalanche time (t_{ava}) is longer, deeper layers of the device with more distance to the “active” drift zone could be heated up during the pulse. Therefore, a longer interval of one second between consecutive pulses has been applied in order to avoid heating effects. The temperature swing was calculated from the pre-calibrated temperature dependent breakdown voltage [4]. In case of short clamping time for 12 μ H, almost 100 A were flowing through the diode during avalanche breakdown. The avalanche energy is $E_{ava} \approx 10$ J/cm², which is an extreme condition for the diode. However, some of the diodes survived for 100 k pulses, see [4].

After 100 k repetitive UIS pulses, all test devices showed a forward voltage degradation, Schottky barrier lowering and increase in the leakage current. Since the current peak and temperature swing is very high, another test device was subjected to avalanche stress (at $L=3.1$ mH) with lower dissipated energy $E_{ava}=2.7$ J/cm² and a temperature swing of approximately $\sim 65^\circ$ C. Since the avalanche energy is lower, the test device showed stable behaviour without any degradation even after 100 k pulses.

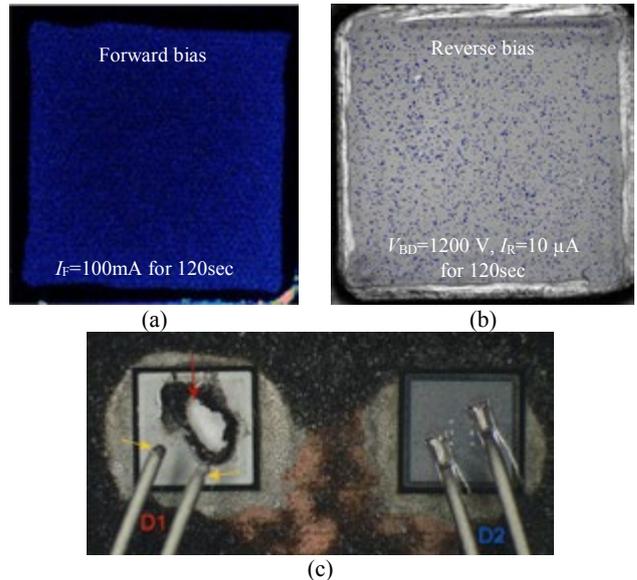


Figure 4: Failure patterns of the 1.2 kV SiC MPS after repetitive UIS tests. (a) and (b) after 100 k repetitive avalanche pulse without destruction. (c) failed test device during repetitive UIS measurement

Failure analysis

In order to investigate the cause of degradation, the test devices were subjected to several failure analysis methods. To investigate possible stacking faults, some of the test devices which showed V_F drift have been subjected to emission microscopy (EMMI) similar to [5]. For this purpose, the back-side lead frame was removed carefully. The tested devices were subjected to forward and reverse bias as shown in figure 4 (a) and (b) respectively. A homogenous current distribution was observed across the chip surface, meaning no recombination induced stacking faults have occurred. A possible physical reason could be connected to the fact that at high electric field the drift velocity of the carriers becomes saturated. Hence, during avalanche multiplication with $v_{sat}=10^7$ cm/s and base width in the range of 10 μ m, the carrier transit time w_B/v_{sat} is in the range of 0.1 ns which is too short for significant bipolar recombination. Consequently, no recombination can occur.

The p+ islands of the MPS diode are hardly visible from the EMMI picture due to a strong change in the Aluminium (Al) metallization. Therefore, the front-side covering mould compound was removed and inspected optically. Certain abnormal grains were observed on the front side metallization, see [4]. This metal surface modification could be caused due to the high temperature swings during the repetitive UIS stress.

One example of a failed test device during repetitive UIS measurement is shown in figure 4 (c). The used TO-247 package consists of two diodes with common cathode. The left side diode D1 was tested under the same conditions as shown in figure 3. However, in this case, the test device survived up to ~80 k pulses, then a massive damage was observed in the middle of the chip. The chip was completely melted at the location of bond wire due to very high avalanche energy far beyond the SOA of the device. The neighbouring diode D2 was unaffected.

Conclusion

The measurements and extensive failure analysis show that the above mentioned modifications and V_F shift in the diode after repetitive UIS stress is due to change in the front side metallization by Al modification caused by the high temperature swing. EMMI pictures show a homogenous current distribution and no stacking faults (SFs) are visible. Even at very high current peak (~100 A), no recombination induced SFs could be found, since the transit time of carriers is too short for significant recombination.

In general one can conclude that the 1.2 kV SiC MPS diodes from Infineon show high avalanche ruggedness even at extreme conditions, far beyond the specified maximum rating of the device.

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ATEX and the Power Management of Smart Gas Meters

Smart meters have become very reliable and practical in the last decade. As their increasing ability to provide real-time data monitoring, advanced alarms and remote operation led to greater global demand, so too arose an equivalent demand for ultra-low-power electronics.

By Omar Hegazi, Texas Instruments

Smart meters need to keep their power-consumption levels as low as possible, but that poses a challenge for electronics suppliers. For example, one requirement for smart gas meters is 10 years of battery life. Smart meters are also expected to reliably function in extreme environments and weather conditions. Gas meters function in an explosive atmosphere, so they must include protections to operate safely. ATEX, derived from the French phrase “ATmosphère Explosive,” is another name for European Directive 2014/34/EU, which aims to regulate explosion protection in industries that have explosive environments. In this article, I'll explain how the TPS62840 step-down converter in the DGR package [1] can help system and equipment design teams meet aspects of the ATEX Directive [2] and achieve battery lifetime goals.

The ATEX certification

ATEX is a European Union directive for standardization that covers “equipment and protective systems intended for use in potentially explosive atmospheres.” [2] Explosive atmospheres may occur when flammable gases, vapors, mists or even dust mixed with air accumulate. The ATEX certification aims to minimize or completely eliminate the risk of ignition in such atmospheres and to limit harmful effects in case of an explosion. Explosive atmospheres are present in various industries. In the chemical industry, chemical processes may create explosive mixtures of combustible gases and liquids. Gas suppliers inherently operate in a potentially explosive environment because gas is flammable. Wood processing companies, waste management companies, energy production companies and refineries also operate partially or fully in environments with explosion hazards. These industries use a lot of electrical and mechanical equipment and the safety

of their operation in such environments is always a concern. There are different equipment groups and categories within ATEX - depending on the environment, the nature of the explosive atmosphere and the frequency of its occurrence. Table 1 lists the classification of explosive atmospheres caused by mixtures of air and gases, vapors or mists. Residential smart gas meters usually fall in category 3 zone 2, the last row of the table.

Although ATEX is European and not harmonized with equivalent American, Canadian or Asian standards, many aspects of the standards are very similar. Let's review the ATEX intrinsic safety requirements for power-management integrated circuits (ICs) in residential gas meters, along with what you have to consider when designing an IC for this application.

How can power design engineers achieve ATEX certification in residential gas meters?

In order to reduce explosive hazards, the ATEX standard considers ignition sources as the most important factor. For power-management ICs, ignition sources are usually:

- Electric sparks. The amount of electric energy content of the spark determines its risk as an ignition source.
- High surface temperatures.
- Electrostatic discharge, which cause electric sparks and a sudden increase in temperature.

The probability of any of these three events occurring has to be limited or eliminated to ensure safety. The IC package choice for an ATEX-compliant device is the most important contributor in controlling ignition sources. In general, the parameters that reduce such ignition risks are the IC package's power dissipation capability and its electrical pinout.

Package power dissipation capability

Electronic device development has been moving toward smaller and more integrated and compact designs; so have IC packages. These smaller packages pose a challenge when it comes to thermal management, however, especially at high loads. Whereas a quad flat no-lead package (QFN) and a wafer chip-scale package (WCSP) are more suitable for applications where solution size is a priority, larger packages achieve superior thermal performance and keep device temperatures relatively low, even at high loads. A high thermal performance very-thin shrink small-outline package (HVSSOP) is a thermally enhanced package with an exposed pad soldered directly to the printed circuit board (PCB). The exposed pad increases the power dissipation capability as much as 1.5 times over standard shrink

Category	Zone G [gas]	Explosive atmosphere	Frequency
1	0	Intended for use in areas with explosive atmospheres caused by mixtures of air and gases, vapors or mists	Continuously - for long periods or frequently
2	1		Likely to occur occasionally
3	2		Unlikely to occur or, if they do occur, likely to do so infrequently and only for a short period

Table 1: Classification of different zones for explosive environments [2]



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small-outline packages (SSOP) and thus reduces the device's operating temperature. A lower self-temperature rise also enables a higher range of ambient temperatures. Figure 1 shows how an HVSSOP device dissipates around 80% of its heat through the exposed pad, with the help of the thermal vias below it. The rest of the heat mainly dissipates through its leads to the ambient environment. [3]

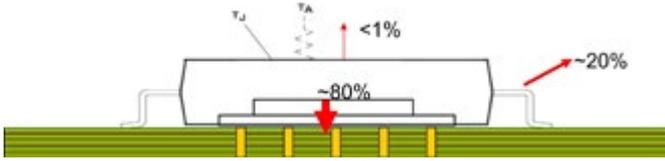


Figure 1: The power dissipation of an HVSSOP device

Figure 2 shows a thermal image of the TPS62840 in the HVSSOP operating at a 25°C ambient temperature, with an input voltage (V_{IN}) of 6.5 V and an output voltage (V_{OUT}) of 3.6 V at a load (I_{LOAD}) of 750 mA, which is the full load of the device. The device maintains a maximum temperature of 30.1°C while the inductor has a maximum temperature of 32.7°C. These are less than 10°C temperature rises.

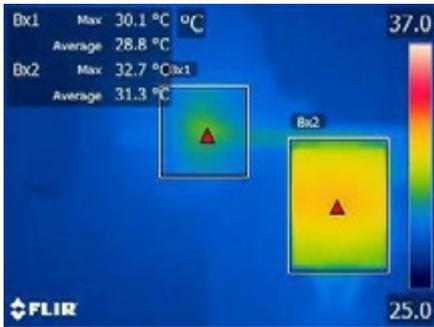


Figure 2: A thermal image of the device at a full load

Package electrical pinout

In addition to the excellent thermal performance, the electrical pinout and the structure of the package leads are also important. The HVSSOP has a big pitch and thin leads, which enables greater distances between each lead and adjacent leads, and eventually between their

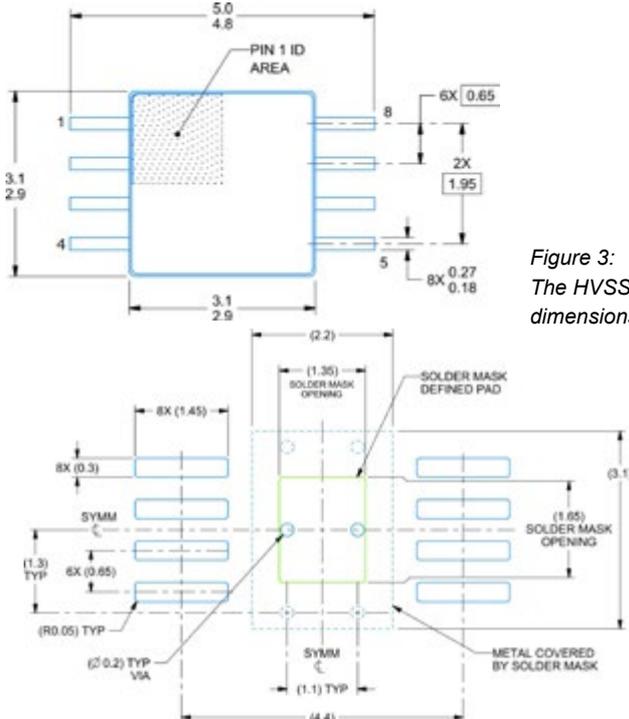


Figure 3: The HVSSOP dimensions

Figure 4: The HVSSOP's PCB land pattern

PCB land patterns. Figures 3 and 4 show the package dimensions and its PCB land pattern. You can see that the distance between the pins on the PCB land pattern is about 350 μm. This is suitable for ATEX intrinsic safety protection, which requires more than 300 μm of spacing for zone 2 protection. [2]

Moreover, as shown in Figure 5, the VIN and GND pins are separated by a no-connect pin, which increases their spacing to around 1 mm. This amount of spacing mitigates board-level electromigration risks in humid environments and increases the IC reliability.

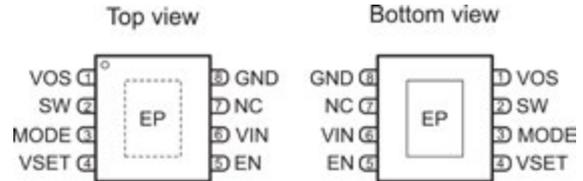


Figure 5: The pinout of the TPS62840 in the DGR package

Electrical performance

In addition to ATEX-compliant features, the TPS62840 in the DGR package has an ultra-low quiescent current (IQ) of 60nA, and can prolong the battery lifetime of devices that rely on it for power management by increasing efficiency at light loads. With modern microcontrollers having different modes and load currents that can go very low to reduce energy consumption, the device still maintains efficiency of 80% at a load of 1 μA, as shown in figure 6. The device also has a wide input voltage range of up to 6.5 V, allowing you to choose different battery technologies (alkaline, lithium-thionyl chloride or lithium-ion) that suit your system best.

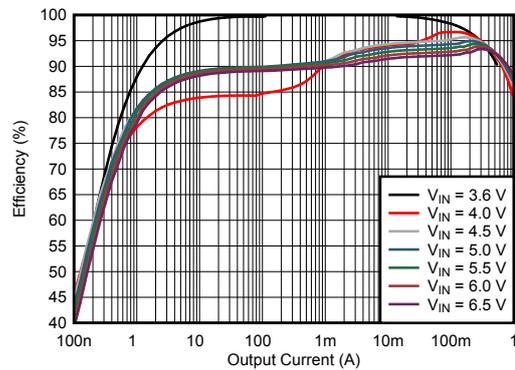


Figure 6: The efficiency curve of the device vs. the load current at $V_{OUT} = 3.6 V$

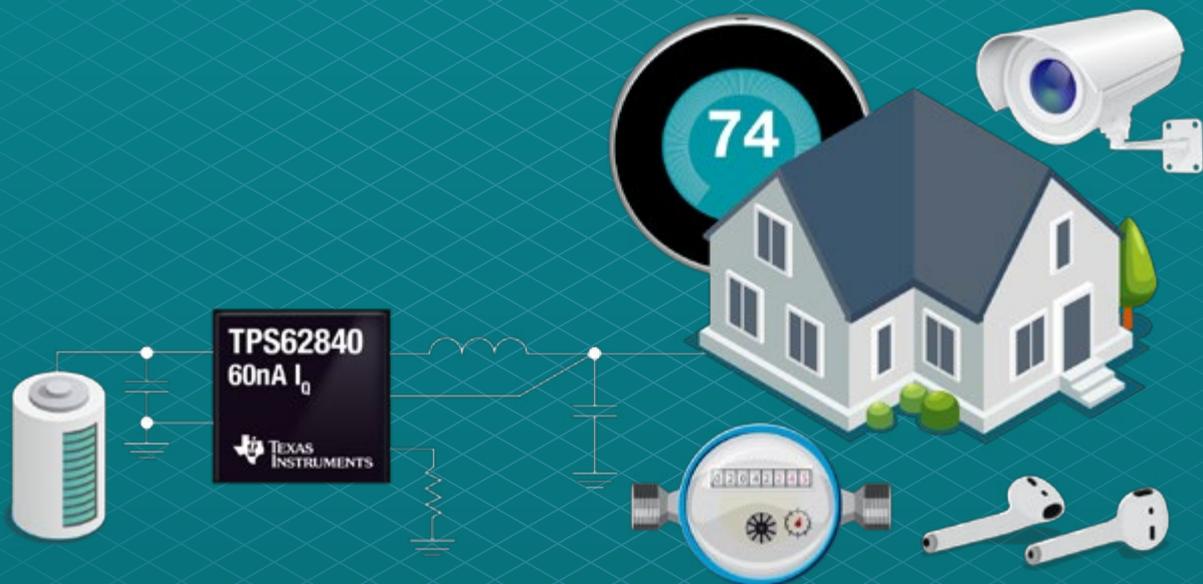
Conclusion

The increasing adoption of smart water, heat, gas and electricity meters, along with the safety requirements imposed by the ATEX Directive, present challenges for power-management design engineers. A long battery life of 10 years or more, an ATEX-compliant IC and very efficient performance at different load profiles are a few requirements that this market needs. With its package's power dissipation capability and electrical pinout, as well as an extremely low 60 nA I_{Q} , the TPS62840 in the DGR package meets the needs of smart meters and other ultra-low-power systems.

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Successful Completion of the Automotive Research Project InMOVE

FTCAP Implements Suitable DC Link Capacitors for an Electric Drive Module

In the InMOVE project initiated in 2016, a consortium developed integrated power electronics for drives systems in electric and hybrid vehicles – with success: The research partners have succeeded in implementing a drive module with an impressive power output of 80 kW. For this project, FTCAP (part of the Mersen Group) provided a suitable DC link capacitor, which allows alternating currents of 70 A at a frequency of 13.5 kHz. This high current load is made possible by an innovative cooling system and the flat design, which improves heat dissipation.

By Jens Heitmann, Account Manager/Marketing Manager, FTCAP GmbH

The InMOVE project was led by the car manufacturer Volkswagen and involved, in addition to FTCAP, the Fraunhofer Institute ISIT, Danfoss, Vishay, Reese+Thies Industrielektronik, and the Kiel University of Applied Sciences. The goal of the project was to develop a modular drive concept for small and mid-sized drive power in plug-in vehicles on the basis of modern gear concepts, with a differing number of electric machines depending on the vehicle class. This enables scalability of the electric drive power and variable drive architecture with the use of the same components. The drive motors are designed as compact, high-rpm electric machines with an integrated converter.

The modular concept for performance scaling and variability of possible drive technologies enables economies of scale and reduces development costs for the electric drive components. However, this requires integrated power electronic components with a compact design. The overall concept of the project therefore was to use innovative mechatronic technologies in order to implement the drive system concept described above. After simulation in a demonstrator the innovative technologies were examined and evaluated with respect to their functionality. Meanwhile, the project has been successfully completed: The partners have succeeded in implementing a drive module with an impressive power output of 80 kW/litre.

Suitable DC link capacitor required

The task of FTCAP was to provide suitable DC link capacitors for the demands of the application. The specifications required implementation of an 800V system with a switching frequency of 13.5 kHz and a high current carrying capacity of 70A - 80A. In addition, the ESR needed to be low to minimise generation of power losses. Other requirements included the ability to withstand temperatures up to 125°C, a low volume and long service life – not to mention low production costs for the capacitors.

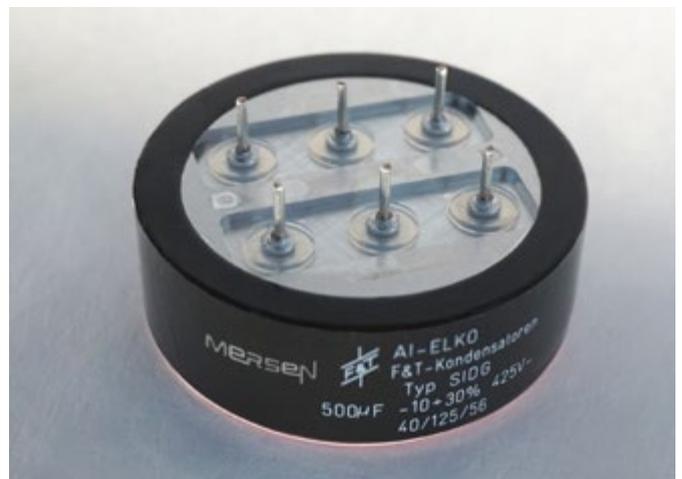


Figure 1: FTCAP provided the suitable DC link capacitor for the InMOVE research project

Initially the company pursued the goal of developing a temperature-optimised DC link capacitor on the basis of two different dielectrics. For this purpose, the two fields of aluminium electrolytic capacitors and film or foil capacitors were examined. Both technologies should be capable of handling the high-current and high-temperature requirements of the DC link. However, tests conducted during the design phase showed that a film capacitor cannot currently be implemented for this application with temperatures up to 125°C using the materials available on the market. Although the base material PEN-HV is suitable for temperatures up to 125°C, the base material (and therefore the dielectric) is mechanically weakened after coating with metal, which substantially reduces the dielectric strength, therefore making the material unsuitable for this application. The development of the film capacitor version was therefore abandoned.

Comparison of different approaches to the solution

Within the consortium, several general concepts for suitable aluminium electrolytic capacitors were then developed; two of these, with various advantages and disadvantages, were examined more closely. The main consideration was cooling, since the higher ESR would most probably result in higher power loss and also higher temperatures under load. Version 1 consisted of twelve narrow, long standard capacitors, while version 2 consisted of two flat, wide capacitors. Although version 1 would have allowed inexpensive production, the probability of failure would have been much higher, due to the large number of capacitors. In addition, the length of the housing resulted in a poor thermal connection to the cooler, since the design reduces the cooling surface on the base.

Version 2 was based on two capacitors designed for optimal cooling with a threaded connection – the GW series from FTCAP. A special stepped base, in combination with a Sil-Pad, ensures optimal thermal dissipation. The stepped base and use of a ring clamp allow virtually seamless mounting of the capacitors on a heat sink. The heavy-duty, laser-welded solid aluminium housing contributes to a long service life. An innovative multi-pin cover ensures a low ESR and therefore a high current-carrying capacity. Although the cover is difficult to manufacture and generally involved a great deal of development work, the consortium decided to use this version 2.



Figure 2: The individual solution for InMOVE is based on the threaded connection capacitors of the GW series, which are designed for optimal cooling

Research on thermally compatible electrolytes

During implementation of version 2 FTCAP first determined which electrolytes were available for the aluminium electrolytic capacitor in a temperature range of 125°C. Lab tests showed that while one potential 125°C electrolyte was able to withstand high temperatures, it did not have the required properties such as dielectric strength, conductivity and viscosity. In coordination with the consortium it was therefore decided to continue the research with a suitable 110°C electrolyte system. After calculation of the capacitor and testing of its feasibility in production, the engineering work began, and prototypes were built.



Figure 3: During the InMOVE project FTCAP conducted research to determine which electrolytes are suitable for the high temperature range and the required electromechanical properties

The results of the first article inspection confirmed the expectations with respect to both the mechanical and electrical properties. Afterwards, the capacitor was operated under near-real conditions to conduct tests of the thermal and electric functionality at the required AC load of 70A. In a current load test, the temperatures were checked simultaneously at specific positions in and on the test capacitor. In addition, it was attempted in this test to simulate possible application temperatures by means of external temperature control using a Peltier element. To achieve the necessary alternating current of 70 A at a frequency of 13.5 kHz, an excitation coil with a power exciter was integrated by means of a coupling coil in a series-resonant circuit (consisting of a test capacitor, a resonant capacitor and a resonant coil). The tests showed that the capacitor is capable of an AC load of 70 A. Since the temperature control by means of the Peltier element can be used only as an initial approximation of the real cooler, temperatures of up to 140°C occurred. Additional tests at the Kiel University of Applied Sciences confirmed, however, that the hotspot temperature in the capacitor does not exceed 110°C when it is installed in

a real cooler. As a result, the consortium now had a suitable DC link capacitor that made it possible in the end to implement the 80 kW drive module.



Figure 4: Aluminium electrolytic capacitors from FTCAP are available in numerous versions and can be individually adapted for particular applications

Research and development is fundamentally a high priority at FTCAP; the company regularly participates in research projects at the interface of science and industry. Currently it is primarily the automotive industry – with the development of e-mobility – that is creating new challenges with respect to DC link capacitors: They need to be more compact and also more powerful, with a special requirement for a high current carrying capacity. In addition to specific research projects, FTCAP is working both on new film capacitors and new aluminium electrolytic capacitors for this industry. Multi-pin capacitors, for example, could create serious competition for the parallel connected axial capacitors with a soldering star that have dominated the market in the past. Initial tests have produced positive results; now the company is working on a highly versatile, scalable solution that is suitable for large-scale production. This development takes on a certain urgency in view of the auto industry's goal of producing e-cars in large quantities starting in 2020/21.



Figure 5: FTCAP regularly participates in research initiatives at the interface between science and industry – the photo shows another DC link capacitor for the H3-Top project

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Overcoming Challenges Characterizing High Speed Power Semiconductors

Having trouble obtaining consistent results from your Double-Pulse Test (DPT) setup? You are not alone. As the switching frequency of switch-mode power converters increase into the MHz range, rise/fall times are dropping to 10ns or even single digits of nanoseconds.

It is no longer possible to design & measure power converter performance without considering high frequency effects. This article discusses DPT fixture design to obtain repeatable and reliable results from your DPT setup.

By: Ryo Takeda – Keysight Solution Architect, Bernhard Holzinger – Keysight Technical Architect, Mike Hawes – Keysight Power Solution Consultant

International Electrotechnical Commission (IEC) and JEDEC standards have existed for decades, defining tests to dynamically characterize power semiconductors. The DPT setup is the industry standard used for measuring and extracting most of the key dynamic parameters to characterize these devices (Figure 1).

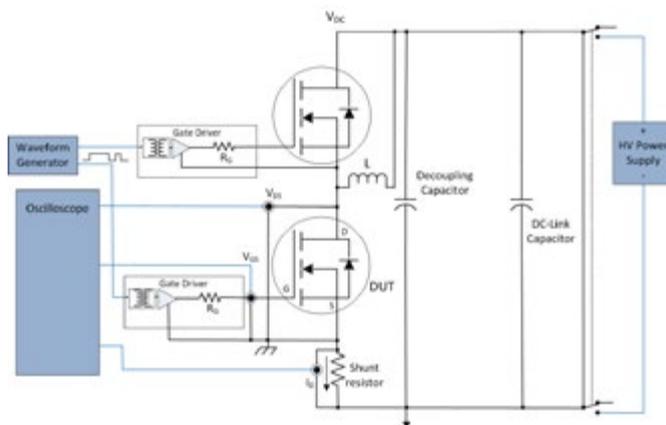


Figure 1: Basic Double-Pulse Test Configuration.

These standards were sufficient for slower switch mode power converters, because BW requirements of measurement equipment and fixturing connecting to the power semiconductor DUT were obtainable with standard low frequency power design practices and measurements. The switching frequencies of power converter designs were in the kHz to 10s of kHz range, not requiring extensive high frequency analysis or design.

With many power converter markets (e.g. automotive and alternative energy) pushing for reduced cost, higher efficiency, higher voltages, and better thermal performance, the pressure on the power semiconductor industry has driven faster Si-based switching capabilities (Si MOSFETs and IGBTs) as well as the emergence of Wide Bandgap (WBG) semiconductor technologies, specifically Silicon Carbide (SiC) and Gallium Nitride (GaN).

To investigate the reason for more difficulty in making DPT measurements with faster switching devices, let's refresh our memory of the mathematical relationship between rise time and bandwidth.

The basic formula relating the bandwidth of a pulse waveform to its

$$t_r \approx \frac{K}{f_{3dB}} \quad [1]$$

Where: t_r = pulse rise time (10% – 90%)

f_{3db} = 3 dB bandwidth

K = constant of proportionality depending on pulse shape (assume 0.35 for single pole exponential decay)

For determining the impact of the parts of the DPT measurement system (e.g. scope, probe, fixture, and DUT), we use the following formula to determine the risetime that would be displayed on the oscilloscope:

$$t_{displayed} = \sqrt{t_{DUT}^2 + t_{DPT\ fixture}^2 + t_{probe}^2 + t_{scope}^2} \quad [1]$$

Armed with these relationships, let's compare two scenarios to illustrate the change in expectation for high frequency consideration.

Scenario #1: Analyze the impact of a 10 kHz switching waveform from a Si power MOSFET with 0.2 μ s rise times. Because mid-range oscilloscope bandwidths are typically 500 MHz or more and their associated voltage probes can have bandwidths of 300 MHz, let's assume these common bandwidths for this scenario. Let's also assume that DPT fixture was designed with low frequency considerations and provides a 20 MHz bandwidth.

$$t_{displayed} = \sqrt{(0.2 \times 10^{-6})^2 + \left(\frac{0.35}{20,000,000}\right)^2 + \left(\frac{0.35}{300,000,000}\right)^2 + \left(\frac{0.35}{500,000,000}\right)^2}$$

$$t_{displayed} = 0.2008 \times 10^{-6} \text{ sec} \quad \text{sec}$$

Result: The displayed value on the oscilloscope is very close (< 1% error) to the actual rise time of the MOSFET, with little to no impact from the DPT fixture, probe or oscilloscope.



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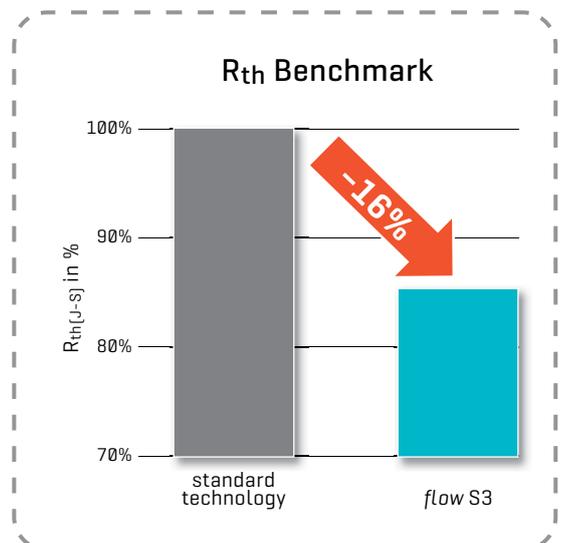
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Scenario #2: Analyze the impact of a 250 kHz switching waveform from a SiC power MOSFET with 10 ns rise times. Let's assume the same situation above for the oscilloscope (BW = 500 MHz), voltage probe (BW = 300 MHz), and the DPT fixture (BW = 20 MHz).

$$t_{displayed} = \sqrt{(10 \times 10^{-9})^2 + \left(\frac{0.35}{20,000,000}\right)^2 + \left(\frac{0.35}{300,000,000}\right)^2 + \left(\frac{0.35}{500,000,000}\right)^2}$$

$$t_{displayed} = 20.2 \times 10^{-9} \text{ sec}$$

Result: The displayed value on the oscilloscope has slightly more than a 100% error! Let's run scenario #2 again with a DPT fixture designed for a 200 MHz BW and see how much impact that will have on the result.

$$t_{displayed} = \sqrt{(10 \times 10^{-9})^2 + \left(\frac{0.35}{200,000,000}\right)^2 + \left(\frac{0.35}{300,000,000}\right)^2 + \left(\frac{0.35}{500,000,000}\right)^2}$$

$$t_{displayed} = 10.2 \times 10^{-9} \text{ sec}$$

Result: The displayed value on the oscilloscope has only 2% error. This is a significant improvement in results by designing the fixture for a 200 MHz bandwidth.

Conclusion

Common instruments, like oscilloscopes, are more than capable to support the needs of a high speed DPT system. More significant challenges to provide repeatable and reliable results involve the design of the DPT fixture, including connection of the measurement probes.

NOTE: Because our analysis involves 2 poles, we must consider the relationship between rise time and bandwidth for second-order systems. Simple second-order circuit simulation was performed to approximate the ratio. The graphed result shows the $t_r \cdot f_{3dB}$ product to be close to 0.35 for $(0.5 < \zeta < 1.0)$. And for $(0.05 < \zeta < 0.5)$ the ratio only drops to ~ 0.27 . Therefore, our conclusion remains valid for second-order systems. [2]

Considerations for DPT fixture design

Because of the faster rise/fall times (i.e. higher bandwidths) required for newer power semiconductors, analysis of the fixture layout and circuit parasitics are critical to provide repeatable and reliable DPT waveforms. If not, DPT waveforms often have second-order under-damped oscillations of the pulsed waveforms (V_{GS} , V_{DS} , I_D), making it impossible to extract repeatable dynamic characterization parameters (e.g. $e_{(on)}$, $e_{(off)}$) (Figure 2).

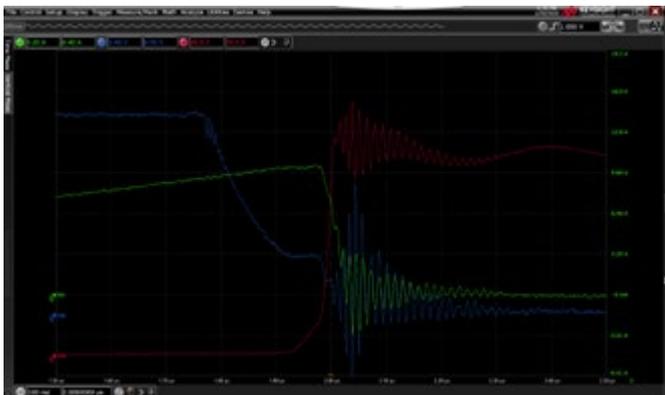


Figure 2: Turn off pulses from a GaN device ($V_{DS}=100V$, $I_D=10A$, $V_{GS}=12V$).

Figure 3 shows the DPT setup with the primary parasitics capacitances, inductances, and resistances that need to be considered when designing your DPT fixture. Some of these parasitics are inherent in the power devices themselves (e.g. C_{gd} , R_g , L_s). Power semiconductor manufacturers continue to develop new packaging materials and designs to minimize the stray parasitics. Once you determine your power semiconductor of choice, the focus is on external parasitics within the fixture.

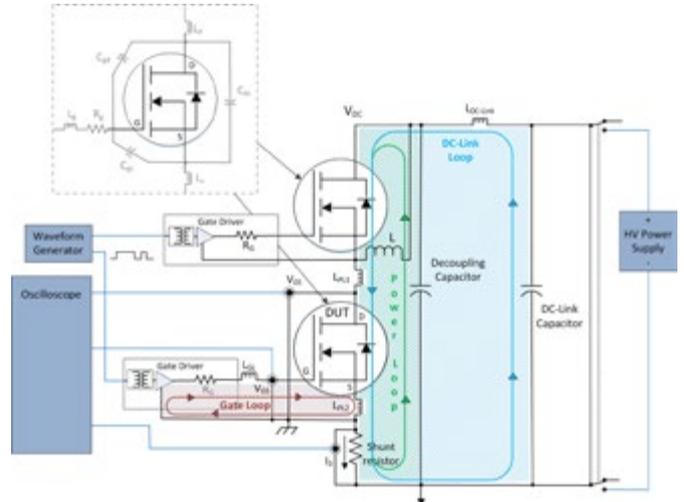


Figure 3: Primary parasitics needing consideration during DPT switching transients.

There are three loops that are worth considering when analyzing the Double-Pulse waveforms (V_{GS} , V_{DS} , I_D): the DC-Link Loop, the Gate Loop, and the Power Loop (Figure 3). As always, it is good practice to minimize the area of the loop, which is proportional to the total loop inductance. This can be done practically by routing PCB traces (main and return) close to each other, or by using twisting pairs, if routing the signals through wires.

The DC-Link Loop should be considered when the DC-Link Capacitor, that is charging the load inductor (L), is interrupted (i.e. when the DUT is turned off). When the DUT is turned off, the current charged up in L recirculates through the body diode in the high-side MOSFET. Therefore, there is no current coming from the DC-Link Capacitor and the DC-Link stray inductance ($L_{DC-Link}$) has a large $-di/dt$. $L_{DC-Link}$ resonates with the Decoupling Capacitor in parallel with parasitic output capacitance from the half bridge, developing a voltage surge across V_{DC} and V_{DS} . This resonant oscillation can be seen on V_{DS} in Figure 4 during both turn-off events. It can also be seen in Figure 2 as the lower frequency oscillation of V_{DS} . It is next to impossible to eliminate this oscillation, but care needs to be taken to minimize it.

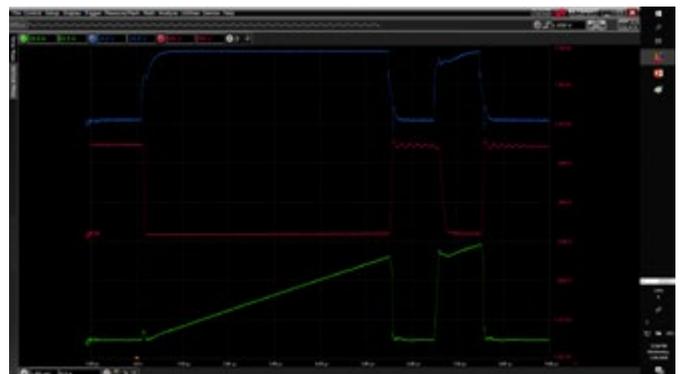


Figure 4: Double-Pulse Test Waveforms (SiC MOSFET, 1200V, 40A).

For the Gate Loop, the main parasitics you have control over in your fixture layout are L_{GL} and L_{PL2} . It is often not possible to minimize this inductance enough to prevent oscillation, depending on the DUT's gate resistance (R_g). If the oscillation still exists, then an external gate resistor R_G is required to dampen the oscillation to enable repeatable parameter extraction. Unfortunately, the trade-off in adding resistance to the gate, is a slower risetime of the gate voltage.

SiC geometries are typically much smaller than Si, and therefore often have larger internal gate resistance (R_g). So, it may not be necessary to add external gate resistance to some SiC devices to dampen the oscillation. While Si MOSFETs may require external dampening, because of the smaller R_g . One often finds many different gate resistor values used in DPT systems to accommodate the specific power device being characterized.

The Power Loop parasitics are another source of oscillation in V_{DS} and I_D . After ramping the current to the desired value in L, during the first of the two pulses, the DUT is turned off. The current in L is recirculated through the body diode. The $-di/dt$ in the power loop inductance (L_{PL1}), creates a voltage surge across the drain and source of the DUT. This voltage surge resonates with C_{ds} of the DUT and the parasitic inductance of the Power Loop (L_{PL1}), creating a higher frequency oscillation that can be seen in V_{DS} and I_D in Figure 2. Although mechanisms are slightly different from turn-on, L_{PL1} continues to be the key parasitic involved. Additionally, with WBG devices having low $R_{ds(on)}$ values, damping of the Power Loop is minimal. Unfortunately, this often means limiting switching speeds to minimize oscillations.

There is one other mechanism that impacts the switching performance of the DUT. This mechanism is caused by the common parasitics (C_{gd} and L_{PL2}) in both the Power Loop and the Gate Loop (Figure 5). For the high di/dt events (turn-on and turn-off), the common inductance L_{PL2} creates a back EMF, which minimizes the effective V_{GS} in the Gate Loop. It is sometimes possible to see the ringing of the power loop superimposed on the V_{GS} due to this coupling (Figure 2). Similarly, the high dv/dt events (turn-on and turn-off) create a displacement current in the Miller Capacitance (C_{gd}) diverting gate current intended to charge C_{gs} . This result also negatively impacts the effective V_{GS} and the ability to quickly turn-on the DUT. Both effects impact the consistency and speed of the switching transition of the DUT.

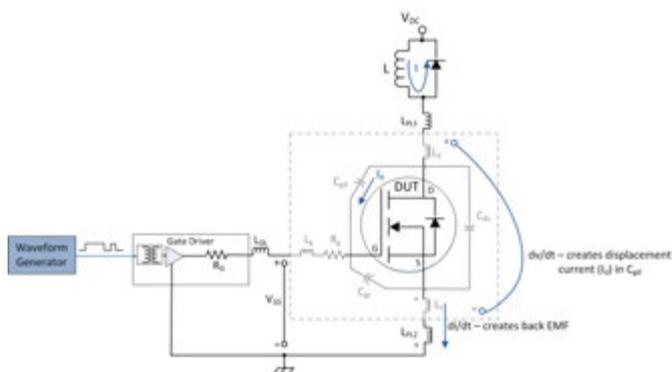


Figure 5: Power Loop parasitics minimizing Gate Loop drive.

DPT fixture design is quite a challenge, and as we've seen, becomes significantly more difficult as rise/fall times continue to decrease. One needs to consider high frequency effects of multiple second-order circuits (loops) and is often limited in the ability to minimize parasitic inductances and capacitances. Fundamental technology barriers

(e.g. low inductance interconnects) exist in designing and constructing DPT systems to characterize newer power semiconductors.

However, the Keysight PD1500A Dynamic Power Device Analyzer/ Double-Pulse Tester was developed to solve these tough problems. The PD1500A is a complete DPT system designed for Si and SiC based discrete power semiconductors. The system was architected to be modular and upgradeable as the market evolves to higher voltages and frequencies. Keysight has plans for additional versions to characterize power modules, GaN devices, and to provide some reliability testing (Short Circuit, Avalanche). Just as you've come to expect from the B1505/6A Device Power Analyzers, the PD1500A provides repeatable and reliable results (see typical waveforms in Figure 4).

The PD1500A's carefully engineered, modular fixture minimizes unwanted parasitics (Figure 6). Multiple gate driver options are provided with some standard resistor values, as well as an option for customer supplied resistors. DUT boards for TO-247 and SMD D2PAK-7 footprints and Si MOSFET, IGBT and SiC devices are also provided. Additional gate driver and DUT board options will be provided in the future.

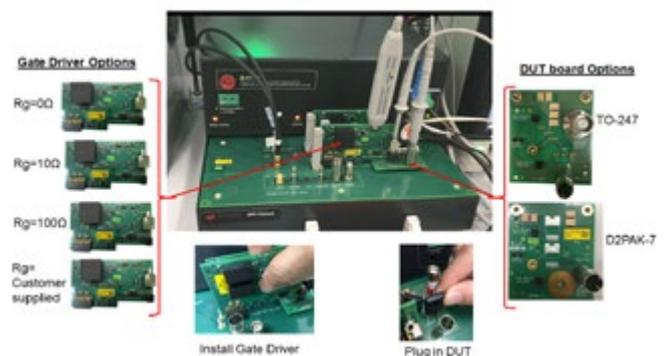


Figure 6: PD1500A DPT Modular fixture.

- [1] H. W. Johnson, M. Graham, "High Speed Digital Design – A Handbook of Black Magic", Prentice Hall PTR, Englewood Cliffs, New Jersey 07632, 1993, pp. 8-10, 399.
- [2] M. T. Thompson, "Intuitive Analog Circuit Design", Elsevier Inc., Second edition, 2014, pp. 35-37.

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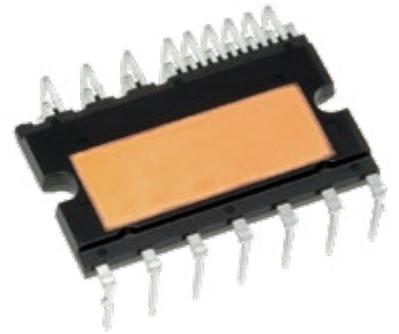
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An Intelligent Power Module for High Switching Speeds

Intelligent Power Module solutions are the preferred driver solution in home appliances, especially washing machines, resulting from several advantages. Low power drives should fulfil not only high efficiency, noise and reliability requirements, but also the requirement of optimized system cost. Mitsubishi Electric pioneered the DIPIPM™ concept in 1997, offering the solution to this market requirements since that time and continuing to present innovations in this segment.



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Introduction

Intelligent Power Module solutions are the preferred driver solution in home appliances, especially washing machines, resulting from several advantages. Low power drives should fulfil not only high efficiency, noise and reliability requirements, but also the requirement of optimized system cost. Mitsubishi Electric pioneered the DIPIPM™ concept in 1997, offering the solution to this market requirements since this time and continuing to present innovations in this segment.

The SLIMDIP™ family is the newest through-hole IPM, which offers reduced space requirements and an optimized pin layout compared to other DIPIPM™ products. The currently available products cover a motor power output range of 0.4kW (SLIMDIP-S) and 1.5kW (SLIMDIP-L).

Topology and protection functions

The SLIMDIP™ modules consists of six reverse conducting IGBTs (RC-IGBT), a high side driver IC, a low side driver IC and three bootstrap diodes with current limiting resistors. A direct control with a standard MCU is possible, due to the bootstrap diodes and the level shifter integrated in the HVIC, resulting in no need of a galvanic isolation and an isolated power supply to control the high side switches. All dies are directly mounted on the lead frame without using a PCB inside the module, offering a market leading lifetime performance. Figure 2 shows the used topology.

Sensor-less control of the spin drive in white goods is state-of-the-art. Therefore the SLIMDIP™ modules are built with open emitters on the low voltage side, to allow independent current measurements via shunt resistors. The output signals of the current measurement can be used for the internal short circuit protection, which prevents the module to operate outside of the SCSOA. Furthermore, the SLIMDIP-W integrates an over temperature protection with an additional temperature output with a linear temperature-voltage dependency, resulting in an easy-to-implement condition monitoring.

All SLIMDIP™ modules leaving the production line are tested regarding their static electrical characteristics and undergo a functional tests

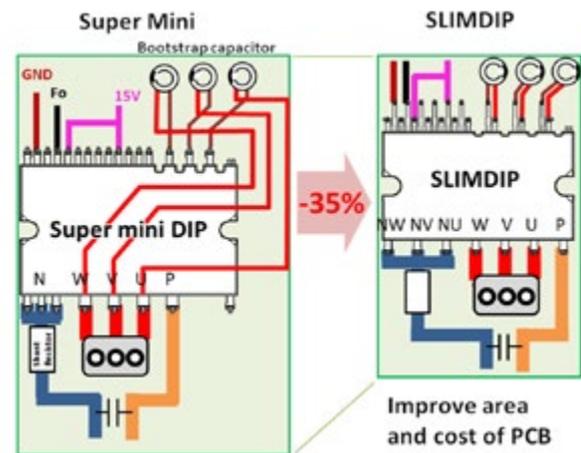


Figure 1: Reduced space requirements

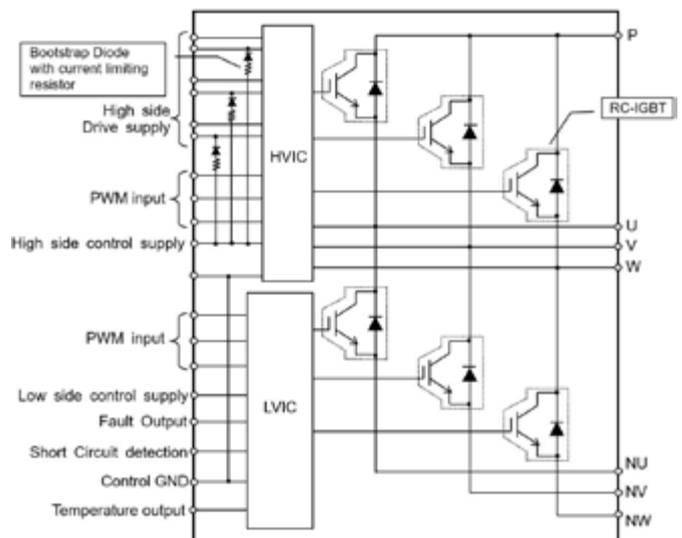


Figure 2: Topology integrated in the SLIMDIP module

with an inductive load. The results are recorded in an individual end-of-line test report in the factory.

The newly developed SLIMDIP-W module is a high-speed switching optimized version of the SLIMDIP-L module to fulfil the market demand of low audible noise inverters, which requires high switching speeds above the audible range of a human. Especially for home appliance products located in the living space, a low noise level is mandatory. For white goods sold in the EU, the EU energy label gives, beside the energy efficiency, the information about the noise level, allowing the customer the easy choice for a silent model.

Trends of the connected smart home lead the designer to develop the next generation of inverters in shorter time and more cost-effective. Especially in the home appliance segment, the SLIMDIP-W fulfils these requirements. One of the main reasons to achieve the compactness and price efficiency is the use of RC-IGBTs. With a blocking voltage of 600V and 2kVrms rated isolated thermal interface, the SLIMDIP-W is perfectly suited for single phase input inverters, not only found in white goods, but also in fans and pumps, both for household and industrial use.

Differences SLIMDIP-L and SLIMDIP-W

Developing the SLIMDIP-W module for high-speed switching required adaption on the chip level using the well proven RC-IGBT technology. Rated for the same current as the SLIMDIP-L, a suiting point for high switching speeds in the trade-off curve of $V_{CE,sat}$ vs E_{off} is chosen to achieve an optimal loss performances. Additionally, the gate driver was optimized, resulting in faster switching times.

SLIMDIP-L and SLIMDIP-W are fully pin compatible. This allows a use of the SLIMDIP-W in existing PCBs for the SLIMDIP-L without any modifications. Thermal design considerations are simplified as well, as the SLIMDIP-W uses the same type of insulation sheet.

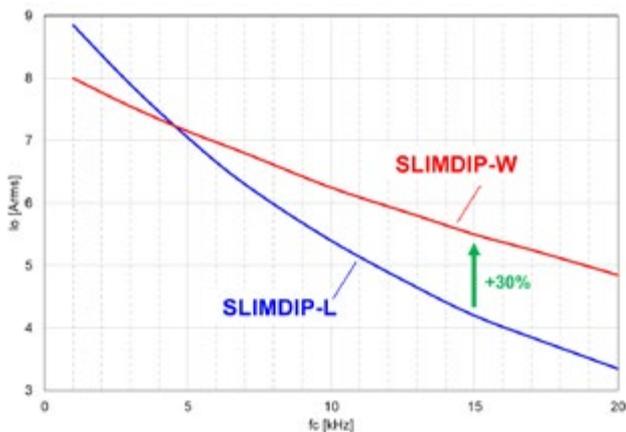


Figure 3: Maximum allowable output current ($V_{cc}=300V$, $V_D=V_{DB}=15V$, $P.F=0.8$, $f_o=60Hz$, $T_j=125^\circ C$ $T_c=100^\circ C$, 3 phase modulation)

Figure 3 shows a significant increase in efficiency at a higher switching frequencies with sinusoidal modulation. With the same application conditions, the SLIMDIP-W allows a 30% higher output current at a switching frequency of 15 kHz. For low switching frequencies, the SLIMDIP-L is the optimal product.

The differences in the losses can be explained with Figure 4. At the shown exemplary conditions, the SLIMDIP-W has higher conduction losses, but decreased switching losses than the SLIMDIP-L. In sum, the SLIMDIP-W outperforms the SLIMDIP-L at these working condi-

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tions. Background is the trade-off between conduction losses and switching losses, which can be optimized for a specified switching frequency. With the aim to provide a product for low audible noise inverters, higher switching frequencies are preferred. Figure 5 and Figure 6 show the static conduction characteristics and switching losses respectively for both devices, illustrating the increased conduction losses, but decreased switching losses in case of SLIMDIP-W.

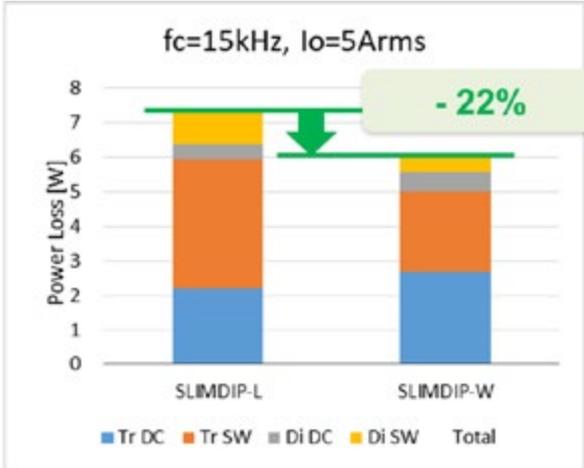


Figure 4: Simulated power loss comparison ($V_{cc}=300V$, $V_D=V_{DB}=15V$, $P.F=0.8$, $f_o=60Hz$, $T_j=125oC$, 3 phase modulation)

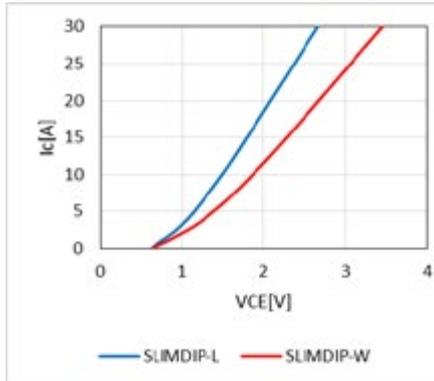


Figure 5: Conduction characteristic comparison

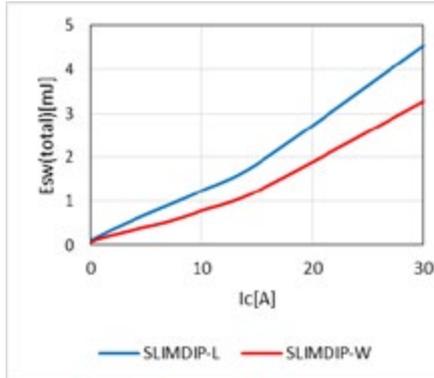


Figure 6: Switching loss comparison

Higher switching speeds comply with steeper switching waveform. Therefore, parasitic inductances and capacitances influence the switching behaviour more. On the strength of the well-designed package design of the SLIMDIP™ series, the switching curves do not show parasitic effects despite the more tough conditions (Figure 7).

Usually, faster switching speeds of the IGBT modules will increase also electromagnetic noise emissions. In this case, by adjusting the characteristics of the IGBTs, the EMI could be even improved, as shown in Figure 8.

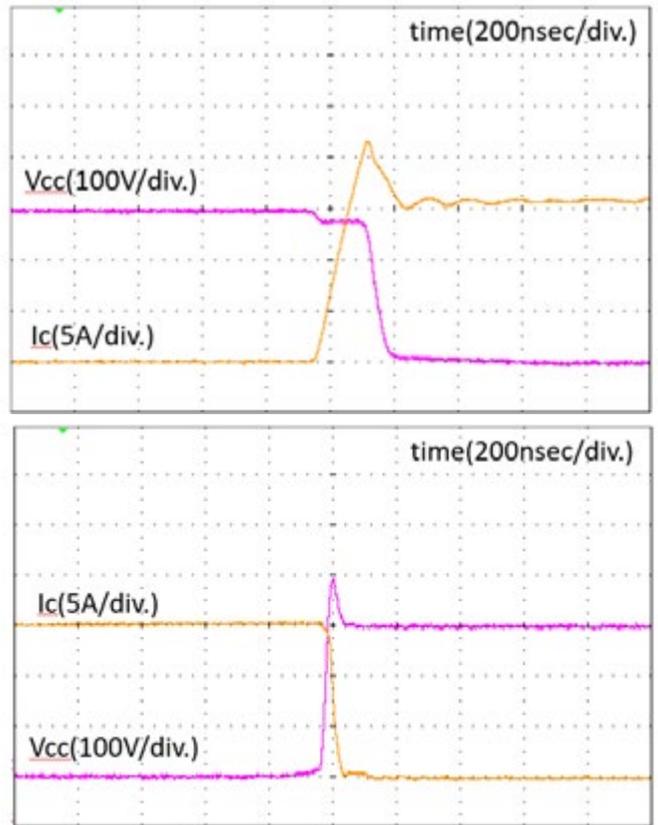


Figure 7: Switching waveforms (phase U, N-side)

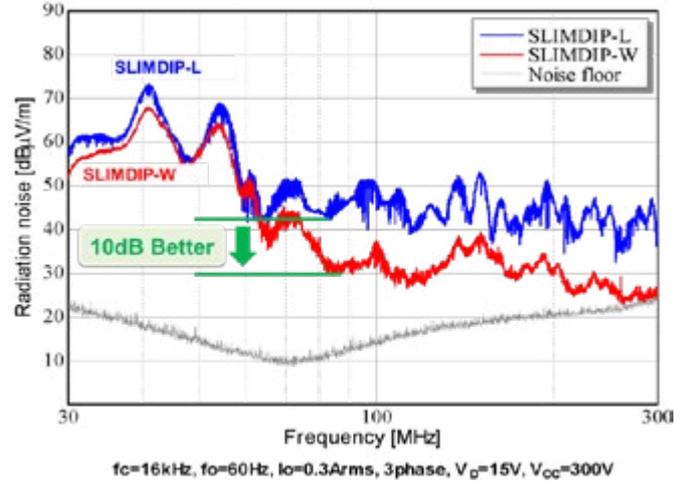


Figure 8: Radiated noise improvement

Conclusion and Outlook

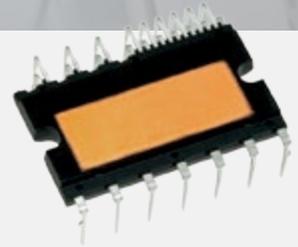
The new SLIMDIP-W module is the answer to the market demand for compact and price sensitive inverters in home appliance and small industrial applications with high switching speeds. Built with Mitsubishi Electric's long experience in producing transfer mould IPMs, a high reliability can be achieved. Due to the functional compatibility to the SLIMDIP-L module, existing inverters can be optimized for high-speed switching with minor effort. Moreover, the SLIMDIP-W shows improvements in the radiated electromagnetic noise to reduce challenges in the inverter design stage. The SLIMDIP-W will be in mass production in Q2/2020, samples are available at the German Branch of Mitsubishi Electric in Ratingen.

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Home appliances are becoming more and more demanding regarding functionality, reliability and efficiency. In the field of Power Semiconductors Mitsubishi Electric had created the necessary basis over 20 years ago as the pioneer of the DIPIPM™ transfer molded package intelligent power modules, followed by the continuous development and expansion of this series. Consequently, with the new SLIMDIP™-W a new Intelligent Power Module in the well-established SLIMDIP™ package has been added to the line-up to enable low losses with high switching frequencies, while keeping the electromagnetic noise low. The versatile integrated features give, for various applications in the industry and residential field, the benefit of reduced development time for the complete inverter system.

**New IPM in SLIMDIP™
package with latest RC-IGBT
chip technology**



The high-switching speed SLIMDIP™-W

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- Integrated driver ICs (HVIC and LVIC)
- Integrated bootstrap diodes and capacitors
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TDK is not only a leading manufacturer of EMC filters, but also a competent service provider in the field of EMC measurement technology. Such measurements during the development of snow guns are performed even under extreme conditions such as those in the Pfelders ski area in Italy.

*By Michael Vornkahl,
Director Development EMC Filter,
Magnetics Business Group,
TDK Electronics*



TechnoAlpin from Bolzano in Italy is the world market leader in the development and manufacture of snow guns. These are incredibly complex machines that have an intricate control system and whose drives for pumps and fans are controlled by converters. The TDK Electronics development department for EMC filters in Heidenheim, Germany, was commissioned to develop and manufacture a combined EMC and harmonics filter (Figure 1) for the type TR08 snow gun. The subsequent measurement of the complete system in standalone operation in TDK's own EMC laboratory in Regensburg, Germany, revealed a total harmonic distortion (THD) value of the current of around five percent.

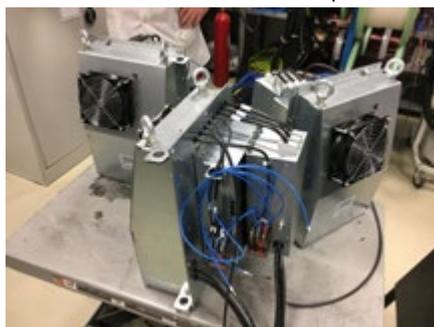


Figure 1: Combined EPCOS EMC and harmonics filters for the type TR08 snow gun from TechnoAlpin.

EMC measurement at an altitude of 2000 meters

To verify the functionality of the snow guns under real-life conditions it was necessary to perform an EMC measurement at an altitude of 2000 meters at the location of use in the Pfelders ski area. Consequently, all the measurement equipment had to be transported – by ski, in some cases – to this altitude. The measurements aimed to test in accordance

with EN6100-3-12, which stipulates the limit values for harmonics of the current.

Harmonics measurements in the field are not comparable with acceptance measurements for standards performed in the laboratory. Standard-compliant measurement is performed on synthetic power supply networks, which is not possible in the field, since other suppliers and loads are also attached to the same infeed section. For this reason, the quality of the existing network must be assessed before carrying out measurements on the object to be tested. In the actual example, the network also served the drives of the ski lifts that are operated via a thyristor-controlled soft-starter and produce a typical commutation notch at a 60° phase angle. In this operating mode alone, the measured THD of the current already stood at 7.3 percent. The Power Quality (PQ) box used for measurement detects the network quality and, in the case of a recognizably poor network, assesses this on a non-normative basis. This meant that a diagnosis using the PQ-Box was possible only to a limited extent.

In the measurements with the activated snow gun it was ultimately a matter of recording the difference in the harmonic components under the widest range of operating states. In addition, it was necessary to test whether specific operating states cause the harmonics filters of the snow guns to resonate.

In the ski area, under all tested operating conditions and under partial and full load, the THD did not exceed 8.1 percent; the

distribution across the various operating conditions was 0.5 percent

(Figure 2). This not only verifies stable operation but also confirms that the significant proportion of the THD does not originate from the snow guns.

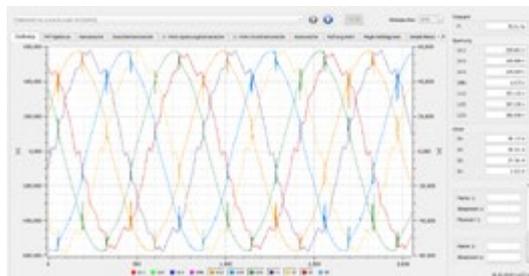


Figure 2: Screenshot of the voltage and current curves at full load, with all loads connected. A maximum THD of the current of 8.1 percent was not exceeded.

Although an evaluation for standards purposes could not be performed under the circumstances, it was possible to provide an estimate based on the measurement results according to the EN 61000-3-12 standard. Table 3 "Emission limits for harmonic currents for symmetrical 3-phase networks" shown in the standard was used for the assessment. A significant factor for the selection of the individual harmonic current components (I5, I7, I11, I13) is the specification of the short circuit ratio R_{sce} . This was defined with a value of 150. Not only were all resulting limit values complied with, but also the associated permissible characteristic values of the harmonic current. Conclusion: The TDK EMC filters meet the requirements of the system tested in the field.

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Double Pulse Testing: The How, What and Why

Testing the switching performance of power semiconductors in a safe and controlled environment is a challenge. Two or double testing is a key implement in the tool box of power electronics engineers that enables comprehensive and accurate measurements to be made early in the design cycle and so can help reduce time to market.

By David Levett, Ziqing Zheng and Tim Frank, Infineon Technologies

Introduction

There is an old engineering joke where at the start of a new design the program manager asks the engineer for a list of unforeseen problems that will come up during the project. Now the famous bard once wrote, "many a true word hath been spoken in jest" (1), and the reality is that unforeseen technical issues can put any project months or even years behind schedule. This is especially true if these occur late in a project. The earlier in any project technical issues can be identified the less impact they will have on the overall project timeline. So what has this to do with Double Pulse Testing (DPT)? Amongst the many benefits of DPT the most valuable is the ability to test a power stack under worst-case corner operating conditions early in the design cycle and so reduce risk of unforeseen problems popping up later in the program timeline.

A DPT is a tool which enables a power switch to be turned on and off at different current levels as shown in figure 1. By adjusting the switching times T1, T2 and T3 the turn on and turn off waveforms of the Device Under Test (DUT) can be controlled and measured over the full range of operating conditions.

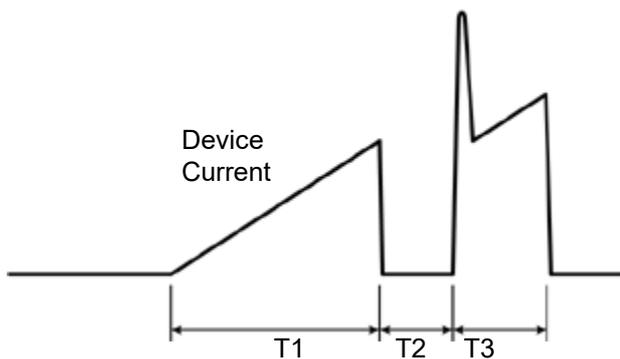


Figure 1: Double pulse waveform

How: Test setup circuit

Figure 2 shows a typical circuit diagram for a DPT experimental setup. Here the DUT, which is a SiC MOSFET, device 2 the lower left device in the "H" bridge, is instrumented so that the source current, drain to source voltage and gate to source voltage can all be measured while the device is switched. The switching times T1, T2, T3 and hence, currents can be adjusted using a programmable pulse generator. The complementary SiC MOSFET, device 1, is also switched for synchronous rectification operation. A load inductor limits the rate of di/dt. The key considerations for the selection of this inductor include:

- It should not saturate at the peak test currents.
- It should limit the di/dt so that the switching times (T1, T2 and T3 in figure 1) are not less than 10 μ s, to ensure the devices have fully turned on or off.
- The di/dt should not be so low that the switching times are longer than 200 μ s so as not to cause the DC bus voltage to dip by more than \approx 5 percent, and so change the switching performance. In addition, if the current pulse is long, then the chip temperature can increase by more than a few $^{\circ}$ C, again affecting the switching performance.
- The inductor should be mounted well away from the test setup to prevent EMI interference or magnetic field coupling into any gate drive circuits or instrumentation.

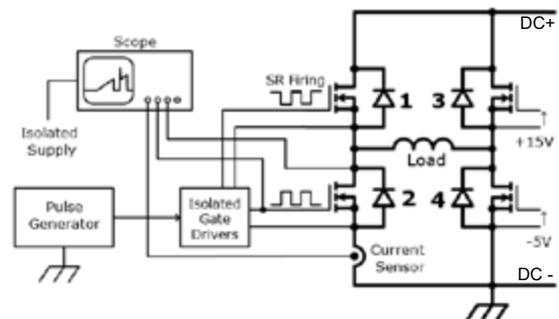


Figure 2: Typical DPT circuit diagram

The DC bus voltage level can be adjusted using a variable DC supply. Some frequently asked questions are:

Why the second pulse? It is important to build up current in the complementary device or diode so that when the switch turns on, the effects of any reverse recovery current firing can be evaluated.

Why is the configuration an H bridge as shown in Figure 2? Can a single half bridge be used with the load inductor connected to either DC+ or DC-? An H bridge is shown in Figure 2 as in many applications the load is switched between two half bridges and so this topology is a representative implementation of the final system. However, a single half bridge topology with the load inductor connected to either DC bus rail is simpler and will provide accurate results for most operating conditions. It is recommended that the full H bridge be used when testing modules in hard parallel. This H bridge can also be useful for evaluation of device performance under phase-to-phase short circuit conditions or under short circuit type 2 events depending on the customer application requirements.



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Can this be used to test a three level topology? Yes. This is shown in more detail later in this article.

Why is the DC minus supply connected to ground? In this case when measuring a lower device and using a “floating” DC bus power supply the DC minus supply can be grounded allowing instrumentation to be grounded and the use of single ended voltage probes rather than differential probes.

How do you test the complementary diode switching performance? The active switch can be pulsed in the same way; but, the instrumentation set up to measure the current through and voltage across the diode.

How: Safety

It is hard to over-emphasize the importance of safety when performing a DPT: high voltages can be lethal. Safety is critical during double pulse testing. Lethal voltages are often present and when components fail, the results can be dramatic and lead to the ejection of hot materials. For this reason, it is strongly recommended that the high voltage portion of the test setup be enclosed inside a protective cover (figure 3). This barrier can work both directions, keeping unwanted materials out, for example, a hand or cup of coffee, and keeping unwanted materials in, such as electrolyte from a failed capacitor.

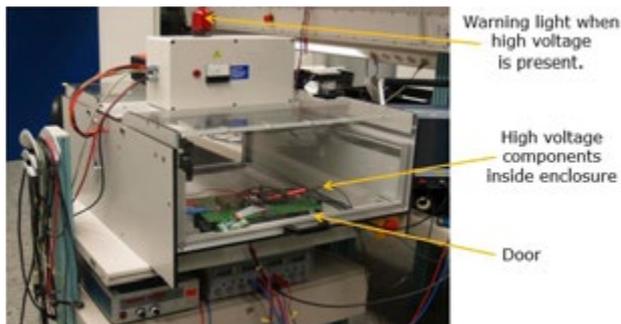


Figure 3: Example of a DPT enclosure

An additional layer of security can be added for the “distracted” operator by having a warning light when high voltage is present and an interlock on any access door, which, when opened will immediately cut power and discharge any high voltage capacitors.

Following are some suggested rules to be taken under serious consideration:

- Follow all company and lab health and safety guidelines.
- Always keep all high voltage components within a safe enclosure. A test enclosure can protect from accidental contact with high voltage circuits and provides a physical barrier during potential dramatic failure events.
- Disconnect high voltage supplies and discharge any high voltage capacitors before accessing high voltage circuits inside the enclosure. The addition of a permanent discharge resistor can provide another layer of safety.
- Use correct grounding for instrumentation. Employ safe methods to measure upper devices (e.g. differential probes). Ensure a good low impedance ground connection to the module mounting plate and enclosure metal structure or surfaces.
- In case of a module failure, ensure that the high voltage DC supply has a current limiting feature or fast acting fuses to limit fault energy.
- Never work alone when high voltages are present.
- Ensure all equipment users have received correct safety and first aid training.

- Ensure the equipment has a clearly marked and easily accessible emergency power off button.

As shown in Figure 2, it is possible to ground the DC minus when measuring the lower devices and so have instrumentation at a safe ground potential. For measurement of upper devices, isolated current sensors and differential voltage probes must be used enabling the scope to operate at a safe ground potential.

It is good to use the “buddy” principle in the event of an incident so someone is available to provide cardiopulmonary resuscitation and call for emergency aide. Finally, if high temperature chip switching tests are being performed, components surfaces can be at temperatures $>50\text{ }^{\circ}\text{C}$ and so cause burns. Caution is required.

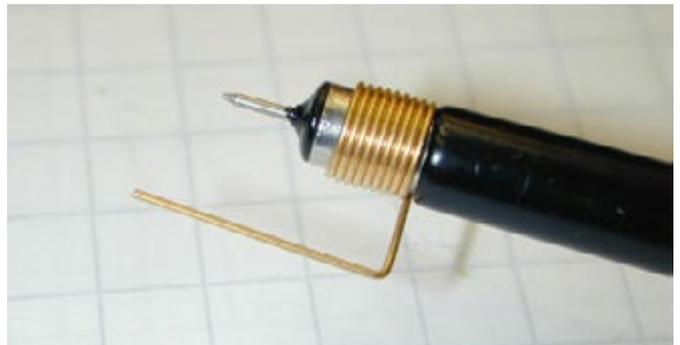


Figure 4: Voltage probe tip to reduce inductance in measurement loop



Figure 5: Voltage probe with some added common mode impedance

How: Instrumentation

To measure the DUT voltages as shown in Figure 2, it is possible to use single ended probes. Figure 4 and 5 show some techniques to reduce loop inductance and coupling in the measurement path and how some turns around a ferrite core can add common mode impedance to the measurements signal. To measure voltages at non ground reference potentials, differential probes are required and should be selected with a high common mode rejection ratio, as the DUT can be moving at very high dv/dt levels with respect to the scope ground. Ensure that all voltage probes have the required voltage rating.

To measure the actual device switching current, a current sensor must be inserted into the collector/emitter or source/drain of the DUT. This can be a challenge as accuracy is required but it is important

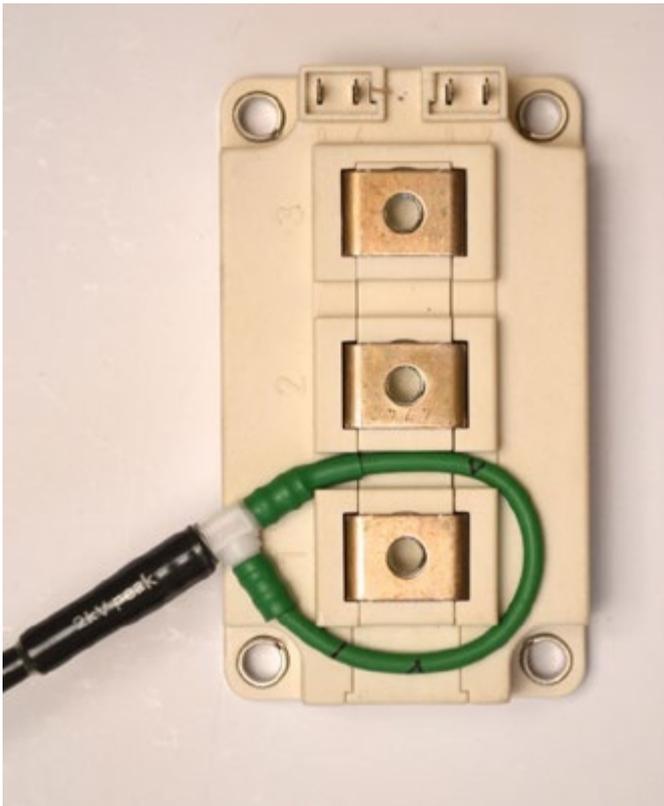


Figure 6: Rogowski coil fitted around the terminal of a 62 mm module



Figure 7: Rogowski coil fitted around a standoff fitted into the terminal of an EconoDUAL™ 3 module



Figure 8: Rogowski coil fitted around the terminal of a PrimePACK™ 2 module

not to add a large amount of loop inductance which would distort any results. Typical methods include; but, are not limited to:

Pearson current sensors (2): These have a very high bandwidth and accuracy. However, they have the disadvantage of being large, so making it difficult to insert into the power circuit without increasing the loop inductance. They also have a metal case which can make it problematic to isolate from live bus bars etc.

Rogowski coils (3): These have a bandwidth of between 15-30 Mhz which is enough for many applications and any delay skew can be compensated for with an oscilloscope. They have the advantage of being flexible and so are easy to insert into the power circuit. Figures 6, 7, and 8 show them used on a 62 mm, EconoDUAL™ 3 with small standoffs and a PrimePACK™ module. In case it is needed, do not be afraid to cut a little plastic to help getting the coil to fit. Some high power modules have more than one screw connection for the collector or emitter current and in this case more than one probe might be required. Figure 9 shows how a coil can be used on a PCB based design with a loop around a current carrying trace. This method requires that the PCB designed with this end in mind.

Figure 10 shows a typical Pearson and Rogowski current sensor. Current shunts can be used especially on low current devices where they can be fitted into a circuit without a significantly increasing the loop inductance.

How: Three level an example

DPT of a three level topology requires additional consideration. Working with Figure 11 as a reference of a Neutral Point Clamp (NPC) I topology, the switching patterns are described in Table 1. Test sequence 1 is shows a switching sequence between the neutral point and DC-. Test sequence 2 shows a switching sequence between the neutral point and DC+. To measure the opposing devices the load inductor can be connected between the output and DC+ and a complementary switching sequence used. Note S1 must always be turned off before S2 to avoid the full bus voltage being applied across S1.

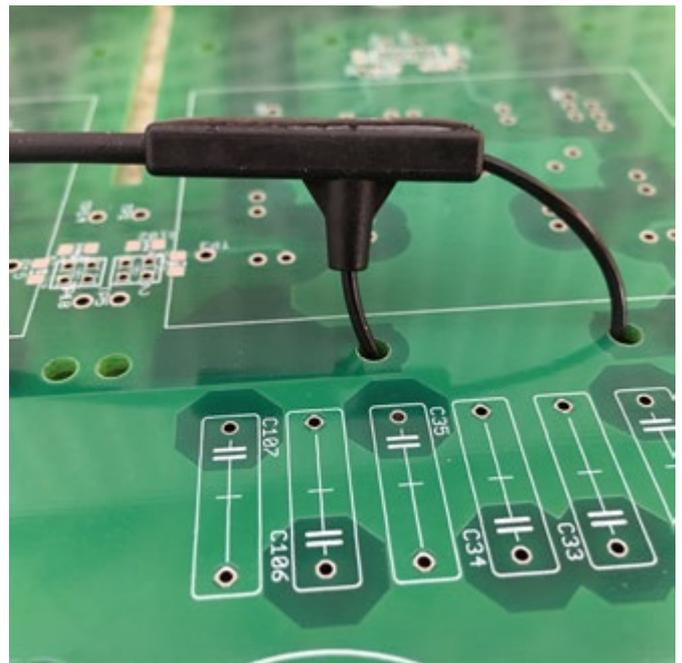


Figure 9: Rogowski coil used to measure current in a PCB trace

What testing should be included in a DPT

It has been shown how the DUT can be switched at different voltages and currents. A third key parameter that affects the switching characteristics of a power semiconductor is temperature. This can be adjusted by mounting the DUT on a plate, which can be heated or cooled. For testing at temperatures lower than 0°C, which can be achieved with a chill plate and freezing water, the test setup can be installed inside an environmental chamber and the temperature reduced to -20°C or -40°C as the application dictates.



Figure 10: An example of a Pearson (left) and Rogowski coil (right) current sensor

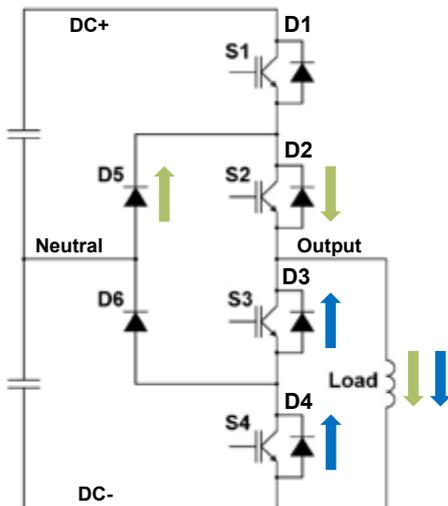


Figure 11: NPC1 topology. For test sequence 1 current shown in green for time periods 1 and 3 and blue for time period 2

With this set of three variables, the DUT can be operated at the key corner operating points, for example, maximum bus voltage, maximum current but low operating temperature. This combination can produce the highest voltage overshoot during turn off, and so is critical to ensuring the DUT remains within its RBSOA. It is recommended to measure both the active switch and any complementary diode under this range of operating conditions.

Test Sequence	Time Period	Switches that are Commanded On (All Other Switches are Commanded Off)	Devices that are Conducting Current
1	1 (Pulse 1)	S2	S2 and D5 Green
	2	None	D3 and D4 Blue
	3 (Pulse 2)	S2	S2 and D5 Green
2	1 (Pulse 1)	S1 and S2	S1 and S2
	2	S2	S2 and D5
	3 (Pulse 2)	S1 and S2	S1 and S2

Table 1: Test switching pattern.

Apart from corner conditions, several other tests should be considered.

- Short circuit and over current protection circuits both phase to phase and shoot through. Note care should be taken, especially with higher current power modules, as the high di/dt levels that occur during a short circuit event can cause magnetic field coupling from bus bars and cables into gate driver circuits, power supplies and instrumentation.
- If the switch dv/dt needs to be limited below a certain level, as is often required in motor drive applications, the value of gate resistor can be adjusted to meet the desired value.
- Accurate measurement of the device switching losses. Although the data sheet is a good starting point for switch loss estimation, typically a design will differ from the operating conditions used to derive the data sheet values (4). These differences, for example in the gate driver and bus inductance, will produce different switching loss energies than those listed in the data sheet. Measuring these dynamic losses is important to estimate system efficiency and the maximum junction temperature of the power semiconductors.
- Measurement of the switching loop inductance, di/dt and voltage overshoot to understand the factors involved in designing within the power device RBSOA.
- Measurement of the switching times can be used to evaluate the values for the dead or interlock delay time to prevent shoot through events (5).
- In a half, bridge topology, check the upper device gate waveform in the off state when turning on the lower device to check for the possibility of parasitic turn on due to the Miller capacitance.
- Sample size and device-to-device parameter variation is a difficult topic. It is very not realistic to measure say 100 devices and create statistical analysis for all parameter variations from the results. It is recommended that engineers collaborate with their power semiconductor supplier to bound the scale of any variations and ensure that suppliers have a high level of consistency and quality in their production processes.

Benefits of testing

There is a considerable investment required to build a DPT setup and it is important to ask for a return on this investment. Some of the re-

turns are that it is safer and faster to make measurements under the controlled conditions of a DPT compared to making these same measurements in a final converter assembly where, for example, the junction temperature is difficult to control or measure.

Waveforms and test results can be stored as reference waveforms and if changes are required later in the design or during production these can be used as templates to evaluate the effect of any design modifications.

Accurate measurement of switching losses is critical for the estimation of the device junction temperature under worst case operating conditions.

Having a standard test plan and setup helps all power converter designs to share a common qualification process.

As stated in the introduction, running these tests early in the design cycle and being able to solve any issues that arise can help keep any project on track.

Now a key and difficult question is when in the design cycle to perform this testing. Too early and the design is not representative of the final system and too late and there is a risk of an issue that can cause significant time delays to the program. Engineers should use good design judgement and try to perform the testing as early in the design cycle as possible.

It must be noted that DPT can cover most of a power semiconductor operating conditions; but it cannot fully emulate operation of a full converter. Issues like noise pick up on control lines, software bugs and effects of magnetic fields, all of which can affect the reliable operation of the power switches, will not be identified with this test. DPT does take time and design effort. However, this effort will provide a payback in terms of safety, accuracy, product reliability and project timelines.

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Higher V_{GS} Threshold Voltage Benefits in Resonant Applications

In this article, was investigated the impact of a super junction MOSFET gate-source threshold voltage (V_{GSth}) in soft switching applications, using a half bridge LLC as test vehicle. A higher $V_{GS(th)}$ impacts many aspects and introduces certain benefits and disadvantages as well.

By Domenico Nardo, Alfio Scuto and Simone Buonomo, STMicroelectronics

V_{GSth} role during turn-off

Our first analysis concerns higher V_{GSth} values during the turn-off of a SJ MOSFET. As shown in Figure 1, the threshold voltage defines t_{off} , and the drain current must fall to zero when VGS reaches the threshold, so a higher V_{GSth} reduces the t_{off} , which equates to lower switching losses. We performed a simulation in SIMetrix that reproduces a double pulse test to verify this behavior. The same spice model was used and only the V_{GSth} parameter was changed. Table 1 shows the results.

Pulse test results				
	dV/dt [V/ns]	dI/dt [A/μs]	t_{off} [ns]	E_{off} [μJ]
V_{GSth} 3V	43.60	655	10.11	11.12
V_{GSth} 4V	46.00	765	9.11	9.01

Table 1: Pulse test result

The model we used corresponds with the same MDmesh™ technology from STMicroelectronics, with the only differences being the gate to source voltage thresholds. The simulation confirms an improvement in switching performance for the higher 4V threshold with respect to a 3V threshold.

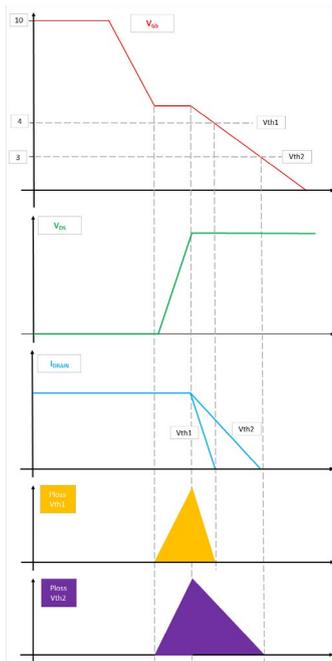


Figure 1: V_{GSth} role during turn off

Figure 2 shows that the peak power associated with the higher threshold is lower than the other, and also confirms the shorter t_{off} time associated with the higher threshold.

Clearly, V_{GSth} impacts the turn-off mechanism in hard switching applications in a similar way to soft switching, but the presence of turn-on losses implies a trade-off between E_{on} , E_{off} and V_{GSth} .

Application results

To confirm the simulation results, the same MDmesh™ technology was evaluated in a Half bridge LLC (HBLLC) resonant converter using identical DUTs except for different gate threshold levels ($V_{GSth} = 3V / V_{GSth} = 4V$). Table 2 shows the measured V_{GSth} values. The HBLLC used is the

EVAlJIG_HBLLC_v4.1 an open loop converter, rated at 600W. The E_{off} is taken at 10%, 25%, 50%, 75% and 100% of the P_{out} (see Table 3), in order to evaluate the differences in terms of switching energy, and how this lower turn-off energy is reflected in terms of higher power efficiency.

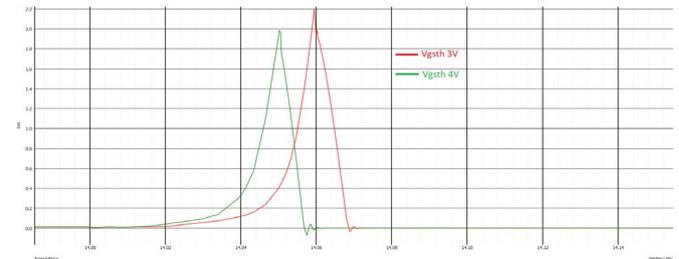


Figure 2: P_{off} switching waveforms for $V_{GSth} = 4V$ in green and $V_{GSth} = 3V$ in red

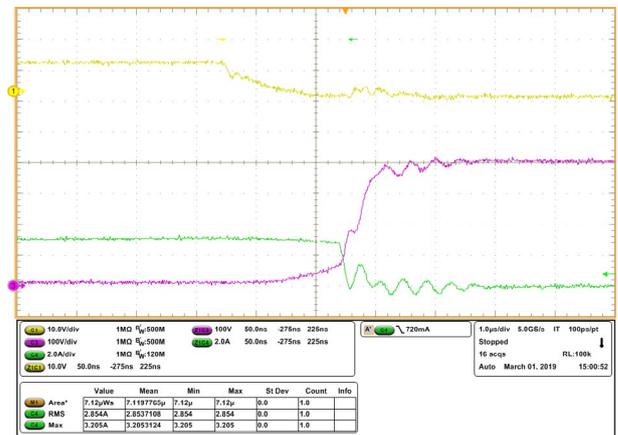


Figure 3: Turn off waveforms, $V_{th} = 3V$

Measured V_{GSth}				
	Higher V_{th}		Lower V_{th}	
V_{GSth} (V) @ 250μA	Q_{HS}	Q_{LS}	Q_{HS}	Q_{LS}
	4.10	4.12	2.97	3.05

Table 2: Measured V_{GSth} value for the four devices under test

Figure 3 and figure 4 show the waveforms taken with an oscilloscope at 10% of the maximum load. The measurement setup used is the following:

- Tektronix AFG 3021, signal generator
- Tektronix DPO 7104C, oscilloscope
- TDK-LambdaGEN 600-5.5, power supply

- Agilent N3300A, electronic load
- Yokogawa WT310, power meter
- Tektronix TCP0030, current probe
- Tektronix P5205A, differential voltage probe
- Tektronix P6139B, passive voltage probe
- Flir E30, thermocamera

Turn-off energy		
E _{off} (μJ)		
P _{out}	V _{GSth} 4V	V _{GSth} 3V
10%	6.67	7.12
25%	10.64	11.54
50%	12.93	14.28
75%	13.5	15.3
100%	14.7	16.95

Table 3: MOSFET turn-off energy for differing V_{GSth} values

Starting from the values in Table 3, it is possible to calculate the power associated with the E_{off} delta for a known switching frequency using the well-known formula shown in Equation 1.

$$P_{SWoff} = E_{off} \cdot f_{SW} \quad \text{Eq. (1)}$$

The results in terms of power efficiency are given in Table 4. Delta power represents the difference in terms of P_{in} for the bridge section (two MOSFETs) of the DUT with V_{GSth} = 3V minus the P_{in} for V_{GSth} = 4V at the same P_{out}; considering only the increase in Pin due to higher turn-off power. While delta efficiency represents the difference in percentage between 4V and 3V.

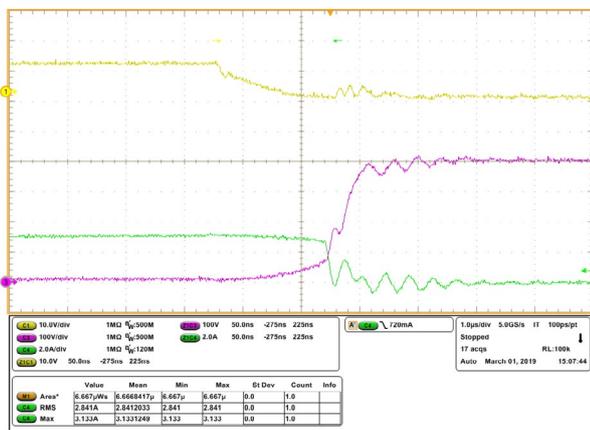


Figure 4: Turn off waveforms, V_{th} = 4V

It is clear that a higher gate threshold leads to higher efficiency, especially at light loads. ΔT represents the difference in temperature for each device with the lower threshold; Equation 2 shows the relation-

Δpower and Δefficiency					
P _{out}	Eff. V _{GSth} 3V (%)	Eff. V _{GSth} 4V (%)	Δpower (W)	Δefficiency (%)	ΔT (°C)
10%	90.96	91.07	0.134	0.111	4.2
25%	92.05	92.19	0.247	0.140	7.7
50%	92.79	92.88	0.327	0.094	10.2
75%	92.55	92.63	0.409	0.078	12.8
100%	92.04	92.11	0.486	0.069	15.2

Table 4: Δpower and Δefficiency

ship between power and temperature, where R_{thj-amb} for a TO-220 package is 62.5 °C/W. It is important to highlight that the MOSFETs used in this test are measured without heatsink.

$$\Delta T = \frac{(\Delta power \cdot R_{thj-amb})}{2} \quad \text{Eq. (2)}$$

Advantages and disadvantages

Below is a summary of the benefits and drawbacks associated with a higher V_{GSth}:

Advantages:	Disadvantages:
<ul style="list-style-type: none"> • Smaller turn-off time • Lower switching losses • Higher immunity to false turn-on due to noise • Lower gate oscillation 	<ul style="list-style-type: none"> • Impact on gate driver • Higher di/dt

The threshold voltage sets the condition when the current starts to flow in the MOSFET; if there are disturbances in the converter or if the ground plane is weak, some current can flow on the gate resistance (through the parasitic gate to drain capacitance C_{GD}) and may create a voltage between gate and source terminals that could turn on the MOSFET and thus compromise the reliable operation of the entire system. Higher thresholds give higher immunity because the voltage required across Gate and Source (i.e., the product of R_{Gon} and noise current) to turn on the MOSFET is higher.



Figure 5: Transfer characteristics for MDmesh™ technology, in purple with V_{GSth} = 3V and in dot blue with V_{GSth} = 4V

The higher threshold also mitigates the gate oscillation that occurs during turn-on and turn-off, which can improve the reliability of the device due to lower gate oxide stress.

A major drawback is the impact on the gate driver. In some lighting applications or chargers, the driving voltage is less than 10V; around 6 to 8 V. Figure 5, which shows the transfer characteristics of two devices with respective V_{GSth} = 3V and 4V values, demonstrates that a higher threshold limits the current capability when the driver is unable to operate with 10V.

Considering all the advantages and disadvantages of higher V_{GSth} in resonant applications, it seems that this approach is the right option as it improves electrical and thermal performance, especially at light loads, and increases noise immunity as well as mitigating gate oscillation.

Wireless Charging – Wireless Disturbance?

With the development of a universal inductive charging system, Finepower GmbH from Munich has underlined its leading position in power electronics and battery charging systems. After many developments in the field of offboard and onboard charging devices for industry and electromobility, Finepower is now already working on improving the charging technology of tomorrow.

*By Dipl.-Ing. (TUM) Georg Heiland, Finepower GmbH
and Dr.-Ing. Christof Ziegler, TDK Electronics AG*

Introduction

Inductive charging systems for electric vehicles are currently hot topics for research, development and standardization. Typical examples of applications include contactless recharging of trucks, forklifts and AGVs in the industrial sector as well as electric vehicles in road traffic. Due to the varying system properties of the vehicles, such as ground clearance, battery voltages, coil geometries and current carrying capacity, at the moment every manufacturer is aiming to develop its own inductive charging unit tailored to the requirements of a particular vehicle fleet. By contrast, as part of the research project UnIndCha (Universal Inductive Charging) sponsored by the Bavarian Ministry of Economic Affairs, Energy and Technology (StMWi), Finepower is currently working on establishing an inductive charging station capable of working with the highest possible number of different vehicle types – with correspondingly different receiver coils and battery systems.

TDK Electronics AG (formerly EPCOS AG) is involved in the project as a manufacturer of transmitter and receiver coils for inductive charging systems and focuses particularly on ensuring the electromagnetic compatibility (EMC) of universal systems. In addition, the Associate Professorship of Energy Conversion Technology at the Technical University of Munich (TUM) and the Technology Network Allgäu (TNA) at Kempten University of Applied Sciences are contributing fundamental research papers.

Frequency tuning versus variable resonant circuit tuning

Normally, inductive charging systems are tuned to a particular frequency, whereby capacitances are connected to the transmitter coil on the transmitter and receiver side. With this combination, the system can be designed for the normatively required transmission frequencies. Such a combination of coils and capacitances creates a resonant (oscillating) circuit, which has a particular natural frequency known as the resonant frequency.

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Depending on the positioning of the transmitter and receiver coils in relation to each other, the resonant frequency shifts to higher or lower values depending on the change of inductance, which defines the resonant frequency.

To maintain the required charging power the transmission frequency then needs to be adjusted accordingly.

Instead of varying the transmission frequency, an alternative method varies the tuning of the resonant circuit. For instance, additional capacitances are switched on or off to keep the resonant frequency constant. Figure 1 shows a circuit built in the research project.

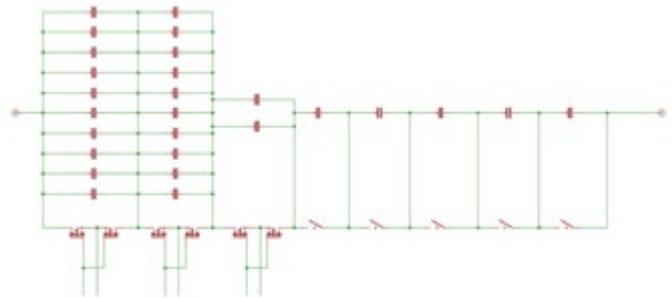


Figure 1: Circuit for variable tuning of an inductive charging system as implemented in the research project

Influence on emitted electromagnetic interference

In inductive charging systems, the energy transfer is performed via the magnetic field that results from the high-frequency AC current flowing through the transmitter coils.

If we look at this current in an oscilloscope, a sinusoidal shape can be seen that corresponds to the resonant frequency of the transmission system. The physics of the electromagnetic waves explain that the time-based change in the magnetic field corresponds to the time-based change in the coil current (Maxwell's law describing the magnetomotive force):

$$N \cdot I = \oint \vec{H} \, d\vec{l}$$

However, despite the apparently perfect curve shapes for the current and magnetic field, such a system cannot satisfy the required normative limits without further filtering efforts due to additional harmonic frequency components, that are more or less distinct depending on the main operating frequency.

These harmonics always occur, if the operating frequency differs significantly from the resonant frequency. Depending on the sign of this deviation, the following examples of current forms can result under the same load conditions (simulated using parameters of the real system).

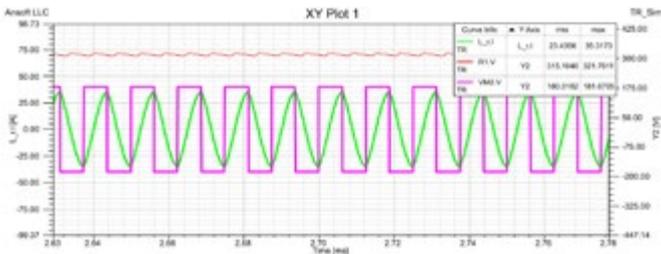


Figure 2: Expected current and voltage forms at the transmitter coils at an operating frequency that is above the resonant frequency of the system (above resonant operation)

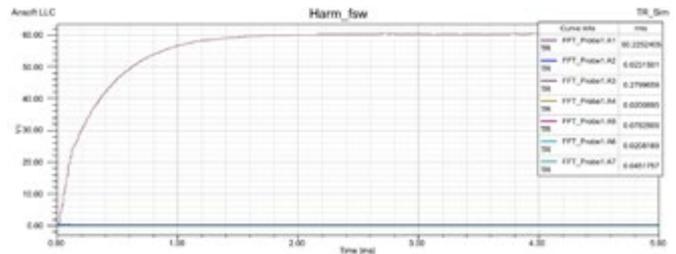


Figure 7: Expected amplitudes of the harmonics of the coil current at an operating frequency that corresponds to the resonant frequency of the system (resonant operation)

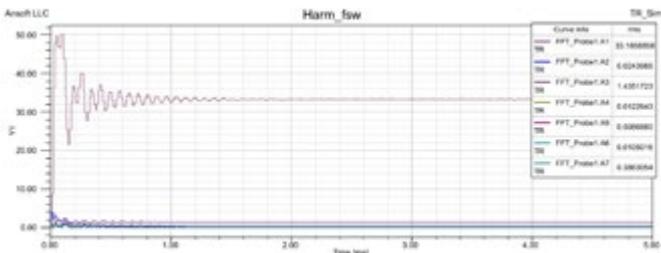


Figure 3: Expected amplitudes of the harmonics of the coil current at an operating frequency that is above the resonant frequency of the system (above resonant operation)

A frequency analysis of the current form (FFT) yields the following values for the harmonics:

A comparison of the harmonics of the coil current shows that the values are significantly lower for the case "resonant operation":

Harmonic	% of fundamental wave	Above resonant	Below resonant	Resonant
1	100.00	100.00	100.00	100.00
2	0.07	0.08	0.04	0.04
3	4.34	5.21	0.47	0.47
4	0.04	0.03	0.03	0.03
5	1.81	1.95	0.13	0.13
6	0.03	0.03	0.03	0.03
7	1.17	1.38	0.07	0.07

Table 1: Coil current harmonic analysis in dependence of operating point

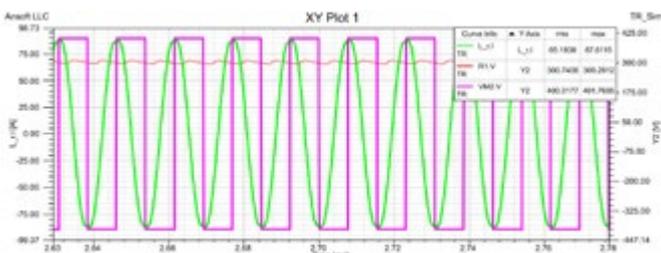


Figure 4: Expected current and voltage forms at the transmitter coils at an operating frequency that is below the resonant frequency of the system (below resonant operation)

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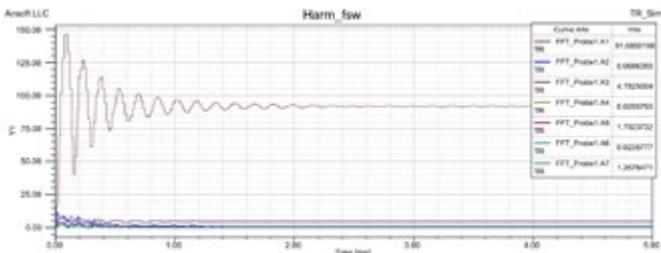


Figure 5: Expected amplitudes of the harmonics of the coil current at an operating frequency that is below the resonant frequency of the system (below resonant operation)

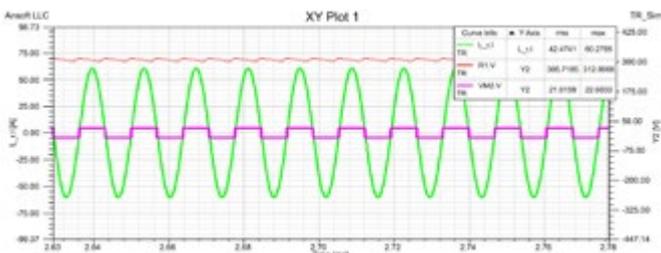


Figure 6: Expected current and voltage forms at the transmitter coils at an operating frequency that corresponds to the resonant frequency of the system (resonant operation)

However, normative requirements are related to magnetic field strength, not the coil current. The following assessment provides a qualitative overview of the resulting emitted magnetic fields based on the current harmonics in Table 1.

For a straight conductor through which a current flows, a circular magnetic field can be assumed with an amplitude that is inversely proportional to the distance between a magnetic field line and the conductor (near field).

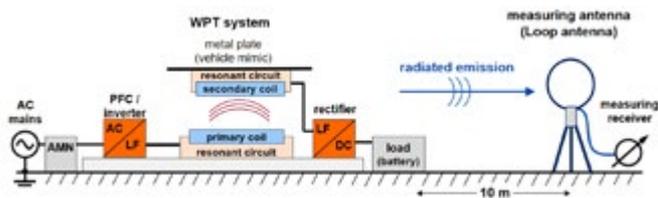


Figure 8: Principle measuring the magnetic field strength with a loop antenna for evaluation of the emitted EMC interference in the frequency range between 9 kHz and 30 MHz

$$|\vec{H}| \approx \frac{I}{2\pi r}$$

The applicable standards require the magnetic field to be measured at a distance of 10 m. In the example shown above, this yields the following approximate field strengths (peak values):

Harmonic [dBµA/m]	Above resonant	Below resonant	Resonant
1	114.5	123.3	119.6
2	51.6	60.8	51.3
3	87.2	97.6	73.0
4	45.6	53.6	50.1
5	79.6	89.1	61.9
6	44.9	51.6	50.5
7	75.9	86.1	57.1

Table 2: Magnetic field harmonic analysis in dependence of operating point [peak values]

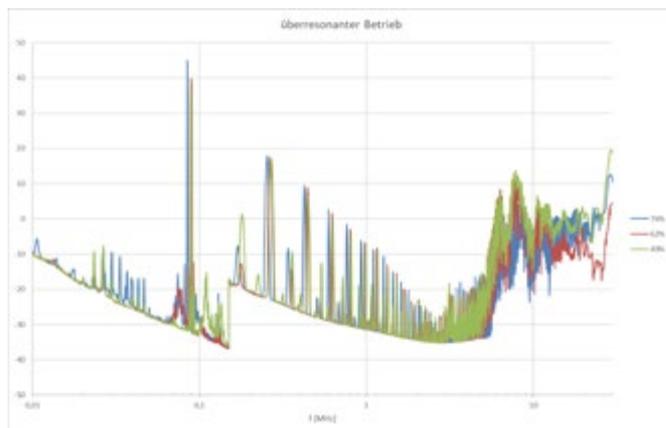


Figure 9: Magnetic field spectrum during operation with different tunings of the resonant circuit, out of resonance in each case

It is easy to see that the spectrum of the current or magnetic field varies extremely at different operating frequencies. In the calculated example above, the lowest emitted interference is expected when the system is operated in resonant mode.

Measurement results

In the research project UnIndCha, a prototype of an inductive charging system was set up and the emitted magnetic interference in the frequency range between 9 kHz and 30 MHz was measured at different transmission frequencies of the WPT system.

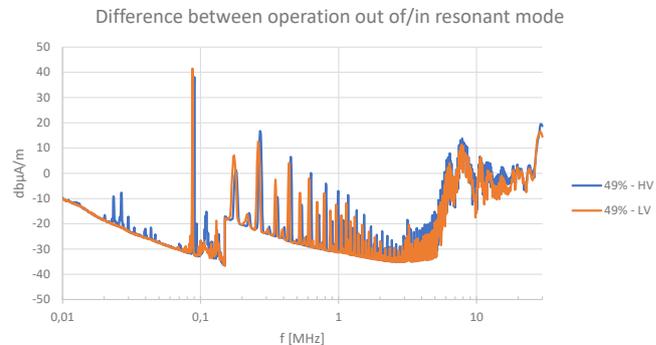


Figure 10: Magnetic field spectrum during operation with the same resonant circuit tuning, with different frequencies (out of/in resonant mode)

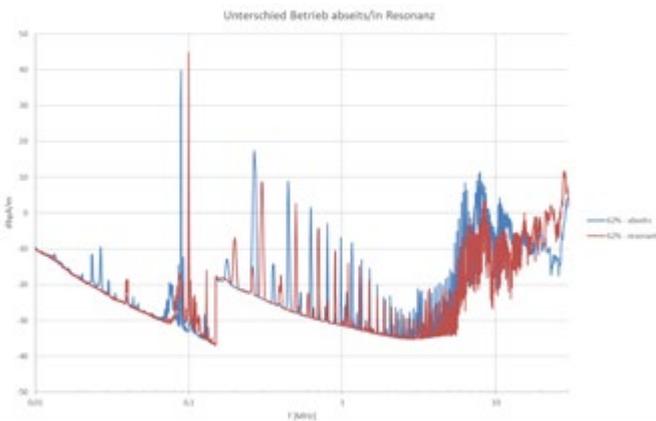


Figure 11: Magnetic field spectrum during operation with the same resonant circuit tuning (but different to Figure 10), with different frequencies (out of/in resonant mode)

The results show that different resonant circuit tunings lead to different levels of emitted interference at otherwise identical operating parameters. These differences are caused by varying deviations between the operating frequencies and the resonant frequency of the system. Depending on the tuning, a reduction of emissions by up to 10 dBµA/m was observed in the various series of measurements.

In line with the theoretical assumptions, the minimum levels for interference emissions were obtained when the system was operated in resonant mode.

In addition, an optimum tuning value of 62% was determined in the measurements, which suggests that with variable tuning the emitted interference increases again if the compensation is too high.

With higher offset positions between transmitter and receiver coil, it can be assumed that the effectiveness of the tuning adaptation increases. Thanks to the option of variable resonant circuit tuning, at higher offset positions it is always possible here to ensure that the system operates within the normatively required frequency range.

Table 3 summarizes the measured harmonic amplitude values at different operating frequencies. Compared to the theoretical values of

- -55 ... +125°C
- LONG LIFE
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- VIBRATION 20...45 G

Table 2, a qualitative match can be found, although the absolute quantitative values differ.

The discrepancies to the theoretical considerations are primarily caused by the measurement principle that allows to measure only one vector polarization (x,y or z) of the magnetic field, which is a greater or lesser fraction of the overall field vector.

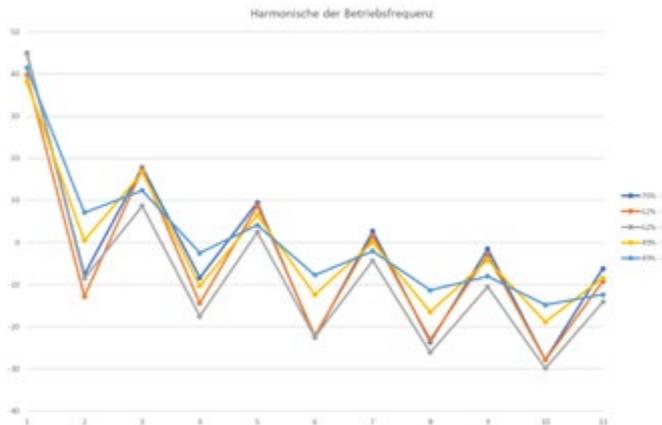


Figure 12: Graphical comparison of the harmonics of the operating frequency of the measured different resonant circuit tunings from Figures 9 - 11

In the theoretical considerations always the maximum value of the field vector was calculated due to the assumption of an ideal, straight conductor and, resulting from this, an ideal, circular magnetic field.

Conclusions

The measurements of interference emissions revealed large variations while operating at different frequencies and tuning settings. A significant reduction of the harmonics was

attained during operation at the resonant frequency. Therefore a circuit design with the option to readjust the resonance tuning is very beneficial, particularly at high coil displacements. Such circuit designs have been investigated by Finepower in the research project UnIndCha.

[dBµA/m]	76% – above resonant	62% – above resonant	62% – resonant	49% – above resonant	49% – resonant
1.	45	39.8	44.8	38.1	41.5
2.	-7.6	-12.8	-8.5	0.5	7.1
3.	17.8	17.4	8.7	16.7	12.4
4.	-8.4	-14.4	-17.5	-10.3	-2.5
5.	9.5	8.8	2.5	6.5	4.1
6.	-22.5	-22.1	-22.4	-12.4	-7.7
7.	2.7	1.6	-4.3	0.1	-2.0
8.	-23.6	-23.1	-26.1	-16.5	-11.3
9.	-1.5	-3.0	-10.5	-4.1	-8.0
10.	-27.9	-27.9	-29.9	-18.9	-14.8
11.	-6.2	-9.2	-14.1	-8.4	-12.4

Table 3: Comparison of measured harmonics of magnetic field strength at different operating points

www.finepower.com

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- as VACSIC 45 g Vibration
- 5 FIT

DC-DC Power Converter for Offshore Windfarm Integration

Real time simulation gains more and more place in the academic field as well as in the industrial one. It helps engineers and researchers to reduce time development of some concepts/ideas and allows their validations especially during test cases that are difficult to reproduce in real life. SuperGrid Institute with its real time platform makes available to their clients all the necessary facilities including resources and support to ensure such experiments in optimal conditions.

By Ahmed ZAMA, Laurent CHEDOT and Luc BOURSERIE, SuperGrid Institute

In the following, an example of study that has been held in SuperGrid Institute real time platform is presented. It deals with Power Hardware In-the-Loop (PHIL) validation of DC-DC power converter for offshore wind energy integration.

DC collector concept

SuperGrid Institute investigates several architectures for an optimal offshore windfarm integration. One proposal configuration is the offshore DC collector concept, where the standard MVAC grid of the windfarm (Figure 1 (a)) is replaced by its MVDC counterpart. As a result, two new DC-DC converters are required to step up the voltage to MVDC levels at the wind turbine generators (WTG) and to HVDC levels at the offshore platform (Figure 1 (b)).

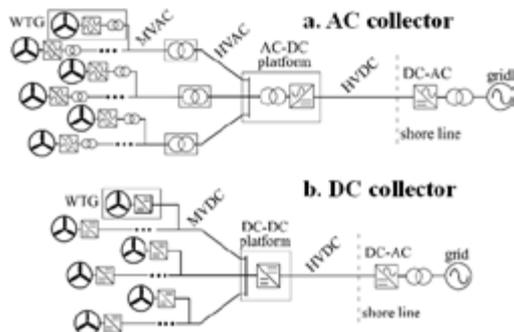


Figure 1: Offshore wind farm with (a) AC collector and (b) DC collector

Following this cost effective architecture, SuperGrid Institute has proposed a new modular DC/DC converter to step up the voltage inside the WTG to MVDC levels of ± 50 kV in order to form the offshore DC collector grid. The basic building block of this converter is the Triple Active Bridge (TAB) cell (see Fig 2 (b)) with a voltage conversion ratio of 4 kV to 8 kV and a nominal power of 800 kW. Using the input parallel output series (IPOS) connection of 12 cells results in the required DC-DC converter that allows to step up the voltage to ± 50 kV and a total power rating of 10 MW.

Before going to the development of the full scale prototype, it has been decided to build a Small Scale Mock-Up (SSMU) for this topology. Thanks to SuperGrid Institute real time platform, power hardware in the loop simulation has been used to:

- Validate the concept of this converter;
- Prototype a control system for the topology and its real time implementation;

- Test the converter behavior with its environment (other converters, cables, wind farms...).

Small Scale Mock-Up (SSMU) components sizing

A small scale mock-up of the power converter was developed in order to validate the topology and its control (see Figure 2). Two constraints were taken into account in order to satisfy the dynamic behavior as close as possible between the Full Scale Mock-Up and the small scale one. To do so, first, the control interface was kept identical. Second, the methodology of scaling used for power circuit was to keep the same electrostatic and magnetic time constants between the SSMU and the FSMU. The electrostatic time constant is used to size the capacitances where the magnetic time T_m , is used to size the leakage inductance of the transformer.

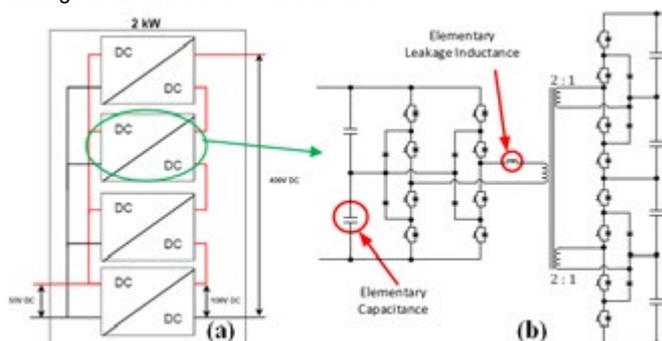


Figure 2: (a) Schematic diagram of the Small Scale Mock-Up "SSMU" (b) Illustration of one cell of the SSMU

Power Hardware in the Loop (PHIL) test bench

Once the SSMU elements are designed and the global topology is built, the next step will be its real time testing. SuperGrid Institute has developed a real time platform to ensure such tests. The later includes all the necessary facilities and expertise to perform these real time tests:

- Several real time targets with more than 30 activated cores allowing to simulate large AC/DC grids including generators, transformers, converters, breakers...;
- FPGA carts programming with Inputs Outputs management;
- Rapid Control Prototyping (RCP) for converter control system as well as for grid protection relies;
- Two power amplifiers adapted to different configurations and cover large bandwidth frequencies.

For the corresponding study “OWF application”, the SSMU is tested with Power Hardware in the Loop (PHIL) environment. This experience consists in combining a simulated environment (AC/DC grids) on a real time target with a real hardware, the SSMU in this case, see Figure 3. To achieve this purpose, analog inputs and outputs are used to exchange signals between the real time target and the device under test (SSMU), as illustrated in Figure 3. In addition, two amplifiers are required to adapt current and voltage levels between the simulation and the SSMU.

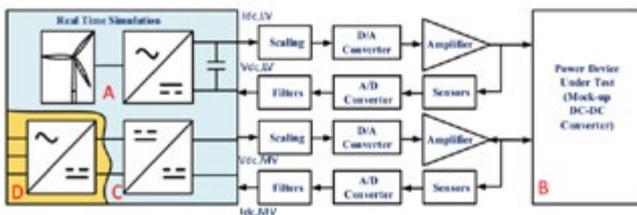


Figure 3: Signals exchange interface between the device under test and the real time simulation

The interface of the PHIL setup is presented in Figure 3 where the exchange signals are illustrated. It has been considered that the input current $I_{dc,LV}$ is imposed by the wind turbines and the voltage bus $V_{dc,MV}$ is controlled at the point of common connection (PCC). Thus, $I_{dc,LV}$ and $V_{dc,MV}$ are the signals sent from the real time system (RTS) to the SSMU. At the same time, $V_{dc,LV}$ and $I_{dc,MV}$ are measured at SSMU terminals in order to send them back to the real time simulation. Therefore, amplifiers must be able to source and sink current and voltage which is possible with the available power amplifiers, see Figure 4.



Figure 4: Experimental PHIL test bench

Power, current or voltage control strategies can be applied for this topology. However, in this work, the voltage regulation is selected because of the architecture specification. The fact that the input current $I_{dc,LV}$ is imposed by the wind turbines forces the LVDC/MVDC converter to regulate the input voltage $V_{dc,LV}$. Likewise, the output voltage $V_{dc,MV}$ is imposed by MVDC/HVDC converter, so balancing the output capacitors needs to be ensured by the SSMU control.

The control system of the SSMU is designed using Matlab/Simulink software which is a suitable software for control design. The time constant of $V_{dc,LV}$ regulation has been set to 1ms while the time constant for the regulation of the balancing MV side capacitors has been set to 3ms. Once the control is built and validated with offline simulation, a complied control C code is generated for its real time implementation in control target.

For PHIL experiments, engineers need to think about all the events that the converter can deal with. It includes all protections to save facilities against overcurrent/overvoltage as well as all the operational

process started from the startup to the shutdown of the test bench. This necessitates to update the initial control system in order to meet these new requirements.

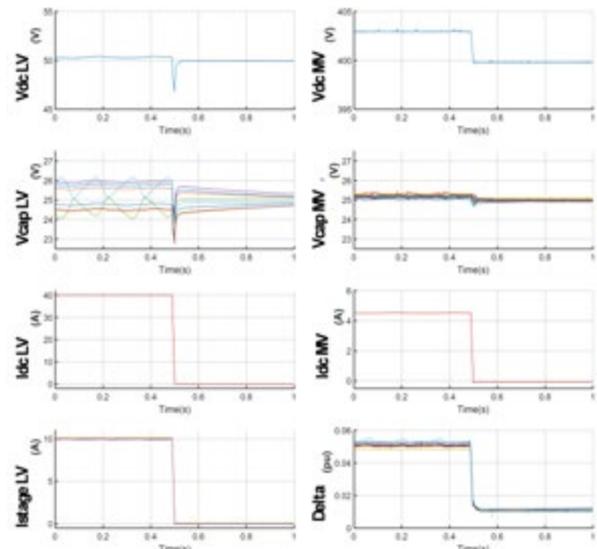


Figure 5: Experimental results during a sudden stop of the OWF connected to the SSMU: total LV DC voltage ($V_{dc,LV}$), total MV DC voltage ($V_{dc,MV}$), the 8 LV capacitors DC voltages ($V_{cap,LV}$), the 16 MV capacitors DC voltages ($V_{cap,MV}$), the total LV DC current ($I_{dc,LV}$), the MV DC current ($I_{dc,MV}$), the DC LV current for each of the 4 stages ($I_{stage,LV}$) and the 8 phase-shifts (Δ)

Once the startup sequence is successfully achieved (performed exactly as for real projects), a scenario that can be tested is a sudden stop of the OWF connected to the SSMU. The experimental results for this test are presented in Figure 5. It can be observed that this event creates a small voltage dip on the low voltage bus which is quickly corrected. After that, both LV side and MV side capacitors voltages are balanced. It is worth noticing that the MVDC collector, $V_{dc,MV}$. The DC currents, $I_{dc,LV}$, $I_{stage,LV}$ and $I_{dc,MV}$, are all very smooth even if there is a dip on the LV bus since the wind turbine is considered as a perfect current source and not a power source for now.

Conclusion

The PHIL approach becomes essential when validating the innovative power converter concepts where the HIL is pushed to their limits. Thanks to the small scale mock up the converter topology and controls can be easily validated within the power system environment. This approach minimizes the converter integration risks and reduces the product development time and cost. As an example, some sequence as the converter energization may be omitted while designing the converter. The fact to think about its integration in an overall system early in the design process when considering PHIL helps to identify these aspects.

The PHIL validation of a DC-DC power converter for offshore wind farm was presented. The selected case study was the full DC wind farm architecture with bidirectional DC-DC power converters. A simulation model of the complete wind farm was developed and implemented in a real-time target. A small scale mock-up of the wind turbine DC-DC converter was developed. The converter mock-up was implemented in a PHIL test bench and the normal operation was demonstrated with a simplified model of the system. Some further investigations are envisaged using the real time simulation model of the complete wind farm in normal and degraded operating conditions.

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Series of Intelligent MOSFET Power Modules

Alpha and Omega Semiconductor announced the release of an intelligent power module, AIM702H50B, specialized for low-power BLDC motor drives system such as fan motors in home appliances and air-conditioners that require highly compact size with reliable and ef-



ficient design allowance. The IPM7 series consists of advanced super junction MOSFETs designed for motor drive and high voltage gate driving ICs with an integrated bootstrap circuit in an ultra-compact surface mountable package. "A BLDC-based inverter has been widely used in fan motors because it is quicker, quieter, and more energy-efficient than the conventional solutions using dc motors or ac induction motors with on/off control. Nowadays, its demand and expansion are becoming a mandatory requirement due to energy saving and regulations. Without a doubt, IPM7 will bring a lot of advantages for fan motor applications by significantly enhancing the cost-effective development of the system, reducing the inverter board size, and obtaining easy and reliable PCB assembly. Quick and precise detection of fault temperature in IPM7 will play a significant role in fan motor drives to secure a reliable design as well as a long time of operation," said Dr. Brian Suh, Vice President of IGBT/IPM product lines at AOS.

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Polymer Aluminum Electrolytics Provides High Ripple Current and Capacitance

The PPC Series of ultra-thin polymer aluminum electrolytic capacitors from Cornell Dubilier represents a totally new capacitor form factor. Designed specifically for applications requiring high ripple current and the thinnest possible profiles, type PPC opens up new product design options. In addition to being just 1 mm thin, the PPC uses versatile packaging technology that makes it possible for capacitors to be formed into custom shapes and sizes to accommodate available space. "A single PPC capacitor offers capacitance and ripple current equivalent to dozens of SMT capacitors or a bulky cylindrical device," said Mario DiPietro, Product Manager at Cornell Dubilier. As an example, the company claims that a single PPC capacitor is equivalent to a parallel bank of 50 or more polymer tantalum capacitors and occupies one fourth the height. Also, circuit reliability is improved by using a single component versus an entire array of SMT capaci-

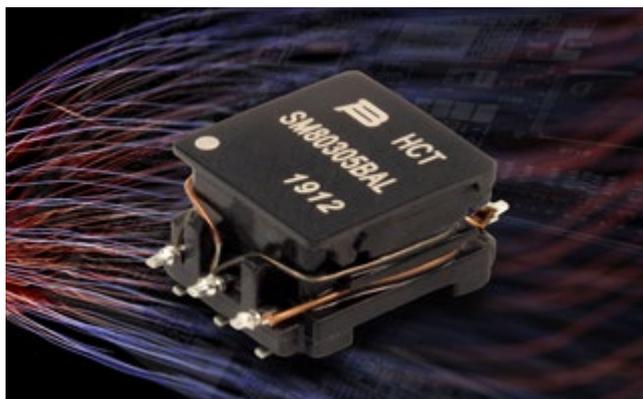


tors. Custom values are available within a capacitance range of 8,000 μF to 20,000 μF , with working voltages ranging from 6.3 to 24 WVDC. The company plans to extend the series to higher operating voltages later in the year. Operating life is 2,000 hours @ 125° C. The PPC is rated for 10 g peak for vibration and withstands shocks up to 100 g's (MIL-STD-202, Method 213, Condition I).

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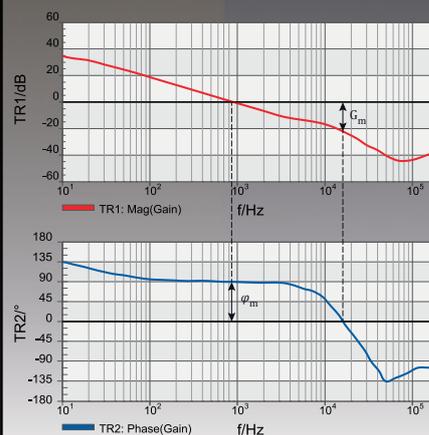
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RECOM announces the launch of its RS12-Z series of 4:1 input DC/DC converters, providing 12W in a SIP-8 package. Leveraging advanced planar technology, RECOM now offers a full 12W output in the industry-standard SIP-8 package from their new RS12-Z series of DC/DC converters up to 75 °C in free air, the highest power avail-



able in this format. With a footprint of just 2cm², the range features 4:1 inputs of 9 – 36V or 18 – 75V with surge ratings to 50V and 100V respectively and regulated single outputs of 3.3, 5, 12, 15 or 24V, all trimmable +/-10% and with remote on/off control. Short circuit and under-voltage protection are included along with 3kVDC/1s isolation and EN 62368-1 certification. EN 55032 class A or class B EMC levels are met with a simple, low cost external filter. The series features a metal casing providing EMI shielding as well as enhanced thermal performance with case tabs providing mechanical stability and additional heat sinking to the customer's PCB. "We have incorporated radical design changes in our new RS12-Z series, with a planar transformer construction and metal casing to push the limits of power density achievable in the SIP-8 package" commented Steve Roberts, Innovation Manager at RECOM. "The series is ideal for nominal 12, 24 or 48V systems where real estate is at a premium and full power is needed over a wide temperature range."

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SiC MOSFET Power Module for E-mobility

CISSOID announces a 3-Phase SiC MOSFET Intelligent Power Module (IPM) platform for E-mobility. This IPM technology offers an all-in-one solution including a 3-Phase water-cooled SiC MOSFET module with built-in gate drivers. Co-optimizing the electrical, mechanical and thermal design of the power module and its proximity control, this scalable platform will improve time-to-market for Electric



Car OEMs and electric motor manufacturers willing to rapidly adopt SiC-based inverters for more efficient and compact motor drives. With this SiC-based IPM solution, CISSOID maintains its focus on addressing challenges for automotive and industrial markets. The first product out of this scalable platform, a 3-Phase 1200V/450A SiC MOSFET IPM, features low conduction losses, with 3.25mOhms On resistance, and low switching losses, with respectively 8.3mJ turn-on and 11.2mJ turn-off energies at 600V/300A. It reduces losses by at least a factor 3 with respect to state-of-the-art IGBT power modules. The module is water-cooled through a lightweight AISiC pin-fin baseplate for a junction-to-fluid thermal resistance of 0.15°C/W. The power module is rated for junction temperature up to 175°C. The IPM withstands isolation voltages up to 3600V (50Hz, 1min). The built-in gate driver includes three on-board isolated power supplies (one per phase) delivering each up to 5W allowing to easily drive the power module up to 25KHz and at ambient temperatures up to 125°C.

www.cissoid.com

Stackable DC/DC Buck Converter

Texas Instruments introduced a 40-A SWIFT™ DC/DC buck converter, offering stackability of up to four integrated circuits (ICs). The TPS546D24A PMBus buck converter can deliver up to 160 A of output cur-



rent at an 85°C ambient temperature – four times more current than competing power ICs. The TPS546D24A has the highest efficiency of any 40-A DC/DC converter, allowing engineers to reduce power loss by 1.5 W in high-performance data center and enterprise computing, medical, wireless infrastructure, and wired networking applications. Solution size and thermal performance are two key considerations for engineers designing power supplies for modern field-programmable gate arrays (FPGAs). With its unique stackability, the TPS546D24A buck converter addresses both. It comes with a PMBus interface that offers a selectable internal compensation network, enabling engineers to eliminate as many as six external compensation components from the board and shrink the overall power-supply solution size by more than 10% (or 130 mm²) for higher-current FPGA/application-specific ICs (ASICs) when compared to discrete multiphase controllers.

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A background image showing a factory floor with rows of battery packs. A person is visible in the center, looking at the equipment. The image has a red tint.

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Fully Integrated Wireless-Charging IC

In the age of 5G communication with ever-increasing demand for more power and higher efficiency, STMicroelectronics' STWLC68 product family provides the best solution for wireless-charging applications with industry-leading efficiency, highest power transfer, and safety.

ST's wireless-charging products operate as both a high-power receiver and a transmitter enabling rapid power transfer and power sharing with FOD (Foreign Object Detection) and other important ST-proprietary safety IPs. ST's proprietary high-voltage technology, paired with

excellent mixed signal design and highest quality assurance, enables our customers to deliver cutting-edge wireless-charging products. The STWLC68 family of highly integrated devices needs a very low external BoM (Bill of Materials), ideal for integration in a wide range of applications from small wearables and appliances to larger ones like smartphones and tablets. Being WPC Qi 1.2.4 compliant, the STWLC68 is fully compatible with all Qi certified devices in the market. With its fully integrated low-impedance, high-voltage synchronous rectifier and low drop-out linear regulator, the STWLC68 achieves high efficiency and low power dissipation, critical for applications that are highly sensitive to unnecessary heat buildup. An I2C interface allows firmware and platform parameters to be customized in the device and the configuration can be programmed into the embedded OTP. Additional firmware patching improves the IC's application flexibility.



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Ridley Engineering will release a product to enhance its product line. The RidleyBox® combines the following—a lifetime license for

RidleyWorks® Design Software, a 4-channel Frequency Response Analyzer, a 4-channel 200 MHz Oscilloscope, a Ridley Universal Injector, and an Intel® computer—all in one product. "This began as a concept to condense our labs for travel and teaching. The resulting product is one from which the entire power electronics community can benefit," commented Dr. Ridley.



www.ridleyengineering.com

Module Meets the Requirements of Industrial Voltage Network

The power modules with fixed 3.3 or 5 V output voltages are now also available with an input voltage of 36 V, following on from versions with maximum input voltages of 28 and 42 V. The components in a SIP-3 package represent cost-effective solutions to meet the requirements for the transient capability of a 24 V industrial voltage network. The modules operate from 6 to 36 V VIN and generate a fixed output voltage of 3.3 or 5 V at a current of up to 1 A. The FDSM series of MagI²C power modules are fully integrated DC/DC voltage converters with fixed output voltage. The modules comprise the power



stage, controller, inductors, and effective operational input and output capacitors. They also come with thermal overload and short circuit protection. No external components are required for operation. The workload of circuit design is thus reduced to a minimum. This allows new applications to be brought to market quickly with very low development costs. The standard THT housing for easy mounting is pin-compatible with the L78x linear controllers.

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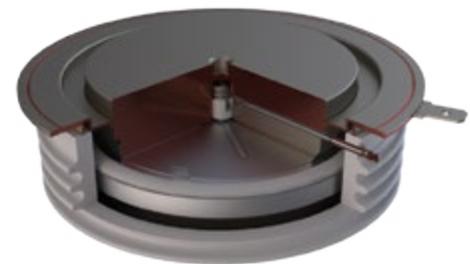


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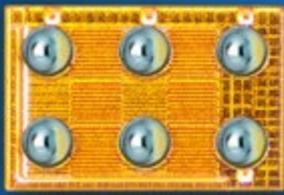
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