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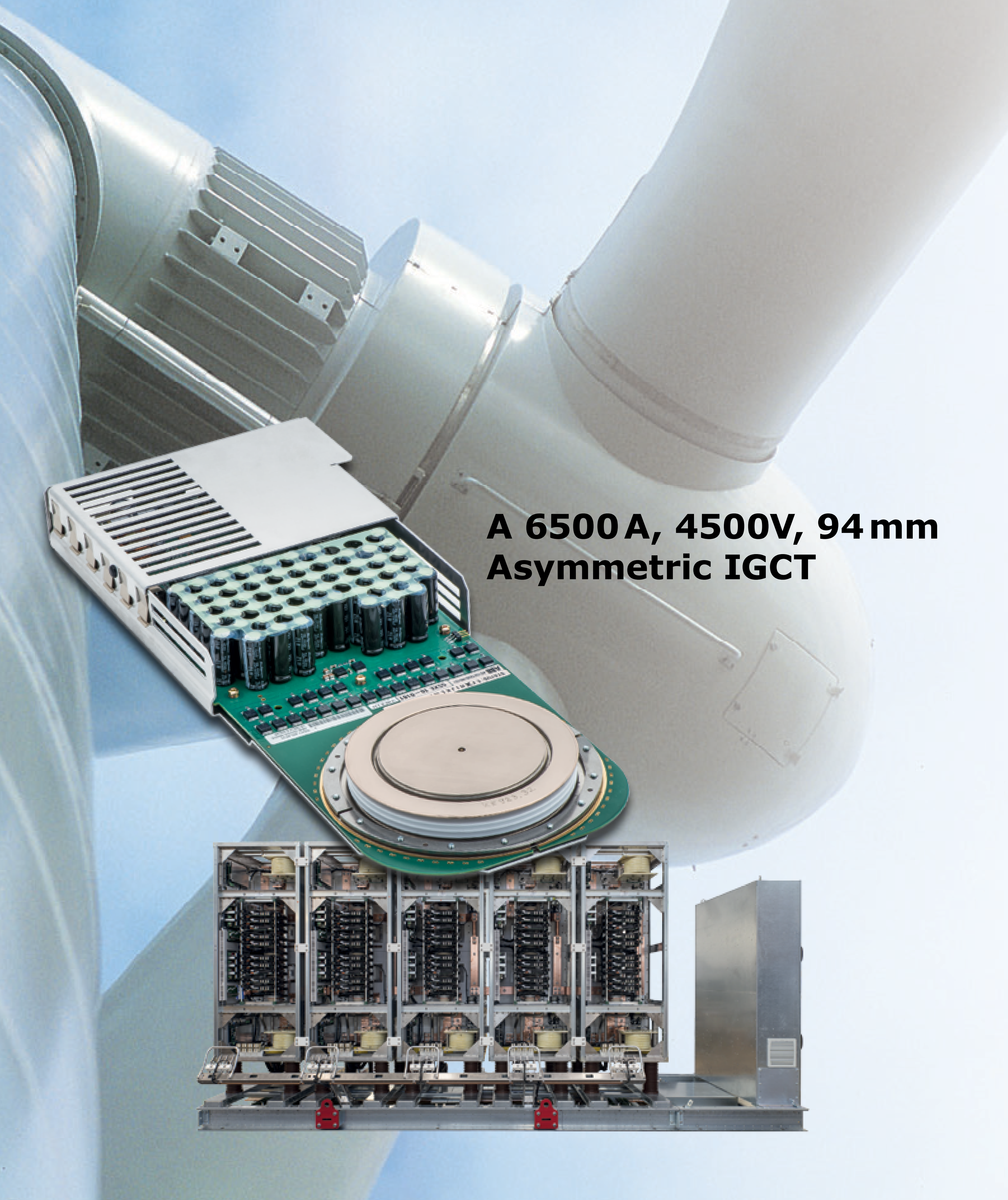
Bodo´s Power Systems®

Electronics in Motion and Conversion

June 2020

A 6500 A, 4500V, 94 mm Asymmetric IGCT

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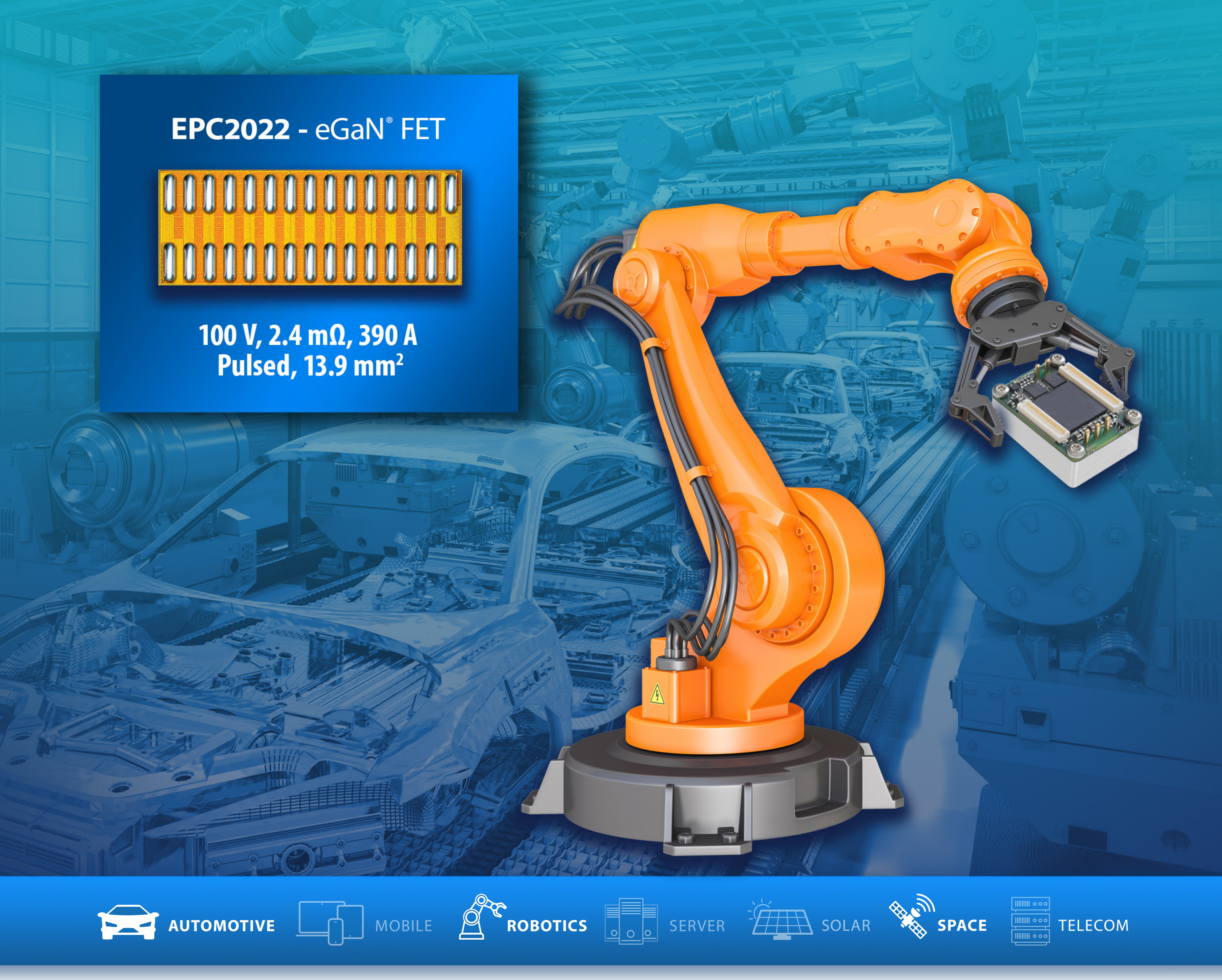
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A Media
Katzbek 17a
D-24235 Laboe, Germany
Phone: +49 4343 42 17 90
Fax: +49 4343 42 17 89
info@bodospower.com
www.bodospower.com
Publishing Editor
Bodo Arlt, Dipl.-Ing.
editor@bodospower.com
Junior Editor
Holger Moscheik
Phone + 49 4343 428 5017
holger@bodospower.com
Editor China
Min Xu
Phone: +86 156 18860853
xumin@i2imedia.net
UK Support
June Hulme
Phone: +44 1270 872315
junehulme@geminimarketing.co.uk
US Support
Cody Miller
Phone +1 208 429 6533
cody@eetech.com
Creative Direction & Production
Bianka Gehlert
b.gehlert@t-online.de
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Let's Give it a Try

Not a day goes by without the announcement of another, now digital, event. Webinars experience a boom like we have not seen in a while. Press conferences are transmitted as live streams. And of course, trade fairs and congresses are looking for new ways to reach their visitors. I wish the teams all the best for the difficult task of building all this from scratch. I am pretty sure I am not the only one who has never yet visited a virtual trade fair, and I also admit that I cannot imagine exactly what to expect. But it seems that this could, if not must, be the way ahead, at least in the near future. For sure, I will try it out shortly. Recently I read a very interesting article saying events in the future may become hybrid. The advantages of a digital fair combined with the benefit of meeting in person. Presentations and information transport electronically and the equally important networking face-to-face. I like the idea - this might be one of the next steps to come.

For the PCIM Digital Days in early July we are offering a special feature. We will have a section within our July issue where we would like to give both the exhibitors and contributors of this event, and also all other interested companies who are currently working on digital alternatives, the opportunity to promote their activities through advertorials. Be sure, the biggest part of the PCIM audience can also be found in our readership, so this is a good way to spread your message. Contact us if you're interested in being part of this, there are still a few slots left. Also, as of today, it is planned by the PCIM organizers to give Bodo a platform to host his traditional podiums discussion. This year's focus will be "SiC & GaN – The Game Changers". We are in contact with the presenters to give you the best possible experience. As the situation is so fluid here, please watch out for updates in our newsletters and on our social media channels.

We are one of the last remaining publishers to produce a printed product and we will continue to do so. We sometimes receive news that there are delays in the delivery of our magazine. This is beyond our control, I am sure everyone will understand that in the exceptional circumstances we are currently experiencing, irregularities are inevitable. We publish every month on the first of each month on time. The digital issue, identical, is sometimes available even a bit earlier for technical reasons.

Bodo's Power Systems is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving North America efficiently. If you are using any kind of tablet or smart phone, you will find our content optimized for mobile devices on the updated website www.bodospower.com. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com

My Green Power Tip for the Month:
We all know about the tiny extra lines under emails that suggests we think about whether it is necessary to print out the email. I came over a similar phrase which also makes sense to me: "Please think twice whom you put on cc. Email traffic is consuming more energy than you might expect!"

Events

SEMICON China 2020
Shanghai, China June 27-29
www.semiconchina.org

Electronica China 2020
Shanghai, China July 3-5
www.electronica-china.com

PCIM Europe 2020
Online July 7-8
https://pcim.mesago.com

SEMICON West 2020
Online July 20
www.semiconwest.org

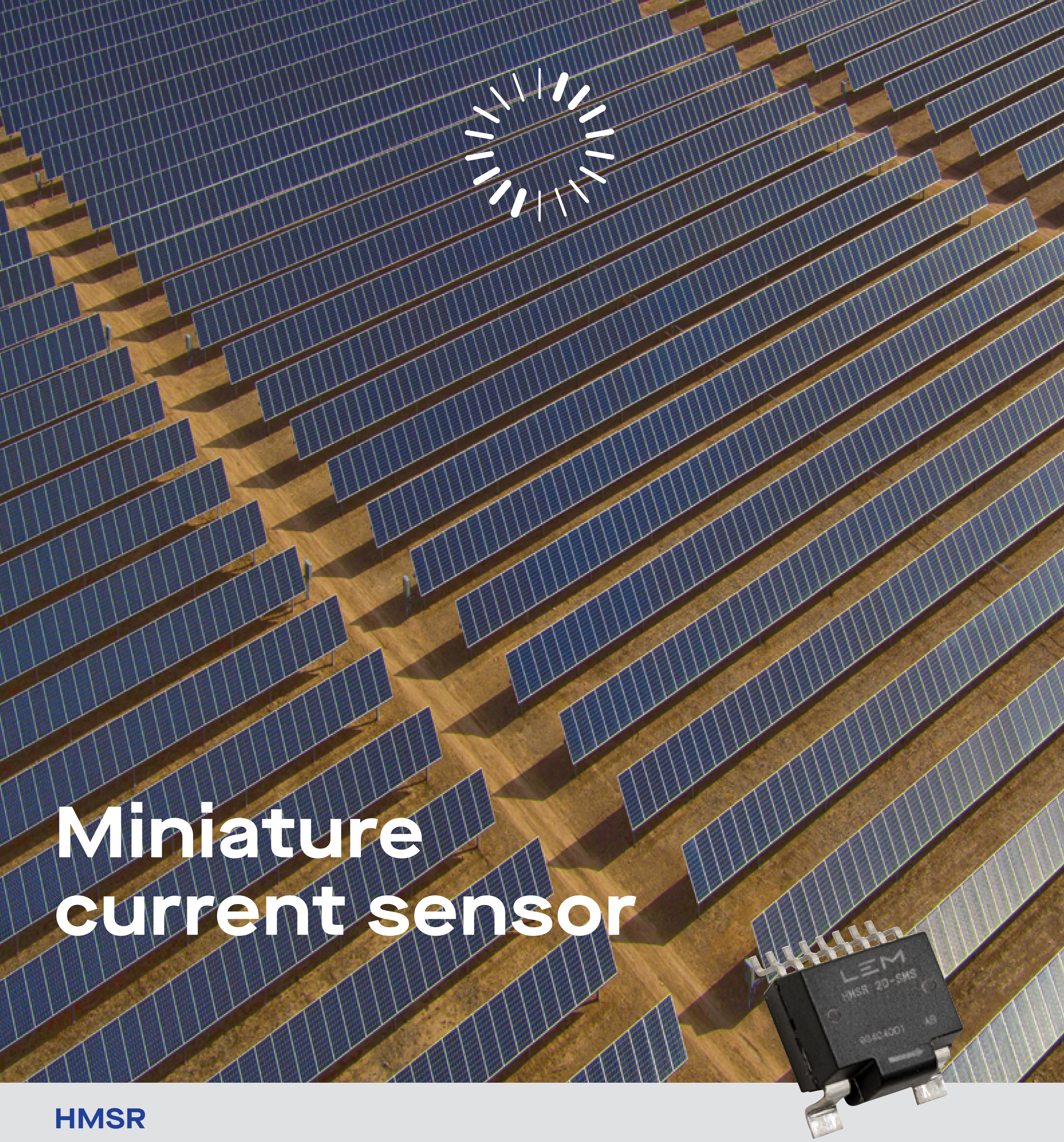
CWIEME Shanghai 2020
Shanghai, China July 29-31
http://cn.coilwindingexpo.com

SMTconnect 2020
Online July 28-30
https://smt.mesago.com/

Thermal Management 2020
Online August 6-7
www.thermalconference.com

EXPO ELECTRONICA 2020
Moscow, Russia August 11-13
www.expoelectronica.ru

World Battery Expo 2020
Guangzhou, China August 16-18
www.battery-expo.com



Miniature current sensor

HMSR

Packaged as SO16 surface-mount device with a height of just 6 mm, HMSR current sensor is adapted to the power electronics world for a perfect integration thanks to its SMD automatic assembly and space saving. As a reinforced insulation level, cost effective and miniature solution for current sensing, HMSR provides solutions to photovoltaic, white goods, windows shutters, air-conditioning, high switching frequencies drives applications.

- **6, 8, 10, 15, 20 or 30 A_{RMS} nominal current**
- **0.5% typical accuracy into the operating temperature range**
- **High performance gain and offset thermal drifts**
- **2 µs response time**
- **Operating temperature range: -40°C to +125°C**
- **Unique primary conductor included withstanding overload current bursts up to 20 kA**
- **Double overcurrent detection outputs**

www.lem.com

LEM

Life Energy Motion

"Sustain our Planet" Design Challenge

Together with the element14 community, Infineon Technologies has initiated a design challenge for the community members. "A few weeks ago, we have reached the landmark of 100 million XMC microcontrollers sold," said Ralf Koedel, Marketing Director Microcontrollers at Infineon. "In this challenge run in partnership with the element14 community, we are asking developers for thought-provoking new designs based on various Infineon devices including XMC that could help sustain our planet. Examples could include buoys to monitor microplastics in the ocean or trash collection robots." In the first step, Infineon and element14 ask community members to come up with design blueprints based on a defined list of Infineon products supplemented with further sensors and actuators as needed. A jury of Infineon and element14 experts will then select the 20 most promising ideas. These sponsored challengers will receive a kit of products to build their designs. Participants are asked to document their project on the element14 community in order to spread their ideas throughout the community and inspire others. A minimum number of ten blog entries is required to qualify for the final selection of the winning designs. Media-rich posts with photos, videos and code samples will score extra points in the evaluation. From all projects finished and documented by August 10, the jury will choose the winning designs.

www.infineon.com

Team from Finland Receives Innovation Award 2020

This year the jury has decided to give the SEMIKRON Innovation Award to a research team from Aalto University in Espoo, Finland comprising Prof. Dr. Marko Hinkkanen, Dr. Seppo Saarakkala, Maksim Sokolov and Reza Hosseinzadeh for their joint work on an ´Bearingless Linear Motor Drive for Future Transportation Systems'. The research team from Aalto University has developed and experimentally tested a novel magnetically levitated linear propulsion system. The system is based on a four-sided arrangement of eight individually controlled three-phase flux-switching permanent magnet (FSPM) linear motors. After developing a real-time control algorithm for this system, a robust levitation in six degrees-of-freedom could be achieved,

while using the same linear motors for producing the thrust force for the propulsion. The SEMIKRON Young Engineer Award 2020 goes to Johannes Büdel from Technische Hochschule Aschaffenburg, Germany for his work on a ´Dual Two-Level Inverter for Safe, Reliable and Highly Efficient Operation of Machines with Superconductive Stator Windings´ supervised by Prof. Dr. Johannes Teigelkötter. With zero electrical DC resistance and the high current densities, superconductors are suitable for electrical machine applications. In particular, superconducting motors are attractive for mobile traction drives for sea transport and aviation where high power levels of several MW per motor are required e.g. for large aircraft propulsion. Johannes Büdel has contributed to the development of a dual two-level inverter for safe, reliable and highly efficient operation of machines with superconductive stator windings.

www.semikron.com

Symposia on VLSI Technology & Circuits Goes Virtual

For the first time in its 40-year history, the 2020 Symposia on VLSI Technology & Circuits will be held as a virtual conference due to concerns over the global coronavirus (COVID-19) pandemic. Despite the change in format, the Symposia program promises to deliver a unique perspective on the integration of advanced technology developments, innovative circuit design, and the applications they enable – such as machine learning, IoT, artificial intelligence, wearable/implantable biomedical applications, big data, cloud / edge computing, virtual reality (VR) / augmented reality (AR), robotics, and autonomous vehicles – the emerging technology ecosystem needed to realize the conference theme of "The Next 40 Years of VLSI for Ubiquitous Intelligence." The now-virtual Symposia will be held from June 14 – 19, 2020 with a comprehensive program of technical presentations, panel discussions, focus sessions, short courses, and the popular "Friday Forum" a focused discussion on "Technologies & Circuits for Edge Intelligence." The Symposia is the microelectronics industry's premiere international conference, integrating technology, circuits, and systems with a range and scope unlike any other conference, charting the roadmap for the connected devices and systems that will drive the next stage of human interaction.

2020 VLSI
TECHNOLOGY SYMPOSIUM

www.vlsisymposium.org

Increased Communication Between Distributors and Manufacturers

With RECOM, the FBDi association has gained a manufacturer of power supply converters as a supporting member. The RECOM group with headquarters in Austria has more than 45 years of experience in the development and production of state-of-the-art current transformer technology in the power range from 0.25W to 30KW. A supporting membership is reserved for manufacturers - they do not provide statistical figures, but benefit from the results, from which they can see, among other things, how individual markets are developing strongly or less well received in their sector via distribution. By participating in regular internal meetings of the Competence Teams they can gain a valuable knowledge advantage. At the same time, the communication and exchange of information opens up additional perspectives for both sides and thus creates new aspects and approaches for day-to-day business.

Quote Uwe Frischknecht, Managing Director and responsible for sales in EMEA: "For several decades, RECOM has deliberately built up and expanded the distribution channel and can now proudly rely on a unique network of leading broadline distributors and high service providers. Thus, the distribution channel has become RECOM's most important sales market. With the FBDi supporting membership we hope to achieve an even closer integration with the distribution, so that RECOM can continue to meet its best-in-class distribution support in the future."

www.recom-power.com

Changes to Global CWIEME Event Series 2020

Hyve, the organiser of the global CWIEME event series, announced changes to the scheduled CWIEME events in 2020. The decision by the German government to postpone large events until 31st August 2020, means that CWIEME Berlin 2020, scheduled to take place from 30th June – 2nd July, has now been postponed. The organisers are working closely with the venue and their partners to find a solution for the Berlin event and will contact everyone involved once new dates for CWIEME Berlin have been agreed. Hyve has also made the difficult decision to cancel CWIEME Americas for this year due to the Covid-19 pandemic and the impact of the continuing travel restrictions. CWIEME Shanghai will continue to take place as planned from 29th – 31st July 2020. "CWIEME is an international event and these changes allow our global community to amend their plans," said Nick Davison, new CWIEME Portfolio Director. "We very much regret that we have to cancel CWIEME Americas for this year, but due to the current coronavirus situation and ongoing travel restrictions we had to make this decision to ensure the safety and health of our exhibitors, participants, and partners. This is an unprecedented and fast-developing situation and we are monitoring global developments closely."

www.coilwindingexpo.com

ISPSD Conference New Dates

In the light of the COVID-19 pandemic, the ISPSD 2020 organizers decided to postpone the 32nd IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD) to September 3–6, 2020. The ISPSD 2020 will take place as originally planned in the Hofburg Palace, Vienna, Austria. The safety of all participants is the top priority. The early registration deadline is extended to July 24, 2020. At this moment, the organizers are investigating the possibility of earlier online publication of the conference proceedings in IEEE Xplore.

www.ispsd2020.com

Establishing Testing Lab in Malaysia

Keysight Technologies has opened a Regulatory Test Laboratory in Penang, Malaysia to deliver accredited electromagnetic compatibility (EMC) testing services for manufacturers of electronic devices and mission-critical industries across wireless communications, IIoT, automotive, healthcare and medical applications. The Penang facility is the next world-class compliance and testing facility established by Keysight to offer expertise, knowledge, efficiency, capacity and exceptional customer service including calibration and testing services. Keysight currently has similar testing facilities in California in the United States and in Boeblingen, Germany.

"As the world becomes more electronically connected, testing becomes more complex. The dramatic number of potential emitters of electromagnetic interference (EMI) in autonomous cars, electric vehicles, 5G and IoT devices, as well as medical equipment require new tests to meet evolving standards," stated Niels Faché, vice president of Service Portfolio, Global Services at Keysight. "Keysight's compliance and testing laboratories around the world and now in Asia, offer expertise and emerging technologies that can help our customers validate designs and accelerate time to production.

www.keysight.com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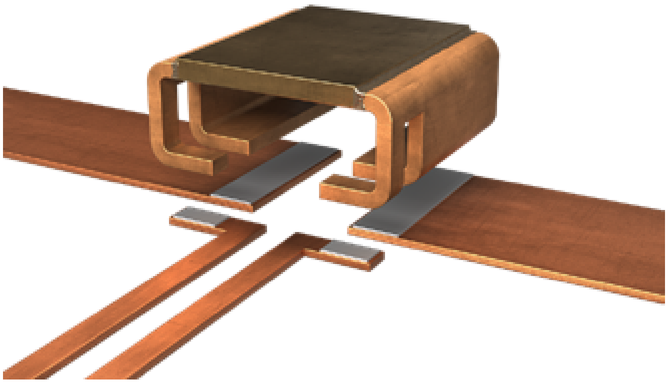
Distribution Partner in the Area of Passive Components

Isabellenhütte has entered into a distribution partnership with Fujitsu Electronics Europe. Fujitsu's role is to distribute standard products world-wide, acquiring and advising potential customers with its own operations. Anton Roth, Global Sales Director for Components at Isabellenhütte, explains: "With this distribution partnership we can expand the global coverage of our customers. By doing so we can use individual on-location consultation to include customers whose development sites are different from their production sites. This way we can ensure that the decision pathways are kept short."



If, for example a customer's development is in Europe, but their production takes place in Asia, the distribution partner Fujitsu Electronics Europe will provide technical consultation to the customer in Europe during the development phase and then also ensure on-location consultation through its affiliates in Asia. Anton Roth: "We have a seamless chain and can follow a project on a global scale."

After starting with an agreement with Fujitsu Electronics Europe, more contracts will be signed shortly with the further Fujitsu locations in America, Korea, Shanghai and the head company in Japan. With this step Isabellenhütte advances its global network and ensures a streamlined organization and simplified handling of international orders. The customers benefit from closer consultation throughout the value-added chain.

www.isabellenhuette.de

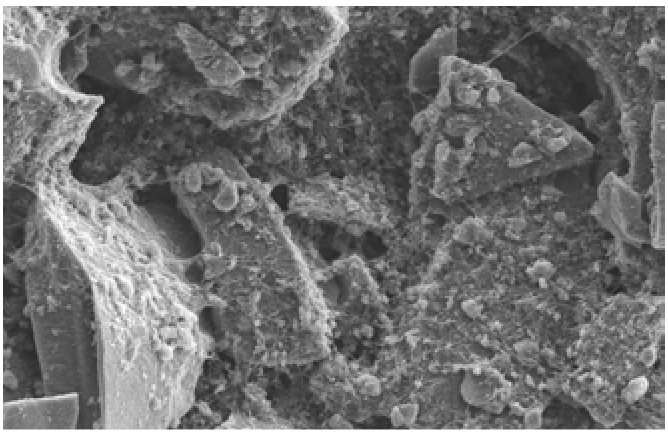
Semiconductor Industry's First Green Bond

Analog Devices announced the successful closing of the first green bond offering in the semiconductor industry. The company's green bond issuance consisted of $400 million aggregate principal amount of 2.950% senior unsecured notes due April 2025. "At ADI, we are committed to engineering a sustainable future and this is an important next step in driving sustainable growth for all ADI stakeholders. We are proud to lead the semiconductor industry with our green bond issuance," said Vincent Roche, President and CEO of Analog Devices. ADI intends to use the net proceeds from the offering to finance or refinance eligible projects that offer sustainability benefits, furthering the company's commitment to environmental sustainability. The eligible categories for the use of the net proceeds – renewable energy, energy efficiency, green buildings, sustainable water and wastewater management, pollution prevention and control, clean transportation, and eco-efficient and/or circular economy adapted products, production technologies and processes – are designed to protect and regenerate the environment and are in alignment with the United Nations Sustainable Development Goals. In connection with the green bond, ADI worked with Sustainalytics, a leading global provider of environmental, social and corporate governance research and ratings. Sustainalytics reviewed ADI's green bond framework and opined that it is credible and aligns with the four core components of the Green Bond Principles 2018.

www.analog.com

Hybrid Material Improves the Performance of Silicon in Li-ion Batteries

To minimise the reducing effect of high charging rates on the capacity of silicon anodes, researchers from the University of Eastern Finland have developed a hybrid material of mesoporous silicon (PSi) microparticles and carbon nanotubes (CNTs). According to the researchers, the hybrid material needs to be realised through chemical conjugation of PSi and CNTs with the right polarity so as to not hinder the diffusion of lithium ions into silicon. With the right type of conjugation, also the electrical conductivity and mechanical durability of the material was improved. Further, the PSi microparticles used in the hybrid material were produced from barley husk ash to minimise the carbon footprint of the anode material and to support its sustainability. Silicon was produced through a simple magnesiothermic reduction process applied to the phytoliths that are amorphous porous silica structures found in abundance in husk ash. Next, the researchers are aiming to produce a full silicon anode with a solid electrolyte to address the challenges related to the safety of LIBs and to the unstable solid electrolyte interface (SEI).



www.uef.fi/en

High Power next Core (HPnC)

with Fuji Electric's X series - 7G IGBT

MAIN FEATURES

- **Latest chip technology**
  - Fuji Electric's X series IGBT and FWD with low losses
- **High reliability**
  - CTI>600 for higher anti-tracking
  - High thermal cycling capability with ultra sonic welded terminals and MgSiC base plate
  - Improvement of delta T_j power cycle capability by using 7G Package Technology
- **RoHS compliance**
  - Ultrasonic welded terminals
  - RoHs compliant solder material
- **Over temperature protection**
  - Thermal sensor installed
- **Easy paralleling**
  - HPnC module has a minimized current imbalance
  - Easy scalability

Energy Density and Multiple Packaging Options

Cornell Dubilier Electronics, Inc. announces the availability of its Q Series film capacitors for medical defibrillator applications. Designed specifically for today's quick response and professional use defibrillators, the Q Series meets the reliability demands of Class III medical devices. Used extensively in automated external defibrillators (AEDs), the series offers designers the highest in-class energy density and broadest range of packaging options. Q Series capacitors are designed for use in monophasic and bi-phasic defibrillators with energy densities as high as 2 J/cc. Some designs can deliver in excess of 500 joules when fully charged. Voltage ratings range from 800 Vdc to 6,000 Vdc with capacitance values covering the range from 32 to 500 μF. Standard packages include oil-filled metal cases or epoxy-filled plastic cases, both available in either round or oval configurations.

A multitude of terminations are available ranging from quick-connect blades to insulated wire leads. The company also has the capability of integrating capacitor windings into a custom molded package to achieve the smallest possible profile and highest energy density for the end-device. Over the past 20 years CDE's engineers have advanced the metallized film capacitor technology, processing and testing to help its customers achieve the smallest and most reliable designs. With the capability of withstanding 40,000 charge/discharge cycles (depending on part and application), Q Series capacitors are designed for long-term reliable service where it matters the most.

www.cde.com

Efficiency in all conditions

life.augmented

Highly Integrated and Flexible Synchronous DC/DC Converters for Smart Industrial Applications

ST's new L6983 38 V/3 A synchronous step-down monolithic switching converters maintain high efficiency at all loads with a maximum value of 95%. With a wide input-voltage range from 3.5 to 38 V, L6983 converters are an efficient and flexible solution for 12 and 24 V industrial bus-powered systems, battery-powered equipment, decentralized intelligent nodes such as smart-building controllers and always-on devices including smart sensors.

KEY FEATURES:

- Extremely low quiescent current of just 17µA
- Low current consumption (L6983C) and low-noise (L6983N) variants are available
- Power good output can be used for power-up/ power-down sequencing
- Internal dithering circuit for noise reduction
- Spread Spectrum for improved EMC
- Available in in 3 x 3 mm QFN16 package

Several easy-to-use evaluation boards are available to help reduce development time and costs:

- The [STEVAL-ISA208V1 evaluation board] is based on the **L6983C low consumption version** designed to maximize efficiency at light loads with controlled output voltage ripple, which is ideal for battery-powered applications.
- The [STEVAL-ISA209V1 evaluation board] is based on the **L6983N low noise version** which lets you set the switching frequency and minimize the output voltage ripple overload current range, meeting specifications for noise-sensitive applications.

For more information, visit us at: http://www.st.com/L6983

SWaP Benefits Help Reduce Power Consumption in HighRel Microprocessors

During its 2020 online press conference, Thomas Guillemain, Marketing and Business Development Manager, Data Processing Solutions, of Grenoble-based Teledyne e2v Semiconductors presented different ways to reduce power consumption for systems embedding computer-intensive HiRel microprocessors.

By Roland R. Ackermann, Correspondent Editor Bodo´s Power Systems

Despite the rising power efficiency of new processors, the accelerating demand for computational power often outstrips the ability to cool the systems down and/or to provide them the right amount of current. Furthermore, mechanical/thermal design usually happens late in the development cycle. Consequently, it is likely to run up against thermal limits late in the design process. Designers naturally want to optimize their systems and find acceptable tradeoffs.
Teledyne e2v High Reliability Microprocessors have been the workhorses across a broad range of defence, aerospace and other high-reliability markets for several decades now. Today, contemporary processor advancement is driven by the demands of other future mass markets such as the extreme number crunching needs of autonomous driving. Thus, the changing economic focus of suppliers, like NXP, has deep consequences for high-reliability supply chains. Not least, that products are engineered with less stringent requirements for many applications.
Teledyne e2v, building on its long-term strategic relationship with NXP, is uniquely positioned as a trusted supplier of customized processor options. Customization is possible based on either the power architecture (e.g. T series processors such as the T1042) or ARM architecture (e.g. Layerscape LS1046).

SWaP minimization – three degrees of optimization
Meanwhile SWaP (Size, Weight and Power) minimization persists and informs daily decision making of high-reliability system designers working with harsh environments, even space. After all, processors are a strategic component choice representing a large contributor to the total power budget (the P of SWaP). Equally, thermal dissipation drives heatsinking, impacting upon system size and weight goals (the S & W of SWaP). In many cases, selecting one or even a combination of three degrees of customization can deliver significant value to the design.

Approach 1: Power consumption optimization
Power consumption optimization for a specific customer use case consists of characterizing the processors versus the customer application, prior to selecting those with the lowest total power consumption. It starts with evaluating a population of target components, taking test data and examining the power consumption spread. Ultimately the purpose is to select out only those devices exhibiting the best power consumption characteristics for a given application use case.
Power screening evidence suggests that for some applications when the use case is clearly defined, it is possible to operate a processor well within its operating envelope. However, this requires knowing with greater precision, how the device behaves within the target use case. There is no quick answer to this, but power screening provides the detailed analysis necessary to reach a definitive understanding. In one project, Teledyne e2v demonstrated its ability to source processors with power consumption 46% lower than the worst-case standard product scenario as illustrated in Figure 1, and this by combining characterization of the customer's application and power screening. Here, a device initially believed unsuitable for the task due to assumed excess power consumption, could now be sourced and designed-in with confidence.

Approach 2: Custom packaging
Alternative custom package selection for thermal resistance optimization, which in most cases brings circuit/die protection as well: modifying or redesigning the existing standard product package to lower its thermal resistance from junction to board, or junction to package top:

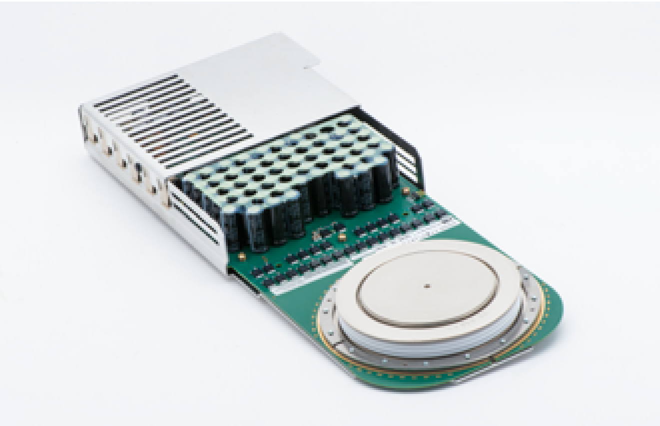
- Can be used to reduce the junction temperature, thus lowering power consumption (assuming the same heatsink remains in place). Alternatively, reduces the cooling system (size/weight) since the package thermal resistance (Rth) is lower, that of the heatsink can be larger.
- An alternative package can enhance vibration protection for the component and/or simplify and improve the thermal interface between the cooling system and the processor.
- To deploy a lid or not to further impact thermal performance.

A lid is the cover that is found on most processors which acts as a heat spreader and protection for the component's die. However, depending on the application, some designers might want a lid to help integrate a heatsink more easily. Others prefer a lidless design because they can't accept the extra thermal resistance of the lid. Also, note that a lid dramatically reduces the junction to board thermal resistance, a clear benefit if it is desired to conduct more heat through the printed circuit board (PCB).
Some components are delivered with lids (e.g. LS1046), others come without (e.g. T1040). Usually the designer doesn't have a choice because with 'commercial off the shelf' (COTS) components, both versions are rarely available. That's where Teledyne e2v has the flexibility to help, by proposing to add or remove a lid.

Approach 3: Extended (i.e. >125°C) junction temperature
Raised maximum junction temperature (TJ) specification can extend operation. This requires additional qualification work at elevated temperatures combined with careful consideration of operating life profile. The key point is to quantify this, since elevated temperature operation affects device failures in time (FIT rates).
This optimization step considers the viability of operating silicon beyond conventional thermal limits of commercial, standard products. Certainly, silicon is not physically limited to operate only up to 125°C, several elevated temperature applications exist and are already served. The benefit of higher junction temperature operation is the extra thermal headroom on offer. But elevated temperatures have an implied penalty namely significantly raised power dissipation. Where a higher junction temperature can pay off is in applications with an operating profile requiring short bursts of increased dynamic power, yet it is critical these bursts can be handled within the thermal capacity of the design.

www.teledyne.com

A 6500 A, 4500V, 94mm Asymmetric IGCT



The IGCT is a semiconductor switch with low on-state loss, making it ideal for medium to the highest power inverters; an application that must strive to maximize power output and energy efficiency to deliver a competitive product. Although application-specific aspects including topology, switching frequency and output filters are principal contributors to inverter efficiency, the semiconductors themselves can make a significant contribution by offering low on-state and switching losses. In this respect, the IGCT is undoubtably the highest-performance silicon device architecture.

By Tobias Wikström, Didier Cottet and Christian Winter, ABB Power Grids Switzerland Ltd.

The development and performance of a 6500 A, 4500 V Integrated Gate Commutated Thyristor (IGCT) is described in this article. Different segment layouts were investigated with the goal of maximizing the controllable current, and these tested layouts are described below. The mechanical design is based on an existing platform for outer-ring-gate, 94 mm-diameter silicon wafers. The best layout variant reliably switches currents exceeding 8000 A at 2800 V in a single pulse, with stable frequency operation up to a virtual junction temperature of approximately 230 °C.

Device architecture

The project aimed to use the lower thermal impedance and increased active area of a 94 mm diameter wafer compared to the 91 mm wafer that has been in production for more than twenty years. The 94 mm platform was first developed for an RC-IGCT designed for STATCOM applications [1] in 2014 - 2016.

The 94 mm and 91 mm housing platforms are identical on the outside; they only differ internally. The 91 mm wafer has its gate connection placed at around half of the device radius. Connecting to the gate on the wafer from the radial outside inevitably means leading it through the cathode pole-piece that constitutes the principal electrode and thermal contact on the cathode side. The gate vias introduce obstructions in both the electrical and thermal circuits of the 91 mm device. In contrast, the gate contact of the 94 mm wafer is placed outside the device's active area, eliminating obstructions in the cathode contact and decreasing the thermal resistance. The space for the device's active area is also improved by more than the area increase of 6-7 % that results from changing the laser cut diameter from 91 to 94 mm. A more effective design, together with improved precision in production that reduces the tolerance required, allows the 94 mm wafer to enlarge the active GCT area from 42 cm² to 51.4 cm², an increase of 22 %.

There are two main advantages with an outer gate contact arrangement. Firstly, the outside of the wafer is as close to the gate unit as possible, which decreases the inductive impedance of the gate leads connecting the wafer and the gate unit. Secondly, the gate metallization on the wafer constitutes the gate contact to all segments on the wafer. The shape of this conductor is beneficial for an outer gate contact: it increases in cross-sectional area as current increases from the inside to the outside of the wafer. The outer gate contact, however, has two disadvantages for the gate circuit impedance. Most importantly, the gate metallization must carry the entire gate current through its tangential cross-section next to the gate contact. For a half-radius gate contact, the inner and outer halves of the gate metallization make up a parallel connection, so that each half carries a portion of the gate current. The second disadvantage is that the maximal distance between thyristor segments and the gate contact increases by approximately a factor of two, raising the inductive impedance load on the most remote segments. In summary, the outer gate ring is a choice that is expected to increase the resistive impedance of the gate metallization on one hand and decrease the inductive impedance on the other hand.

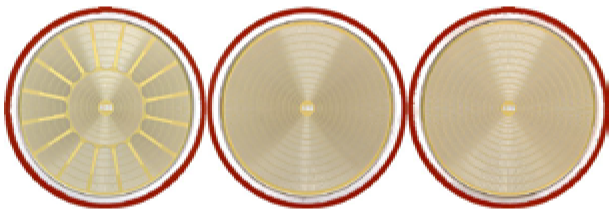


Figure 1: Pictures of experimental wafer layouts investigated. All wafers are cut to 94 mm diameter. Left: HWY layout. Centre: VSW layout. Right: CSW layout

Segment layout experiment

The uncertainty around how the outer ring gate would influence the current controllability and gate metallization robustness of an asymmetric device led to extensive simulation (the simulation method is described in [2]) of the impedance characteristics of the gate metallization in such devices. The simulations sparked an experiment investigating three design approaches to segment placement. An early simulation result indicated that the layout has very little influence on the inductive impedance distribution over the wafer, therefore the experimentation focused on the resistive distribution. Figure 1 shows photographs of the initial three designs that are all made up of twelve segment rings containing a varying number of identical segments.

The rightmost photograph shows a variation of a conventional IGCT wafer layout, named “Constant Segment Width” (CSW). As the name suggests, the segment width does not vary with placement radius and is equal to 250 µm.

The center photograph shows a further refinement of the conventional layout named “Variable Segment Width” (VSW). For this layout variant, the segment width varies with radial placement on the wafer. The VSW concept aimed to help the innermost segments, which have the most disadvantageous placement regarding gate contact, turn off faster by making them narrower. This would compensate for their inherent speed disadvantage given by the later arrival of the gate signal.

A third variant is shown in the leftmost photograph and is named “Highway” (HWY). It is an attempt to avoid loading the approximate outer half of the segment rings with the current generated by the inner half. The HWY concept also features variable segment width, but the distribution is squeezed together in each of the inner and outer segment ring compartments. The HWY layout allows for a wide range of additional trials: for example, changing the location where the gate metal of the two compartments is connected (if at all). The wafer in the photograph has its inner and outer compartments re-connected after ring ten, something that can be difficult for the untrained eye to make out. A further HWY variant investigated made the gate metallization in the highways, or runners, that connect the inner compartment with the gate contact thicker than in the compartments where the segments are placed.

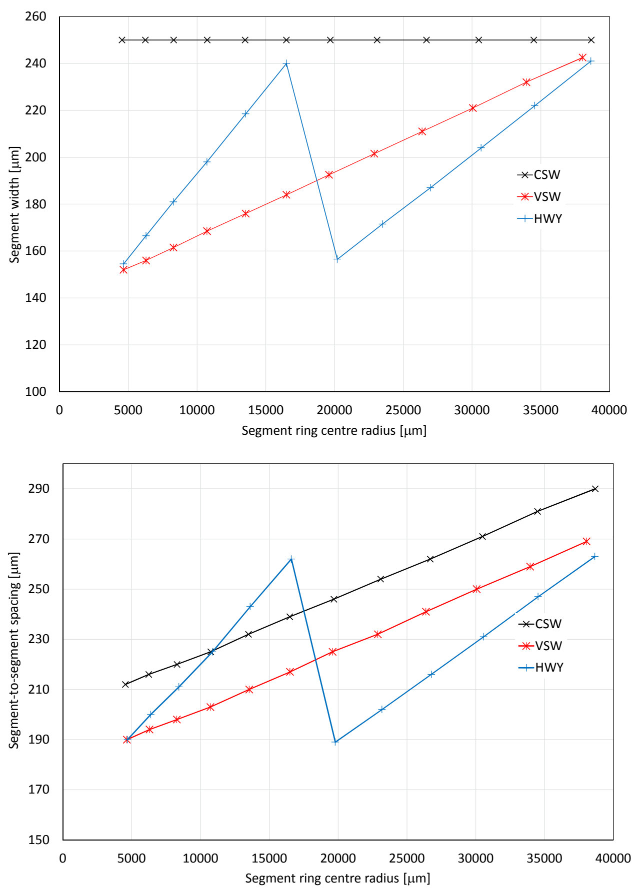


Figure 2: Details of the segment layout of the three designs investigated: segment width distribution (a) and segment-to-segment spacing distribution (b).

All three layout variants were manufactured with different gate metal layer thickness, between one and two times the conventional thickness, to decrease the radial ohmic impedance of the gate metal layer. Physical IGCT segment layouts can be quite accurately described by the segment width and spacing distributions over the wafer. The details of the layout variants that were investigated are shown by the graphs in figure 2, which illustrate how the segment width (top graph) and segment-to-segment spacing (bottom graph) vary with segment ring center radius.

In addition to the maximum controllable current, the segment layout influences the ruggedness of the cathode contact (on top of the segments). The impact is essentially characterized by the ratio between anode pressed metal area and segment pressed metal area. Ruggedness is clearly improved as the segment packing density increases. The same ratio of metal areas also influences the power loss efficiency, albeit to an extent that is bordering to insignificant.

Results

Power loss trade-off

As a consequence of the slightly different segment packing densities, the variants also display a slight difference in the trade-off between static and dynamic losses. The trade-off between on-state voltage and turn-off losses for a few design variants are plotted in the graph in figure 3.

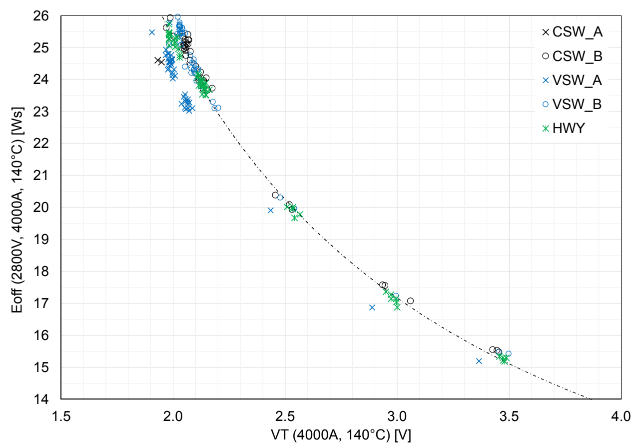


Figure 3: Technology curve at 4000 A, 2800 V and T_j 140 °C

Maximal controllable current

All variants were tested to destruction in single pulse mode at junction temperatures ranging from 25 °C to 160 °C. The current controllability distributions of the three main variations at V_{DC} 2800 V and T_j 140 °C is shown in figure 4. Clearly, the VSW layout has the highest robustness and, somewhat unexpectedly because the simulations promised a better result, HWY the lowest. A sample waveform of one of the highest switched currents, 8000 A, is plotted in figure 5. At low junction temperatures there is a clear performance limit due to inductive

voltage peaks. The over-voltage is a result of the energy stored in the stray impedance and the rapid current transients pushing the voltage transients close to, or above, the avalanche capability of the device. At low temperatures, this happens at current that, were it not for the over-voltage, would be lower than the device could turn off. Figure 6 shows a turn-off waveform at 25 °C, 6800 A and 2800 V, illustrating this effect. To some extent, the device can clamp the voltage by generating avalanche current, resulting a plateau at the maximal voltage. However, the device would fail in this condition if the energy stored in the stray impedance is too high.

Ruggedness at elevated temperature and frequency operation

Both frequency and HTRB testing demonstrated a device capable of operating with a $T_{vj,max}$ well above the required 140 °C. The frequency test was based on a current chopper setup, with the ability to change the switching frequency, current, voltage and duty cycle. Thermal failures were provoked at 100 Hz, 4850 A and 2800 V with a 95% duty cycle. The power losses under such conditions and thermal impedance of the cooling system allowed calculation of the junction temperature (T_{vj}) to be approximately 230 °C.

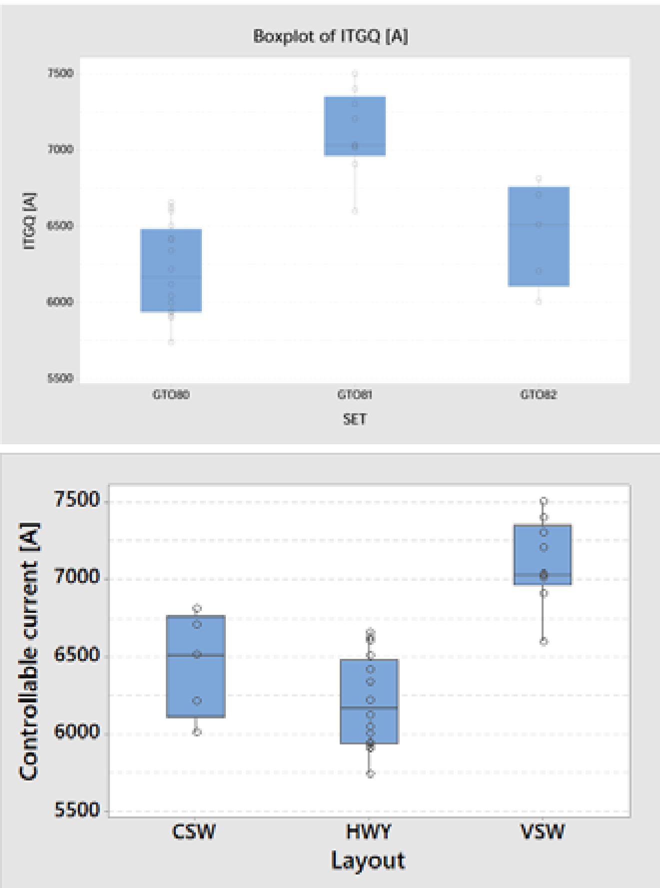


Figure 4: A box-plot showing the distribution of maximum controllable current as tested over the three main layout variants.

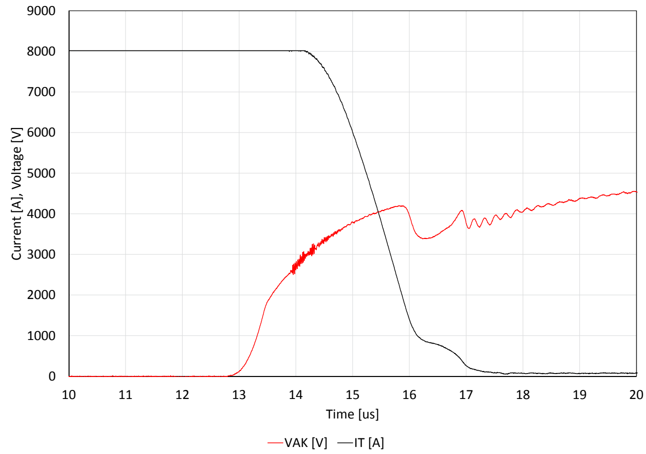


Figure 5: A waveform showing one of the events with the highest switched current at T_j 140 °C, I_T 8000 A, V_{DC} 2800 V.

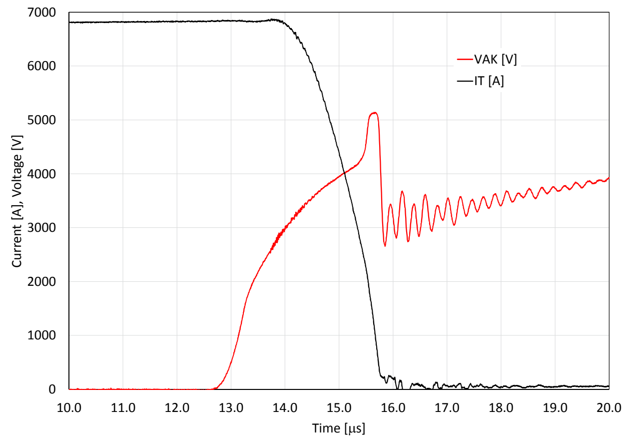


Figure 6: Turn-off waveform at 25 °C, 6800 A, 2800 V_{DC}, illustrating the inductive voltage overshoot that exceeds the avalanche capability of the device. The stray impedance for these measurements amounted to L_σ 325 nH.

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[1] M. Alexandrova and T. Wikström, “A Technology Platform for Reverse-Conducting Integrated Gate Commutated Thyristors with 94 mm Device Diameter”, in Proceedings of the PCIM, 2017, pp. 806–810.

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Unlocking the Full Potential of GaN with Vertical Devices

Substantially higher performing switching devices are required to deliver higher efficiency power conversion systems with increased power density and greater functional integration. Traditional silicon (Si) Super Junction MOSFETs (Si-SJ) have reached their performance limits while the newer silicon carbide (SiC) devices are constrained in their usefulness by their low switching frequencies.

By Dinesh Ramanathan, CEO, Nexgen Power Systems and Wolfgang Meier, Sen. Director of Marketing, NexGen Power Systems

Introducing Vertical GaN™ Devices

This has led to an increased interest in Gallium Nitride (GaN) which, as a baseline material, provides superior properties to produce devices with high breakdown voltage and high switching frequencies, thus enabling the improvement of efficiency and power density needed by future power electronics applications. Current GaN power devices, however, are realized as lateral devices, with thin layers of GaN heteroepitaxially grown on a Si (GaN-on-Si) or SiC substrate. The current flows very close to the surface of the device surface in a 2-dimensional electron gas (2DEG). Although these devices enable high switching frequencies, they do not exploit the high breakdown voltage property of GaN – they do not scale to higher voltages. NexGen uses a fundamentally different approach, creating a 3D Vertical GaN™ device structure by homoepitaxially growing thick GaN layers on a bulk GaN substrate (GaN-on-GaN). Current flows through the bulk of the material, avoiding the intrinsic disadvantages of the close-to-surface current conduction inherent in lateral (hybrid) GaN-on-Si devices.

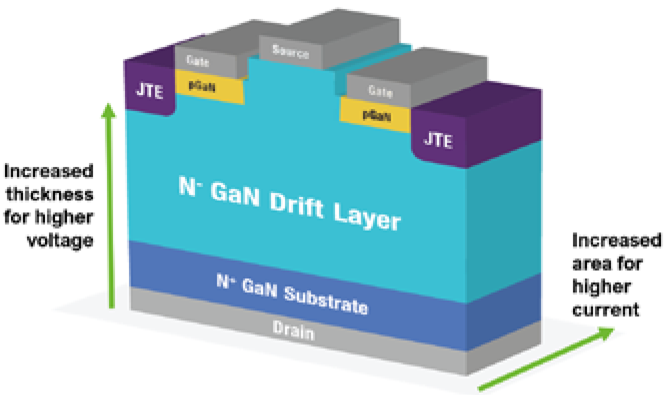

Figure 1: Conceptual View of NexGen's Vertical GaN™ FET

The NexGen Vertical GaN™ device is an enhancement-mode junction field effect transistor (eJFET) in which the vertical n-GaN channel is sandwiched between two p-n junctions. The gate-source voltage controls the extension of depletion regions into the channel and controls the drain current, showing the familiar FET Ids/Vds relationship. The device cross-section bears some resemblance to FinFETs known from silicon logic devices. NexGen's Vertical GaN™ JFETs provide a unique combination of features enabling advanced devices.

Decoupling breakdown voltage from device area and $R_{DS(on)}$: The 3D device construction with the breakdown voltage mainly determined by drift layer thickness does not require large lateral dimensions to achieve a large breakdown voltage. Therefore, the Vertical GaN™ technology leads to small devices which combine low $R_{DS(on)}$ with large breakdown voltages ≥ 1200V and very high switching frequencies.

Very Small Turn-on-Losses: The smaller device area of the Vertical GaN™ technology leads to smaller device area and much smaller device capacitances compared to 1200V SiC devices at similar $R_{DS(on)}$ and drain currents. Vertical GaN™ based devices are smaller than comparable lateral GaN devices with have much lower breakdown voltage specification of 650V. In particular, Coss (and consequently Qoss and Eoss) is very small, greatly reducing turn-on losses

Robust Avalanche Properties: Being a GaN JFET with the gate forming a p-n junction, Vertical GaN™ FETs can robustly avalanche to protect themselves and surrounding application circuitry from transient spikes and other abnormal operating conditions. In contrast, lateral GaN-on-Si devices do not avalanche and may degrade if exposed repeatedly to voltages above their breakdown voltage.

Body Diode Function without Reverse Recovery Charge: Vertical GaN™ devices have no parasitic body diode and do not suffer switching losses caused by minority carrier/reverse recovery charge removal. The Vertical GaN™ eJFET device structure allows current conduction in reverse direction in case of a reversal of the drain-source voltage. In this way, the JFET effectively assumes the function of a freewheeling body diode without reverse recovery switching losses.

Insensitive to Device Surface Effects: The current conduction within the bulk of a Vertical GaN™ device is robust and insensitive to surface effects compared to lateral GaN-on-Si devices, avoiding by construction effects like dynamic $R_{DS(on)}$ variation. Insensitivity to surface effects also simplifies cooling from both sides of the device leading to greatly improved thermal management options.

Intrinsic Reliability: Crystal Lattice and Coefficient of Thermal Expansion mismatch do not exist in the homoepitaxial layer buildup of GaN-on-GaN devices. Increased defect densities at layer interfaces, reliability weaknesses, manufacturing challenges, yield and performance compromises are avoided by construction.

For the first time NexGen's Vertical GaN™ technology combines device properties previously believed to be incompatible and therefore impossible to achieve:

- Devices with superior switching frequency and very high breakdown voltage
- Avalanche robustness better than silicon SJ-MOSFETs and SiC devices with switching frequencies of GaN devices
- Mass production cost scalability with advanced device and material properties

Vertical GaN™ delivers the promise of GaN materials without being subjected to the reliability and cost compromises inherent in the construction of lateral GaN-on-Si devices. The unique combination of properties of the Vertical GaN™ power device allows a single technology to address the full range of power conversion application that currently can only be served by a multitude of technologies.

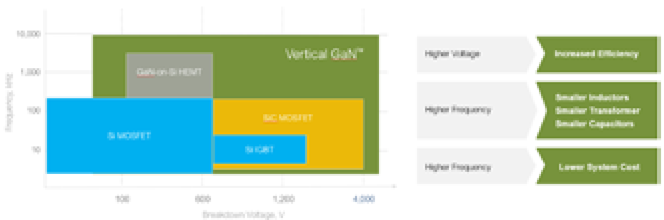

Figure 2: Vertical GaN™: A Superset of existing Power Semiconductor Technologies

Application Benefits

NexGen has developed a range of application demonstrators to showcase the superior performance of Vertical GaN™ devices in high voltage, high switching frequency applications. Details of 1MHz, 100W, 800V Buck and Boost converters as well as a 1 MHZ, 20W T8 LED driver are described in Application Notes on NexGen's website (https://NexGenpowersystems.com/)

NexGen's Vertical GaN™ eJFET devices are compatible with existing superjunction MOSFET drivers, only two resistors and one small capacitor are needed to match a standard MOSFET driver to NexGen's eJFET. Complicated and costly technology-tailored drivers are not needed, thus making the integration of Vertical GaN™ devices into existing designs extremely easy, allowing customers to benefit from superior device performance almost immediately without undergoing elaborate redesigns.

Currently a range of power supplies with output power above 100W are in development. The performance of Vertical GaN™ devices allow operation at switching frequencies of higher than 1MHz and employ novel control features in PFCs and LLCs.

Particularly in soft-switching topologies, the extremely small and almost linear output capacitance of Vertical GaN™ devices dramatically reduces the requirements on circulating current (a source of power dissipation) and dead-time (a fundamental switching frequency limitation) necessary for ZVS operation. This enables high frequency operation with high efficiency, allowing to reduce the size of passive components and leads to an estimated volume reduction of 50% for passively cooled power supplies.

NexGen Introduction and Vertical GaN™ Product Schedule

Founded in 2017, NexGen operates a state-of-the-art GaN device fabrication facility (fab) in Syracuse, New York. NexGen is the First Mover in this space, with an IP portfolio of 100+ fundamental patents in device architectures, process technology and circuits for Vertical GaN™ products. NexGen's 66,000 sq. ft. fab is dedicated to GaN and combines device development with production. It has the necessary metrology and failure analysis capabilities to achieve fast cycles of learning. By operating its own fab, NexGen is afforded the critical independence necessary to reduce development time and accelerate the commercialization of Vertical GaN™ devices.

Figure 4: NexGen's GaN Fab in Syracuse/NY

Beginning in Q3 2020, NexGen will sample 1200V and 700V devices with R(DSon) of 85mΩ, 170mΩ and 290mΩ in standard 8x8 DFN and TO247-4 packages. Customers participating in NexGen's early adopter program receive early engineering samples in mid-Q2 2020, including design support.

The comparatively small die size of Vertical GaN™ eJFETs together with volume-based cost reductions of 4" GaN wafers allows NexGen to compete very effectively with Si-SJ pricing. NexGen enables designers to overcome the limits of existing devices and employ robust Vertical GaN™ devices with high switching frequencies and high breakdown voltages in cost sensitive applications.

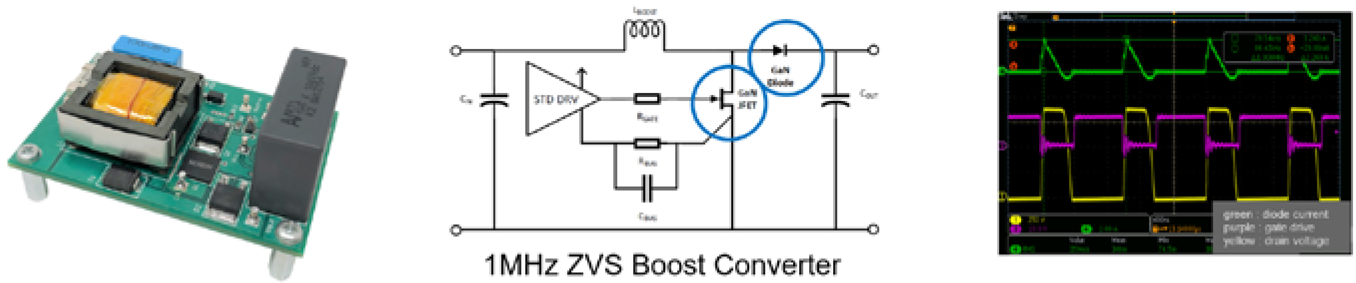

Figure 3: 1MHz Boost Converter

Application-specific Capacitors for Laser Power Supply Units

Power supply units for high-power laser diodes in research systems require special capacitors: They must ensure fast discharge of the energy that is needed for generation of high-current pulses. Mersen delivers custom solutions that are successfully used in the power supply units of Schumacher Elektromechanik GmbH.

By Jens Heitmann, Account Manager/Marketing Manager, FTCAP GmbH

Back in 1949 Schumacher Elektromechanik GmbH started manufacturing transformers and industrial electronic components, as well as power supply units. Among other achievements, the company made a major contribution to the development and production of the first model wireless remote control. In the 90s Schumacher produced the first special power supply units for lights, and later also for industrial and laser applications – the latter including the necessary software controllers. Today Schumacher Elektromechanik GmbH specializes in the development of laser power supply units, as well as integrated cooling units and their controllers. This is achieved by means state-of-the-art production systems, which can also be used for the manufacture of externally developed products.

Figure 1: Mersen FTCAP capacitors are the right choice for special applications in small and medium quantities

Application-specific capacitors for laser power units

“We are very active particularly in the areas of laser power supply units and controllers”, explains R. Winkler, Head of Purchasing at Schumacher Elektromechanik GmbH. “The fact is that the various laser types require custom solutions.” The Schumacher product spectrum ranges from CW power supplies for argon lasers and high-voltage power supplies for CO2 lasers through CW and pulse power supplies for light-pulsed and diode-pumped lasers, all the way to integrated cooling elements, Pockels cell drivers, TEC controllers, Peltier power supplies and controller supplies for excimer lasers. Of course, it is also possible to combine different supply types. The power supply units cover power ranges from a few watts to 20 KW.

Buffering of the voltage in the power supply units requires capacitors, which Schumacher has been purchasing from Mersen for many years. The main demand is for aluminium electrolytic capacitors of the SIH and GW series. The latter are used for example in the power supply units for high-power laser diodes in research systems: Such systems require fast discharge of the energy for generation of high-current pulses of about 100-500µs. “The capacitors are integrated in the capacitor bank of a laser power unit, where they buffer the supply voltage”, explains R. Winkler. “The aluminium electrolytic capacitors are very reliable in this application and fulfil the requirements of our specifications.”

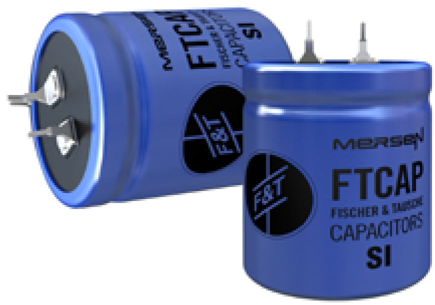

Figure 2: Schumacher also purchases aluminium electrolytic capacitors of the SIH series from Mersen

Thermally optimized for high ripple currents

The GW series are threaded FTCAP capacitors that are insensitive to high ripple currents. As a side effect, however, the high currents also cause increased temperatures in the capacitors. Special winding constructions therefore ensure optimal heat dissipation at the capacitor base. In addition, the GW series is optionally equipped with base cooling by means of a Sil-Pad that dissipates the heat.

Figure 3: The GW series capacitors are used by Schumacher for example in the power supply units for high-power laser diodes in research systems

A special feature of the GW series is the patented stepped base: This design ensures that the base of the capacitor is flat despite the adjacent heat shrink tube. Air inclusions are therefore reduced, which would hinder dissipation of heat from the capacitor to the heat sink. Thermal resistance is substantially lower, for processing of high loads despite the compact design. In addition, the cup features an outer bead, which allows seamless mounting of the capacitor to a heat sink by means of a ring clamp manufactured in-house by Mersen. A positive side effect is that the pad and the use of a ring clamp for mounting electrically insulate the capacitor from the heat sink. This provides a large leakage distance that prevents the flow of residual earth-fault currents.

GW series aluminium electrolytic capacitors are designed for high performance despite their compact size. Their optimised internal construction achieves a high CV (capacity-voltage) product. The advantage is minimal power loss as soon as an electrical load is applied. Since the special design not only saves space but also improves cooling performance, this also reduces costs to the user.

Custom developed capacitors for successful applications

R. Winkler is very satisfied with the GW series capacitors: "Like all Mersen components, they function with absolute reliability." Another advantage for the head of purchasing is that the Mersen location based in the North of Germany can also implement custom requirements if needed: "Mersen produces custom tailored capacitors for several of our applications." This versatility is a unique selling proposition in the industry – FTCAP capacitors are the right choice for special applications in small and medium quantities. The special field is customized special solutions.

In addition, the company offers a range of high-quality standard products, but always with the option of adapting them – for example, if a customer needs a normal form with requirements for adaptation of other factors, such as voltage, current, dimension, pulse resistance, and oil resistance. "The cooperation – from development through to large-scale production – is very well structured and the subsequent production process is streamlined and well organized. We are satisfied and look forward to future challenges", concludes R. Winkler.

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The Challenges of Obtaining Repeatable and Reliable Double-Pulse Test Results – Measurement Science

In our April article, we discussed the challenges of fixture design to obtain repeatable and reliable results from your Double Pulse Test (DPT) setup.
In this article, we continue the discussion, but focus on measurement science. There are many measurement aspects to consider. This article concentrates on several aspects that significantly influence your DPT measurement waveforms, and the associated extracted dynamic parameters (e.g. t_r, t_f, $e_{(on)}$, $e_{(off)}$).

By Ryo Takeda – Keysight Solution Architect, Bernhard Holzinger – Keysight Technical Architect, Michael Zimmerman – Keysight R&D Engineer, Mike Hawes – Keysight Power Solution Consultant

The Challenges of Obtaining Repeatable and Reliable Double-
By considering measurement science and techniques for measuring the switching waveforms, V_{GS}, V_{DS} and I_D in a DPT setup, you positively impact the repeatability and reliability of your results. Before addressing the specific measurements, let's first analyze the basic DPT setup (Figure 1).

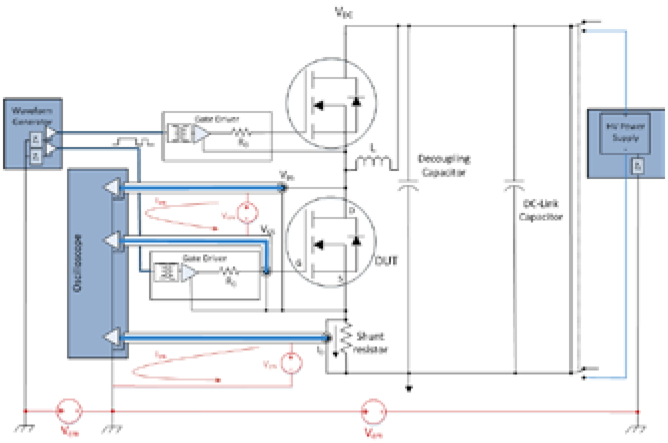

Figure 1: Basic Double Pulse Test Setup

We've added additional detail to the diagram from April's article to highlight several important considerations. All measurement instrumentation is referenced to earth ground. Oscilloscope inputs are single ended, when using conventional probes, with the ground leads essentially being at earth ground potential. For many power supplies, the + and – terminals "float" from earth ground to a specified limit (i.e. Maximum voltage between earth and output terminal is 500V). This isolation from earth ground can be modeled as isolation impedance (Z_i) for these instruments. Likewise, many Waveform/Function Generators are isolated from earth ground, typically ± 42V. Why is this important?

Common Mode Effects
Ideally, we'd like to assume earth ground is the same potential across our DPT setup and there is no current flowing in earth ground. The reality is there are differences in potential between the earth ground contact points, which are referred to as common mode voltages (V_{cm} in Figure 1). The common mode voltages induce common mode 'error' currents that impact our measurement instruments (i.e. oscilloscope). Even the isolated instruments (e.g. HV power supply) provide common mode current return paths through Z_i, especially as we consider the higher frequency energy switching in the setup. Therefore, common mode currents need to be addressed in the DPT setup.

Typical DPT setups use the HV power supply to charge the DC-Link Capacitor with the energy needed to complete a single instance of the DPT. To eliminate potential common mode currents, the power supply should be disconnected using switches (Figure 1) from the DPT setup prior to executing the DPT test. This technique addresses the concern of any common mode coupling from the power supply. Similarly, the Waveform Generator is typically isolated in the Gate Driver, removing any potential for common mode coupling.

The oscilloscope is a different challenge. It is the instrument that measures the DPT waveforms. Without differential or isolated probes, conventional oscilloscope probes will have long "earth referenced" return paths from the point of measurement, making them susceptible to common mode noise. There are also challenges in making the V_{GS}, V_{DS} and I_D measurements without isolated/differential probes.

To start with, most DPT setups test the low side device (i.e. DUT in Figure 1) to avoid large common mode voltages present when testing the high side device. Additionally, if making I_D measurements with a shunt, one can arrange the voltage probe measuring the shunt by placing the ground lead at the same node the ground leads are connected for V_{GS} and V_{DS} measurements. This establishes the DUT 'source' terminal as the earth ground reference point in the setup, enabling the three measurements to be made without isolated or dif-

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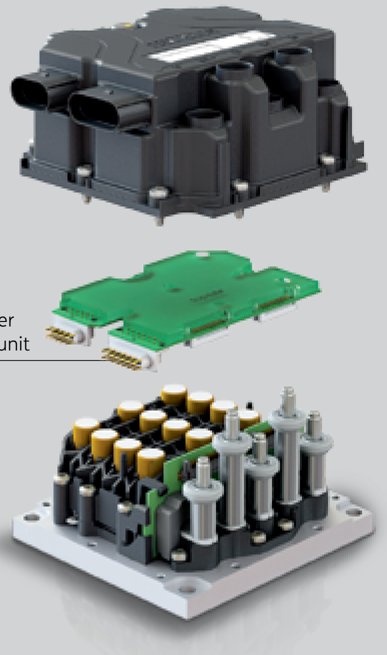

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ferential probes. The trick then is to reverse the polarity of the voltage measured across the shunt to determine I_D.

We still have the problem of common mode currents flowing through the oscilloscope probes, in both the center conductor and shield. To minimize this error, the probes are wound through a ferromagnetic core or common mode choke (Figure 2). Because the common mode current in the probe center conductor and the shield flow in the same direction, the associated fluxes in the core add together. This effectively creates a larger opposing magnetic field to the common mode current. Whereas, for the differential (desired) mode current, the fluxes in the core cancel, removing the opposing magnetic field and therefore, allowing the differential signal to pass through the probe to the oscilloscope.

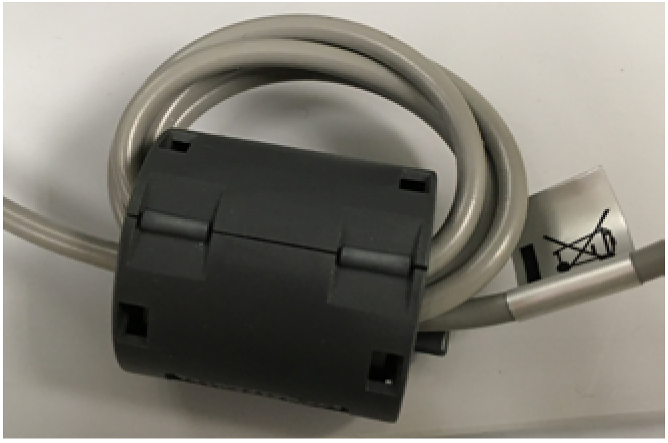


Figure 2: Common Mode Choke

Having established some basic understanding of the DPT setup, let's look at some of the specific measurements.

V_{DS} Measurement

One major challenge of measuring V_{DS} is the large dynamic range required to measure it in both the "on" and "off" states. In the "on" state, the DUT is conducting, and the voltage drop from drain to source is small (1V - ~10V). It is critical to make an accurate measurement because $R_{DS\ (on)}$ is calculated from this V_{DS} measurement divided by the corresponding I_D measurement. In the "off" state, the DUT is blocking the operating voltage selected for the test (> 1000V). With 2-3 orders of magnitude difference between the measurements, it requires a much larger dynamic range than is afforded with an oscilloscope.

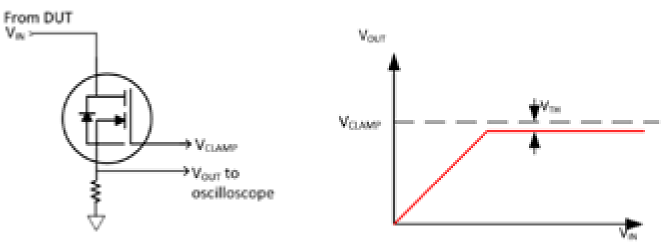


Figure 3: Simplified V_{DS} Clamp Circuit and Graph

For measuring V_{DS} when the DUT is off, we use an appropriate high voltage probe based on the operating voltage selected, which will attenuate the signal within the oscilloscope's range. To measure V_{DS} when the DUT is on, we want to use a standard 10:1 probe to get the most accurate measurement possible. We do this using a clamp circuit. The goal of the clamp circuit is to limit the voltage applied to the oscilloscope, when the DUT is turned off, so it does not damage the oscilloscope. But when the DUT is turned on, allow the signal to pass, so the 10:1 probe measures the low V_{DS} voltage. The simplified schematic and graph illustrate the capability of the clamp circuit (Figure 3).

For V_{IN} less than $V_{CLAMP} – V_{TH}$, there is a linear 1:1 relationship between V_{IN} and V_{OUT}. When V_{IN} reaches $V_{CLAMP} – V_{TH}$, the FET turns off and effectively clamps V_{OUT} just below the V_{CLAMP} voltage, regardless of the value of V_{IN}. All you need to do is select a clamp voltage that is above the expected $V_{DS(on)}$ value and below the maximum input voltage of the oscilloscope. The result is an accurate measurement of $V_{DS(on)}$, when the DUT is turned on and a clamped voltage when V_{IN} is greater than V_{CLAMP}.

I_D Measurement

In general, current measurements are more difficult than voltage measurements for DPT setups. One of the main limiting factors is bandwidth. As mentioned in our April article, the frequency content of DPT signals is increasing dramatically, requiring higher and higher bandwidth measurements. Most current sensor bandwidths are typically less than what is needed for faster DPT measurements. Rogowski coils are attractive current sensors, because they are cheap, relatively easy to setup and use the changing magnetic field from a conductor to measure the current. However, they do require connecting their sensor loop around the conductor to be measured. This is not feasible with some setups. Additionally, they have limited bandwidth ~30 MHz and are also not able to measure DC current. A bandwidth of several hundred MHz is important for measuring current of faster power semiconductors.

Current shunts are another way to measure current. The current flows through a "known" precision shunt resistor, developing a measurable voltage used to subsequently calculate the current. Current shunts require breaking the current path to insert them into the circuit of interest. It is important to have a low impedance to minimize the influence of the shunt in the circuit. Some commercially available shunts specify bandwidths in the 100s of MHz. We characterized the S_{21} transfer function of several shunts (same model and specification) to see how consistent their bandwidth was (Figure 4).

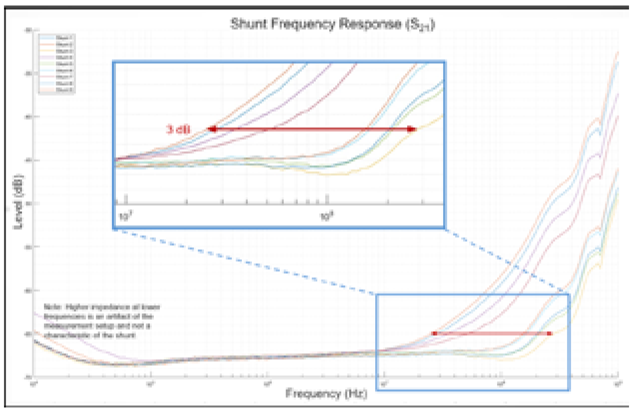


Figure 4: S_{21} transfer function of coaxial shunts

The 3dB bandwidth of these shunts ranged from ~ 25 MHz to ~ 280 MHz, more than an order of magnitude variation in performance! This difference significantly impacts the waveforms captured in a DPT measurement (Figure 5). You notice more overshoot for I_D with the 25 MHz shunt compared to the 280 MHz shunt, distorting the power waveform that is ultimately used to integrate $e_{(ON)}$. This distortion is an artifact of the shunt, not the power device. Therefore, the 25 MHz shunt ultimately results in a larger and incorrect $e_{(ON)}$, extracted from the distorted waveform.

Signal Skew

We can't discuss measurement challenges for dynamic testing without mentioning the aspect of signal skew. Because of the high frequency and sharp edge transitions in DPT waveforms, it is important to realize there are different signal paths through each oscilloscope probe out to each measurement point. These different paths impact the propagation of each signal resulting in signal skew (Figure 6). Depending on which signal (V_{DS} or I_D) is delayed, $e_{(ON)}$ and $e_{(OFF)}$ calculations could underrepresent or overrepresent the resulting switching loss.

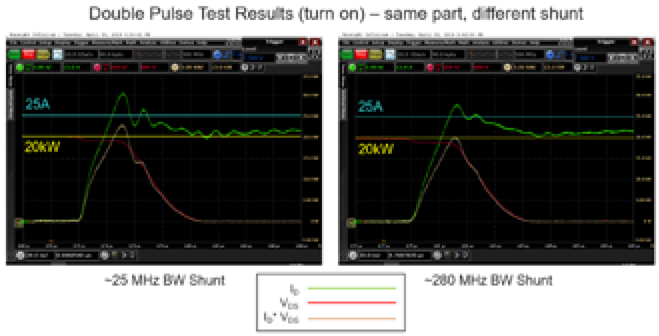


Figure 5: Impact of BW on current shunt measurements

Figure 6: Time skew in oscilloscope inputs, measured on DPT fixture

Conclusion

The Keysight PD1500A Dynamic Power Device Analyzer/Double-Pulse Tester was developed to solve these measurement challenges. In addition to supporting the common mode recommendations and a modular clamp circuit, we've developed and implemented compensation techniques to address the other issues we've raised. Specifically, we have a software guided routine to adjust the oscilloscope and probes to eliminate signal skew at the DPT fixture. Additionally, we characterize each shunt resistor used in our systems in the factory by measuring the S_{21} transfer characteristic up to 400 MHz. We then compensate for that specific's shunt's characteristics, essentially flattening the frequency response and eliminating distortion from low bandwidth shunts. As in many Keysight solutions, we provide an autocalibration routine. This software guided routine uses an accurate Source Measurement Unit (SMU) with 100 nV resolution as an internal system reference. Measurement points across the range of each oscilloscope channel/probe pair are compared to the corresponding SMU reference values. From this data, gain and offset errors are determined and compensated for in the system, providing improved accuracy and more repeatable results. Figures 7a and 7b, illustrate the possible impact on your DPT measurement results when using the compensation techniques described. We measured DPT waveforms and extracted e(off) from a SiC MOSFET (1200V, 40A) with the same operating conditions (800V, 30A, R_g=10Ω, room temperature) with and without compensation.

Figure 7a shows the DPT waveforms and extracted results without compensation. As we might expect, the ringing in I_D, and consequently the power (V_{DS} * I_D), is more exaggerated in these waveforms, undoubtedly due to a lower bandwidth shunt. Combined with the other potential signal skew and autocalibration errors, the resultant extracted $e_{(off)}$ result is 218.50 µJ. Compare this to Figure 7b where we used compensation techniques. The ringing is reduced and the extracted $e_{(off)}$ result is 296.60 µJ. In the case of $e_{(off)}$ for this device, the PD1500A measurement techniques remove a 26% error caused only by incorrect measurement science!

Figure 7a: $E_{(off)}$ waveforms and extraction without compensation

Figure 7b: $E_{(off)}$ waveforms and extraction with compensation

Keysight designed the PD1500A Dynamic Power Device Analyzer as a complementary dynamic characterization solution to the B1505A/B1506A Power Device Analyzers you've learned to count on. We focused on providing repeatable and reliable dynamic DPT measurements for discrete Si/SiC based power semiconductors. We are continuing our R&D investment in state-of-the-art measurement techniques for DPT solutions. Stay tuned for new solutions focused on discrete GaN and Si/SiC power modules.

To learn more about Keysight's PD1500A Dynamic Power Device Analyzer, please visit the website (https://www.keysight.com/en/pd-2996110-pn-PD1500A/dynamic-power-device-analyzer-double-pulse-tester?nid=-32875.1266898.00&cc=US&lc=eng) and view the video demonstrating its operation (https://www.youtube.com/watch?v=CiBJbHcZFAM&t=46s). Look for future articles from Keysight, with more discussion regarding repeatable and reliable Double-Pulse Test results.

www.keysight.com

Demystifying Resonance

Resonant power is tricky—to state it mildly! The devil is not in the details! Not initially at least. One can easily mistake the forest for the trees, getting truly lost, and not even realize it. We need a soft transition from the relative comfort of our familiar world of classical ("PWM"-based) power, into the yet-nonintuitive world of resonant power, including wireless power transfer (WPT). Preferably with a stopover at the "LLC topology".

By Sanjaya Maniktala, CTO and Founder, ChargeEdge, Inc. and Michael Doktor, CCO and Founder, Foxy Power

WPT and LLC are very much the same topology, or should have been, but most WPT solutions today use the "double resonator" shown as the second from top circuit in Figure 1, (shaded red), which actually creates multiple resonant peaks (lower half of Figure 2). This strange and wholly anticipated gain profile is unfortunately not even amenable to any proper control or tracking/optimization algorithm. We need to disband it quickly. The upper half of the figure, is what we get with only primary-side resonance, which is strongly recommended even for creating proper correct WPT, as also commonly used in LLC. It is amenable to smart, but possibly proprietary control algorithms for enhancing "user experience" and handling variable coupling, the key distinguisher between LLC and WPT.

Defining the "Kernel"

We can take any kernel and scale it to any power, frequency and input voltage range.

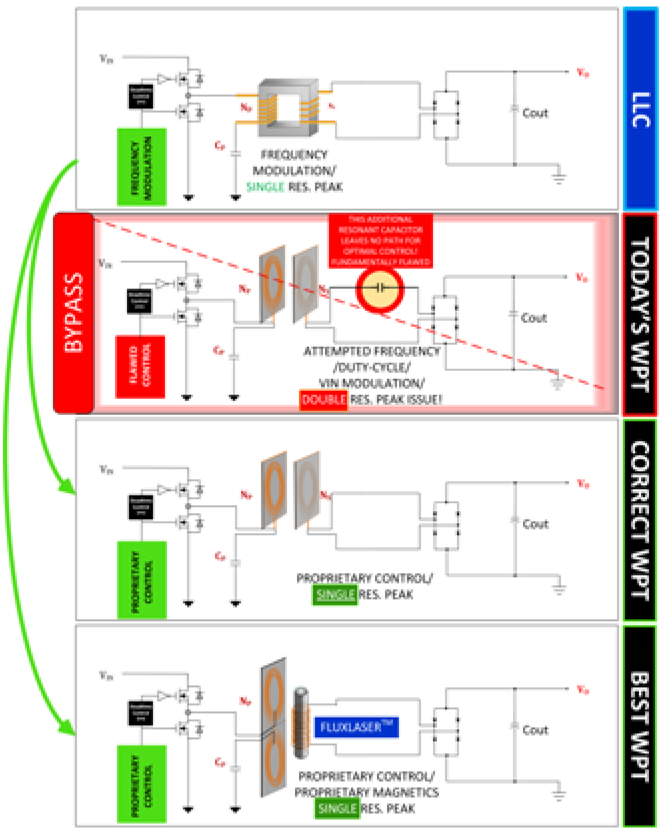


Figure 1: Multiple resonant peaks

As a primer, here are the scaling law patterns that we will be using. To double the power, halve the inductance and double the capacitance

- To double the frequency, halve the inductance and halve the capacitance
- To quadruple the power, double the input voltage

Instead of "double" or "halve", we can use other scaling factors to generalize, quite obviously. The trend is clear.

Here, just for historical continuity, we have used the same values of LP and CP (57.2µH and 225.8nF) that we had arrived at for the PoE application in Switching Power Supply Design and Optimization, Second Edition. Since we are scaling anyway, we could actually use any initial kernel.

We then inputted these LP and CP values into a general Mathcad spreadsheet, to generate the graphical aids presented herein.

In Figure 2, just to throw more light on the gain curves that we typically get in an LLC topology, as an intermediate step, we have used our Mathcad spreadsheet to suggest the "recommended" load resistor of 20.6 ohms, for the PoE application. Then we have used multiples, or fractions, of that 20.6 ohms "recommended" resistor, to generate the stacked gain plots, to reveal the general trend. Note that "20.6 ohms" is the equivalent AC load resistor, not the DC load in the final DC-DC converter. It is the one meant to be applied to the equivalent AC-AC, non-isolated model using the First Harmonic Approximation (FHA).

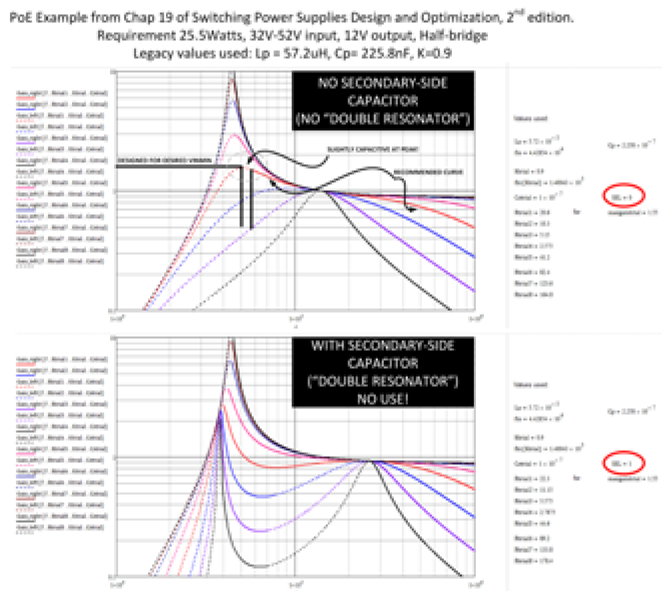


Figure 2: Plotting Gain curves for the PoE converter, with and without CS

In Figure 3, we see that the resonant peak shifts dramatically as a function of load. In fact, it is also a function of coupling K, because the right extreme, fHI, is simply the resonance of the leakage with the resonant capacitor. fLO is the resonant peak at very light loading.

Note that simple control algorithms, as being currently used, just can't suffice. Frequency modulation techniques, based on trying to raise the gain by simply lowering the frequency, are in obvious danger of rolling "over the top", as the peak flattens and shifts to the right as load increases. We can easily land up on the wrong side of the resonant peak, to its left, where power suddenly collapses as we lower the frequency futher. Now, expect a "mysterious" turn-OFF (and an Amazon return!). Other simplistic control methods, try to use modulation of duty cycle, or phase or input voltage, while keeping a "fixed frequency". They also easily land up on the wrong side of the resonant peak, and not only is the wrong side "lossy", but EMI increases dramatically due to hard-switching, negating the very purpose of "fixed-frequency" methods. Those actually have no place in resonant power, as the wireless electric vehicle charging (WEVC) teams around the world are realizing. These mistakes are magnified at higher power levels. And we haven't even yet considered the effects of the "double resonator" flaw, which introduces another capacitor into the picture, thus causing two moving peaks, not one. Because now we have an LLCC, not an LLC!

For example, if any current method is based on an intrinsic assumption that the resonant peak is fixed at 100kHz, and has thus described a "control algorithm" which simply states: "head to 115kHz to increase power", a good question to also ask is: what if the resonant peak has not just moved to "100 /√0.5 = 141.4kHz"? That would be true for K=0.5, and single resonant peak case, including LLC. For a higher coupling, say K=0.7 it would shift to 100 / √0.3 = 182.6 kHz. For K=0.8, it would be 100 / √0.2 = 223.6kHz. It gets much worse in the case of double peaking. But most likely, the current method has also mandated that the maximum upper frequency of operation is fixed at say, 200kHz (a plausible/laudable goal, to simplify power circuitry). But then it means, we will perpetually be on the wrong (left) side of the peak. We can never get to the right side, literally. How can we even ever hope to regulate? Such a charging pad may "sort-of work" for some random receiver, or odd placement (coupling), but the interoperability question looms large.

Let us move on, without CS here-ever-after!

Practical Design Example of a Wide-Input 900W LLC/WPTconverter

With the above kernel, we have generated two key design curves, shown in Figure 4, and Figure 5. Keep in mind that the values used here, were LP = 57.2µH and CP = 225.8nF. So, this is the challenge:

We want to deliver 900W into a 48V output. Select the best L and C values for the converter for an estimated coupling of K = 0.5. For EMI compliance reasons, we want to stay below 150kHz guaranteed. What are the best operating frequencies to carry out meaningful simulations, to test its performance? We are assuming an input DC varying from 200 to 400V.

On account of the high-power, the obvious choice is a full bridge, not a half bridge. At 400VDC therefore, the equivalent AC wave applied to the input of the resonant network is as per the first harmonic approximation (FHA):

$$V_{INMAX\_AC} = V_{INMAX\_DC} \times \frac{4}{\pi} \quad \text{Volts}$$

$$V_{INMAX\_AC} = 400 \times \frac{4}{\pi} = 509.3 \quad \text{Volts}$$

This is the equivalent amplitude of the sine-wave applied as per FHA. (For a half bridge we would have divided this by 2).

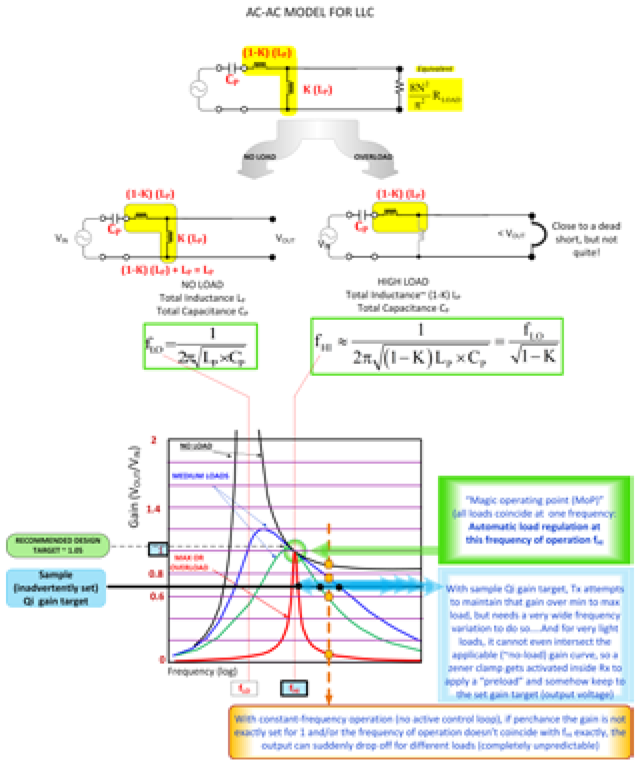


Figure 3: Varying load in an LLC, causes a frequency shift, depending on coupling

From Figure 4, for a coupling of 0.5 and a VINMAX/VINMIN ratio ("gain factor") of 2 (to allow us to reach 200VDC from the original 400VDC), we see that the recommended resistor to be placed on the output of our non-isolated AC-AC equivalent circuit is 14.7 ohms.

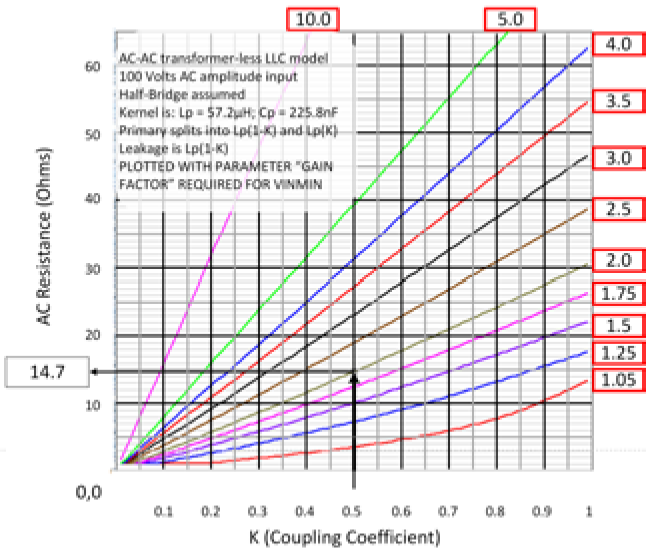
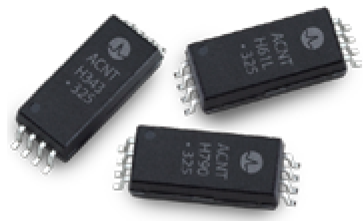


Figure 4: Resistance lookup aid based on PoE kernel



This load resistor is actually valid, irrespective of the applied/assumed input actually, because it produces just the right amount of "bulge" in the gain profile curve, in conjunction with the selected C and L (the critical "C/L" ratio in effect, which determines the power capability of a resonant network, in relationship to a given load, R), to allow for a gain of 2, occurring somewhere between f_{HI} and f_{LO}, before the gain curve rolls off! If we achieve that, there is no hint of overdesign either! No excess costly resonant capacitors. Just the right "bulge" in the resonance curve.

Now, had we applied an input of 400VDC through a full bridge, or an equivalent AC voltage of 509.3 Volts, the power at the peak of the AC sine wave input would have been

$$\mathrm{Peak\_AC\_Power} = \frac{V^2}{R} = \frac{509.3^2}{14.7} = 17650 \quad \text{Watts}$$

Note that the average of any Sine-squared function is known to be half. In other words, the average (DC) power we got from the kernel, with the desired maximum input applied to it, is

$$\mathrm{Average\_Kernel\_Power} = \frac{\mathrm{Peak\_AC\_Power}}{2} = \frac{17650}{2} = 8825 \quad \text{Watts}$$

But we want only 900W from our proposed LLC converter, So the Power Scaling Factor we need to apply is less than 1 in our case:

$$\mathrm{Power\_Scaling} = \frac{\mathrm{Desired\_Power}}{\mathrm{Average\_Kernel\_Power}} = \frac{900}{8825} = 0.102$$

Coming to the frequency scaling factor, the fHI of our kernel (for the desired K=0.5) is

$$\mathrm{fhi\_Kernel} = \frac{1}{2\pi\sqrt{(1-K)L_P C_P}} = \frac{1}{2\pi\sqrt{(1-0.5)\times 57.2\mu \times 225.8n}} = 62.63\mathrm{kHz}$$

To stay below 150kHz, we would like to set fHI of the new converter exactly at 145kHz. So, the desired frequency scaling factor is

$$\mathrm{Freq\_Scaling} = \frac{\mathrm{Desired\_fhi}}{\mathrm{fhi\_Kernel}} = \frac{145k}{62.63k} = 2.315$$

Final step, the recommended LP and CP values for our 900W converter are thus

$$C_P = C_{P\_KERNEL} \times \frac{\mathrm{Power\_Scaling}}{\mathrm{Freq\_Scaling}} = 225.8\mathrm{nF} \times \frac{0.102}{2.315} = 9.95\mathrm{nF}$$

$$L_P = \frac{L_{P\_KERNEL}}{\mathrm{Freq\_Scaling} \times \mathrm{Power\_Scaling}} = \frac{57.2\mu\mathrm{H}}{2.315 \times 0.102} = 242.24\mu\mathrm{H}$$

These are the values to try out in a simulation. They establish the desired power capability of the resonant network in effect, at the desired input voltage, allowing for the desired input variation too, and based on out estimate of K.

In the simulation, the calculated L_P will need to be split up as follows

L_{LKG} = (1 - K)×L_P = (1 - 0.5)×242.24 μH = 121.12 μH
L_{MAG} = K×L_P = 0.5×242.24μH = 121.12μH

Now, if we had applied 400VDC at the input, then that would have given us exactly 400VDC output too, for the gain target of 1, if we introduced a 1:1 transformer and a diode bridge and output smoothing capacitors. In other words, we calculated it all for a VOR = 400V (or slightly higher as recommended earlier). So, with a 48VDC output instead, to appear as 400VDC in the equivalent DC-DC transformer-less circuit, the desired turns ratio is

$$N = \frac{V_{INMAX}}{V_O} = \frac{400}{48} = 8.33$$

That is exactly how voltages scale through transformer, and we are just using the same principle to reflect 400V into the Primary, from 48V at the Secondary.

Note: when we actually wind the transformer, we will be using full (or maybe half) integral turns, so we will not get exactly 8.33 as recommended above, anyway. Further, we want to aim for a slightly higher VOR than V_{INMAX}, i.e. to set a gain target slightly more than unity, to assure that we can regulate fully between f_{LO} and f_{HI}, never needing to go higher than f_{HI}, for any load. So, if we manage to set the actual turns ratio N_P/N_S slightly greater than the calculated value above, it would work better. We may have to wind a few iterations of the transformer, to ensure that we stay within f_{LO} and f_{HI} always, with no "mysterious" dropouts.

Simulators usually use the inverse of this as their "turns ratio". So, for them we may need to input the following turns ratio into the transformer used in our simulations (connected across the magnetizing/coupled inductance only)

$$N_{SIM} = \frac{V_O}{V_{INMAX}} = \frac{48}{400} = 0.12$$

We also realize that in the simulator, to test it for 900W (at the desired output voltage), we simply need to put a resistive load of value

$$\mathrm{Rload} = \frac{V_O^2}{\mathrm{Power}} = \frac{48^2}{900} = 2.56 \quad \text{Ohms}$$

Finally, looking at Figure 5, we see that the gain factor = 2 curve intersects with the K=0.5 to give us a frequency ratio of 0.75. That is the ratio of the location of the resonant peak of the applicable resonant curve with respect to f_{HI}. Now, this ratio will remain unchanged through the scaling exercise, though the f_{HI} has changed, and is now at 145kHz. So, assuming the same ratio, the location of the resonant peak, at which we should be able to get 900W at 200VDC input is 0.75 × 145kHz = 108.75kHz. That is the frequency we need to use at the lowest input voltage, to confirm maximum RMS current too.

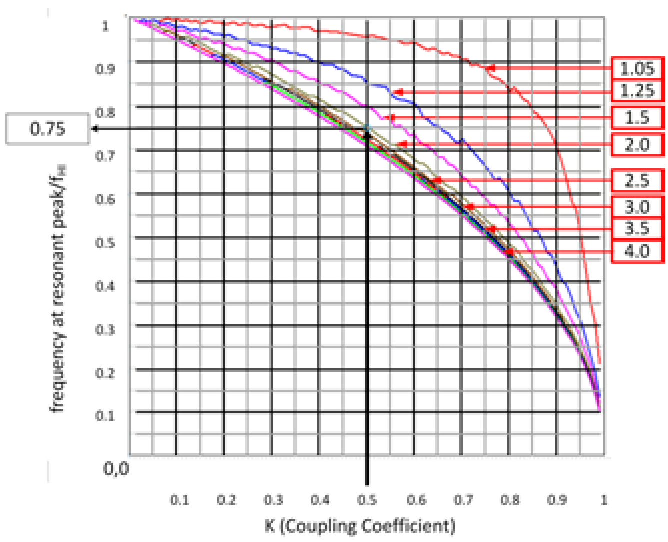


Figure 5: The location of the resonant peak

Note: There is no point doing a simulation at maximum input and f_{HI}, i.e. 145kHz to "validate" our design. That simulation point is meaningless. We will definitely get the desired output voltage because we are assuming that at least the correct turns ratio has been set in the transformer. But we also get almost any power we want really! We can keep reducing the load resistor, and we can get 1800W, or 3000W, you name it! Because looking at Figure 2, we realize that at exactly 145kHz ("f_{HI}"), we essentially have a converter that can deliver as much power as we want, assuming ideal conditions (parasitics not included, or too small to matter).

Every LC network has an inherent power capability, which in practice affects the input range we want it to handle. Knowing that fact, we can arrive at an optimal design, instead of "just make the copper as thick as possible". If a converter is inadvertently designed for more power by an incorrect choice of L-C components, then of course, if we understand basic power scaling, that has come about because we have too large a C value, and too small an L value (but far thicker copper of course). Because to double the power for example, we always halve the inductance (but not the size of the inductor though, which depends on LI^2!), and double the capacitance! Keep in mind that resonant capacitors are far more expensive than coils or windings! Overdesign will cost us money.

Think of the money already saved by removing the receiver side resonant capacitor (C_S) too!

With that we conclude this article. We have learned to scale a documented and closely modeled kernel to any power level, any frequency, and capable of being the "front-end" converter too, since it is tolerant to quantifiably wide input variations too. No overdesign either. The ability to change coupling too, to almost any desired value, means we can use it even for relatively loosely coupled wireless power transfer systems.

Interested parties can contact michael@chargedge.com for more information.

www.chargedge.com

A Game Changer for DCB Substrates Compared to AMB Substrates

A patented paste, CuB+, uses ceramic-copper composites as DCB hybrid technologies to provide enhanced electro-thermal and mechanical performance compared to standard DCB technology.

By Christian Winkler and Munsoo Han, Consultants, Global BA GmbH

DCB substrates with AMB performance – at DCB cost?
CuB+ paste can be applied as a homogeneously-oxidized copper powder to all common substrate types, including Al2O3, ZTA, AlN and Si3N4. Used this way, CuB+ increases the mechanical performance (thermal cycling) of standard DCB substrates, making it directly comparable with AMB substrates.

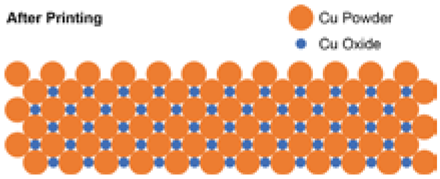


Figure 1: Shows the applied copper paste after screen printing. The paste may also be applied with other common coating techniques such as dispersion or inkjet.

As well, manufacturing cost is significantly reduced since the use of expensive AMB active solder is avoided and there is no requirement for vacuum and second etching processes.

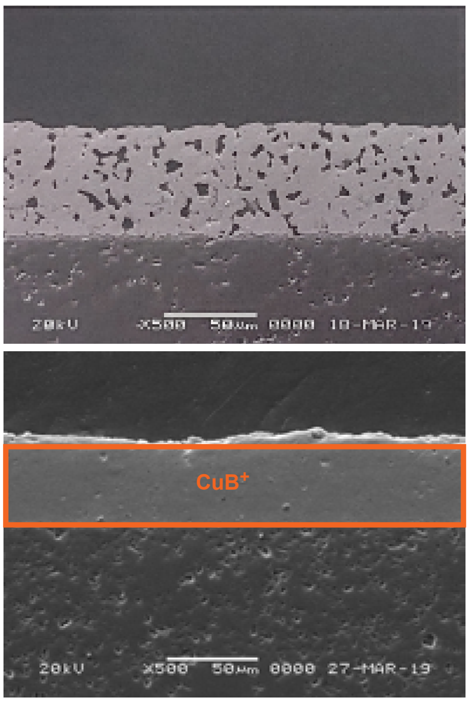


Figure 2: Conventional copper printed thick layer solution.
Figure 3: New and non-porous CuB+ connection technology.

Partial discharge-free?
The homogeneous coating and pore-free connection enable the achievement of partial discharge-free DCB substrates for high voltage over 1,7kV applications as well.

Power and logic on one device?
The freedom offered by the coating technology allows for delivery of power and logic on a substrate as a DCB hybrid solution. Hermetically- sealed through-connections for high frequency or low inductance requirements are also easy to implement.

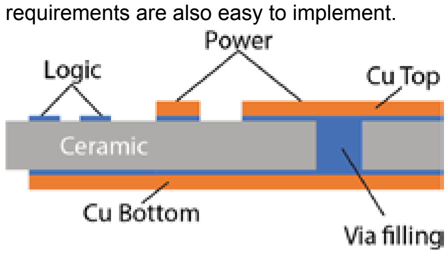


Figure 4: DCB substrate with Integrated power and logic on one device for low-cost and low-inductance power module designs with via filling.

Warpage control and hysteresis behaviour on DCBs?
The use of selective copper paste on the upper surface of the substrate can reduce warpage by reducing the bi-metal effect that arises from the relative deficiency of copper with respect to the bottom surface.

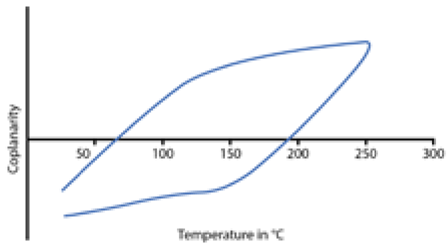


Figure 5: The warpaging behaviour during power module soldering, return ideally back to the original condition.

CuB+: a clear booster for DCB substrates and power modules
- No use of heavy metal e.g. lead, cadmium (RoHS conformant).
- High purity copper layer (> 99.0%).
- Partial discharge-free (< 10pC).
- Excellent electrical and thermal properties, equal to copper.
- Applicable to Al2O3, ZTA, AlN and Si3N4 ceramics.
- Excellent wire-bonding and soldering / sintering properties.
- A wide variety of applications.
- Lower process cost than AMB.
- Zero-void technology by DCB-bonding.
- Available for licensing or technology transfer

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A Guide to the Selection and Proper Operation of Switching Power Transistors – Part 2

With 3 materials and about 8 types of transistors to select from - although not all combinations are available - the choice of the optimum switching transistor is difficult This article is especially also written for the benefit of our young engineers.

By Dr.–Ing. Artur Seibt, Vienna

5. Drive circuits and hints for the proper operation of Si mosfets.

A general remark regarding manufacturers' Application Notes and circuit diagrams: with a few exceptions those are unfit for any series production.

Basically, the drive circuit has to charge and discharge the gate input capacitance, but this is not constant.

When switching from off to on and vice versa the transistor will cross its linear region. Due to the very high transconductance of mosfets and jfets the capacitance between drain and gate will be multiplied by a high factor. The driver will hence, while crossing the linear region, be severely loaded, this causes the gate voltage to remain on a plateau. Switching will thus be slowed down considerably unless the driver can deliver several amps. Such powerful output stages demand large, expensive chips, especially in CMOS.

Any comparisons of switching speed are meaningless unless the driver is also considered. A resistor in series with the gate is normally required, which determines the speed of turn-on. It has to be paralled by a fast diode, a 1 N 4150 (not 4148) is good enough for most medium-sized mosfets. The need for this diode is two-fold: it prevents the build-up of too high a voltage across the resistor during turn-off, and it speeds up turn-off. A driver powerful enough to deliver several amps and a low-value gate resistor minimize the switching times.

As mentioned short switching times are not only an advantage: they reduce switching losses, but they generate stronger emi, and the isolation materials in transformers etc. are subjected to higher dielecric stress. This will not always cause immediate failure, but all isolation materials have a limited life which is dependent upon the operating temperature and the dielectric stress which is given by the operating frequency and the dv/dt. At 100 KHz standard polyester foil takes only 1/10th of the voltage it takes at 50 Hz. This seldomly mentioned when fast switching is praised. See e.g. the life curves for triple-insulated wires.

5.1 Conventional drivers.

The ideal output stage is a low impedance CMOS driver which also clamps the gate at ground and Vcc. As the other circuitry of a driver is mostly bipolar, this requires a BICMOS chip. Therefore most drivers are low-cost bipolar and feature a quasi-complementary npn output stage with the disadvantage that this can neither pull to ground nor to Vcc, at best down to + 1 V and up to Vcc - 1 V. Si power mosfets have a minimum threshold of typically 2 V, some as low as 1 V, so a resistor from gate to ground is mandatory. At turn-on the upper level is less critical as long it is > 10 V. More than 12 V is unnecessary and only injects excess gate charge which has be removed at turn-off.

The leakage current can easily turn the mosfet on if the impedance to ground resp. source is too high, the maximum leakage current at the highest operating Tj is to be considered. In practice this resistor should be < 100 K, rather closer to 10 K. Another often overlooked reason: all driver ic's need a minimum Vcc before they operate, below this minimum voltage is reached, the output to the gate remains high impedance, hence the gate is open-circuit! Disregarding leakage can lead to parasitic turn-on which causes increased losses, but even destruction due to thermal runaway.

If a driver's output stage is too weak a complementary emitter follower can help, a BC 330-40/BC 327-40 is often sufficient.

5.2 A glimpse at the Miller effect and the cascode.

Both originate from analog high frequency amplifier circuitry and are known since decades; pulse circuits are just overdriven amplifiers.

Figure 5.1 shows an amplifier of any shape with the gain v and the capacitance CAE between output A and input E. It does not matter whether the amplifier consists of only one transistor or whether there are any number of stages. Also it does not matter whether it is inverting or not. In any case the capacitance between output and input sees the difference voltage v_{In} - v_{out}. This has the same effect as if there was an effective input capacitance C_{equ}. , the "Miller capacitance". Note that this effect is only present when the amplifier is energized; it can then be measured with a capacitance meter. The amplifier must be in its linear range, the effect disappears when the amplifier is overdriven, because the gain becomes zero.

Cequiv = C output to input (1 - v).

The gain v has to be entered with sign!

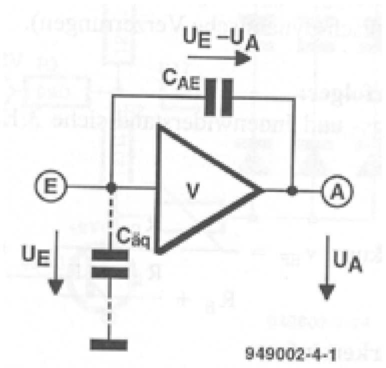


Figure 5.1: How the Miller effect comes about.

Note that C_{equiv} can be higher or lower than the actual $C_{output\ to\ input}$ depending on the sign of v! An important practical case is the emitter or source follower with the ideal v = + 1; here C_{equiv} = 0, both ends of C_{output} to input see the same signal so there is no signal current, the value of C can be any. Another way of expressing is to say that both ends of this capacitance are bootstrapped.

Any pulse circuit suffers from Miller effect because the switching device must traverse its linear region from on to off and vice versa. Mosfets feature a very high transconductance, hence the Miller effect will be pronounced. In the very moment when the transistor enters its linear range, the driver will be loaded with a considerably higher capacitance, so the input waveform will exhibit a plateau until the transistor leaves its linear range. For faster switching high drive currents are necessary which require expensive drivers. In wideband amplifier circuits the Miller effect can be compensated, this is not possible in pulse circuits. All that is possible is to minimize the external output to input capacitance, due to the tiny transistor resp. ic cases an effective shielding between input and output is hardly possible, a problem which the cascode solves. Switching times comparisons between different transistors are meaningless unless the drive circuits are also considered! Note that is is not possible to feed excessive input currents into a switching transistor because these currents must be sunk resp. generated by the transistor's output.

The cascode, known from high frequency tube amplifiers, is the ideal switch. The name is a combination of "pentode" and "cascade". It consists of two amplifying devices in series connection as shown in Figure 5.2. There is a great number of cascode circuits, any combination of tubes, bipolars, mosfets and jfets is feasible. including socalled folded cascodes; these consist of transistors of opposite polarity such that input and output can be on arbitrary potentials, also both transistors can operate with different currents. Inside amplifier ic's cascodes are standard.

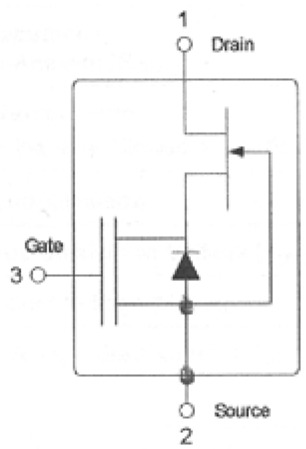


Figure. 5.2: One of a great many executions of a cascode, here a favourable combnation of a standard n-channel lv mosfet and a jfet, in particular a GaN or SiC jfet. This combination does not require an auxiliary gate voltage. The intrinsic diode of the mosfet is used in bridge circuits where the current must also flow in reverse direction. A jfet passes current in both directions. Most GaN and SiC jfets on the market appear as cascodes.

The standard cascode is a combination of a lv n-channel mosfet with the source at ground and a second one with the gate at (ac) ground. The first one feeds into the source of the seond one; it is hence the combination of a grounded-source and a grounded-gate stage.

Ideally, a transistor has infinite input and output impedances, i.e. its drain output is a current generator Ideally a transistor has infinte transconductance, this means that its input impedance at the source is zero, i.e. the source input is a virtual ac ground resp. a current sink. The ac current coming out of the lower transistor's drain enters the source and comes out of the upper one's drain. This has a series of consequences:

1. Except for the cascode type shown in Figure 5.2 cascodes require an auxiliary gate voltage supply for the upper transistor, typically + 12 V. If the lower transistor turns on, it automatically applies the 12 V between gate and source of the upper transistor.
   Note that a jfet is fully on with zero gate voltage. If the input = gate of the lower one is driven, the source of the upper one (jfet) is pulled to zero, so the voltage between gate and source becomes zero. The capacitance gate-to.source of the upper is discharged by the extremely low (milliohms) Rdson of the lower one. If the lower one is turned off, the ac source current of the upper one quickly charges the capacitance at the node lower drain-upper source until the voltage at this node reaches the pinch-off voltage of the upper one, turning it off. The voltage swing is only between zero and $V_{pimch\text{-}off}$, i.e. < 20 V, so a small lv mosfet is sufficient. In practice, a zener is required at this node limiting the voltage during switching. The additional cost for turning a single Coolmos into a cascode is minimal.
2. Due to the zero impedance of the source (as an input) there is no ac voltage at the lower's drain, hence there is no Miller effect. The input capacitance of the cascode is the lowest possible and consists only of the sum of gate-to-drain and gate-to-source capacitances. The cascode is the easiest- to- drive switch. This one reason why it so fast.
3. The connection between the lower's drain and the upper's source is uncritical because there is no ac voltage, the signal is a pure current, the capacitance to ground sees no ac voltage and does not affect the switching. Both transistors can therefore be set apart, so the critical capacitance output-to.input can be minimized in order to avoid "Miller effect all around". This would be detrimental because the gain of a cascode is the highest achievable in one stage, it is simply the product of the transconductance of the lower transistor times the load impedance of the cascode. The upper transistor sees the output impedance of the lower one in its source; this is infinite because it is a lv mosfet. So even if the upper transistor is a jfet with a fairly low output impedance the output impedance at its drain = cascode output is practically infinite. Therefore very high load impedances are possible (in amplifiers) and gains of several thousand. However, the inductance of the interconnection is critical. The board layout of a cascode is a challenge. This is a GHz circuit resp. a ns switch. Even offline voltages like 360 V can be switched in < 5 ns.
4. It is vital to realize that the (ac) grounded-gate upper stage does not amplify, but it just passes the ac drain current of the lower transistor along to its drain = output. The upper transistor can be almost any: a high fT bipolar, a standard mosfet, a Coolmos, a Si, GaN, SiC jfet, a GaN or SiC enhancement mosfet, it does not matter! This is very important to understand, because GaN and SiC manufacturers which offer cascodes try to convince customers that GaN resp. SiC cause the fast switching. In fact if a Si Coolmos is used in place of the GaN or SiC the switching speed is identical, because it is solely the merit of the lower standard Si mosfet. Why none of the Coolmos (Superjunction) manufacturers put cascodes on the market is hard to understand. The GaN resp. SiC cascodes have no advantages whatsoever in switching stages with one exception: bridge circuits where the intrinsic diode of the lower mosfet passes current in reverse direction. Both GaN and SiC have no avalanche ratings. The lower capacitances of GaN or SiC are hardly noticeable, because there are always at least 3 components at a node. In the simply case of a PFC, the contribution of the switch is much lower than that of the choke or the SiC diode.

For further details about the cascode see the article in Bodo's Power, May 2015, p. 80.

5.3 Some additional hints.

1. The susceptabiliy of ic's to current fed into their outputs varies widely; if the ic's from one manufacturer will function the same type ic from another one will be destroyed.
2. The ubiquitous cheap polyester insulation on inductive components is not really safe for offline SMPS; above 130 C it will

disintegrate. The withstanding voltage decreases sharply with the frequency; at 100 KHz polyester will only take 10 % of the voltage at 50 Hz! Higher temperatures also decrease the withstanding voltage and the life of the material. Also the triple-insulated materials like TexE consist of polyester and nylon layers. If such a transformer burns, contact between primary and secondary becomes possible. Kapton is more expensive, but it withstands 400 C and disintegrates at 800 C, it is also, next Teflon, the best dielectric we have. Hence two layers should be used as insulation between primary and secondary in offline transformers.

3. Due to their avalanche-proofness protective components in the drain of Si power mosfets are normally not necessary, however, as mentioned, continuous avalanching is not advisable, also because it generates additional losses and emi. The highest stress is in flyback circuits. For offline SMPS 800 V mosfets are not necessary, 650 V Coolmos will do. A damper circuit consisting of a fast high voltage diode such as BYV 26 E and a parallel combination of a resistor and a PP or ceramic hv capacitor should always be provided. Additional RC's in parallel with the primary and secondary windings may be necessary; the capacitors must be NPO, the resistors non-inductive. In order to keep losses low, the capacitor should be as small as possible, typically < 100 p.
4. Use only 100:1 probes with appr. 2 p and watch the ground return: best is the use of a Tektronix probe receptacle.
5. The insulation material between the transistor and the cooling surface is critical and often underestimated. The high dv/dt generates substantial dielectric currents through the insulation which not only create losses therein, but generate strong emi. Ceramic materials are best but expensive and difficult to install. The best compromise is 0.4 mm silicon rubber filled with ceramic powder (e.g. Kerafol, 86400.) Thinner material is likely to be damaged by the uneven surface and sharp edges of the transistor. Note that the Rth between the chip and the cooling surface is increased, but is seldomly specified. It is best to measure it by mounting a resistor in the same case as the transistor, e.g. TO-220, with the same material.
6. Even if there is no potential difference between transistor body and cooling surface do not expect both to be flat; at best there will be a line or point contact and thus poor heat transfer. Grease is obsolete and highly undesirable in production environments. The industry has developed interface materials which are dry at room temperature. When the transistor heats up the first time grease will ooze out and fill the gaps for optimum heat transfer.
7. If especially low emi is asked for, e.g. in medical equipment, and if thick ceramic insulators are not desired, it is possible to use a stacked insulation, i.e. first an insulator, then a copper foil and then a second insulator. The copper foil is connected to the same ground as the switching transistor. Beware of Kapton here, because its heat transfer is very poor!
8. Transistor mounting with screws or even rivets is out, the only acceptable method is the use of spring clamps which press upon the plastic body. This is the only way to uphold enough pressure over time.
9. Temperature measurements on the live drain of an active switching transistor will disturb most instruments, the high capacity of the probe can also interfere with the operation. One measures hence directly after turn-off.
10. The power dissipation can only be approximately calculated, turn-on and turn-off are complicated. The best method: One measures the case temperature directly after switching off. Then one mounts a TO-220 power resistor in place of the transistor with the identical insulation. With a power supply one heats the resistor to the same temperature the transistor had; the power required is identical to the transistor's dissipation.
11. The inverse diode is in fact the collector-base diode of the parasitic npn and quite slow; there are mosfets with faster ones. One has to be carefull when turning these diodes on during switching, this may cause destruction.

6. Si IGBTs.

One of the most commercially successful inventions was the IGBT = insulated gate bipolar transistor. It is ubiquitous.
The IGBT offered a fundamental solution to the problem of the loss increase with the square of the current with mosfets. It is a bipolar transistor driven by a mosfet; as such it can simply mobilize more charge carriers, i.e. electrons as well as holes. The voltage across it only increases very little with the current. This feature and the low cost explain the enormous economic importance of the IGBT: almost all drive electronics in the transportation business rely on IGBTs. Hv bipolars suffer from very low current gain, this problem is remedied by the mosfet input. However, during turn-off, the bipolar is left with open base, a horror to every experienced design engineer. Turn-off is hence slow, so the IGBT suffers from high losses during turn-off. This is why it is confined to low frequency operation with offensive audible noise from traction vehicles. Meanwhile there are appr. 7 generations of IGBT's on the market which also allow supersonic operation.
Only lately SiC transistors started to replace IGBTs due to their much higher operating frequency, low Rdson's and also higher operating Tj's. Their disadvantage is higher cost.

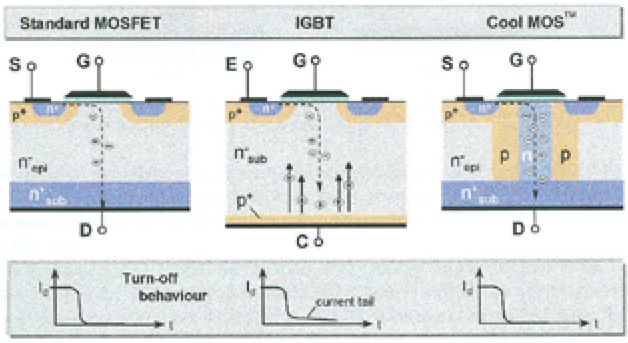


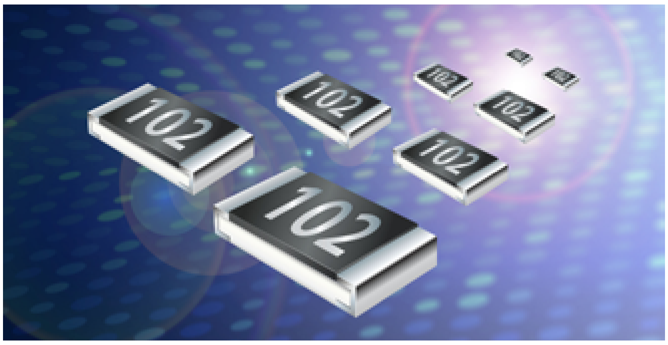
Figure 6.1: Differences between the two mosfets and an IGBT. Note the tail current.

Figure 6.1 shows the differences between the mosfets and the IGBT. The backside p layer (pnp collector, with IGBTs called "emitter") injects additional charge carriers. These charge carriers are in balance with the electrons in the channel, hence a much greater concentration of charge carriers is created as that caused by the doping, hence the conductivity of the drift zone is increased. But during turn-off these additional charge carriers have to be removed from the drift zone which causes the long "tail" of the current.
Operating frequencies remained mostly in the KHz range. The saturation voltage Vsat can not be appreciably decreased and also the losses while the Rdson of SiC mosfets reaches milliohm regions.
A major advantage of the IGBT is its low cost because it remains a bipolar transistor. Note that the main difference to a standard mosfet is the additional bottom p layer.
There are two families of IGBT's: PT = puch-through and NPT = non punch-through. The difference lies in the form of the electric field. In the NPT the field does not reach into the backside emitter, the wafers are inexpensive with one doping.
SiC mosfets will always remain more expensive, but their use allows savings otherwise, e.g. in the passive components. In the long run they will replace IGBTs.

... to be continued in July 2020

AEC-Q200 Compliant Thick Film Resistor Series

Bourns announced the availability of an AEC-Q200 compliant series of thick film chip resistors, the Model CRxxxxA series in eight compact form factors—from small 0201 (0603 Metric) up to 2512 (6431 Metric). The CRxxxxA series is part of the Bourns® CR line of general-purpose thick film chip resistors. Bourns designed this family of devices



in five different versions to support specific application requirements: CR standard, CR-PF ultra-low lead content, CR-AS sulfur resistant, CRxxxxA-AS AEC-Q200 compliant and sulfur resistant and CRxxxxA AEC-Q200 compliant.

The CRxxxxA series features rated power from 0.05 to 1 watt and a wide resistance range from 1 ohm up to 20 megohms. These features make this series an optimal circuit conditioning solution for a broad range of consumer, industrial, telecom and other applications. Bourns manufactures its latest resistors using a thick film element that is printed onto a ceramic substrate. This type of advanced ceramic substrate offers excellent heat dissipation. The resistive element is coated by an epoxy overcoat layer, which isolates the resistive element electrically to help protect it against mechanical damages and environmental effects such as humidity and gasses. Available now, Bourns® Model CRxxxxA series is RoHS compliant and halogen free.

www.bourns.com

Type-C Power Delivery 2-in-1 Combo Protection Switch

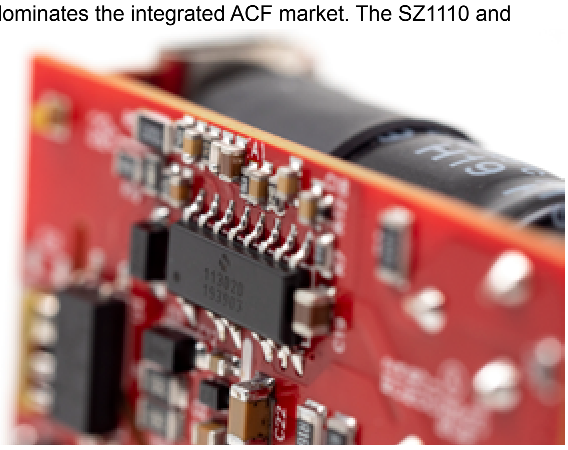
Alpha and Omega Semiconductor announced a Type-C Power Delivery compliant 2-in-1 combo protection switch capable up to 28V absolute maximum voltage. The AOZ1380 is a smart protection switch combining both current source and sink function into a single small thermally enhanced 3mm x 5.2mm DFN package. Made possible by AOS' advanced copackaging technology, AOZ1380 combines a high-performance IC with protection features and AOS' stateofthe-art high SOA MOSFET. This device provides true reverse current blocking intended for applications where protection from exposure to high voltages is required. The AOZ1380 provides an ideal solution for the

latest notebooks, ultrabooks, Chromebooks, and docking stations, with Thunderbolt/USB Type-C PD ports. In the sinking application, two discrete back to back MOSFETs along with resistors and capacitors provide soft start functionality to prevent Type C power adaptor brownout at the plugin. However, programmability and protection features such as reverse-current blocking and over-voltage and over-temperature protection are lacking in this implementation. As a Type C port must also provide power delivery of up to 15W in a notebook application, there's also a need for a 5V current limited load switch with protection features. The AOZ1380 provides all this functionality and reduces board footprint by over 50% compared to competing solutions.

www.aosmd.com

Flyback PWM Controllers with Integrated Active Clamp Circuits

Silanna Semiconductor announced the launch of an expanded portfolio of Active Clamp Flyback (ACF) Controllers. Silanna Semiconductor focuses on the ultimate Power Management challenges with best-in-class power density and efficiency that delight customers with unprecedented BoM savings. First announced at APEC 2019, Silanna Semiconductor has delivered on the customer expectations and market penetration of Active Clamp Flyback Controllers and now dominates the integrated ACF market. The SZ1110 and



SZ1130 devices are Active Clamp Flyback PWM Controllers that integrate an adaptive digital PWM controller and the following Ultra High-Voltage (UHV) components: an Active Clamp FET, Active Clamp Gate Driver and a Startup Regulator. This unprecedented level of integration facilitates designing efficient, high-power-density adapters with low BoM cost to satisfy power-hungry mobile phones, tablets, notebooks and video game consoles. Customers can see demonstrations of the ACF controllers, delivering over 94% efficiency with an all-silicon design and 27 W/in3 power density at 65W for AC/DC power adapters together with the extensive DC/DC and AC/DC products at the demo room in https://www.powerdensity.com/sz1110-sz1130.

"Less than a year ago we launched the SZ1101, the world's first Active Clamp Flyback Controller, to an incredible customer and industry response," said Mark Drucker, CEO of Silanna Semiconductor. "This expansion into higher power and smaller form factors speaks to our core power density leadership. Silanna Semiconductor delivers AC/DC solutions with the highest Power Density and Efficiency while simultaneously delivering the greatest value and reduced BoM costs."

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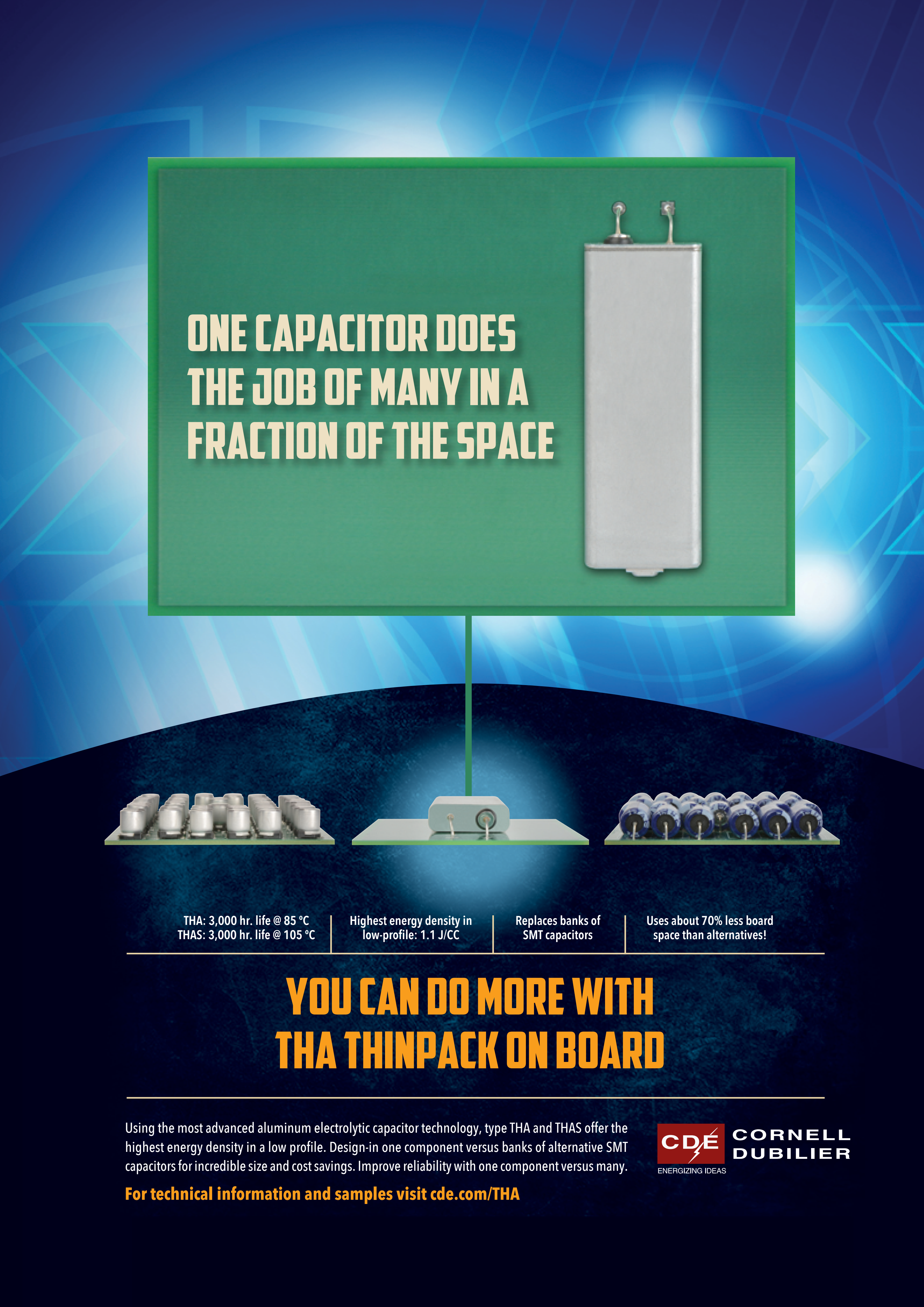
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EMC Line Filters

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