

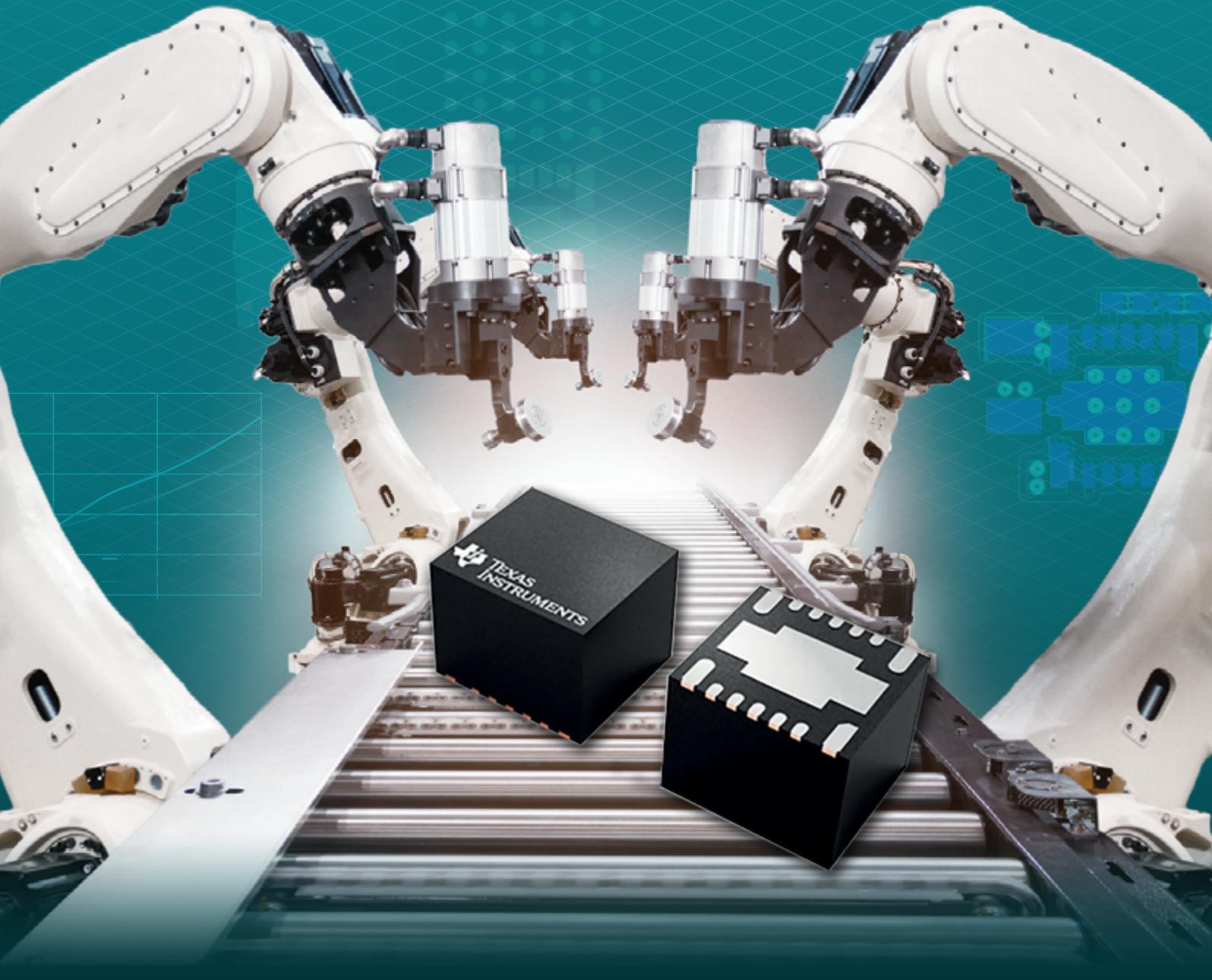
Bodo's Power Systems®

Electronics in Motion and Conversion

September 2020

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Enhanced HotRod™ QFN package helps shrink power supply footprint by 30% and improve thermal performance.





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CONTENT

Viewpoint	4
Information on Demand	
Events	4
News	6-10
Product of the Month	12
Bonding Ribbon for the Next Generation of Power Electronics	
Green Product of the Month	14
Reduce Space and Increase Efficiency with the N-series 1200V SiC-MOSFET	
Blue Product of the Month	16
Win a MPLAB PICKit 4 In-Circuit Debugger	
Cover Story	18-21
Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology	
<i>By Denislav Petkov, Systems and Applications Manager, Texas Instruments</i>	
Wide Bandgap	22-24
Testing Gallium Nitride Devices to Failure Under Extreme Voltage and Current Stress	
<i>By Alex Lidow Ph.D., CEO and Co-founder, Efficient Power Conversion</i>	
Power Modules	26-28
Hard Paralleling SiC MOSFET Based Power Modules	
<i>By Andre Lenze, David Levett, Ziqing Zheng and Krzysztof Mainka, Infineon Technologies</i>	
IGBTs	30-33
The Switch to More Efficient Induction Heating Designs	
<i>By Georges Tchouangue, Chief Engineer Power Semiconductor, Toshiba Electronics Europe GmbH and Kazuhiro Goda, Expert, Toshiba Electronic Devices & Storage, Kawasaki, Japan.</i>	
Renewable Energy	34-35
The Difference that DC Makes	
<i>By Andreas Berthou, Global Head of HVDC of Grid Integration business, Hitachi ABB Power Grids</i>	
Wide Bandgap	36-39
Advantages of 100V GaN in 48V Applications	
<i>By Lei Kou, Power Electronics Applications Engineer, and Juncheng (Lucas) Lu, Applications Engineering Manager, GaN Systems</i>	

EMC	40-43
Optimizing EMI Input Filters for Switched Mode Power Supplies	
<i>By Marcus Sonst, Application Development at Rohde & Schwarz in Munich</i>	
Measurement	44-47
Lineup of Modern Clamping Systems for Tests of Power Semiconductor Devices with Force up to 150 kN	
<i>By Alymov D., Gorodnichina A., Semenov P., Sytyi A., Kazarov A. and Verkhovets V., Proton-Electrotex</i>	
Thermal Management	48-50
Piece of Metal or Highly Innovative Product?	
How 3D Printed Liquid Cooled Heatsinks Brings Innovation Into a Stale Industry	
<i>By Dr. Thomas Ebert, CEO, IQ Evolution, Christopher Rocneanu, CEO, Foxy Power</i>	
Power Supply	52-54
Bipolar, Single Output, and Adjustable Power Supplies Based on the Common Buck Converter	
<i>By Victor Khasiev, Senior Application Engineer, Analog Devices</i>	
Technology	56-57
Preserved Echoes Diagnose Component Failures	
<i>By Tom Adams, consultant, Nordson SONOSCAN</i>	
Design and Simulation	58-59
Universally Accessible Education in Power Electronics	
<i>By Dr. Shivkumar V. Iyer, Python Power Electronics</i>	
New Products	60-64

OHM CONFINEMENT

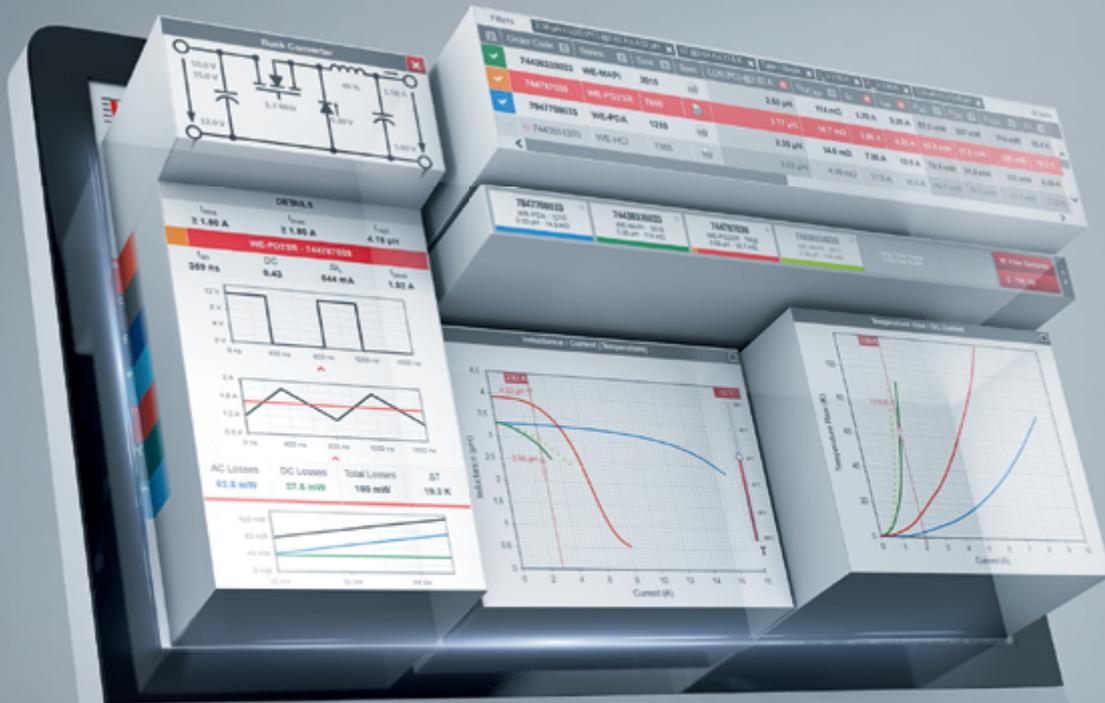
CEO RETURNS



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The Gallery





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Free Subscription to qualified readers

Bodo's Power Systems
is available for the following
subscription charges:

Annual charge (12 issues)
is 150 € world wide

Single issue is 18 €
subscription@bodospower.com



Printing by:

Brühlsche Universitätsdruckerei GmbH
& Co KG; 35396 Gießen, Germany

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www.bodospower.com

Information on Demand

August brought us a period of sunny weather, and once again we were lucky to relax at the Baltic Sea and enjoy all of the fun activities that it offers. This year, more than ever, taking a vacation in your home country is extremely popular. We experienced packed beaches and traffic jams up to the horizon. The authorities here in northern Germany shut down some roads, as beach capacities reached their limit. Also, in some areas even the drinking fountains moved to a critical level. A wise person gave me some advice - which nearly made it to a Green Power Tip. She said "Stop watering the lawn. It's like a weed - it will always come back".

Travelling, for business or leisure should still be limited as much as possible. It is the right decision that many events are changing their format to digital, as we have done with our annual Power Conference in December. The event will now be held online on December 8th and 9th. The topics will cover Wide Bandgap Semiconductors (SiC and GaN), Passives, and Test/Measurement. Invitations have already been sent to prospective speakers. If, for any reason, you have not heard from us, just reach out to your existing contact and we will be happy to share information. It will be a shame to miss Bavaria in the pre-Christmas season - but let's hope for a better 2021!

Our successful podium at the PCIM digital days demonstrated that it is possible to share information this way. The tools and apps are getting better and, if you are in a stable network, video sessions are the modern way of collaborating. If you missed the event, you can find all of the presentations on our website within the Wide Bandgap section. During these times, on-demand content is the preferred way of "sitting in" at a conference.

Without travel, there is this problem called time shift. It is simply not possible to find one time which is convenient to everyone:



whether you are in Europe, USA or Asia. Nobody wants to spend hours in front of a screen - that is why our magazine and website provides on-demand-information that is narrowed down to individual topics significant to the reader. For all of these reasons, we will continue to make all of our content available online - at your demand! By the way, the magazine has been offering this for more than 14 years already.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving North America efficiently. If you are using any kind of tablet or smart phone, you will find all our content optimized for mobile devices on the updated website www.bodospower.com. If you speak the language, or just want to have a look, don't miss our Chinese version: www.bodospowerchina.com

My Green Power Tip for the Month:

If you're working from home, take advantage of our offer to send your print copy to your home address and help us to save paper by not sending the magazines to Nirvana. Of course, you can change back to your office later. Just e-mail us and we'll take care of it.

Best regards

Events

EU PVSEC 2020

Online September 7-11
www.photovoltaiac-conference.com

EPE 2020

Online September 7-11
www.epe2020.com

ISPSD 2020

Online September 13-18
www.ispsd2020.com

EDI CON ONLINE 2020

Online October 6, 13, 20, 27
www.edicononline.com

ECCE 2020

Online October 11-15
www.ieee-ecce.org

EV Tech Expo 2020

Online October 14-16
www.evtechexpo.com

GPECOM 2020

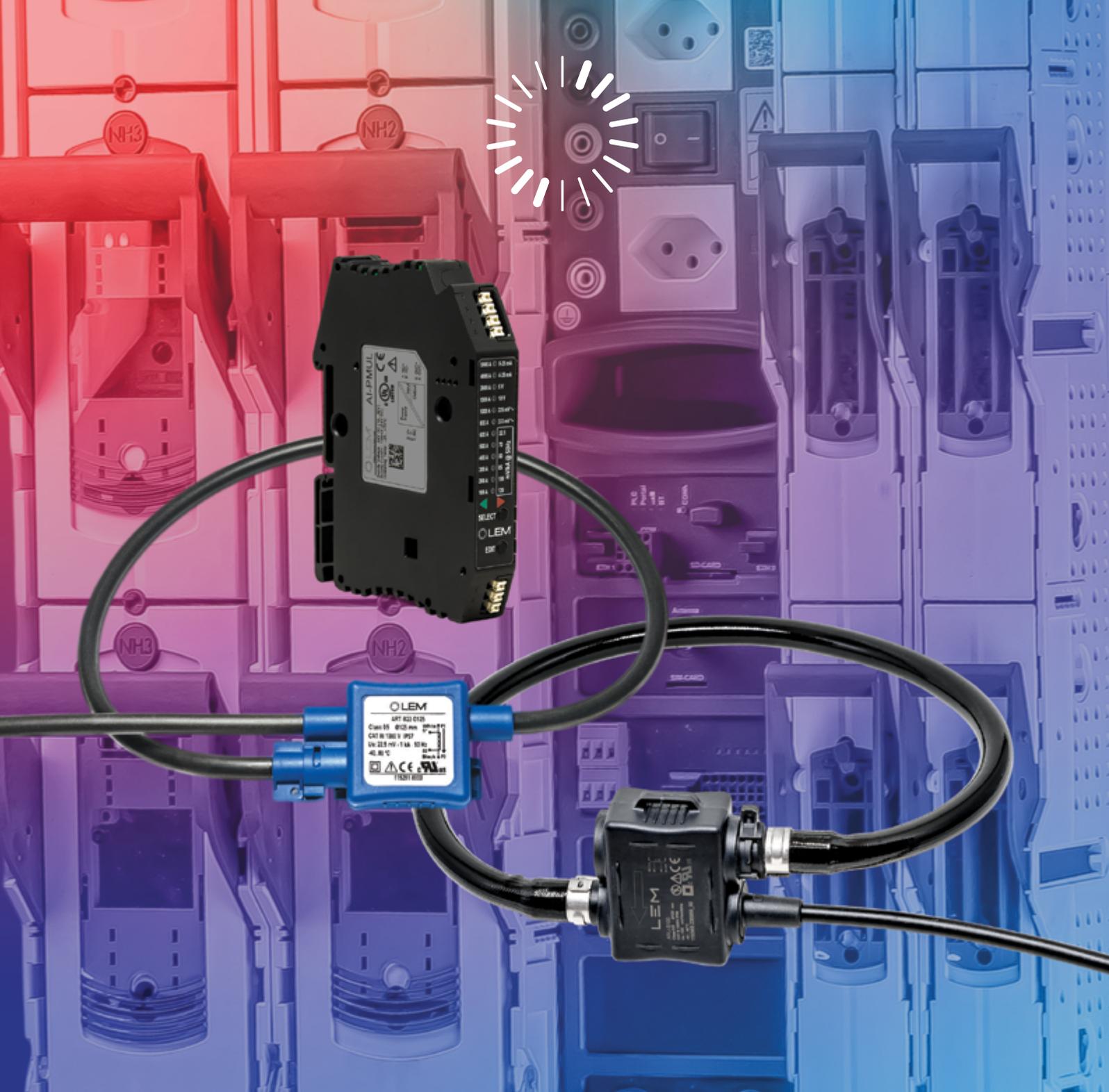
Online October 20-23
www.gpecom.org/2020

Electronica 2020

Munich, Germany November 10-13
www.electronica.de

PCIM Asia 2020

Shanghai, China November 16-18
www.pcimasia-expo.com



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CEO Transition Announced



Vincotech announced that its Board of Directors has appointed Eckart Seitter, Senior Vice President of Sales and Marketing, as Vincotech's Chief Executive Officer (CEO) and Chairman of the Board effective October 1, 2020. Eckart Seitter will succeed Vincotech's CEO and Chairman of the Board Joachim Fietz, who will retire from the company and board after 12 successful years as CEO. This smooth CEO transition demonstrates the long-term continuity of the company as a

reliable and trusted partner for its global customers, counting on Eckart Seitter's tremendous business and leadership skills, his strategic

insight and his customer-focused mentality. Eckart Seitter has been with the company for more than 20 years. He became Managing Director Sales and Marketing in 2013, and thus has made a strong contribution to Vincotech's development and success. "Joachim Fietz set exceptionally high standards of achievement during his leadership for more than a decade, and I am very much looking forward to this new challenge to follow him, and to working together with the management team," said Eckart Seitter. "Together, we want to set the course for our further global growth. Our goal is to continue the development of Vincotech, a strong brand within Mitsubishi Electric Corporation, and to sustainably fulfil our primary obligation to serve customer needs quickly and flexibly".

www.vincotech.com

Bringing Disruptive Power Electronics to the Road Track and the Skies

GaN Systems and BrightLoop Converters announced their strategic partnership to develop the latest AC/DC and DC/DC Converter products for electric motorsport and aerospace applications. Leveraging GaN Systems' 650V GaN transistors, BrightLoop produces a range of converters that are smaller, lighter, and more efficient than currently available in the market.

GaN is a key component for applications in industries requiring high power performance and reliability. BrightLoop's most recent family of DCDC converters, including the 1.9 kW, 4.8 kW, and 9.6 kW DCDC converters designed for hybrid and electric racing, incorporates GaN Systems transistors and are around half the size and weight of the company's first generation DCDC converter developed without GaN. BrightLoop continues to make advancements using GaN to



produce lighter and more compact converters.

BrightLoop's DCDC converters are now used in many of the Formula E teams and the winning team from 2019. The converter's function is to power all the low-voltage electronics including pumps, lighting, and radio. Most recently, the World Sporting Consulting (WSC) Group, the premier motorsport event and racing promotion organization overseeing Touring Car Racing (TCR) and ETCR (Electric Touring Car Racing) brands, announced BrightLoop as the sole supplier of DCDC converters for ETCR cars. ETCR is the world's first electric touring car championship, which will begin this summer 2020.

www.gan-systems.com

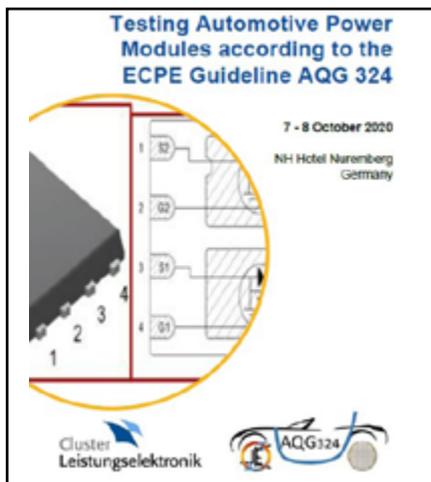
www.brightloop.fr

Tutorial on Testing Automotive Power Modules

The ECPE Guideline AQQ 324 is prepared and released by the ECPE Working Group 'Automotive Power Module Qualification' comprising ECPE member companies from the automotive supply chain. The original version is based on the supply specification LV 324 which has been developed by German automotive OEMs together with representatives from the power electronics supplier industry.

The described tests concern the module design as well as the qualification of devices on module level (i.e. the assembly) but not the qualification of semiconductor chips or manufacturing processes. The requirements, test conditions and tests presented in the tutorial essentially refer to power modules based on Si power semiconductors while wide bandgap power semiconductors (e.g. SiC or GaN) are addressed but not yet fully covered by the Guideline.

The Tutorial, 7 - 8 October 2020 in Nuremberg, Germany, with speakers from the AQQ 324 Core Team will give practical information and advice how to test power modules



according to the AQQ 324 Guideline under comparable conditions. It aims at direct users from beginners to senior experts coming from power module suppliers, automotive tier 1 suppliers or test service and equipment providers.

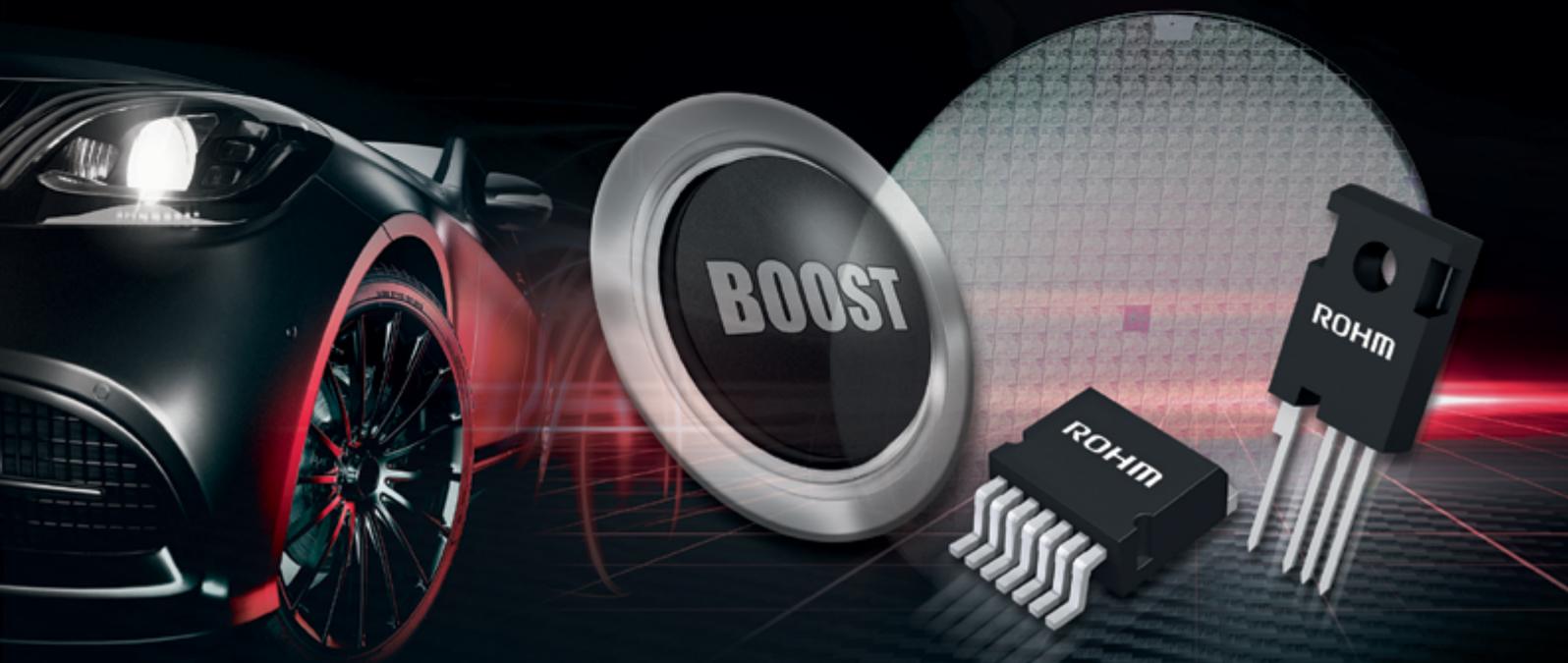
Course Instructors:

- Peter Dietrich, Richardson RFPD Germany
- Steffen Ewald, Fuji Electric Europe
- Dr. Gabor Farkas, Mentor Graphics
- Frank Heidemann, Mathias Gebhardt, SET
- Dr. Martin Rittner, Robert Bosch
- Stefan Schmitt, Semikron Elektronik
- Prof. Dr. Markus Thoben, Fachhochschule Dortmund

All presentations and discussions will be in English.

www.ecpe.org

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Established, experienced, evolved: As a technology leader ROHM is shaping the power solutions of the future. Our advanced SiC technology boosts the performance of automotive power systems. We produce SiC components in-house in a vertically integrated manufacturing system and thus guarantee the highest quality and constant supply of the market. Take the next development step with our latest SiC solutions.

SMALLER inverter designs
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STRONGER performance
by higher power densities

FASTER charging
and efficient power conversion



AUTOMOTIVE



INDUSTRIAL

www.rohm.com

Positive Outlook for SPS 2020

The Bavarian Government has approved the protection and hygiene concept for exhibitions in Bavaria signaling the go-ahead for the SPS 2020 in Nuremberg from 24 - 26 November 2020. In addition to numerous national exhibitors, many international exhibitors have also confirmed their attendance and are looking forward to the exhibition season with eager anticipation. The exhibition area and confirmed number of exhibitors to date are only slightly down on the same period last year despite the corona pandemic. This underlines the exhibition's importance for the industry. "The importance of exhibitions to the economy is akin to that of automation for industry – one of the most important drivers. SPS is a fixed date on the calendars of automation companies and we are all very much looking forward to meeting up in Nuremberg in person at the end of the year," sums up Sylke Schulz-Metzner, Vice President SPS of Mesago Messe Frankfurt.

For the event organizer Mesago, the well-being of all attendees of SPS 2020 is paramount. Together with NürnbergMesse, it has therefore developed a concept covering all the necessary organizational, hygiene, and medical aspects. The entire exhibition has been organized to accommodate observance of the minimum social

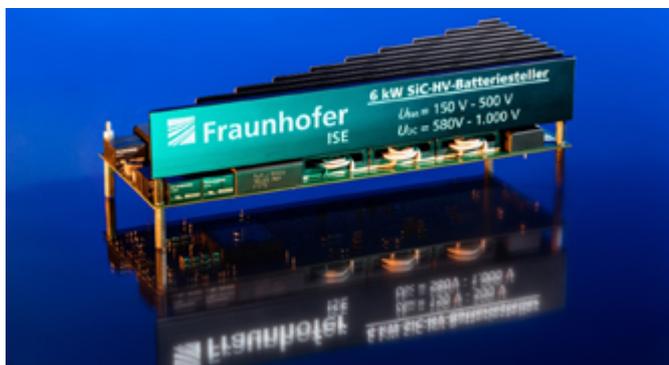


distancing requirement of 1.5 m at all times. In addition, a mandatory face covering requirement has been introduced for anyone inside the building plus amendments to the catering concept and the provision of sufficient space in the hall entrances and waiting areas. There will be no ticket sales on site, visitors must register in advance via the ticket shop.

www.sps.mesago.com

Silicon Carbide Transistors Improve Efficiency in Home Storage Systems

A major challenge of PV home storage is that the batteries are charged within a few hours in intense sunlight and then discharged at very low power, or partial load, over a long time period during the night. Because of this, battery inverters in home storage systems should have high conversion efficiency over the largest power range



possible. In the HyBaG project, which started in 2017, the Fraunhofer Institute for Solar Energy Systems ISE in collaboration with Kaco New Energy and STS - Spezial-Transformatoren Stockach has developed a low-loss hybrid inverter which functions efficiently even at partial load. A central component of Fraunhofer ISE's work in the project was to develop compact and modular battery controllers. This could be achieved by using novel gallium nitride (GaN) and silicon carbide (SiC) power components. These modern transistor bridge circuits are the core of modern battery chargers and enable increasingly faster switching with lower losses. In the project, various approaches to optimize the partial load efficiency were examined by simulation. Prototypes were then constructed using the best resulting concepts. Both the hardware as well as the control software for the power electronics were optimized. Different circuitry topologies were investigated and their partial load efficiencies were evaluated at low power levels.

www.ise.fraunhofer.de

Customer Sales Support Team Expanded



Silanna Semiconductor announced the appointment of Larry Wasylin as Vice President of Worldwide Sales. Mark Drucker, Chief Executive Officer (CEO), Silanna Semiconductor: "Larry is a proven senior-level executive with extensive customer-facing and cross-functional experience. He brings a valuable combination of sales and business insight to his new role, and is well-equipped to help us grow our business at a rate that outpaces the market." In his new position, Mr. Wasylin will be based in Taiwan to have close access to Silanna Semiconductors' customer base throughout Asia. Larry will lead the company's Sales, Distribution, Field Applications Engineering and Customer Applications Engineering team in the Philippines. All these functions directly support Silanna Semiconductor's customers worldwide. Armed with a growing portfolio of power semiconductor solutions with best-in-class power efficiency and density, the company expects he and his teams to ag-

gressively grow the business and expand market share. The company is also looking to Mr. Wasylin to increase the total value proposition of Silanna Semiconductor by leveraging the technical expertise of the company's power design tools and Field Application Engineering (FAE) teams, and capitalizing on the expansion of the company's progressive supply chain programs.

"I'm delighted to expand my role with Silanna Semiconductor. Being based in Taipei, Taiwan I feel I am perfectly situated to support our customer growth with the support of our Asian field and applications teams. During my time with Mobiverse I supported Silanna Semiconductor's Asian sales teams, witnessing first-hand the Silanna Semiconductor global management team's determination to solve the toughest power management challenges. Delivering both DC/DC and AC/DC solutions with the highest Power Density and Efficiency while simultaneously delivering the greatest value and reduced BoM costs." Said Mr. Wasylin.

www.powerdensity.com

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High Voltage IGBT

Full SiC 3.3kV Power Module in nHPD²

nHPD²



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Automotive

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- Low Inductance
- Segmented Film
- Custom Design
- AEC-Q200

info@muecap.de

www.muecap.de

Representative for the Midwest

Sanan Integrated Circuit (Sanan IC) has signed manufacturers' representative firm JF Kilfoil to oversee the company's portfolio of power electronics and optical foundry services for the Michigan, Ohio, Kentucky, Indiana, Pennsylvania and West Virginia territories.



Founded in 1953, JF Kilfoil has successfully positioned itself as the Midwest's most reliable source for semiconductors, electro-mechanical components, connectors and printed circuit boards from market leading suppliers. The firm boasts a customer base spanning automotive, white goods, contract manufacturing, and test and measurement. JF Kilfoil will oversee Sanan IC's GaN and SiC wide bandgap power electronics for automotive and home appliance markets, as well as its optical chip technologies for automotive LiDAR. For inquiries, contact Tim Kilfoil at tmkilfoil@jfkilfoil.com.

www.sanan-ic.com

Dirk Knorr and Josef Wörner Take Over Management

Dirk Knorr and Josef Wörner have been appointed as General Managers for the German business of the Würth Elektronik eiSos GmbH & Co. KG, having been a part of the management circle of the company for years. Dirk Knorr, a graduate industrial engineer and trained industrial electronics technician, was recently head of international quality and environmental management at Würth Elektronik. The 44-year-old was also responsible for risk management and material compliance. Before joining Würth Elektronik in 2005, he worked as a project manager for key accounts at a company for system solutions in the electronics industry.

Josef Wörner (51) started his training as a telecommunications engineer at Deutsche Bundespost and made his career in sales at a German manufacturer of passive components. Since 2001, he has held various positions at Würth Elektronik eiSos, including the title of Director responsible for the Electrome-



chanics Division since 2017. He will continue to be responsible for this division.

Both will remain as General Managers of the German Würth Elektronik eiSos, but as part of their functions on the Management Board, they will devote more time to the management and strategic orientation of the entire Würth Elektronik eiSos Group, which includes a continuously growing number of companies and production sites all over the world.

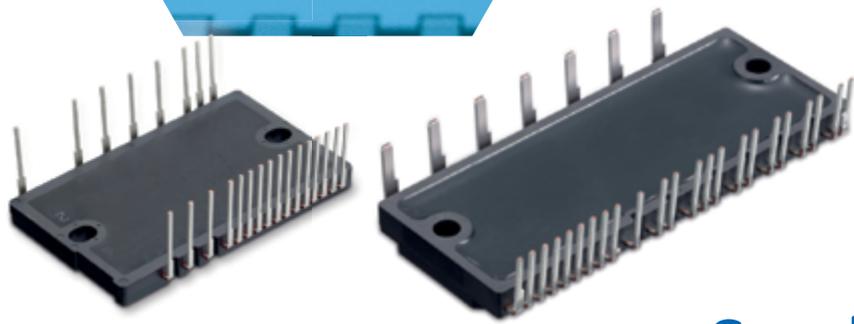
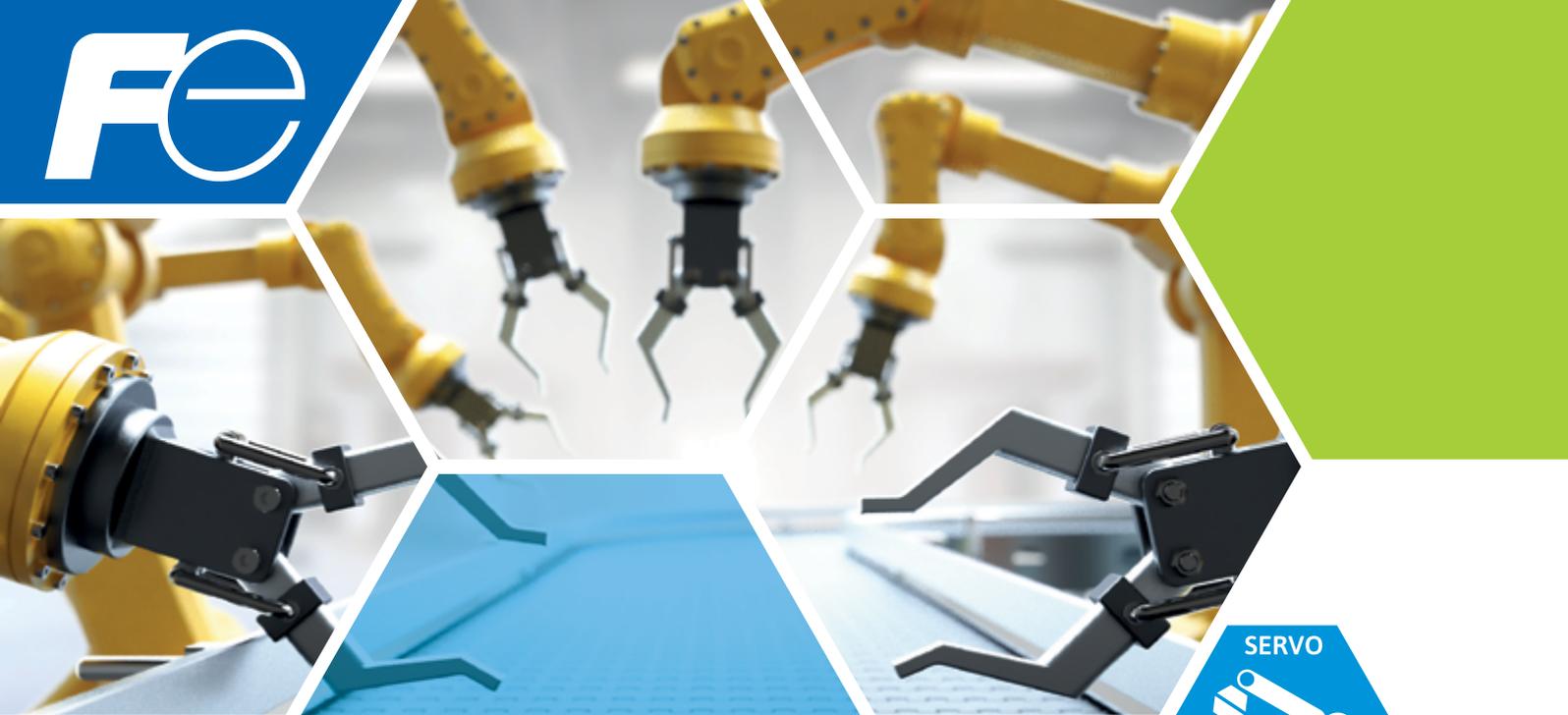
www.we-online.com

Joining Forces

Foxy Power GmbH, a Berlin based company focused on strategy, business development, and sales for innovative and disruptive technologies in power electronics, and Electronic Minds LTD have signed a cooperation agreement. "With our product value maximization concept we can also provide manufacturers valuable market information and customer feedback", says Christopher Rocneanu, CEO and Founder of Foxy Power, "now with the support of Electronic Minds we can additionally offer in-depth application support and technical insights into all stages of the product life cycle".

"Foxy Powers focus on disruptive technologies in power electronics fits very well with our proven experience in providing high performance solutions in eMobility and energy applications utilizing wide bandgap semiconductors and real time digital control" adds Dr. Iain Mosely, CEO and Founder, "this new partnership will provide a complete solution for new market players and startups." Interested customers can send requests to sales@foxypower.com or call +4915121063411.

sales@foxypower.com

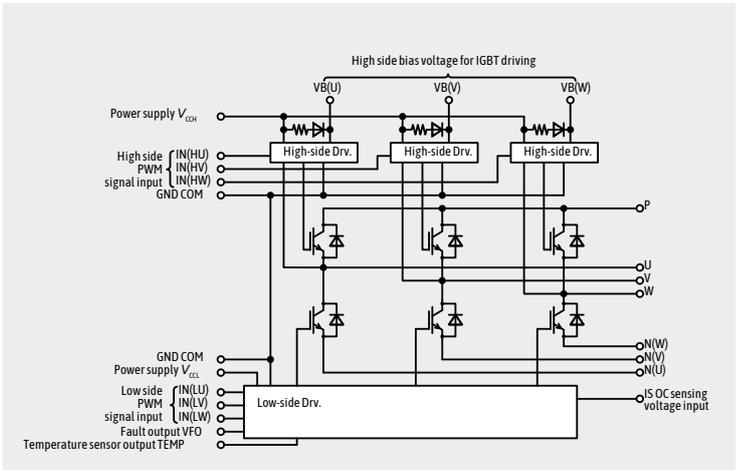


Small-IPM Series

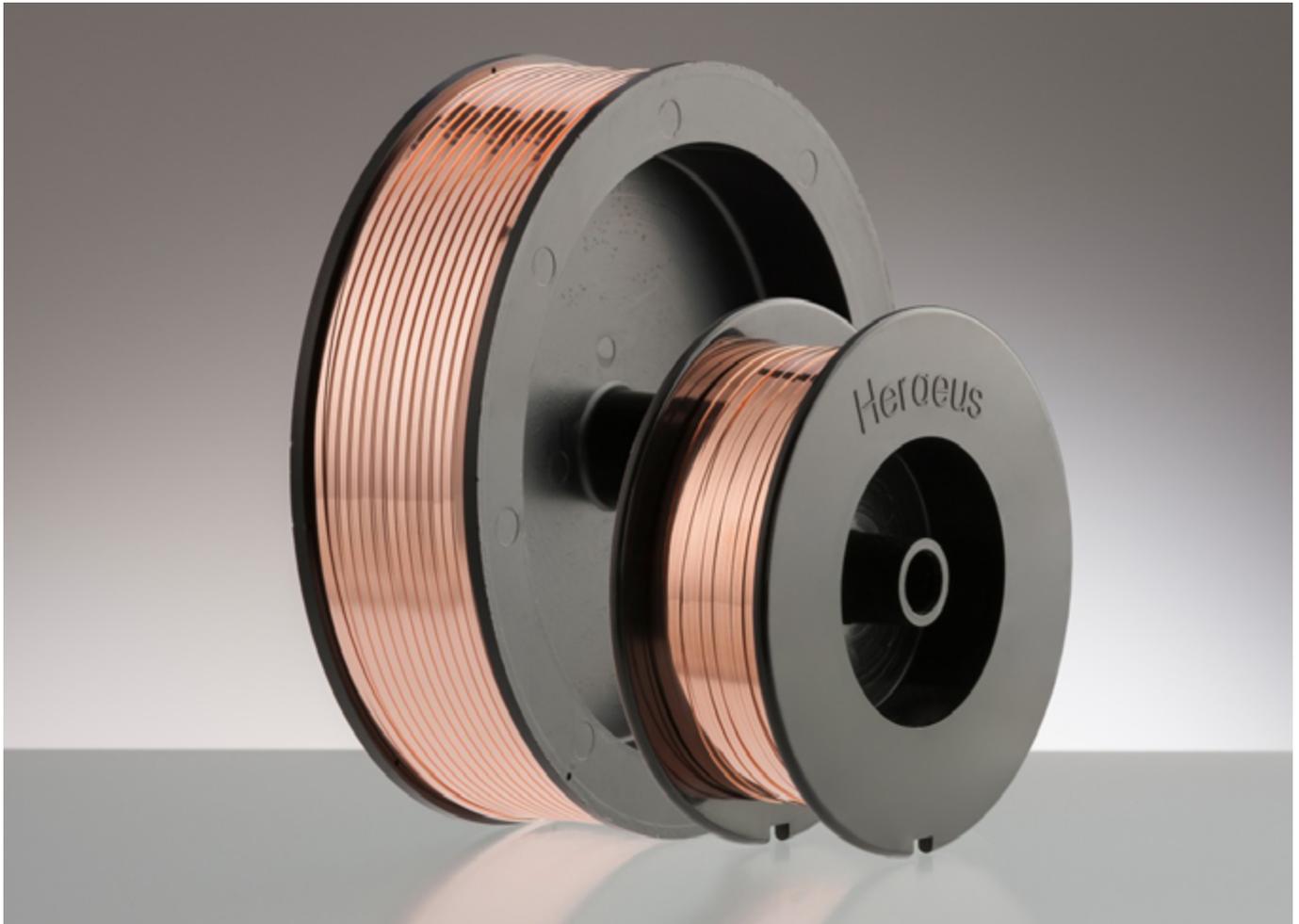
3 Phase IGBT inverter bridge with drive and protection functions

MAIN FEATURES

- ▶ Built-in gate driver IC – optimal driving condition
- ▶ Overheating protection or temperature output function
- ▶ Short circuit and under voltage protection
- ▶ Fault signal output
- ▶ Very low internal impedance
- ▶ $T_{vj,max} = 175\text{ }^{\circ}\text{C}$
- ▶ UL1557 certified



Bonding Ribbon for the Next Generation of Power Electronics



Heraeus Electronics announced the expansion of the PowerCuSoft product family with a copper bonding ribbon. The product enables power modules to be designed and manufactured more reliably, efficiently and cost-effectively.

PowerCuSoft Ribbon is optimized for surface contacting on wide bandgap semiconductors based on silicon carbide (SiC). With this bonding ribbon generation, it is possible to use the full potential of new SiC chips, optimally.

Copper offers better thermal, electrical and mechanical properties compared to aluminum wire and ribbons. The material heats up less than aluminum and can withstand higher module temperatures – this improves the lifespan and reliability of power modules. PowerCuSoft Ribbon can withstand module temperatures of up to 250 °C. In tests, copper ribbons show a ten to twenty times longer service life than comparable products made of aluminum, while at the same time increasing the energy density in the module.

"SiC semiconductors are in the fast lane due to their high power density," says Christian Kersting, Product Manager Power bonding wires at Heraeus Electronics. "In order to be able to use the advantages of these products, module manufacturers need high-performance packaging and interconnection technologies."

Compared to copper wires, ribbons also offer cost advantages, as one ribbon replaces several copper wires. Manufacturers are thus able to optimize the manufacturing costs per module as output increases. Depending on the module design, even twice the number of modules per hour can be produced.

www.heraeus.com



RT BOX 1:
THE ORIGINAL

RT BOX 2:
MULTI-CORE

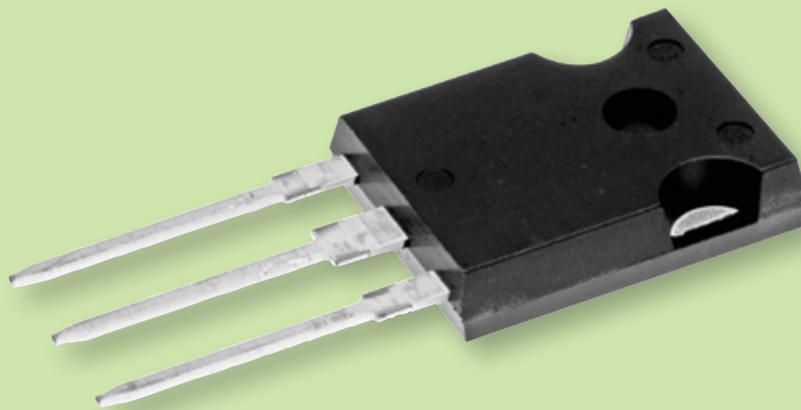
RT BOX 3:
HIGH I/O COUNT

THE REAL-TIME FAMILY HAS GROWN

Building blocks for HIL simulation
and rapid control prototyping

Find specs and pricing at www.plexim.com

Reduce Space and Increase Efficiency with the N-series 1200V SiC-MOSFET



In recent years, SiC power semiconductors have drawn increasing attention to their potential from the point of view of energy saving and environmental protection due to the significant reduction of power losses. Since the commercialization of its first power module with Silicon Carbide Schottky Diode (SiC-SBD) and SiC-MOSFET in 2010, Mitsubishi Electric has continuously contributed to the size reduction and energy efficiency of inverters for household appliances, industrial plants and railway drives. With the addition of the new N-series SiC-MOSFETs in a TO-247 package (under development) to the product portfolio in the near future, the company also covers applications that require high blocking voltages like on-board chargers and solar inverters.

Mitsubishi Electric's doping of the JFET area in the MOSFET channel reduces both switching losses and forward resistance, achieving an industry-leading¹ "Figure of Merit" (FOM) of 1450 mΩ·nC. The power dissipation in power supply systems is reduced by approximately 85% compared to conventional Si-IGBTs. By simultaneously reducing the Miller capacitance, the robustness against parasitic turn-on is improved by a factor of 14 compared to comparable products.

This allows a fast switching process to be realized, which contributes to the reduction of switching losses. The reduced switching losses allow for a reduction and simplification of cooling systems as well as the reduction of peripheral components such as magnetic components. The reason for this is the higher switching frequency that can be achieved. By using the new N-series SiC-MOSFETs, the cost and size of the entire power supply system can thus be reduced.

The product portfolio is divided into three ratings ($R_{DSon} = 22\text{ m}\Omega$, $40\text{ m}\Omega$, $80\text{ m}\Omega$) in the TO-247-3 package, which are optionally qualified according to the AEC-Q101 standards. As a result, the N-series SiC-MOSFETs can be used not only in applications such as solar inverters, but also in on-board chargers for electromobility. The products comply with the Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) 2011/65/EU and 2015/863/EU.

www.mitsubishielectric.com



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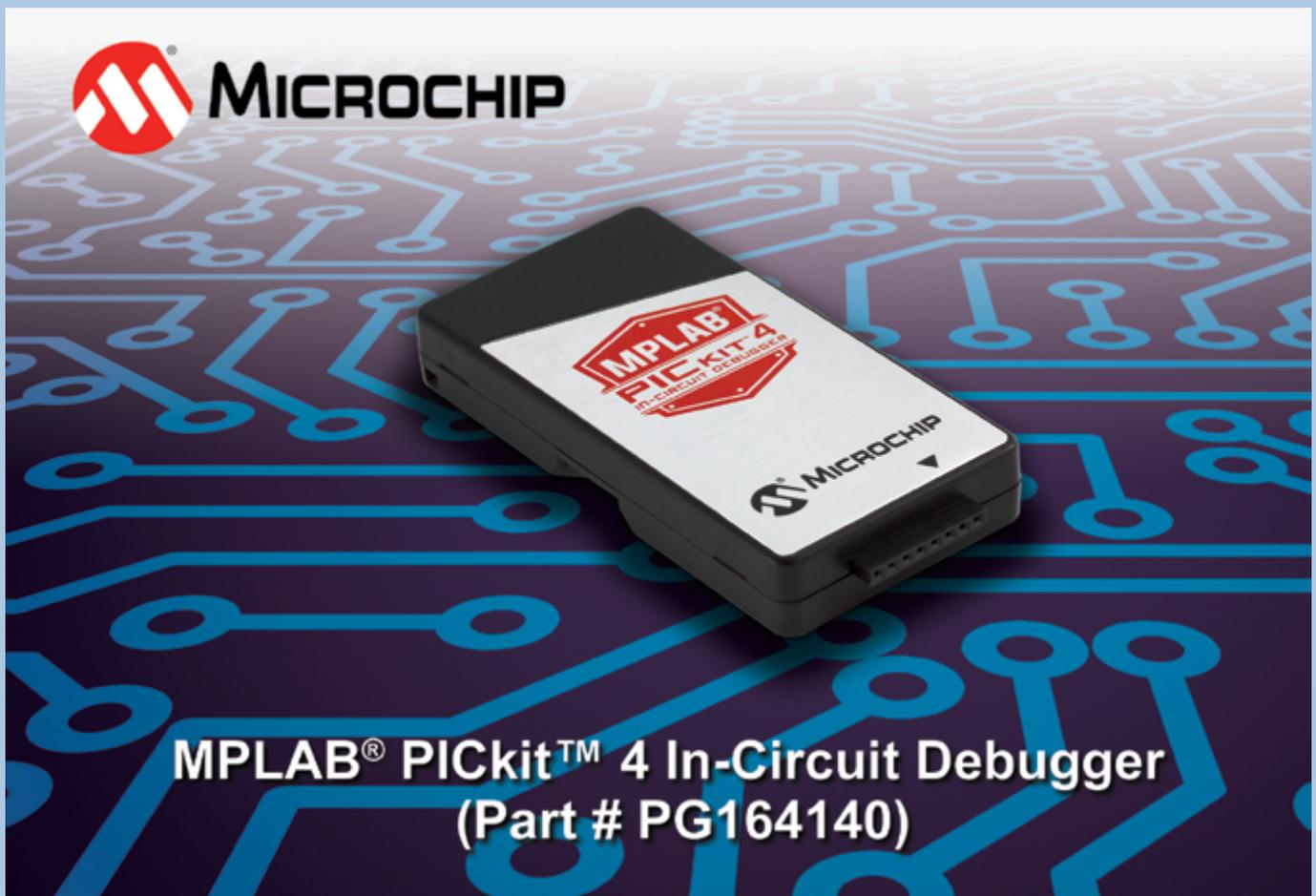
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By Denislav Petkov, Systems and Applications Manager, Texas Instruments

The constant battle to balance size, efficiency, heat and noise levels in DC/DC regulators is especially true for power modules. The balance could heavily depend on the packaging technology used for the module construction. Enhanced HotRod™ quad flat no-lead (QFN) package technology from Texas Instruments addresses multiple design challenges and enables power-converter and module manufacturers to push the industry envelope on package size, efficiency, thermal dissipation capability and noise performance. Let's explore some of the challenges when designing power modules and see how Enhanced HotRod QFN technology addresses them.

Size

As Figure 1 illustrates, a typical DC/DC power module can integrate a power-converter integrated circuit (IC), power inductor(s), some bypass capacitors and feature-programming resistors, all in the same package.

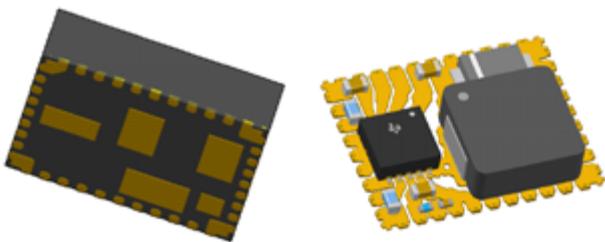


Figure 1: A typical power module with packaged silicon and an inductor side by side on a standard copper leadframe.

The overall size or “volume” of the power module is highly dependent on the converter's operating frequency and the size of the magnetics. Operating the power converter at high frequencies can reduce the size requirements of the power inductor, but there will be conversion efficiency and heat dissipation trade-offs. The overall module area also depends on the package construction. Packages that can integrate the power inductor such that it straddles over the internal module components will result in area savings, but at the expense of overall package height (Figure 2).

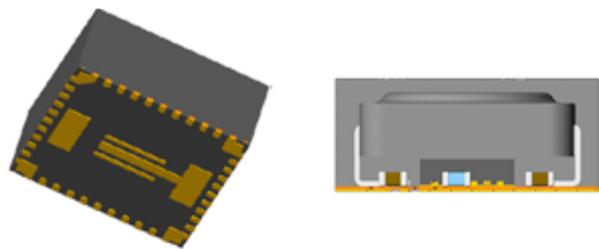


Figure 2: A power module with an inductor straddling internal module components.

The Enhanced HotRod QFN package integrates bare silicon into the module package, leaving more room to integrate the inductor and other passive components. The connection from the chip to the leadframe is realized with copper posts directly underneath the chip, instead of using bond wire. This results in lower package parasitic inductance and space savings inside the module (Figure 3).

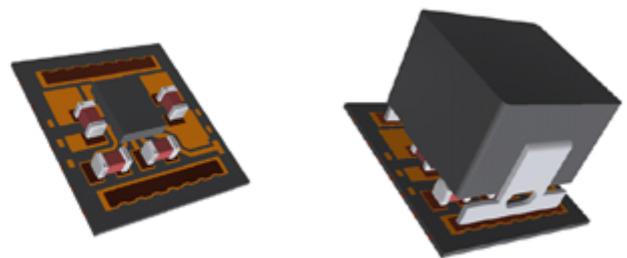


Figure 3: Inside an Enhanced HotRod QFN module: high-performance IC die, with the bypass capacitors and inductor located over the components.

Mounting bare silicon with copper posts on a standard copper leadframe is not a new module technology. In the Enhanced HotRod QFN case, however, the leadframe enables a very user-friendly footprint, with near-perfect routing between the module's internal components and an optimized thermal connection. Another benefit is that the inductor can be packaged over the rest of the components, enabling x-y area space savings. The result can be a compact module structure with integrated high-frequency bypass capacitors (Figure 4).



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Efficiency

Efficiency is an important specification for a power converter. Conversion losses occur mainly in the converter IC and the power inductor. These losses fall into two general categories – switching and conduction – and depend on the IC process and inductor specifications. Not all power-converter ICs are created equal. Having access to a silicon process with a better figure of merit (such as $R_{DS(on)} \times \text{gate charge}$) can result in a more optimized balance between switching losses and conduction losses in the IC.

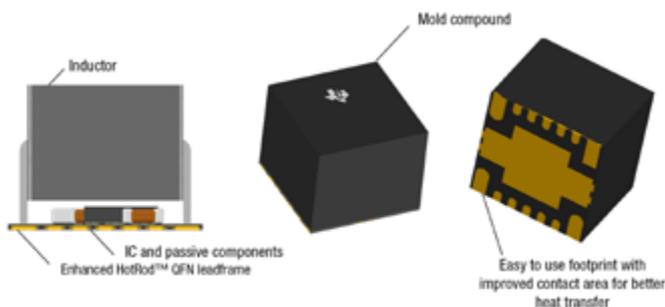


Figure 4: Power module example in the Enhanced HotRod QFN package

You can also choose to run the converter at a lower switching frequency to minimize switching losses. Operating at a lower switching frequency demands higher inductance from the power inductor, however. A higher inductance results in more wire turns and a physically larger inductor for the same current rating. The challenge is how to achieve better efficiency than previous-generation converters while decreasing the overall size and maintaining viable thermal performance.

Integrating a high-performance IC is a first step to achieving good efficiency. The IC inside an Enhanced HotRod QFN package connects to the leadframe with copper pillars, resulting in lower parasitic inductance. The placement of a high-frequency bypass capacitor together with the direct copper connection to the die results in greatly improved switch-node ringing and lower switching losses. Also, the ability to mount the inductor over the rest of the components enables additional area for the inductor without sacrificing the overall x-y package area. Because the inductor has a major effect on overall efficiency, this two-level packaging approach allows you to integrate a larger-size inductor with lower power losses (Figure 5).

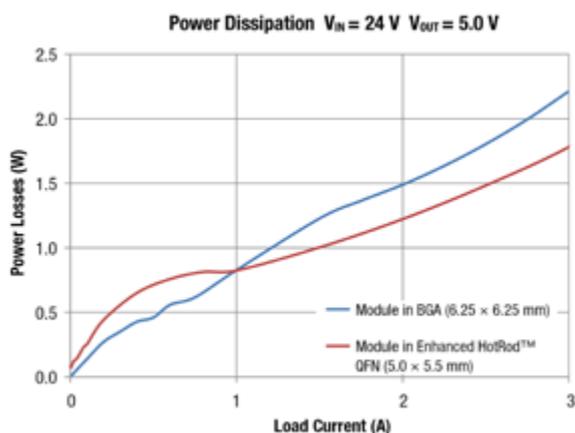


Figure 5: The power dissipation of a 6.25-mm-by-6.25-mm ball grid array (BGA) package with side-by-side inductors vs. a 5-mm-by-5.5-mm Enhanced HotRod QFN package with an over-the-top inductor.

Heat dissipation

Thermal design is an inevitable aspect of power-converter designs. No converter is 100% efficient. Conversion power losses will dissipate as heat, which has to be managed properly. The heat generated in the converter has to be transferred to the rest of the environment so that the power converter stays within its safe operating area (SOA) and the overall system temperature is acceptable for the particular application. At best, the module package should enable a low-enough thermal resistance to dissipate the generated heat into the board and ambient air. Also, the pinout of the package should be friendly enough to enable a thermally viable layout without introducing breaks in the thermal dissipation path.

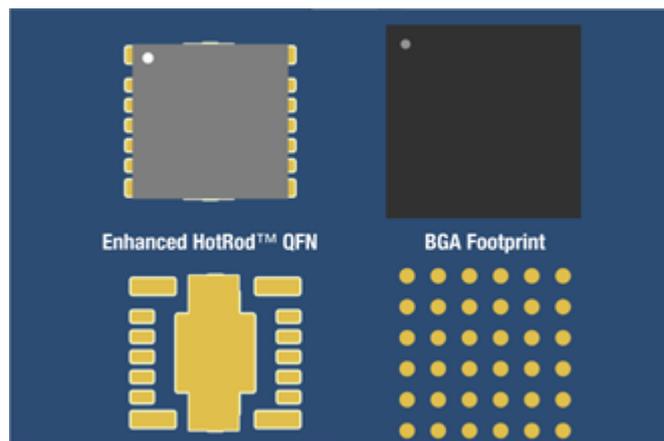


Figure 6: Thermal contact area advantage of a 5-mm-by-5.5-mm Enhanced HotRod QFN package over a 6.25-mm-by-6.25-mm BGA package.

Considering that all of the major power-dissipating components are packaged together in a module, thermal management can be a huge bottleneck in the module's ability to deliver the designed power output. The Enhanced HotRod QFN package lets you design a footprint that maximizes the contact area to the printed circuit board (PCB). A larger contact area facilitates thermal transfer so that heat can dissipate into its surroundings before pushing the converter outside of its thermal SOA. When compared to a similar size BGA-style module package, an Enhanced HotRod QFN package module can have a much larger contact area with the PCB, as illustrated in Figure 6. This can unlock either a higher operating ambient range or increased output power for the same-sized converter.

The simplicity of the Enhanced HotRod QFN package footprint also enables continuous unbroken copper under the module (Figure 7), without cuts and breaks in the thermal path. This further maximizes the usable copper area on the board for proper heat sinking.

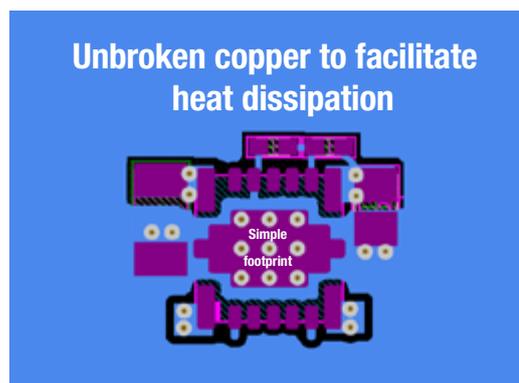


Figure 7: Easy layout with continuous copper for good thermal design.

Noise

Due to the switching action, high transient currents (di/dt), and package and layout parasitics, switch-mode power converters can be noise generators. Noise can affect the proper operation of other noise-sensitive circuits around the power converter, so there are application-dependent noise limits that each product has to meet in the form of EMI standards.

The noise generated by one converter can vary significantly when compared to another. Even with the same converter, noise levels can vary depending on the board layout and components used in the design. Noise generation is typically worse at higher switching speeds (assuming faster switching rise and fall times) and greatly depends on the parasitic elements in the high di/dt loops.

The parasitic elements of the package depend on the package construction, internal routing, internal components used and eventually the board layout. The converter package should minimize the internal parasitic elements in critical high di/dt loops and allow an optimal pinout for proper bypass capacitor placement. Some packages can also enable the integration of high-frequency bypass capacitors, with placement as close as possible to the IC.

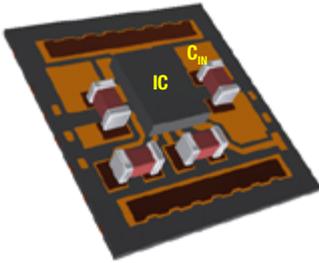


Figure 8: Placing a high-frequency bypass capacitor as close as possible to the chip minimizes the high di/dt loop area.

Minimizing the area of high di/dt current loop(s) in the switching regulator is a critical first step for mitigating noise (Figure 8). Through the integration of bare silicon, ceramic capacitors and improved routing design rules, the Enhanced HotRod QFN package minimizes high di/dt loops in the converter design. Another advantage of the Enhanced HotRod QFN construction over a standard copper leadframe package is the ability to have a ground plane immediately underneath the IC and bypass capacitors, which results in lower switching noise, lower output noise and better EMI.

Summary

Balancing between efficiency, size, and thermal and EMI performance presents many design challenges for power-converter designers. Enhanced HotRod QFN package technology enables power-module manufacturers to take on these design challenges and ultimately produce smaller, more efficient, cooler and quieter power-converter modules resulting in easy-to-use and highly optimized power converters such as TPSM53604 that greatly simplify the process of DC/DC converter design.



About the Author

Denislav Petkov is the Systems and Applications engineering manager for the Wide VIN Power Modules team at Texas Instruments. He has been involved with power electronics since 2005 having worked for National Semiconductor and Texas Instruments. He has held various engineering roles in power Systems and Applications throughout his professional career. Denislav is based in Santa Clara, California.

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Testing Gallium Nitride Devices to Failure Under Extreme Voltage and Current Stress

Standard qualification testing for semiconductors typically involves stressing devices at-or-near the limits specified in their data sheets for a prolonged period of time, or for a certain number of cycles, with the goal of demonstrating zero failures. By testing parts to the point of failure, an understanding of the amount of margin beyond the data sheet limits can be developed, but more importantly, an understanding of the intrinsic failure mechanisms of the semiconductor can be found.

By Alex Lidow Ph.D., CEO and Co-founder, Efficient Power Conversion

By knowing the intrinsic failure mechanisms, the root cause of failure, and the device's behavior over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions [1].

Stressors and Intrinsic Failure Mechanisms

The key stress conditions for all power transistors involve voltage, current, temperature, and humidity as listed in Table 1.

Stressor	Device/Package	Method	Intrinsic Failure Mechanism	Evidence
Voltage	Gate-Source	HTGB	Dielectric failure (TDBB)	Gate-Source Leakage
	Drain-Source	HTRB	Threshold shift	Gate-Source Threshold
Current	Drain-Source	DC current	Electromigration	$R_{DS(on)}$ Failure
			Thermomigration	$R_{DS(on)}$ Failure
		Pulsed current	Thermal	DC SOA failures
			Thermal	Pulsed SOA failure
Voltage rising/falling	Drain-Source	Super-hard switching tests	Unknown mechanism	Hyper-fast high current pulses
Current rising/falling	Drain-Source	High current narrow pulse	Unknown mechanism	Hyper-fast high current pulses
Temperature	Package	Storage Temperature	Unknown mechanism	MSL1 testing High temp storage
Chemical	Package	Humidity	Dendrite formation/ corrosion	H3TRB testing HAST testing
Mechanical strain	Package	Temperature cycling	Solder fatigue	Temperature cycling test
		HOL	Solder fatigue	Temperature and Current test
		Bending force test	Delamination	I_{D1} Failures
		Die shear	Solder strength	Solder strength test
		Package force	Device breakage	Device pressure testing

Table 1: Stress Conditions and Intrinsic Failure Mechanisms for eGaN® FETs

By stressing devices with each of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test (DUT) can be determined. To generate failures in a reasonable amount of time, the stress conditions typically need to significantly exceed the data sheet limits of the product.

This article focuses on the stressor of current. Parts were tested to failure under two specific conditions that demonstrate the exceptional robustness of eGaN FETs; (1) Safe Operating Area (SOA), where eGaN FETs are exposed simultaneously to high current (I_D) and high voltage (V_{DS}) for a specified pulse duration; and, (2) short circuit withstand time, where eGaN FETs are subjected to a short circuit with the gate turned on up to its maximum voltage.

Safe Operating Area

The primary purpose of SOA testing is to verify the FET can be operated without failure at every point (I_D , V_{DS}) within the data sheet SOA graph. It can also be used to probe the safety margins by testing to fail outside the safe zone.

During SOA tests, the high-power dissipation within the die leads to a rapid rise in junction temperature and the formation of strong thermal gradients. For sufficiently high power or pulse duration, the device simply overheats and fails catastrophically. This is known as thermal overload failure. In Si MOSFETs, another failure mechanism, known as secondary breakdown (or Spirito effect [2]), has been observed in SOA testing. This failure mode, which occurs at high V_D and low I_D , is caused by an unstable feedback between junction temperature and threshold V_{TH} .

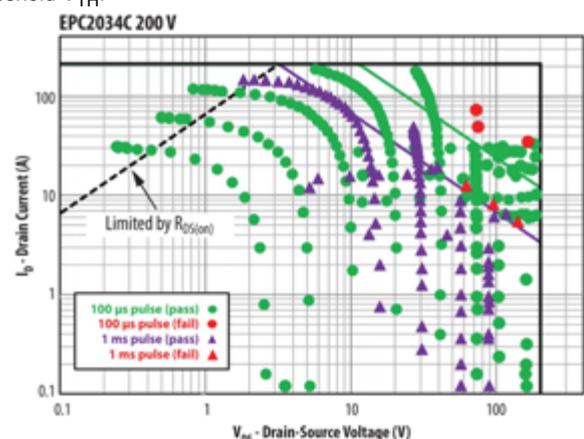


Figure 1: EPC2034C SOA plot. "Limited by $R_{DS(on)}$ " line is based on data sheet maximum specification for $R_{DS(on)}$ at 150 °C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown. Failures are denoted by red triangles (1 ms) or red dots (100 µs).

Figure 1 shows the SOA data of a 200 V EPC2034C. In this plot, individual pulse tests are represented by points in (I_D , V_{DS}) space. These points are overlaid on the data sheet SOA graph. Data for both 100 µs and 1 ms pulses data are shown together. A broad area of the SOA was interrogated without any failures (all green dots), ranging from



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low V_{DS} all the way to $V_{DS,max}$ (200 V). All failures (red dots) occurred outside the SOA, indicated by the green line in the data sheet graph. The same applies to 1 ms pulse data (purple and red triangles): all failures occurred outside of the data sheet SOA.

Figure 2 compares SOA data between a commercial power MOSFET (dotted lines) and an EPC2045 eGaN FET (solid lines) with a similar rating. The secondary breakdown is evident in the Si power MOSFET at drain voltages as low as 10 V_{DS} for 1 ms pulses.

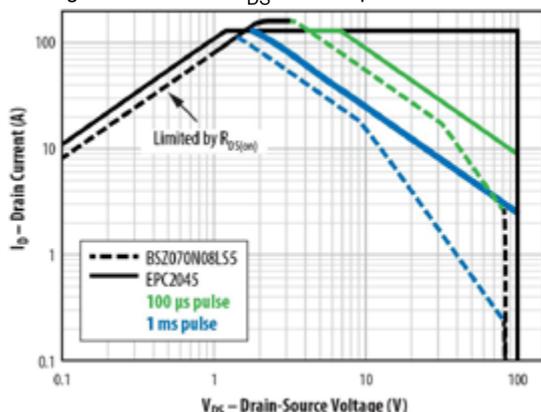


Figure 2: Comparison between a BSZ070N08LS5 MOSFET and an EPC2045 eGaN FET safe operating area

Short Circuit Testing

Short-circuit robustness refers to the ability of a FET to withstand unintentional fault conditions that may occur in a power converter while in the ON (conducting) state. In such an event, the part will experience the full bus voltage combined with a current that is limited only by the inherent saturation current of the transistor itself and the circuit parasitic resistance. If the short-circuit state is not quenched by protection circuitry, the extreme power dissipation will ultimately lead to thermal failure of the FET.

The goal of short-circuit testing is to quantify the withstand time the part can survive under these conditions. Typical protection circuits can detect and react to over-current conditions in 2-3 μ s. It is therefore desirable for eGaN FETs to withstand unclamped short-circuit conditions for about 5 μ s or longer.

Two representative eGaN FETs were tested: EPC2203 (80 V), a 4th generation automotive grade (AEC) device, and EPC2051 (100V), a 5th generation commercial-grade device.

To gather statistics on the withstand time, cohorts of eight parts were tested to failure. Table 2 summarizes the results. EPC2203 was tested at both 5 V (recommended gate drive) and 6 V ($V_{GS,max}$), with mean withstand time of 20 μ s and 13 μ s respectively. Note that the part survives less time at 6 V because of the higher saturation current. EPC2051 exhibited a slightly lower time-to-fail (9.3 μ s) compared with the EPC2203 at 6 V. This is expected because of more aggressive scaling and current density of this device. However, in all cases, the withstand time is comfortably long enough for most short-circuit protection circuits to respond and prevent device failure. Furthermore, the withstand time showed small part-to-part variability.

The lower rows in Table 2 provide pulse power and energy relative to die size. To gain insight into the relationship between these quantities and the time to failure, time-dependent heat transfer was calculated to determine the rise in junction temperature, ΔT_J , during the short-circuit pulse. The results are shown in figure 3.

The intense power density during the pulse leads to rapid heating in the GaN layer and nearby silicon substrate. For EPC2203, both the 5 V and 6 V conditions fail at the same junction temperature rise of 850 °C. The same is true for EPC2051, where both conditions fail at the same ΔT_J of 1050 °C.

Short Circuit Pulse $V_{DS} = 60$ V	EPC2203		EPC2051	
	$V_{GS} = 6$ V	$V_{GS} = 5$ V	$V_{GS} = 6$ V	$V_{GS} = 5$ V
Mean TTF (μ s)	13.1	20	9.33	21.87
Std. dev. (μ s)	0.78	0.37	0.21	2.95
Min. TTF (μ s)	12.1	19.6	9.08	18.53
Avg pulse power (kW)	3.211	2.554	5.516	3.699
Energy (mJ)	43.36	50.24	50.43	77.34
Die area (mm ²)	0.9025		1.105	
Average power / area (kW/mm ²)	3.558	2.83	4.99	3.35
Energy / area (mJ/mm ²)	48.05	55.67	45.64	69.99

Table 2: Short-circuit withstand time statistics for EPC2203 and EPC2051. Average pulse power and energy correspond to a typical part within the population.

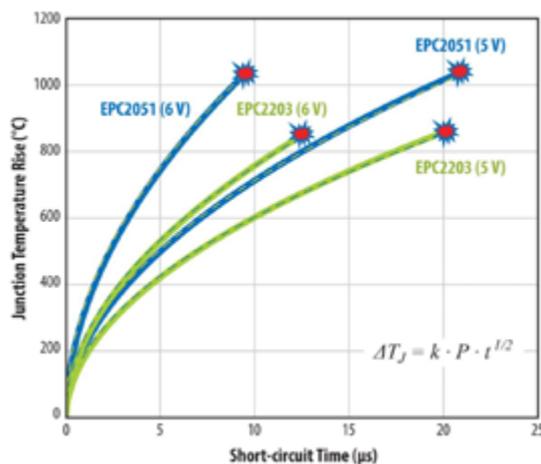


Figure 3: Calculated junction temperature rise vs. time during the short-circuit pulses for EPC2051 and EPC2203 at 5 V and 6 V V_{GS} . Measured failure times are indicated by red markers.

Conclusion

Further analysis is required to determine the exact mechanism of failure. Nonetheless, the experimental results presented in this study demonstrate the outstanding capability of eGaN FETs under extreme voltage and current stress.

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Hard Paralleling SiC MOSFET Based Power Modules

Perhaps the most fundamental question concerning this topic is to ask why parallel modules? What is the advantage of paralleling 2 x 200A modules to make a 400A module, why not simply use a 400A part? On the commercial side, in the 1200V class, IGBT modules are available in multiple current ratings and packages up to 3600A.

By Andre Lenze, David Levett, Ziqing Zheng and Krzysztof Mainka, Infineon Technologies

For SiC MOSFETs the options at higher currents (>400A) are much more limited, especially if industry standard packages or multiple sources are required. Also, physically smaller packages which are manufactured in high volumes often can be produced at a lower cost than mechanically larger lower production volume packages.

However, the main reasons for paralleling modules are technical and these reasons become more important with SiC MOSFETs than with IGBT's for several reasons:

- Multiple packages can be spread out on a heatsink and improve cooling. This allows more current to be delivered from what are more expensive SiC MOSFET modules.
- Larger physical packages have higher inductances in both the power loop and the gate driver circuits due to mechanical spacing and the use of screw terminal connections used to carry the higher currents.
- Using a large number of chips makes internal symmetrical layout and equalization of gate inductance for all the chips very critical and hard to optimize with packages that have limited terminal options.
- The two previous points enable faster switching speeds and hence lower switching losses and lower voltage overshoots during turn off to be achieved with these smaller packages.

Paralleling differences between IGBT's and SiC MOSFETs

On closer examination, despite their fast switching speeds when it comes to paralleling SiC MOSFETs, they have some advantages when compared to IGBTs.

- SiC MOSFETs typically have a higher $R_{ds(on)}$ positive temperature coefficient, when compared to a Si IGBT $V_{CE(sat)}$ characteristic. This acts as negative feedback during static current sharing. If one device is taking more current those chips or modules, get hotter increasing the $R_{ds(on)}$ and hence reducing the current. This negative feedback reduces the level of thermal imbalance.
- Si IGBTs show a large increase in switching losses with increasing temperature and this has a positive feedback effect on temperature imbalance. A hotter chip has higher losses so getting even hotter. SiC MOSFETs show a very small increase in switching losses with temperature significantly reducing this effect.
- SiC MOSFETs have a softer transconductance curve meaning that small changes in gate voltage, when operating in the gate threshold region, have a smaller effect on drain current than an equivalent Si IGBT. This aids in dynamic current sharing.
- A statistical analysis of the Infineon trench gate devices shows that in terms of parameter distribution, modules with a higher $R_{DS(on)}$ have a lower switching losses which helps to match losses part to part.

Experience with a Paralleling Test Platform

We will consider several aspects of this design platform.

1. Module internal layout
2. Power PCB layout
3. Gate driver circuit design
4. Gate driver PCB layout
5. Instrumentation
6. Static current sharing performance
7. Dynamic current sharing performance

Module internal layout

Paralleling must start with consideration of the module internal power and gate layout. The internal chip layout and module pin out can be designed to provide equal and symmetrical power and gate driver layout for the multiple chips in parallel. This is achieved while also keeping a low inductance layout switching loop inductance. In general, the pin grid array of style of PCB based modules allows the flexibility to optimize the layout.

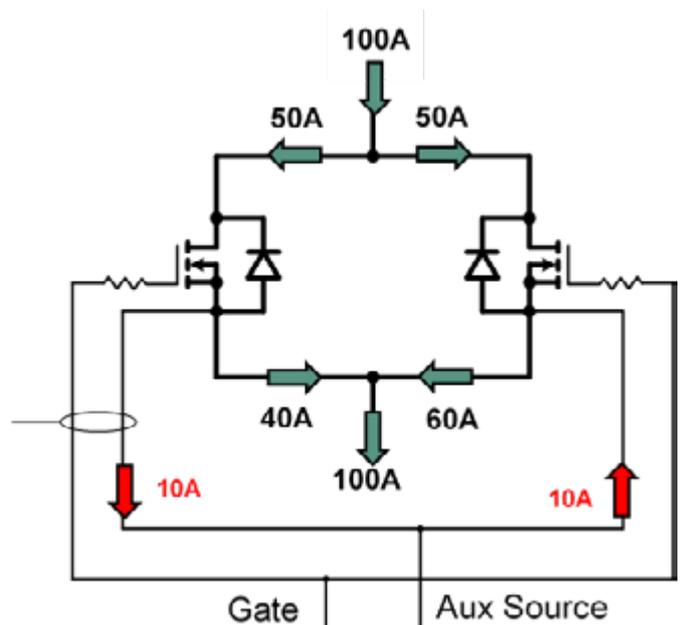


Figure 1: Paths for current flow with a common auxiliary source connection

Power PCB Layout

For the power layout the module is divided into two symmetrical halves. To match this symmetry the power layout was made as a mirror image down the centerline like butterfly wings. This is required to keep equal current sharing among the chips internal to the module. An exact facsimile of the layout was used for each of the four modules to keep current sharing between modules equal. It is also important to keep the external switching loop inductance low and this is achieved by overlapping the DC+ and DC- bus connections with multiple PCB copper planes and using local decoupling capacitors.

Gate driver circuit design

When using a common gate driver circuit for all 4 modules with multiple gate connections, it is important to reduce any currents flowing in the auxiliary source connection. Figure 1 shows, in a simplified example of two modules, how the auxiliary source connection offers a natural parallel conduction path to the main current path. Some electrons which we call them “teenager electrons” because they like to take a different path from everyone else, can flow in this auxiliary source parallel path. This current can be large enough to cause gate oscillations and even fuse open the module internal auxiliary bond wires.

The circuit shown in Figure 2 was used to reduce these unwanted circulating currents. It is a combination of a common mode choke, which shows low impedance to normal gate currents where the in and out currents are equal, but high impedance to unwanted source currents flowing only in the source connection. In addition to this, a separate local boost stage was used for each pair of device gate connections. This allows for resistance in the source connection, but, with local capacitors, any current flowing in this path does not affect the gate waveforms. This is not the case if only a simple source resistor is used as any current flowing in that source resistor affects the gate source voltage which reduces the level of direct control and increases the potential for gate oscillations.

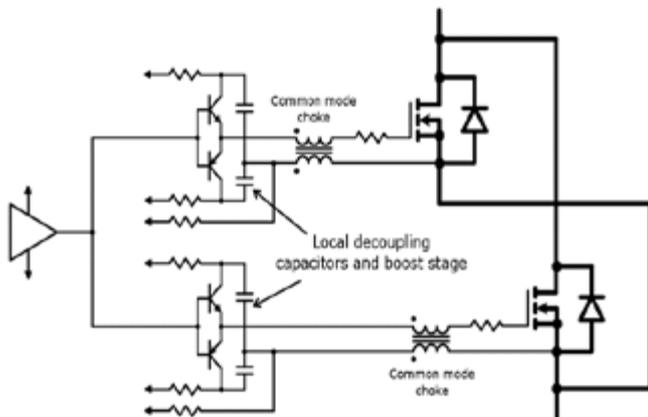


Figure 2: Gate Driver Circuit

Gate driver PCB layout

The 6 mΩ module has dual gate source pins and dual power drain and source connection points to reduce inductance and improve current sharing amongst the SiC MOSFET chips internal to the module. The first challenge of the gate layout is to have a symmetrical layout for both pairs of gate source connections.

After this is it key to turn on and off the gates of all four modules at the same time. The “tree” structure achieves this with low inductance trace gate/source pairs with similar lengths. Also for the local boost stage for each pair of gate source connections the layout was symmetrical. Measurements showed a worse case timing skew of less than 5nS difference between the gates during switching.

Instrumentation

Figure 3 shows the schematic used for the Double Pulse Test-ing (DPT). It is important to measure the current sharing with the topology set up as an as an H bridge so that the current flows and magnetic fields match the final application. Also, it is required to have the capability to generate synchronous rectifier switching pulses for the complementary device under test with dead times that meet the system dead time requirements.

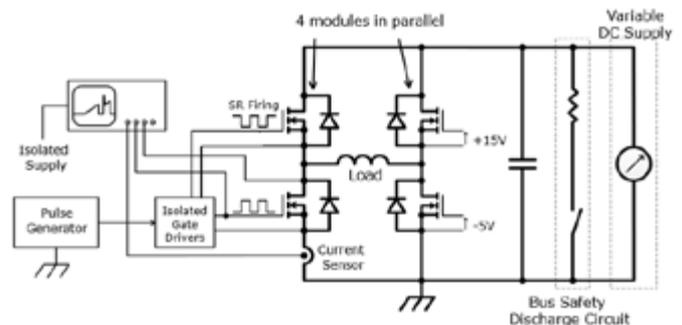


Figure 3: Double Pulse Test (DPT) Schematic

To measure the drain and source currents, the DC bus PCB traces were laid out with holes on both sides to allow the use of a Rogowski coil. These are allowing the measurement of the current in the DC-bus, which is the source current of the lower switch, and the DC+ bus current which is the drain current of the upper device. Also allowance was made to be able to measure the output current balance between the two sets of module output pins

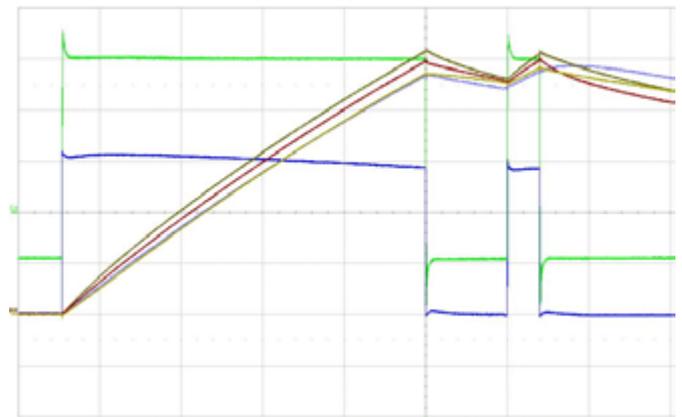


Figure 4: DPT Current Waveforms for 4 Paralleled Modules (50 μ s/division and 50 A/division)
Green Vgs 5 V/division. Blue Vds 100V/division.

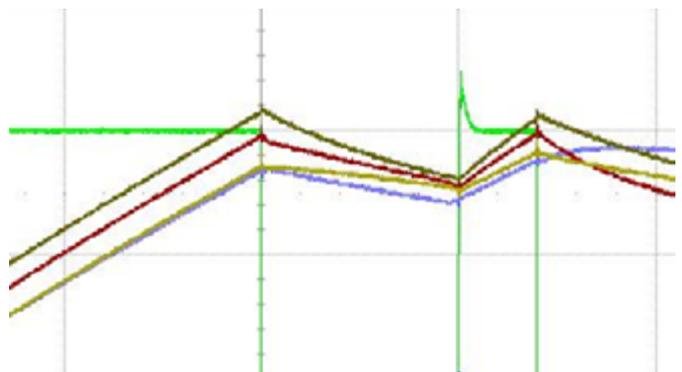


Figure 5: DPT Current Waveforms for 4 Paralleled Modules (50 μ s/division and 50 A/division)

Static Current Sharing

Figure 4 shows the source current in the four lower devices during a DPT. Synchronous rectification was used after the first pulse to turn on the upper SiC MOSFET, following the dead time; but, not after the second pulse which allows the current to free wheel through the upper body diode. Current sharing of four matched modules was +/- 3%. Note that the current sharing is worse after the second pulse when the MOSFET is not gated and only the body diode is conducting current.

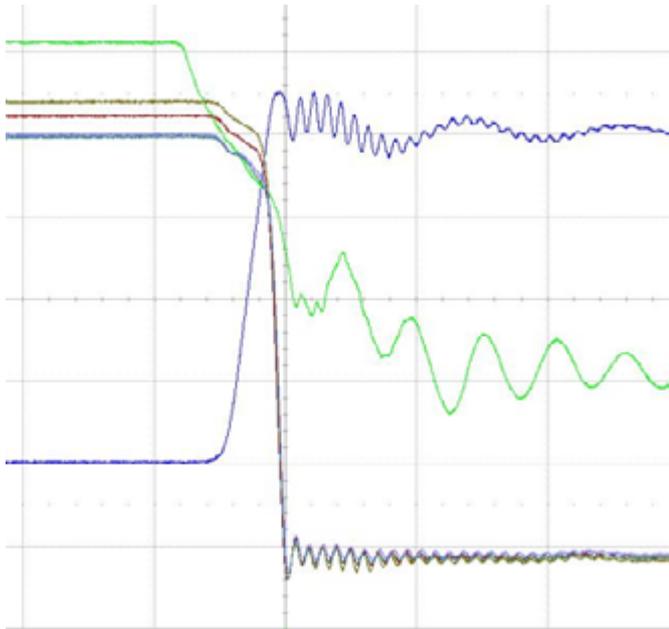


Figure 6: DPT Turn-off Waveforms for 4 Paralleled Modules (200 ns/division and 50 A/division)
Green Vgs 5 V/division. Blue Vds 100V/division.

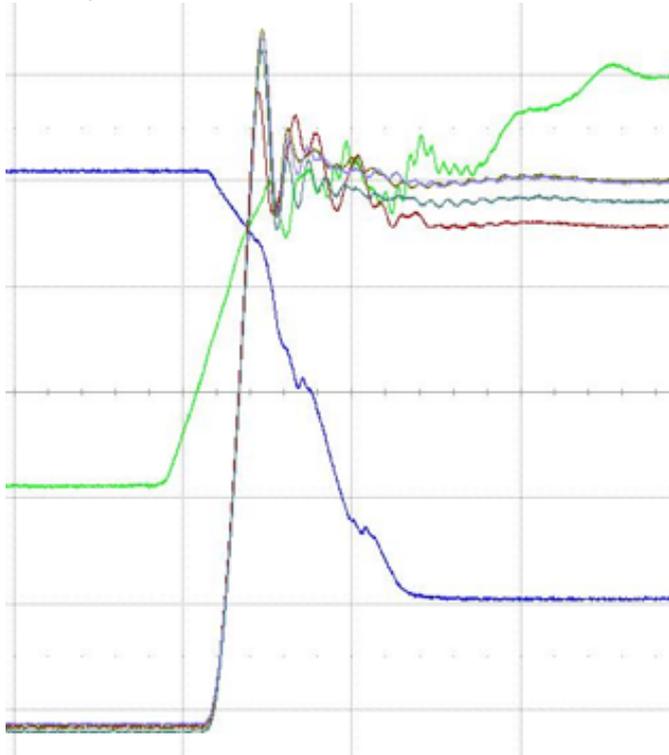


Figure 7: DPT Turn-on Waveforms for 4 Paralleled Modules (200 ns/division and 50 A/division)
Green Vgs 5 V/division. Blue Vds 100V/division.

This initial test was done with modules selected to have an $R_{DS\ on}$ variation of less than 2%. Tests were also performed with modules with a 7% $R_{DS\ on}$ variation and the sharing was only marginally worse at +/- 4%. Additional testing at high temperature and switching upper devices showed equally good performance. Figure 5 shows an expanded view of the current waveform in Figure 4.

Dynamic Current Sharing

Dynamic sharing for both turn on and off waveforms of the lower devices showed excellent sharing as shown in Figures 6 and 7. No current oscillations were observed which indicates the devices are sharing current during the turn on and off sequence. Testing at different temperatures, measuring upper devices and with 7% $R_{DS\ on}$ variations all showed similar performance.

Current sharing in lab vs high volume production

So excellent current sharing has been shown in the lab with a very small sample. However, if this design has to be translated into a high volume commercial product, current sharing for randomly selected modules with their normal distribution of electrical parameters must be calculated. The method used for this is referred to as a Monte Carlo analysis named after the famous casino in Monte Carlo. A set of four modules are selected (each one randomly) from the statistical production spread of $R_{DS\ on}$ and switching losses values. Using these parameters for each module, the current in each module is calculated and the junction temperature estimated. As the $R_{DS\ on}$ and switching losses are temperature dependent, an iteration is used to calculate the final current and junction temperature of each module. This process can be repeated for say 50,000 sets of randomly selected modules and the normalized distribution of T_j calculated. In this case, the results was a variation at +/- three sigma of +/- 7C. Another wrinkle in the calculation is that there is a cross correlation between $R_{DS\ on}$ and switching losses E_{tot} where parts with a lower $R_{DS\ on}$ trend to a higher E_{tot} value.

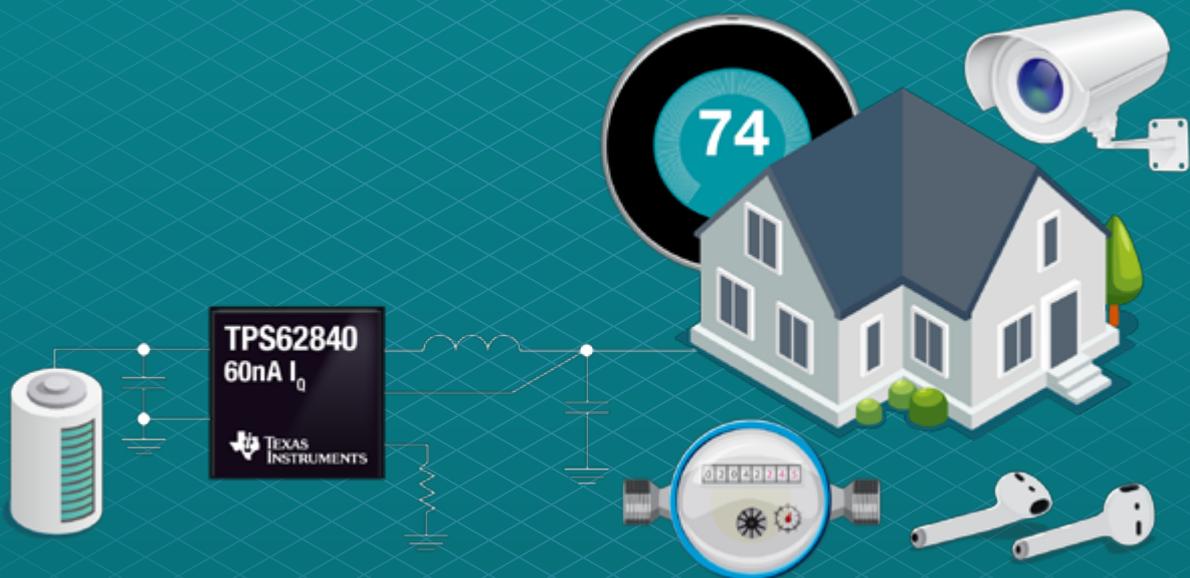
Summary

This article has shown that four modules can be paralleled with excellent current sharing in both static and dynamic operating conditions and with a Monte Carlo analysis parts can be selected at random and still achieve good sharing for volume production. Care must be taken with the gate driver auxiliary circulating currents and of course engineers must follow the three most important design rules when paralleling power semiconductors namely symmetry, symmetry and symmetry.

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The Switch to More Efficient Induction Heating Designs

A frying pan, cut in half, sits on a cooking hob with an egg carefully broken into its centre. The half on the pan has a perfectly cooked, glistening white, while the remaining half is clear and uncooked. It's a powerful image that makes abundantly clear how much more efficient induction hobs are over alternative cooking appliance technologies. The message: induction heating places the energy where it is needed.

*By Georges Tchouangue, Chief Engineer Power Semiconductor,
Toshiba Electronics Europe GmbH and*

Kazuhiro Goda, Expert, Toshiba Electronic Devices & Storage, Kawasaki, Japan.

The semiconductor industry has responded to the demand for induction heating appliances by continuously tuning and improving the switching technology required for its optimal implementation. Thus, induction technology commonly also appears in rice cookers, milk frothers, and hot-plates.

Tackling induction heating applications

It is the principles of the common transformer that form the basis for induction heating applications. However, whereas a transformer induces a current in a secondary coil from a primary coil, an induction heater uses the primary coil to induce current in the cooking vessel itself. This ensures that the resulting heating effect is concentrated precisely where it is needed. It is the Eddy currents that are induced in the material of the cooking vessel that resulting in the heating effect that is known as Joule heating. High resistance is offered by vessels made of magnetic materials such as stainless steel and iron, while non-magnetic materials, such as aluminium and copper, provide less resistance.

Due to the high frequencies used, the current in the primary coil flows principally in the surface of the conductor, a property known as the skin effect. Induction heating coils make use of a special type of copper wire, known as litz wire, that is made up of many thin individual strands. This has the effect of increasing the surface area of the coil, thereby reducing the AC resistance.

Topology choice and their function

There are several approaches to topology choice but, due to price pressure in many of the markets targeted by these applications, the Single-Ended Parallel Resonance (SEPR) circuit is a common choice (figure 1). This soft-switching topology makes use of a resonant tank network consisting of a capacitor, C_r , and the litz coil, L_r . An IGBT, operating under zero-voltage switching (ZVS) conditions together with parallel diode, complete the design. Rather than implementing a discrete approach, the diode is typically integrated into the IGBT, with the characteristics of the diode being optimised to the needs of this type of circuit. Switching frequencies of 20 – 30 kHz ensure any noise is outside audible range, making this circuit suit-

able for magnetic cookware. Higher frequencies may also be used as part of a soft-start function.

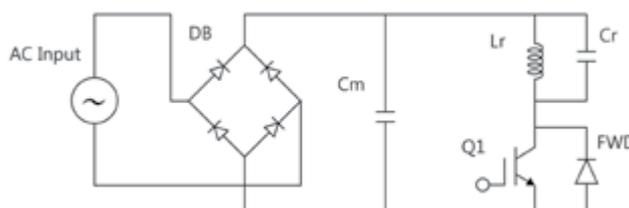


Figure 1: A single ended parallel resonance (SEPR) circuit is typically used for voltage-resonant circuits.

The operation of the voltage-resonance circuit is broken down into four time periods (figure 3) and is applicable for the case that the start-up process has been completed (i.e. C_r is full charged):

1. T1 – The cycle starts with Q1 being turned on, allowing current to flow from C_m through L_r and Q1 and causing the current flowing to increase linearly until it reaches the desired level. During this time the voltage across C_r is clamped to the voltage across C_m .
2. T2 – Next Q1 is turned off, causing L_r and C_r to go into resonance. The peak resonance voltage attained increases proportionally to the on-time T1.
3. T3 – The resonance current flow changes direction, causing the voltage over C_r to decrease.
4. T4 – The polarity of the voltage across C_r now reverses. When it exceeds the voltage across C_m , current starts to flow through the diode bringing the polarity and voltage of C_r back to that of C_m .

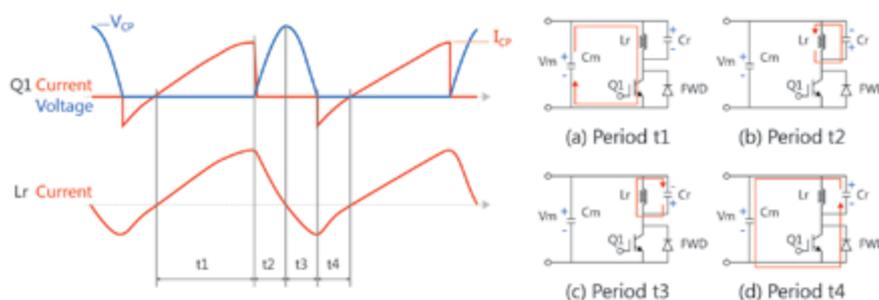


Figure 2: The four phases of operation in a SEPR voltage-resonance design.



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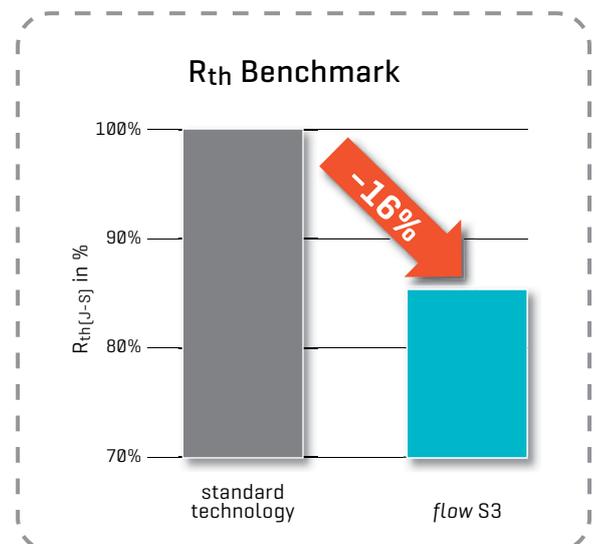
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- / **Smaller price tag** – No copper baseplate
- / **Lower production cost** – Press-fit pins and pre-applied TIM



The rating of the IGBT will depend on the voltage peak Q1 sees, which for 100 VAC supplies will require a V_{CES} rating of between 900 and 1200 V, or 1350 to 1800 V for 220 VAC supplies.

As power requirements increase, a half-bridge current resonance approach using two IGBTs with integrated diodes is typically used (figure 3). Such designs can also support 'all metal' use, where switching frequencies of 80 to 100 kHz can even support the use of non-magnetic cooking vessels. The resonant circuit is implemented as a series LC or LCR construction.

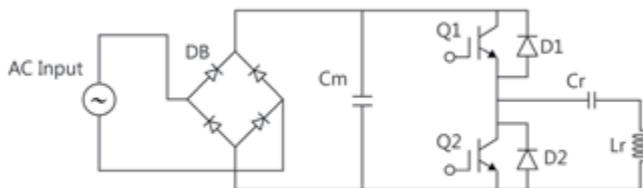


Figure 3: Induction heater half-bridge circuit with current-resonant series LC.

The operation of this circuit can also be described in four phases (figure 4), once the start-up process is completed, as follows:

1. T1 – The upper switch, Q1, is turned on, resulting in a current flowing from the capacitor, C_m , into the resonance current circuit Cr-Lr.
2. T2 – Switch Q1 turns off, leaving Cr to charge due to the current flowing from Lr through the lower switch's diode.
3. T3 – Switch Q2 is turned on, allowing a resonant current to flow from Cr through Q2 and into Lr. At this point, the VCE of Q2 is clamped at the forward voltage of the parallel (or integrated) diode, thereby enabling a ZVS.
4. T4 – Switch Q2 is turned off, allowing a freewheeling current to flow from Lr through Cr, the diode parallel to Q1, and C_m . At this point, the VCE of Q1 is similarly clamped to the forward voltage of the parallel (or integrated) diode, enabling ZVS for the next phase, T1.

As a result, the peak voltages are limited to the sum of the peak AC input voltage, allowing IGBTs to be specified with a V_{CES} of 600 to 650 V for inputs of 220 VAC. The higher currents involved preclude the use of this design with 100 VAC inputs.

Selection of suitable IGBTs for use in induction heating appliances

It is clear that appropriate understanding for the voltages generated across V_{CES} is a critical factor in IGBT selection. The gate drive voltage, V_{GES} , also needs review. This is typically operated at 18 V to

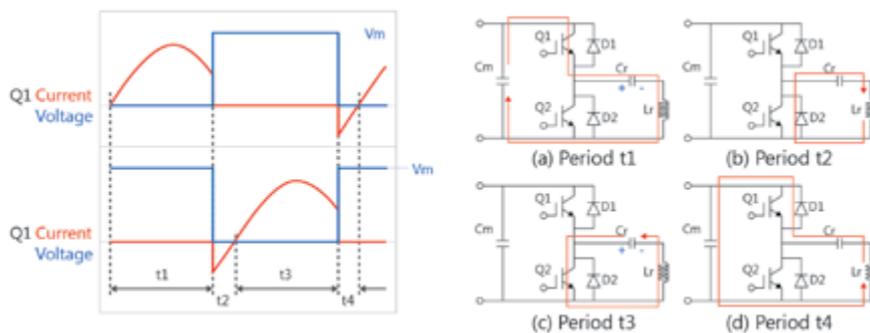


Figure 4: The four phases of operation in a half-bridge current-resonance design.

reduce power losses in the IGBT. However, fluctuations in mains supply in many markets, sometimes as much as 20%, means that designers will need to ensure that the datasheet indicates enough headroom for these parameters. Thermal parameters, such as $R_{th(j-c)}$, provide guidance on the cooling concept required, while tests should be undertaken on electromagnetic compatibility (EMC), especially the turn-off at lower testing frequencies.

Another critical aspect to review is the $IC(sat)$ rating, a parameter that is relevant during the short circuit currents that flow to charge Cr at initial power up until its voltage matches that on C_m . Finally, the forward-biased safe operating area (FBSOA) maximum permissible collector current, V_{CE} , should be checked for different pulse widths.

Punch-through (PT) IGBTs are the device of choice in such applications, supporting higher switching frequencies than non-PT types of the past. Latest advances have thinned the P collector layer to create structures known as field stop (FS) IGBTs. This allows the creation of an N layer to enable a reverse conducting (RC) body diode, leading to RC-IGBTs. With a reduced tail current, they are well suited to soft-switching circuits. Toshiba's latest RC-IGBT, the GT20N135SRA, is a new generation of device with support for 20 A @ 100°C and 1350 V. This is ideal for 220 VAC supplied induction heating applications for 2200 W, medium capacity appliances.

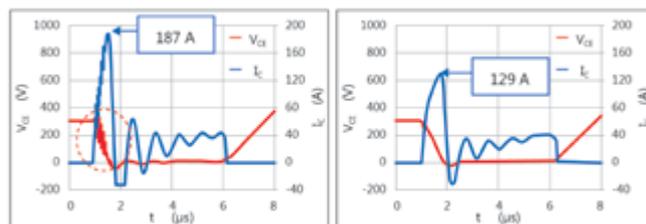


Figure 5: The short-circuit collector saturation when Cr is not charged is significantly improved in the GT20N135SRA (right) compared to the previous generation of IGBTs (left) and results in reduced oscillation (red circle).

Compared to previous generation devices, the short-circuit current, $IC(sat)$, is limited to around 150 A at 100°C. During the start-up phase of the circuit, as Cr is charged, this help to reduce collector saturation current and suppress voltage oscillation (figure 5). The wider FBSOA also means that higher currents can flow, but this must be balanced against some of the losses being converted into heat. The GT20N-135SRA has a maximum $R_{th(j-c)}$ of 0.48 °C/W so, assuming the IGBT needs to dissipate 35W in an appliance implementation, the junction-case temperature would be around 6°C lower than previous generation devices (GT40RR21 – 0.65 °C/W).

The improved N layer has also brought a reduction in the forward-voltage, V_F , of 0.5 V compared to previous generation devices. With a typical value of 1.75 V at 25°C defined, this reduces losses and improves efficiency. The turn-off operation of IGBTs can make it challenging to meet the CISPR standard, requiring a resistor in the gate path to slow switching speed. However, this results in increased losses. Around 10 dB more margin at 30 MHz is now achieved without such a resistor in the same table-top application with the GT20N-135SRA, providing a better trade-off between radiated emissions and power dissipation (figure 6).

Summary

While induction heating appliances provide more efficiency and better control compared to many alternative technologies, the onus falls upon the design engineer to deal with the complexity of the control electronics to implement them. The semiconductor industry has

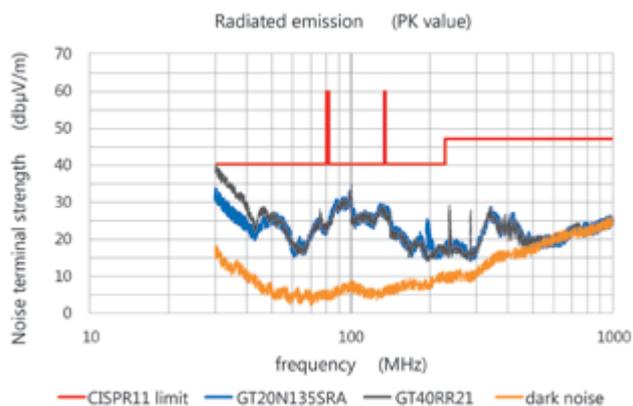


Figure 6: An improved turn-off results in 10dB more CISPR margin at 30 MHz for the same appliance.

responded with IGBT switching devices that, over several generations, have continued to improve the characteristics that are critical for optimal performance, from heat dissipation and EMC, to voltage and current capability and improved reverse conducting body diode.

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The GT20N135SRA, Toshiba's latest generation of RC-IGBT, makes it easier to bring products to market that fulfil radiated emissions tests, while also being more efficient. While optimised for 220 VAC current-resonance applications, future products will expand to cover the higher-current needs of larger cooking vessels and higher voltages occurring in 100 VAC appliances.

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The Difference that DC Makes

For the past century, alternating current (AC) systems have been the global standard for electrical transmission to businesses, applications and homes. However, over the last decades High Voltage Direct Current (HVDC) has emerged as a viable complement to AC power transmission, with the ability to connect asynchronous AC grids and allow power transmission across long distances with minimal losses.

By Andreas Berthou, Global Head of HVDC of Grid Integration business, Hitachi ABB Power Grids

This is essential for applications such as offshore wind farms, which can operate at considerable distances from where the power they generate is needed. In this way, HVDC technology is on course to unlock the full potential of Europe's offshore resources and increase the efficiency and compatibility of energy systems across the world. Andreas Berthou explains the benefits of this transmission system.



Figure 1: Offshore wind

AC vs DC

AC transmission has established itself as the preferred global platform over the past century, due to the convenience of transformers in stepping voltage up or down as needed, as well as being easier to interrupt than DC grids. However, high-voltage AC transmission has a number of limitations, including shorter distance constraints and transmission capacity, as well as the impossibility of connecting two AC power networks of different frequencies. Owing to a number of innovations over the years, HVDC transmission is now primed to supplant AC transmission, with HVDC offering an improved capacity for distance transmission and higher efficiency over those distances. While AC transmission is impossible between two networks of different frequencies, HVDC transmission can connect networks that operate on any frequency or voltage. This allows renewable energy from various sources to be easily integrated into existing power grids, facilitating an efficient transition to renewable energy sources.

HVDC transmission is reliable and easy to control, providing instant and precise control of power flow for new and existing energy infrastructures. This precise power flow allows new energy sources to be integrated seamlessly into power grids without the volatility that such an integration can introduce to existing grids. HVDC can expand the energy networks, making them more stable. HVDC is more environ-

mentally friendly than AC, providing more energy per square metre over greater distances more efficiently than AC systems, as well as lower losses and less space requirements. This increased efficiency reduces the carbon footprint of HVDC compared to AC, with losses being reduced from around 5-10% in AC transmission to around 2-3% for the same application in HVDC.



Figure 2: DC overhead lines

What is HVDC?

HVDC, pioneered by Hitachi ABB Power Grids in the 1920's, and commercially established in the 50's, differentiates itself from AC transmission systems through electrical current converter technology, converting AC to DC to more efficiently transmit across large distances with fewer transmission lines needed. HVDC is also commonly used to connect asynchronous AC networks, stabilising the surrounding grid while increasing grid capacity and affording greater control over power flow. HVDC systems use high-power semiconductor valves, tuned specifically by Hitachi ABB Power Grids for their applications. HVDC is the method of choice for subsea electrical transmission and long-distance power transmission, owing to its ability to send large amounts of electricity across greater distances than AC transmission, with minimal losses. Offshore wind is becoming increasingly important, with WindEurope estimating that Europe's offshore wind capacity will reach 450GW in 30 years, and HVDC transmission is an essential part of connecting remote offshore wind farms to the cities and areas where this electricity is used. To enable this integration with offshore energy, a hybrid HVDC breaker designed by Hitachi ABB Power Grids was recently tested by KEMA Laboratories as part of the EU-funded "Progress on Offshore Meshed HVDC Transmission Networks" project. Using optimised power semiconductor valves developed in-house by Hitachi ABB Power Grids, this breaker

overcomes existing technical limitations by allowing the HVDC transmission system to maintain power flow even if there is a fault on one of the lines, breaking the direct current on the line and isolating the fault. Another important development is HVDC Light®, a voltage-sourced converter solution pioneered by Hitachi ABB Power Grids in 1997, recently hailed by the World Economic Forum as “one of the greatest global energy innovations” of the last decade. HVDC Light provides more secure power control and quick power restoration, and allows long-distance underground high-voltage transmission, enabling easier transition to renewable energy in urban areas.



Figure 3: HVDC light valves

The future of HVDC

While AC fulfils an important role for energy transmission across shorter distances and to the end-user, HVDC technology is a more viable energy transmission solution in our increasingly connected global energy ecosystem. HVDC's efficiency across long distances will be an essential part of global renewable energy solutions, seamlessly integrating clean energy into existing power infrastructures and ensuring that renewable energy is accessible and affordable. This potential is already being shown through large-scale global developments using HVDC in renewable energy systems. Hitachi ABB Power Grids is supporting China in building the Zhangbei HVDC grid in the

Beijing-Tianjin-Hebei area, the first grid installation of its kind in the world. When completed, this grid is expected to provide the area with a consistent supply of renewable energy through the integration of remote wind, solar and hydro energy, and could facilitate the adoption of similar systems in Europe and the US. Just last month Hitachi ABB Power Grids announced a major project with Scottish and Southern Electricity Networks (SEN) Transmission, part of the UK energy giant SSE plc, to enable Europe's first multi-link VSC HVDC connection. The link, which will connect Shetland to the UK transmission system for the first time, will enhance security of power supply and help transmit wind power generated on the islands, contributing to the UK's decarbonization target of bringing all greenhouse gas emissions to net zero by 2050. Another exciting HVDC project is the Dogger Bank development in the UK, consisting of three wind farm projects in the North Sea. The development will be the UK's first offshore wind application of HVDC and is expected to power 4.5 million homes when completed in 2030. These developments not only represent the massive potential HVDC has for the future of the energy industry, but they are playing an essential role in strategies to reduce global warming and contributing to the UN Sustainable Development Goal of increasing access to reliable and affordable energy for all.



Figure 4: HVDC Classic valves from North East Agra multiterminal link in India

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Advantages of 100V GaN in 48V Applications

In both consumer electronics and automotive electrification, we are in a cycle of “more” right now. For consumers, more videos, pictures, Insta-this, Snap-that are all driving data demands skyrocketing. In automotive, more features and functions are added every model cycle including entertainment peripherals, safety features, hybrid motion torque and additional and brighter LEDs. Providing “more” requires more power to be delivered. More power is typically constrained by size and/or weight restrictions. This is why a growing number of industries are moving to higher-voltage, 48V distribution versus conventional 12V distribution.

*By Lei Kou, Power Electronics Applications Engineer,
and Juncheng (Lucas) Lu, Applications Engineering Manager, GaN Systems*

Why 48V? I^2R conduction losses in a system can be detrimental to system efficiency and can reduce the power flow to the load effectively given cable, connector and/or PCB limitations. As an example, server processor power has increased from 100W-200W to 400W and higher. Distributing this increased power to multiple server processors creates more losses unless mitigated by higher voltage distribution or larger copper bus bars. The conventional datacenter/server power architecture is illustrated in Figure 1(a), where all major processor/memory devices are powered from a 12V bus. The I^2R loss for a 12V bus is excessive, and there are many energy conversion stages, which reduces the total system efficiency. To mitigate the heavy bus-bar loss and reduce energy conversion stages in the power distribution path, a 48V bus datacenter/server architecture is shown in Figure 1(b). This power architecture has the advantage over current design practices by eliminating online UPS, cables and harness. The trend clearly shows that the power conversion benefits from 48V bus with more energy saving and lower expenditure (CAPEX and OPEX).

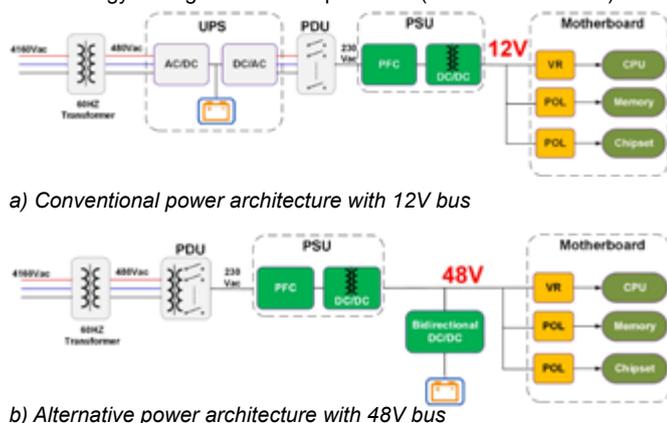


Figure 1: The architecture evolution of datacenter/server from 12V to 48V

With “more power in less area” being the norm, moving from 12V to 48V power distribution using high frequency power transistors allows engineers to meet their efficiency, cost and size/weight metrics.

The GaN Systems 100V product line is a solid solution candidate for 48V applications that meets high frequency, high efficiency, and high-power density power conversion requirements. Compared to MOSFETs, GaN transistors have wide band gap, high electron mobility, and high electron velocity to allow the system switching frequency to be pushed up to high kHz and MHz frequencies to maintain high efficiency and increase power density [1]-[4].

To optimize the system, a deep understanding of conduction and switching losses is required [5]. This information for higher voltage devices, e.g. 650V transistors, can usually be found in the datasheet as well as PLECS/Python simulation models provided by semiconductor companies. However, for 100V devices, the E_{on}/E_{off} data is typically not published because of the difficulty of accurate measurement. An ultra-low parasitics E_{on}/E_{off} measurement platform is described in this article. With this test platform, accurate E_{on}/E_{off} data of 100V GaN Systems devices has been achieved.

GaN Systems provides the switching loss model including PLECS, Python and Excel-based for both 650V and 100V products. GaN Systems 100V GaN products, evaluation boards, modules and the new set of PLECS simulation models provide a comprehensive place to start new system designs.

Accurate switching energy measurement platform for 100V GaN Devices

When comparing transistors with different semiconductor materials, or analyzing trends from a specific manufacturer, the use of a standard figure of merit (FOM) is a useful tool. For example, to compare the $R_{DS(on)} * Q_G$ FOM of a 650V GaN Systems transistor versus a super-junction MOSFET, there is more than a 10x difference in FOM and this has direct implications on system losses. Unlike 650V devices, the difference in FOM between GaN transistors from different suppliers and compared to silicon MOSFETs is not as large. The data below illustrates that additional understanding and measurement of device loss with accurate device loss models is required to determine the real system performance of the transistors in low voltage applications.

To measure the switch current during the switching transition process, a high bandwidth current shunt must be connected in series with the device under test (DUT). The parasitic inductance introduced by a large current shunt causes severe voltage overshoots when compared to the voltage rating of 100V devices. This results in the measured switching energy data being much higher than the value in real-world applications (without a current shunt used for measurement). As a result, power semiconductor vendors rarely publish switching energy data for 100V and below devices.

GaN Systems has designed an ultra-small parasitics Double-Pulse Test (DPT) platform, shown in Figure 2. The parasitic inductance of the power commutation loop is reduced from more than 10nH to 0.8nH, including the large current shunt (model #SSDN-005). When two adjacent conductors are located near each other with opposite current directions, the magnetic flux generated by the two directions of current will cancel each other, reducing the parasitic inductance.

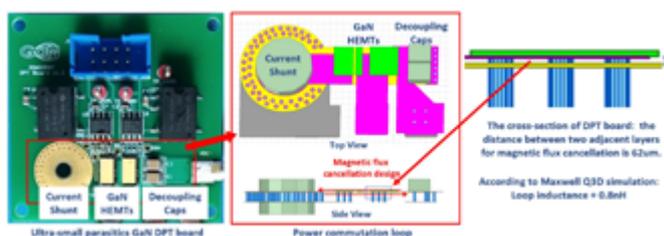


Figure 2: Ultra-small parasitics DPT platform for 100V semiconductor devices

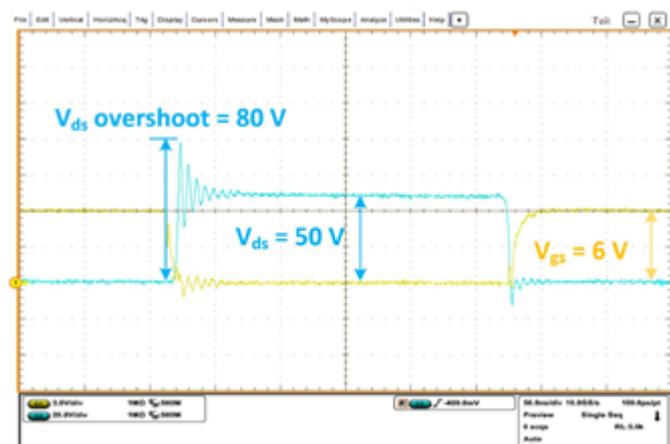
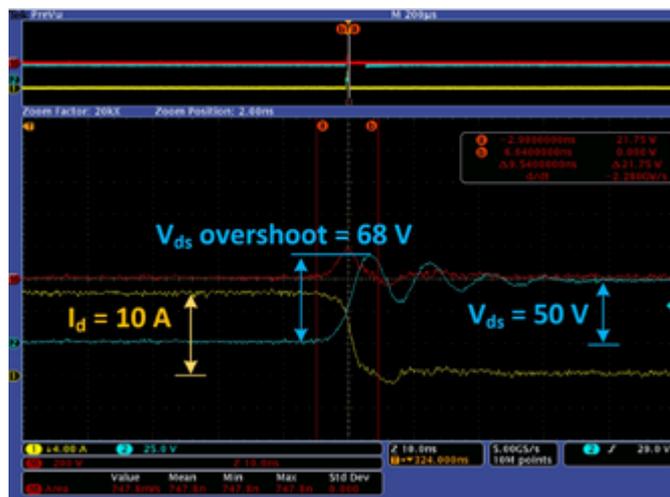


Figure 3: Comparison between the GaN Systems test platform (with Shunt) and other company evaluation board (without Shunt)

The distance between the two adjacent flux canceling layers of the DPT board is 62µm. The simulated power commutation loop inductance, according to ANSYS Q3D software, is 0.8 nH.

The comparison between the GaN Systems' DPT platform and GaN transistor evaluation board for a different supplier, without a current shunt, is shown in Figure 3. Under the same test condition ($V_{ds} = 50V$, $I_d = 10A$, GaN device: GS61008T, $R_{g_on} = 4.7\Omega$, $R_{g_off} = 1\Omega$), the drain-source voltage spike on the DPT board is lower on GaN Systems design compared to the other design (68V versus 80V). This validates the flux cancelling, low parasitics design of the GaN Systems test platform, even with a current shunt in circuit. Had a current shunt been used in the other design, the ringing would be significantly higher than 80V, and measuring Eon/Eoff would be highly inaccurate.

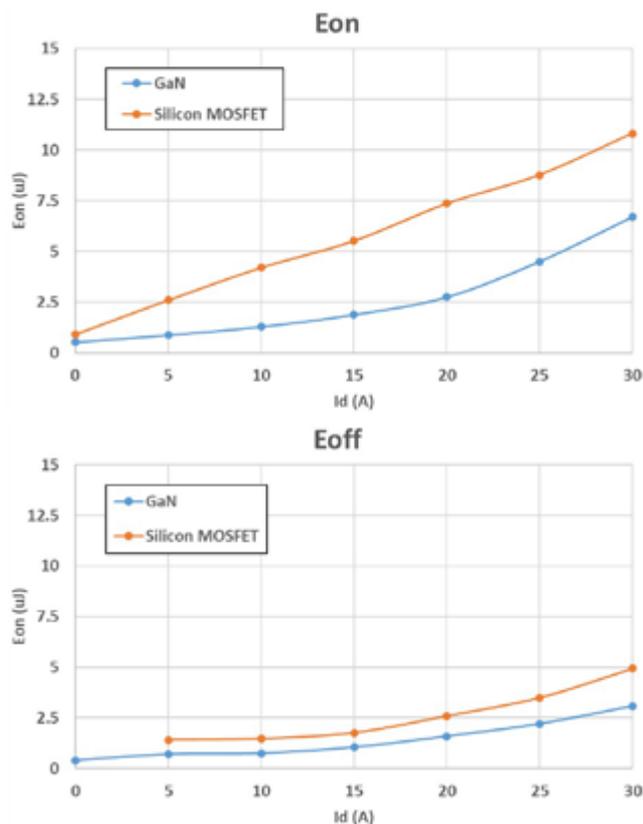


Figure 4: Eon/Eoff comparison between GaN Systems (GS61008T) and a silicon MOSFET

With the GaN Systems switching energy measurement platform, accurate Eon/Eoff data is achieved. A switching energy comparison between a GaN Systems device and a silicon MOSFET was achieved through testing. Both, the GaN transistor (GS61008T) and silicon MOSFET, have similar $R_{DS(on)}$. The results in Figure 4 show the GaN Systems device has lower Eon/Eoff than the silicon MOSFET.

Perhaps a more interesting comparison is between 100V GaN from different suppliers, as shown in Figure 5. Both GaN devices have similar $R_{DS(on)}$ values. However, the GaN Systems device has lower Eon/Eoff.

Figure of Merit

As described above, FOM is sometimes used to compare the in-circuit performance capability of a given device technology in different applications. The following section shows how this can lead to incorrect conclusions with 100V device analysis.

In hard switching applications, two device parameters have major impact on the switching losses: 1) Q_{GD} , the miller charge, controls the voltage rising and falling speed; and 2) Q_{GS} , the gate source charge from the device threshold voltage to the gate plateau voltage, controls the current rising and falling speed. Therefore, the hard switching FOM = $(Q_{GD} + Q_{GS}) * R_{DS(on)}$ is usually used to compare the in-circuit performance capability of different device technologies.

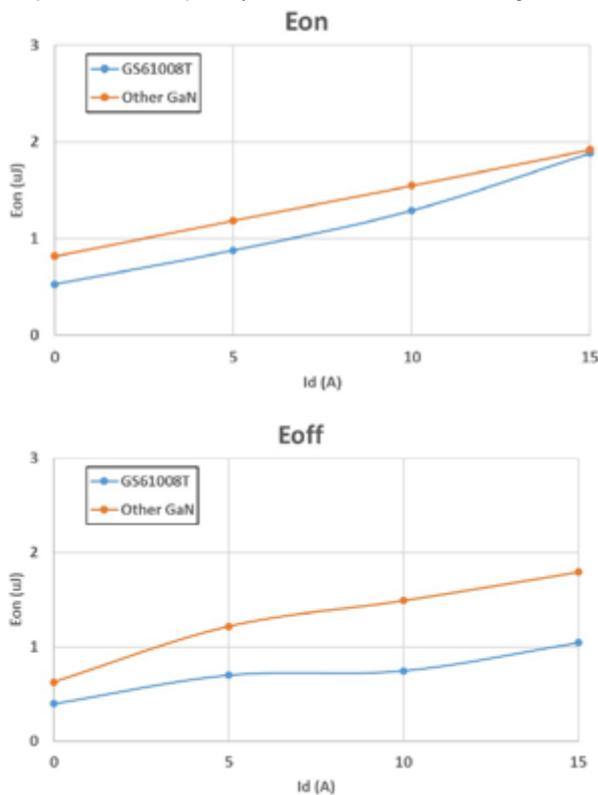


Figure 5: Eon/Eoff comparison between GaN Systems GaN (GS61008T) and other GaN with similar $R_{DS(on)}$

In soft switching application, Q_{OSS} , the output charge, directly impacts the energy required to achieve zero voltage switching (ZVS) and zero current switching (ZCS). Q_G , which is the gate charge, is also a major switching loss characteristic in high frequency soft switching applications. So, to compare parameters that influence the in-circuit performance of different device technologies in soft switching applications, FOM = $(Q_{OSS} + Q_G) * R_{DS(on)}$ is often used.

	GaN Systems GS61008T	GaN Supplier 2	GaN Supplier 3	Silicon MOSFET
$R_{DS(on)}$	7 mΩ	5.6 mΩ	15 mΩ	6 mΩ
Q_{GS}	3.5 nC	1.9 nC	1.3 nC	10 nC
Q_{GD}	1.7 nC	0.8 nC	0.6 nC	6 nC
Q_{OSS}	21.3 nC	25 nC	21 nC	41 nC
Q_G	8 nC	6 nC	3.8 nC	30 nC
Hard switching FOM ($Q_{GS} + Q_{GD}) * R_{DS(on)}$	36.4	15.12	43.5	96
Soft switching FOM ($Q_{OSS} + Q_G) * R_{DS(on)}$	205.1	173.6	372	426

Table 1: FOM comparison of different semiconductor devices

A FOM comparison of four different semiconductor devices (three GaN transistors and one silicon MOSFET) is shown in Table 1.

According to the FOM comparison table, it can be observed that: 1) GaN devices have a lower FOM than silicon MOSFETs (remember that lower FOM is better); and 2) the product from GaN supplier 2 has the lowest FOM among the GaN devices. Interestingly, in this case, the device with the lowest FOM does not have the best performance in the targeted application. Recall from the Eon/Eoff analysis that the GaN Systems device has lower losses than the other GaN device. In addition to the Eon/Eoff losses, the thermal performance also contributes to overall functionality.

Thermal performance and system level comparison

In most applications, FOM and loss analysis is important but not the complete picture to achieve higher efficiency. Device thermal performance is also a very important factor to determine the system efficiency. GaN transistors have a positive temperature co-efficient $R_{DS(on)}$ characteristic. Also, switching losses increase as junction temperature increases. Therefore, devices with good FOM but difficulty managing thermal performance can have higher losses and be limited in efficiency and/or power.



Figure 6: Thermal resistance comparison

As seen in Table 1, one GaN device has a better FOM compared to the GaN Systems device. However, there are some high power thermal challenges due to the “chip-scale” style package of the device. As shown in Figure 6, the GaN Systems device, in a low parasitic, thermally enhanced package, operates at ~50% lower $T_{JUNCTION}$ versus the chip-scale type device. To demonstrate the importance of thermals in an application, a system level comparison is presented with the four different semiconductor devices from Table 1 used on identical 48V to 12V evaluation boards.

The maximum current versus switching frequency in Figure 7 shows that the GaN Systems' device has 2.3x higher output power at 1MHz switching frequency compared to the other GaN devices and the silicon MOSFET.

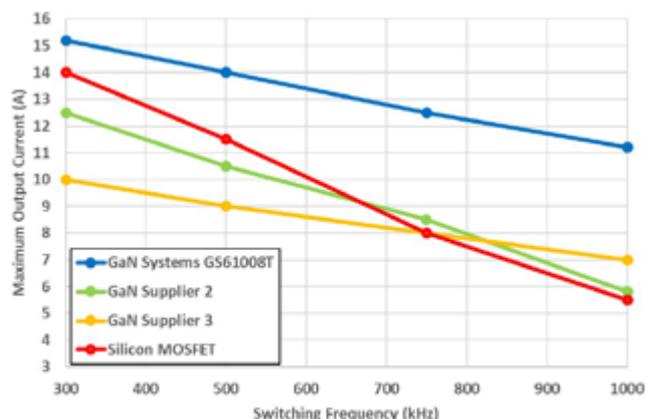


Figure 7: Maximum current comparison vs. different switching frequency

The efficiency curve in Figure 8 shows that:

- GaN transistors have much better efficiency over silicon MOSFETs;
- the GaN Systems device has the highest efficiency;
- the GaN Systems device can support much higher power compared to others.

Note that the tests were stopped when the specific device showed signs of thermal starting to limit output power. In this 48V to 12 V application, the data illustrates that a combination of FOM, Eon/Eoff and thermal performance must be considered to determine the best performance.

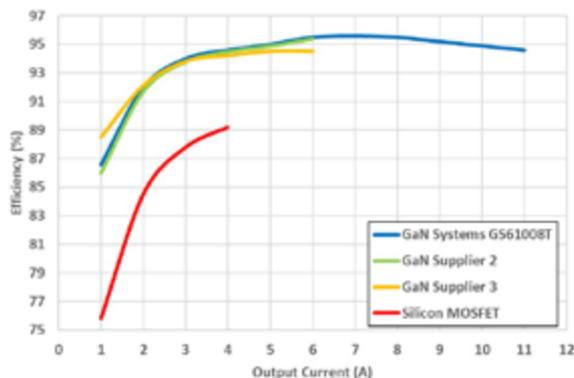


Figure 8: Efficiency comparison of different semiconductor solutions

Conclusion

GaN power transistors can switch at higher frequencies than traditional silicon MOSFETs and therefore are excellent power semiconductor candidates for 48V application challenges. System loss analysis is critical to optimize the power system design. To achieve accurate

Eon/Eoff data for 100V GaN devices, GaN Systems has developed an ultra-low parasitics double-pulse test platform. The Eon/Eoff data acquired from this test platform shows that GaN transistors have lower Eon/Eoff than silicon MOSFETs and other GaN power devices. A system level comparison in a 48V to 12V application shows that 1) GaN Systems solutions achieve much higher efficiency than other GaN or silicon solutions, and 2) important factors such as Eon/Eoff loss analysis, packaging and thermal effects must be accounted for to achieve high system efficiency.

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Optimizing EMI Input Filters for Switched Mode Power Supplies

Any switched-mode power supply (SMPS) needs an EMI (Electro Magnetic Interference) input filter to avoid causing disturbances in power lines, with the accompanying interference in other components or systems connected to the power lines. Consequently, designing and optimizing the input filter is an important task for SMPS development. While both common-mode and differential-mode noise filter elements have to be added, they are rarely optimized separately. In particular for high-power applications, this can result in a significantly larger EMI filter than actually required.

By Marcus Sonst, Application Development at Rohde & Schwarz in Munich

In this article, we discuss a simple method to separate common-mode and differential-mode noise components using a dual output LISN (Line Impedance Stabilization Network) and an oscilloscope with at least two channels, which makes it possible to optimize common-mode and differential-mode filter components separately, resulting in more accurate data for designing an optimal input filter.

EMI is becoming even more important with wide-bandgap semiconductors

Due to its nature of switching large currents, an SMPS generates a fair amount of noise. The choice of SMPS topology is significant and influences filter design; for example, a dual interleaved boost topology creates less noise than a simple boost converter. Once the topology is chosen, there are several design parameters that influence the noise level. The switching frequency of the converter is a key value. Very often, a high switching frequency is chosen to obtain a compact design. However, a high switching frequency can be a cause of excessive EMI. It is very important to understand the correlation between rise and fall time of the switching element and the generated noise. Typically a fast switching element is the first choice. Nowadays, even wide-bandgap devices based on SiC or GaN are very popular in power converter designs to increase efficiency. Such fast switching elements accentuate noise generation if the design is not very carefully optimized to avoid noise generation. In addition to the design parameters, it is always helpful to minimize the parasitic elements in the whole design including the printed circuit board. For example, the high-voltage switching element combined with a connection to a metal housing for cooling will create a parasitic capacitance, which can act as a path for common mode noise to leave the system.

Typical EMI Input Filter Structure

An EMI input filter typically consists of two functional parts; one part to suppress unwanted common-mode noise, the other part to suppress differential-mode noise.

For an AC/DC converter, the key components for the differential-mode EMI filter part are the differential-mode inductors and the X-capacitors. For the common-mode EMI filter part, the common-mode choke and the Y-capacitor. In some cases, the differential-mode inductors can be omitted as the common-mode choke can also act as differential mode inductor.

Separating Common-Mode and Differential-Mode Noise

The EMC standard requires that the conducted emissions on both power lines are measured and that the voltages are below the specified limit at every frequency in the frequency range. This measurement is performed sequentially on one power line, followed by the other. While this is sufficient to pass the conducted emission test standard, it does not provide any insights into the noise propagation mechanisms, because the measurement is a combination of common-mode and differential-mode noise on the conductors. The principle, how the noise current flows within the system is shown in figure 1.

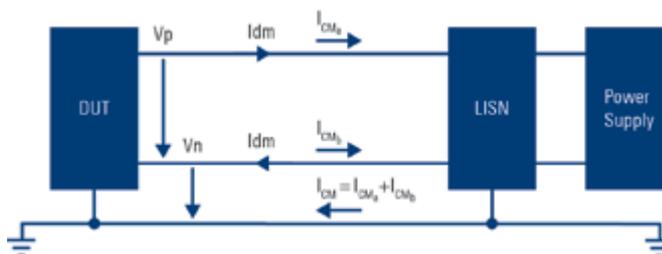


Figure 1: Common Mode / Differential Mode Flow

The Common Mode current portion I_{cm} flows from the DUT (Device Under Test) on both lines into the LISN and to the DUT back via the external ground path, resulting in the sum of the two current portions in the external ground path. The amplitude and phase are the same on both conductors, positive and negative. The Differential Mode current shows a different characteristic; the current on the positive conductor flows into the LISN, the return path of the noise is the negative conductor. The only difference is the phase between these two currents; they differ by 180° and ideally they should cancel out. With a little bit of mathematics, it is possible to separate the common-mode and differential-mode noise terms. Using the individual currents:

$$I_P = I_{CMa} + I_{DM}$$

$$I_N = I_{CMb} - I_{DM}$$

we can easily calculate the voltages on the two conductors:

$$V_P = (I_{CMa} + I_{DM}) * Z_{LISN}$$

$$V_N = (I_{CMb} - I_{DM}) * Z_{LISN}$$



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Based on the relations between individual voltages and common-mode and differential-mode voltages:

$$V_P + V_N = V_{CMa} + V_{CMb}$$

we can calculate the common-mode and differential-mode voltages as follows:

$$V_{CM} = V_P + V_N$$

$$V_{DM} = \frac{1}{2} (V_P - V_N)$$

The simple subtraction results in a value that is twice the Differential Mode noise level, or 6dB extra, which has to be taken into consideration during result evaluation. Using these simple calculations, distinguish between common mode noise and differential mode noise (including subtract 6dB from the differential result). The simple math calculation works best, if the setup (cable, components of the LISN, etc.) is as symmetrical as possible; the noise on the two conductors must be measured at the same time. A simple but effective setup to separate common-mode and differential-mode noise is shown in figure 2. A dual-output LISN (or two identical LISNs) is used to probe on both power lines and the signals are captured by two channels of an oscilloscope. The sum and difference signals are calculated on the oscilloscope as well as the (Fast Fourier Transformation) FFT. This gives directly access to the common-mode and differential-mode noise signal.

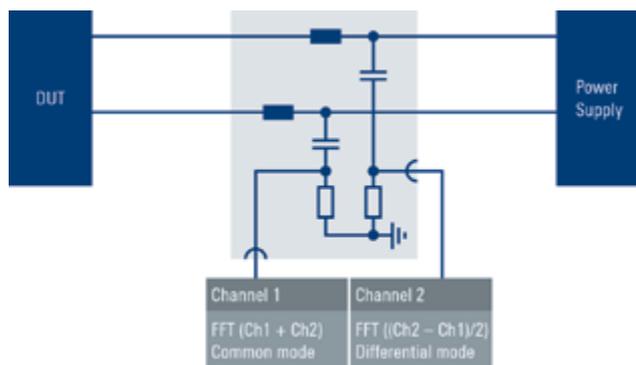


Figure 2: Enhanced Measurement Setup

While any non-symmetry between the two LISNs will have some influence on the measurement result, practically this method provides reasonably accurate results. Important aspects to consider are to use the same cable length, as well as to use cables with sufficient quality to avoid shift in time or loss in amplitude, which would directly have an impact on the ability to separate the noise components.

Furthermore, an oscilloscope with a sufficiently low-noise frontend, direct input of frequency parameters such as start and stop frequency, or resolution bandwidth, and a sufficiently fast FFT function should be used.

Case Study

The DUT used to demonstrate the new method is a simple step down buck converter. The DUT input filter is a simple PI-LC-filter, which is very effective for damping differential mode noise. The setup makes either applying or excluding the PI-LC-Filter simple. No common mode filters are included on the PCB, so a common mode choke is attached externally to the PCB. The converter has no housing; the PCB is simply placed on an isolation block on a metal ground plane. The setup deliberately avoids generating excessive common mode noise.

The first measurement, as seen in figure 3, was taken to show the highest spectrum in the input power conductors. A reference level measurement has already established the noise level of the system while the DUT is switched off. The extra 6dB in differential mode was compensated by dividing the sum expression by 2 before performing the FFT. For common mode, the sum expression is used directly as the total amount of common-mode noise is represented by the sum of the two measurement channels.

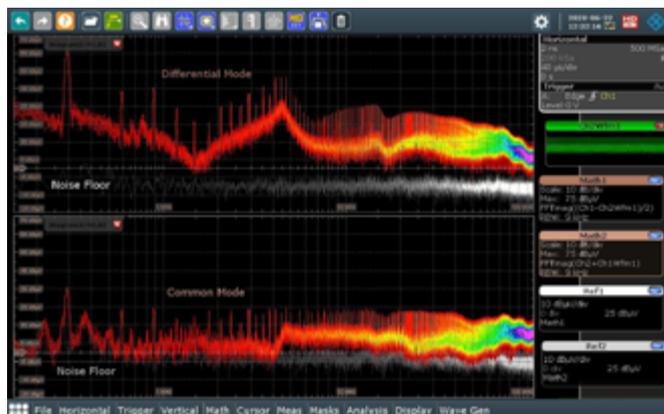


Figure 3: No EMI Filter Applied

The peak at 300 kHz in the reference line is caused by the system, not the converter, and can be ignored at least up to 25dB μ V. The high magnitude differential mode noise (approximately 65dB μ V) during the measurement at 300 kHz is caused by the switching frequency of the converter. The harmonic and all higher odd multiples of this frequency are caused by the reflected ripple current, which dominates the differential mode spectrum. In the common mode spectrum some peaks are also visible; these are not filtered by a differential filter.

An LC Filter is calculated to damp the fundamental magnitude at 300 kHz. The calculated filter resonance frequency is at 19.3 kHz, which should result in a suppression of about 40dB at the switching frequency. The filter structure is of second order and thus the damping is about 40 dB/Decade. The measurement in figure 4 shows the effect of the filter on the spectrum.

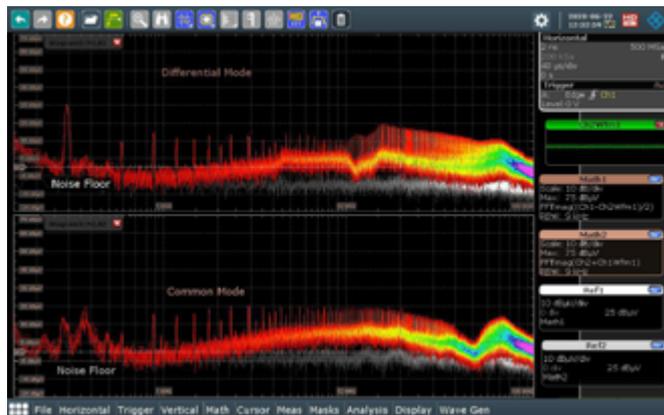


Figure 4: Differential Mode Filter Applied

The differential mode noise is reduced up to 10 MHz very efficiently, damped up to 30dB compared to the previous unfiltered value. Especially the fundamental at 300 kHz and the multiple harmonics are much lower in the magnitude. In the higher frequency region, the filter is not as effective; noise is only damped up to 10dB.

The common mode noise is not reduced significantly because the filter was designed to filter the differential mode noise. To damp the common mode noise, an additional filter is added. A common mode choke from Würth Electronic is inserted.

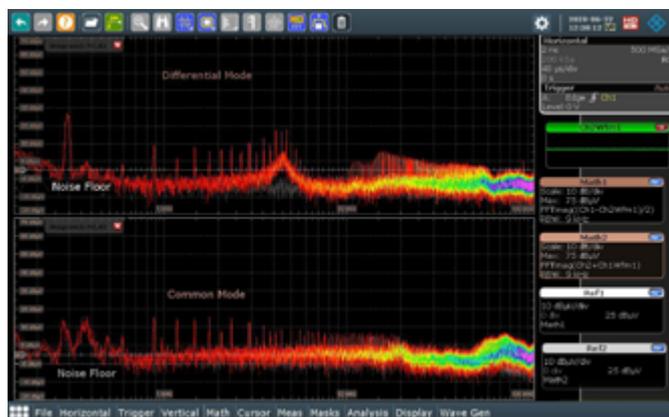


Figure 5: Common Mode Filter Applied

The common mode noise is reduced in particular from 2 MHz to 60 MHz. In addition, the differential mode noise is also damped as the common mode choke is not ideal and the resulting leakage induc-

tance functions as a differential filter. Furthermore, the differential mode noise may also be affected because the setup was not optimized (No PCB for the CM choke) and therefore some asymmetrical components may lead to this additional damping effect. However, figure 5 shows, it is clearly visible that the common mode noise was damped very efficiently due to the inserted CM-Choke.

Conclusion

An effective input filter design is essential to fulfil the EMI standards for conducted emission of a switching mode power supply. Often, the EMI filter consists of both a common-mode and a differential-mode filter, both elements have to be designed and optimized. Accurate information on the common mode noise, respectively the differential mode noise contributions, greatly aids the task of designing and optimizing the EMI input filter. Using a dual-output LISN, (or two identical LISNs) and some mathematics on the oscilloscope common-mode and differential-mode noise can be separated directly on an oscilloscope. The result is an effective tool to optimize both parts of the EMI filter using the FFT functions of the oscilloscope every power supply circuit designer is bound to have.

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Lineup of Modern Clamping Systems for Tests of Power Semiconductor Devices with Force up to 150 kN

Power semiconductor devices have many parameters and characteristics that must be measured using specialized equipment. Design of such equipment must account for many factors such as reliability, flexibility, ergonomics, and attention to overall aesthetics. This article describes the steps of development and research carried out to design a clamping system for disc semiconductors and analyzes the encountered issues. A number of technical solutions were used to improve ergonomics, later proving their efficiency in real operation.

By Alymov D., Gorodnichina A., Semenov P., Sytyi A., Kazarov A. and Verkhovets V., Proton-Electrotex

Today power semiconductor devices are the fundamental design elements of various equipment in many industries. Power electronics is constantly evolving and improving, therefore, requirements to the accuracy of measuring their main parameters are also increasing. The Automation Laboratory at the R&D Center of Proton-Electrotex JSC has developed a lineup of test equipment designed to measure parameters of power semiconductors meeting all requirements to accuracy, reliability and ergonomics. It is capable of measuring the following parameters for bipolar semiconductors:

- Parameters in open state: V_{TM} , V_{FM} , I_{TSM} , I_{FSM} , I_L ;
- Blocking parameters: V_{RRM} , V_{DRM} , V_{DSM} , V_{RSM} , I_{DRM} , I_{RRM} , $(dV_D/dt)_{crit}$;
- Gate parameters: V_{GT} , I_{GT} ;
- Thermal parameters: R_{th} , Z_{th} ;
- Dynamic parameters: Q_{RR} , t_q , t_{gd} .

The test equipment (Fig. 1) is a complex including a clamping system and individual measuring units installed in a 19" rack. Each block performs a specific function. Control is carried out using a HMI unit with a 17" capacitive touch screen. The software allows to make several successive measurements in automatic mode. The complex is serviced by one operator. The operator's responsibilities include selection of the measurement profile, installing the device under test in the

clamping system and launching the tests with the "Start" button.



Figure 1: The tester with the clamping system

Previously the company used test equipment with a number of drawbacks. To make a series of measurements it was required to switch from one test station to another resulting in much lower productivity. Each station occupied production area and required more operators. The operator had to manually adjust the equipment to the required test conditions before each measurement. The

clamping systems were based on a pneumatic actuator with several disadvantages: insufficient force to clamp large diameter devices, the inability to dynamically change the speed and force of clamping.

To eliminate these main disadvantages, the Automation Laboratory has developed a state-of-the-art clamping system. The tester consists of two standard 19" racks with measuring units and a clamping system inside. This modular design made it possible to customize the equipment for a specific task by selecting the units needed in the tester. Besides, it made maintenance and repair of the equipment much more convenient significantly reducing the downtime. It is only needed to disconnect the failed unit and replace it with a backup, then the complex is ready for continued operation. Automation of the measurement process minimized the influence of the human factor on the quality and reliability of measurements, while the work of the operator became less critical.

Ergonomics and aesthetics were also considered. Initially the clamping system was designed as a separate mechanism connected to the tester, but this configuration resulted in unused space in the rack above the clamping system. Some units need to be connected with the shortest possible conductors (cables and buses) to ensure precise measurements, so it was decided to include

the clamping system in the tester and place the measuring units in the free space above it.

The operator's workplace includes a touch screen, clamping system and a table to put the devices. For convenience, the touch display is detached from the tester on a bracket, allowing the operator to adjust its position as needed. Several ergonomic improvements were made after a survey of operators from the manufacturing. A recess for leg space was made in the housing at the operator's workplace. It was also revealed that the clamping system provides insufficient lighting for the operator to control the process of clamping the system and to track wear of the contact surface. The clamping system was analyzed for the required lighting conditions and light sources were selected and installed both inside and outside the tester.

The measuring and auxiliary units (Figure 2) are placed in housings of various heights designed for a standard 19" rack. Light indicators on the frontal panel inform about the correct operation, while connectors and output buses are located on the rear. To increase the accuracy of measurements a bifilar arrangement of buses is used, both inside and outside the unit.



Figure 2: Measuring and auxiliary units

The clamping system included in the tester (Fig. 1) is designed to clamp disc diodes, thyristors and separate basic units. The device provides an even distribution of pressure across the entire area of the semiconductor's contact surfaces. It is a separate mechanism consisting of a frame, a drive, a misalignment compensation system and a control unit. The maximum force of 150 kN is enough to clamp large-diameter devices up to 150 mm.

Large-diameter devices have a weight of almost 3 kg. It is physically difficult for the operator to manipulate such a device, and having to use both hands increases the chance of damaging the surface of the device during installation and positioning. To measure the device in the hot state, the preheated device is installed in the clamp between two contact surfaces heated to 190 °C. In case of large-diameter devices this task becomes extremely difficult and dangerous. To resolve this issue, it was decided to equip the clamping system with a draw-out loading system. The lower contact surface automatically extends after the measurements are complete (Figure 3) allowing to easily install a large-diameter device or a device in hot state. The system is equipped with a sensor monitoring the position of the contact surface. If the surface is not properly retracted, the safety system will engage and an error will be shown on the display. For structures and semiconductors of small diameter with weight from 70 to 1000 g, it is much simpler and faster for the operator to install them in the clamp with one hand or tweezers, while the draw-out system will be

unnecessary and take extra time. When needed, the draw-out system can be turned off using the touch screen.

To draw out the lower stand and to move the middle plate of the clamp it is necessary to disconnect the bifilar power line. A pneumatic contactor was developed and tested for this purpose. It provides reliable current flow without burning and sticking its contact surfaces.



Figure 3: The clamping system with extended draw-out system

Poor contact surface of the clamping system (Figure 4) can damage the exterior of a semiconductor device and it would need to get scrapped. Therefore, the replaceable upper and lower contact surfaces have a high tolerance for flatness and a roughness of Ra 0.8. For convenience, the surface is quickly detachable, so that replacement of damaged or worn replaceable plates requires short downtime of the equipment. A worn replacement plate can pass grinding and then it can be used again in the clamping system.

For high-amplitude current pulses it is critically important to ensure even distribution of force throughout the contact surface of the semiconductor. Since the areas with concentrated force have minimal resistance and the current flows along the path of the least resistance, high current pulses can cause local overheating and failure of the device. To solve this problem, a system was created to compensate the misalignment of the contact surfaces, thereby increasing the uniformity of the force distribution and, thereby, the current flow through the contact surface of the device. The upper and lower contact surfaces are mounted on spring-loaded hinges. If the surfaces were not parallel before clamping, they get aligned due to spring-loaded hinges. To compensate for the plane-parallel movement that occurs during this alignment, the lower contact surface is mounted on a thrust bearing. This solution improves the distribution of force and reduces the likelihood of damage to the device. The contacts are connected to the power bus with highly flexible braided wire (6th class of flexibility). Using such a flexible connection provides free movement of the compensation system.

The initial design had a single hinge on the lower contact surface, but a large number of tests and trial operation demonstrated inadequate

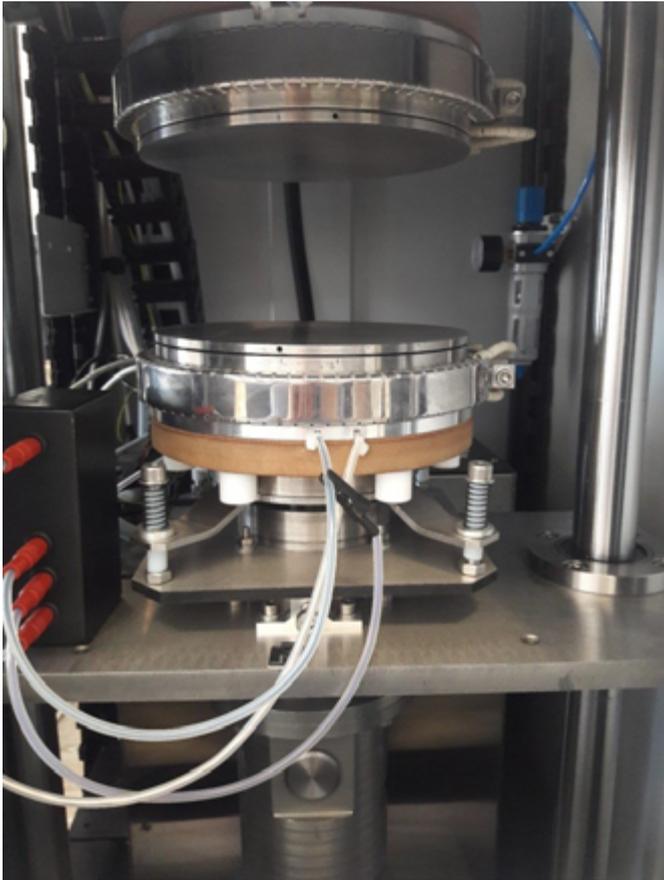


Figure 4: Contact surfaces of the clamping system

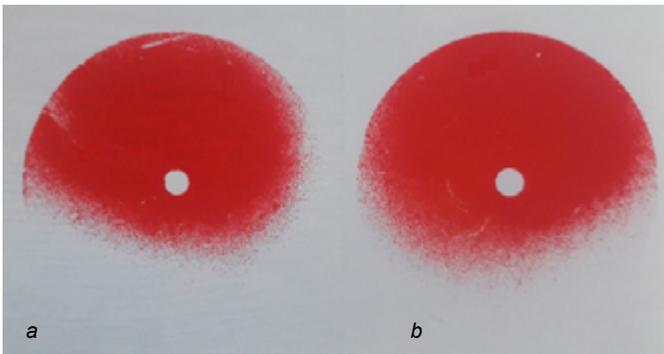


Figure 5.1: a – upper contact surface; b – lower contact surface.

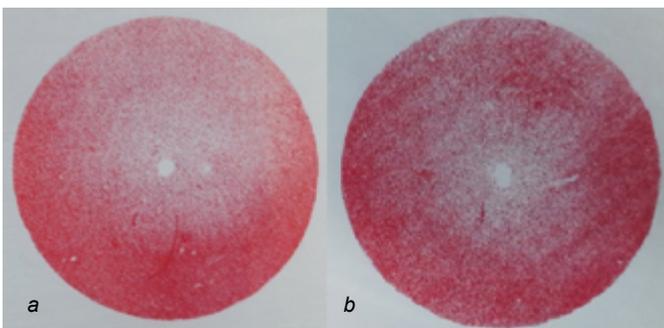


Figure 5.2: a – upper contact surface; b – lower contact surface.
Figure 5: Force distribution between the contact surface and the semiconductor

force distribution and a high chance of damage to small-diameter devices, so it was decided to add it to the upper contact surface too. Figure 5.1 shows the force distribution between the device and the contact surface of the clamping unit with one hinge, and Figure 5.2 with two hinges.

The clamping system is equipped with a servodrive allowing to control the clamping speed and position of the lower contact surface. For higher productivity, the clamping is divided into stages. Initially the drive develops maximum speed, but then the speed is reduced before the moment of clamping to prevent impact and damage to the device under test. The clamping system has an electromagnetic brake that can maintain maximal force for a long period with high accuracy without putting the load on the drive, making it possible to carry out long-term measurements and significantly increase the drive's service life. The drive mechanism is based on a ball screw capable of developing high force and high accuracy of vertical positioning of the device.

The device is also equipped with a heating system to take measurements in the hot state. A ring heater around the contact surface was selected for this purpose since such arrangement does not affect the force distribution. Cartridge or spiral heaters require to make mounting holes in the base of the contact surface resulting in distorted force distribution. Flat heaters were excluded as they are not designed for heavy loads. The heating system is capable of reaching and maintaining a given contact surface temperature of up to +200°C. A temperature regulator and thermal resistance sensors are installed in the measurement zone to maintain and control the temperature.

The clamping system is equipped with potential contacts to measure static losses. They are located in the center of the contact surfaces. The first version had spring-loaded contacts that did not produce expected results. The contact operates at high temperature and experiences mechanical stress during installation. The self-made contact often failed due to sticking, burning and damage, so it was decided to increase reliability by using ready-made spring contacts. Several alternatives were reviewed for this purpose and a series of tests was carried out. The contacts were selected based on dimensions, thermal parameters and spring elasticity. The upper threshold of the operating temperature was at least +200°C. The spring elasticity was chosen based on the weight of the smallest device so that the spring elasticity did not exceed its weight, so a contact was chosen with spring force of not more than 0.8 N. After long-term operation of the selected contacts from several manufacturers to compare their reliability it was decided to use spring contacts made by INGUN.

For operator's safety, an optical safety shutter is installed to prevent access to the working area of the clamping system during testing. Its operation is based on a light curtain of infrared rays formed between the emitter and the receiver located on the same axis. If the beam gets blocked during the device clamping and measuring procedure, it sends a signal to the commutation unit which disconnects the measuring units by hardware and connects the tested device to protective ground, so that the accumulated charge cannot harm the operator. Then the signal is sent to the control unit of the clamping system and the clamping process is suspended. The whole process of stopping measurements and turning off the clamping system takes place in a split second. The emergency stop button located in front of the operator's workplace in easily accessible place works in the same way.

Design of the tester also accounts for the influence of the electromagnetic field loop that is formed when the current flows through the power buses and contacts of the clamping system. A bifilar arrangement

of power buses and a material with a low magnetic permeability index were chosen to minimize its effect on measurements. Initially, steel 40X13 was used as the material of the contact surface resulting in transformation effect or the effect of electromotive force induced to the potential removal line. To understand how this effect occurs, consider the system and the principles of the transformer operation. It is based on the phenomenon of electromagnetic induction. This phenomenon arises from the presence of an alternating magnetic field; it is created in a magnetic circuit consisting of a flux guide with electric windings. One winding is connected to an AC source and is called primary, the other winding is used to remove voltage to power the

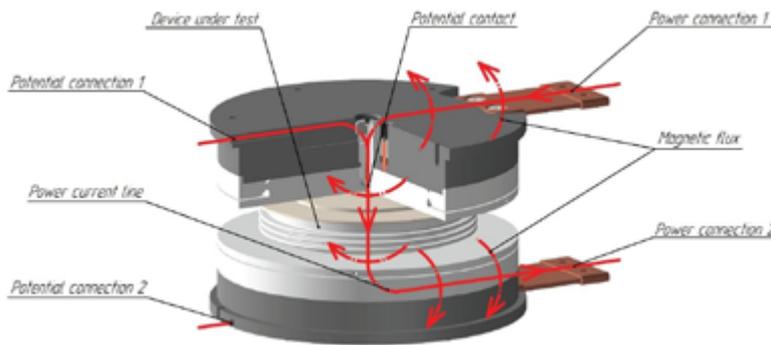


Figure 6: Diagram of creating a parasite transformer in the clamping system

load, this winding is called secondary. If an alternating voltage is applied to the primary winding, alternating current will flow through it, creating an alternating magnetic field around the winding and in the flux guide. It forms a magnetic flux, which passes through the flux guide and crosses the primary and secondary windings and inducing alternating electromotive forces in them.

The clamping system has a power current circuit that passes through the device under test and forms the primary winding of the parasite transformer (Fig. 6). It is necessary to measure the voltage drop that occurs on the power semiconductor device when the power current flows. It is achieved using potential spring contacts located in the center of the upper and lower contact surfaces, which form the secondary winding of the parasite transformer together with the wires. The core of the parasitic transformer is formed by contact surfaces. The additional electromotive force occurs on potential lines as follows. The power current flows through the device along the power circuit and an alternating magnetic field arises, the lines of which are directed according to the screwdriver rule. Accordingly, concentration of the magnetic field in the space between the buses is

higher since the magnetic field created by the power conductors is added up. The magnetic field is much weaker at the point where the potential wires are located because it is farther from power buses. Using martensitic steel 40X13 with high magnetic permeability index as the contact node material enhanced the transformation effect. Therefore, it was decided to use D16T aluminum alloy as the main material of the contact unit, and to make the replaceable plate from austenitic 12H18N10T stainless steel. These materials have a low magnetic permeability index. Steel 12X18H10T is hard enough to use as a contact surface. The aluminum alloy D16T is not suitable for the contact surface, as it is a soft material. Using it results in traces

remain on the contact surface in after several clamping operations, causing damage to the surface of the device.

To summarize, the test equipment developed and manufactured by the Automation Laboratory of Proton-Electrotex JSC meets the requirements of a wide range of consumers. Modular design of the testers allows the customer to select all the necessary parameters. Using components of well-known leading manufacturers ensure reliability of the equipment. Each case of negative feedback acquired during operation was followed by an in-depth analysis (FMEA – failure mode and effects analysis). This approach allowed to offer high-quality ergonomic equipment.

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Piece of Metal or Highly Innovative Product?

How 3D Printed Liquid Cooled Heatsinks Brings Innovation Into a Stale Industry

Aachen, Germany based company IQ Evolution manufactures liquid cooled heatsinks which are made of stainless steel, ultra-light weight, and can be even integrated into the PCB. Further they are 3D printed using a laser process to selectively melt powder to form the heatsinks. The water flow and disturbances within the heatsink have been further optimized, increasing the heatsinks heat flux density to values between 150-200W/cm² (2.000.000W/m²!!!).

By Dr. Thomas Ebert, CEO, IQ Evolution, Christopher Rocneanu, CEO, Foxy Power

Heatsinks from IQ Evolution can increase reliability by enabling extended life of power semiconductors, reduce size, weight, and volume of the system, and thus reduce system costs of the end application. In cooperation with the Institute for Power Electronics and Electrical Drives (ISEA), Aachen a 20kW DC/DC converter has been built with a world record power density of 53kW/kg or 98kW/l. For reference, NASA has asked in the past for 26kW/kg in their state-of-the-art converter.



Figure 1: IQ-Twin

Introduction of the company

IQ Evolution has been founded in 2006 by Dr. Thomas Ebert as a spin-off from RWTH Aachen. After acquiring the first printer machine, the first Nickel based heatsinks have been manufactured and sold into the high-power laser diode market. Throughout the years various patents have been granted worldwide and the latest has been received for a high-power diode laser cooler with a matched CTE (Coefficient of Thermal Expansion, a matched CTE is beneficial for improved reliability and thermal resistance). With various key players as reference customers it is safe to say that the technology has been successfully established in the diode laser market, which typically requires high performance and very reliable products.

Expansion into power electronics market

Recently, the company decided to expand its product portfolio and move into power electronic applications such as electric vehicles, electric aviation motor drives, energy storage, renewables and others. One key challenge has been that Nickel as a material is export restricted, thus complicating the quick adoption into various

applications. Through an artificial intelligence-based optimization of the internal structure, the thermal performance of the heatsinks was significantly increased making it possible to use stainless steel. But first a few basics to explain the process in more detail.

The versatility of 3D printing

The 3D printing (additive manufacturing) manufacturing process of the metal heat sinks does not require any moulds or tools and allows customized cooling solutions. Highly effective cooling structures including inlet areas are manufactured in the micrometer range. The IQ Evolution process enables the production of (micro-) structures that are suitable for economical use in industry, for example, with exceptionally thin cooling plates for integration in multilayer printed circuit boards. Almost all materials can be processed or used as alloys, even adding a layer of insulation material is possible. Complex shapes, which were neither theoretically nor economically possible with conventional processes, can be produced economically with SLM (Selective Laser Melting). As a rule, almost all melt-able materials can be used (such as stainless steel, copper alloys, aluminum, titanium, chromium-cobalt-molybdenum, bronze, nickel, etc.). Various material combinations within a component are also possible. Interesting examples of applications in need of liquid cooling are industrial applications such as high-power laser diodes, power supplies for lasers, server, telecom and aviation or automotive applications such as onboard chargers, DC/DC converters and traction inverters. But not only semiconductors can be cooled. Cooling passives elements such as coils and transformers is necessary as well and will be described in more details in future articles.

In general, the process is suitable for rapid prototyping as well as fast ramp up series production. High volume quantities can be easily achieved as only a few steps are manual and scaling production is done through parallelization of process chains.

To go into production, following steps are required. First a technical discussion with the customer will ensure best and efficient system cooling with an ideally as small cooler as possible. After the customer provides a CAD file a 3D model of the heat sinks is generated which

IQ Evolution will then feed into the machine. Metal powder is loaded into the machine and a laser is used to selectively melt powder particles where desired. As the process does not require any further tools, manufacturing identical parts as well as even variants are possible. One must remember that e.g. adding a hole means additional working steps in conventional technologies but in 3D printing it means less machining time which equals cost. Besides, it is a paradigm shift to place all heated parts into one efficient but small and thin cooler instead of spreading the heated parts all over the PCB. A video of the manufacturing process is available at www.IQ-Evolution.com.

AI optimization increases performance and allows different materials

The great advantage of this process is that structures that are optimized in CAD or a corresponding simulation can be loaded directly into the machine and executed. This is particularly interesting when the optimization (up to 20%) is carried out using artificial intelligence. As a result, even very unusual shapes are possible. Complex structures are very suitable for being optimized by means of AI.

With an initial basic starting structure, the AI algorithm simulates the process under special observation of the pressure drop and heat flux. The results from this simulation are used to intelligently modify the internal cooling structures, and the process starts again. The AI algorithm keeps the beneficial changes and rejects negative ones. At the end, after several thousand modifications, the result is a near optimal cooling and supporting structure. The AI work has been done by Diabatix, Belgium.

This possible increase in performance has prompted IQ evolution to consider a change in the material used. Whereas pure nickel had previously been used, mainly because of its high thermal conductivity, it is now possible to think about other materials which trade off slightly worse thermal conductivity for lower material cost and ease of export restrictions.

First evaluation of a stainless-steel 3D printed heatsink

In this case stainless steel (Material No. 1.4404) was chosen because it is corrosion free which increases the lifetime of the heatsink. Despite its 10x lower thermal conductivity, the first tests with substitute heat sources showed no difference in cooling performance compared to the previously manufactured heat sinks of this series. On the contrary, the optimized heat sinks made from stainless steel showed a better performance and higher than expected dissipation capability.



Figure 2: IQ-Four

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With the AI optimization the technology is capable of safe and reliable cooling with heat flux densities of over 200W/cm² (pure water, no TIM). Even higher densities are possible but need to be further evaluated and measured appropriately. Partnering with the Institute for Power Electronics and Electrical Drives at RWTH Aachen University, the cooling effect on components, and the potential savings in weight, volume and system cost in real use applications has been evaluated.

Examples of the new generation of stainless-steel heat sinks are the IQ-Twin (see Figure 1) or IQ-Four (see Figure 2) which are designed to simultaneously cool two, respectively four TO-247 or similar packages. The measurements for this were carried out by ISEA. SiC-MOSFETs (C3M0016120K) in a TO-247 package were used, which were energized with 50 A for the test. A Hi-Flow[®]-300P insulation foil is used against the metal heat sink to electrically isolate it. The cooler was operated at a fluid pressure of 1.2 bar, resulting in a flow rate of cooling medium (normal water) of one liter per minute. The ISEA experts measured the electrical power delivered to the MOSFETs, the actual electrical power absorbed by the MOSFETs and the amount of heat dissipated by the heat sink.

750 W dissipated power could be transferred from the stainless-steel heat sink into the water. This results in a dissipated power loss of 187 W per MOSFET. With a footprint (cooling area) of the TO-247 package of slightly more than one cm² this results in a heat flux density of more than 175 W/cm².

The AI-optimized stainless-steel heat sink has thus passed its test of courage and found its way into the standard product range of the IQ evolution. In general, stainless steel is now the standard material for these micro-heatsinks, which are manufactured using 3D printing. Should a power electronics application require even higher cooling performance, Nickel or Aluminum alloys could be used again in the heat sink base material at any time, so that customers can benefit from an up to 20% higher thermal conductivity.

Confirmation of the laboratory test in the real application

But laboratory tests are only one side of the coin. What about the other side, the real application? ISEA subjected the metal heat sink to practical tests: Impressed by the enormous cooling capacity and the confidence now placed in the 3D-printed stainless-steel coolers, they found an application in which the new type of cooler should prove itself, a DC/DC converter.

The field test specified that four 1000V SiC MOSFETs in a TO-247 4L package with Kelvin Source connection should be effectively cooled by the printed heat sink, in this case an IQ Double Four (See Figure 3). In contrast to the laboratory setup, the cooler was now unfolded so that the four MOSFETs are no longer two pairs opposing each other



Figure 3: IQ-Double-Four. One side being used to cool the MOSFETs, the other to cool inductors and other components.

but are all placed next to each other. The separate supply of cooling water to the pairs of two is also retained in this arrangement; it is located inside the heat sink and is therefore not visible from the outside. The modified arrangement of the MOSFET packages has a specific purpose: The underside of the heat sink remains free and is thus able to take over further cooling tasks.

The heat sink is mounted with the underside close to the coils and cast together with the coils in the housing. In this way, not only the MOSFETs, but also the coils and the inner workings of the converter are cooled. In addition to the electronics required for the converter, the voltages are also monitored via sensors. A galvanically isolated microcontroller is also integrated for control and communication.

The use of the cooling capacity of the IQ heatsinks and their implementation in the converter design resulted in an extremely compact component, which would not have been possible without the use of the optimized heat sinks. The result is an ultra-compact bidirectional DC/DC converter (see Figure 4) that operates in the voltage range between 400 and 800 V at a frequency of 450 kHz. The DC/DC converter can transmit 20.6 kW. With dimensions of 90 mm x 65 mm x 35 mm, this means a power density of 98 kW per liter or 53kW/kg; according to Prof. De Donker from ISEA this value is a world record in power density.



Figure 4: 20kW DC/DC Converter. Picture courtesy of ISEA, RWTH Aachen

Outlook and summary

In this article we demonstrated what impressive results and heat flux densities can be achieved with the IQ Evolution technology. However, we are just in the beginning of optimizing power electronic cooling. It is the target of IQ evolution to unleash the full potential of semiconductors by optimizing the packages with development partners. Heat sinks with an electrically insulated surface are already being developed, as is the possibility of applying conductive structures directly to the heat sinks. If one thinks about baseplate-less modules, sintered to an optimized, electrically isolated heatsink a quantum leap can be achieved in terms of system cost, weight, and volume reduction as well as efficiency. We are already well progressed in this development and the first measurements look very promising. Furthermore, we are working with partner on developing ideal solutions to cool passive elements such as inductors and transformers. Interested customers can visit the website <http://www.iq-evolution.com> or contact sales@iq-evolution.com (+4915121063411) for inquires and further information.

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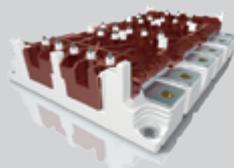
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Bipolar, Single Output, and Adjustable Power Supplies Based on the Common Buck Converter

A bench-top power supply (PS) tends to have an even number of terminals (ignoring the chassis port)—with one positive terminal and one negative terminal. Using a bench-top supply to produce a positive polarity output is easy: set the minus output to GND and the positive output voltage at the plus output. It is just as easy to produce a negative supply by reversing the setup. But what about producing a bipolar supply, where positive and negative voltages are both available to the load?

By Victor Khasiev, Senior Application Engineer, Analog Devices

This is relatively easy, too—just connect the positive terminal of one lab channel to the negative of another channel and call that GND. The other two terminals, minus and plus, are the positive and negative supplies, respectively. The result is a three-terminal bipolar power supply with available GND, positive, and negative voltage levels. Because three terminals are used, there must be some switch between positive and negative supplies downstream of the power supply.

What if an application calls for the same power supply terminal to be positive or negative—a setup where only two terminals are provided to the load? This is not a purely academic question. There are applications in automotive and industrial environments that require bipolar, adjustable two terminal power supplies. For instance, two terminal bipolar power supplies are used in applications ranging from exotic window tinting to test and measurement equipment.

As noted earlier, a traditional bipolar PS produces two outputs using three output terminals: positive, negative, and GND. In contrast, a single output power supply should be equipped with only two output terminals: one GND and another that can be positive or negative. In such applications, the output voltage can be regulated relative to the GND by a single control signal, in the full range from the minimum negative to maximum positive. There are controllers that are specifically designed to implement the bipolar supply function, such as the LT8714, a bipolar output synchronous controller. Nevertheless, for many automotive and industrial manufacturers, testing and qualifying a specialized IC requires some investment in time and money. By contrast, many manufacturers already have prequalified step-down (buck) converters and controllers, as they are used in countless automotive and industrial applications. This article shows how to use a buck converter to produce a bipolar PS when a dedicated bipolar supply IC is not an option.

Circuit Description and Functionality

Figure 1 shows a buck converter-based solution for a bipolar (two-quadrant) adjustable power supply. The input voltage range is 12 V to 15 V; the output is any voltage in the ± 10 V range, adjusted

by the control block, that supports loads up to 6 A. The dual output step-down controller IC is the central component to this design. One output, connected per buck-boost topology, generates a stable -12 V (that is, the -12 V negative rail in Figure 1, with its power train comprising L2, Q2, Q3, and output filter CO2).

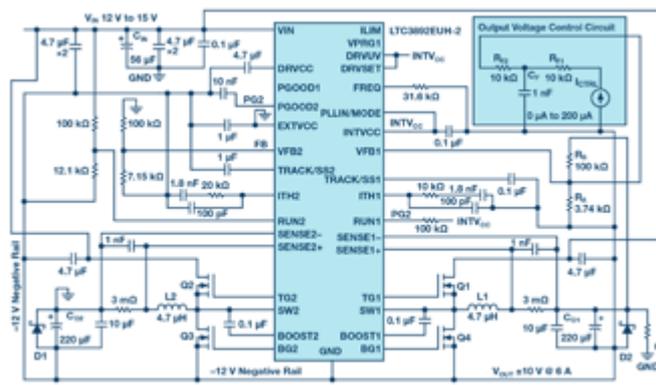


Figure 1: Electrical schematic of the two terminal, bipolar, adjustable power supply.

The -12 V rail serves as ground for the second channel with the controller's ground pins connected to the -12 V rail as well. Overall, this is a step-down buck converter, where the input voltage is the difference between -12 V and V_{IN} . The output is adjustable and can be either positive or negative relative to GND. Note the output is always positive relative to the -12 V rail and includes a power train comprising L1, Q1, Q4, and C_{O1} . The feedback resistor divider R_B – R_A sets the maximum output voltage. The value of this divider is adjusted by the output voltage control circuit, which can regulate the output down to the minimum output voltage (negative output) by injecting current into R_A . The application start-up characteristics are set by the termination of the RUN and TRACK/SS pins.

Both outputs function in forced continuous conduction mode. In the output control circuit, the 0 μ A to 200 μ A current source, I_{CTRL} , is connected to the negative rail as tested in the lab, but it can be ref-

erenced to the GND as well. The low-pass filter $R_{F1}-C_F$ reduces fast output transients. To reduce the cost and size of the converter, output filters are formed using relatively inexpensive polarized capacitors. The optional diodes D1 and D2 prevent developing the reverse voltage across these capacitors, especially at startup. There is no need for the diodes if only ceramic capacitors are used.

Converter Testing and Evaluation

This solution was tested and evaluated based on the LTC3892 and evaluation kits DC1998A and DC2493A. The converter performed well in a number of tests, including line and load regulation, transient response, and output short. Figure 2 shows startup to a 6 A load, with a +10 V output. The linearity of the function between the control current and output voltage is shown in Figure 3. As control current increases from 0 μA to 200 μA , the output voltage decreases from +10 V to -10 V. Figure 4 shows the efficiency curves.

An LTspice® model of the bipolar, two terminal power supply was developed to simplify adoption of this approach, allowing designers to analyze and simulate the circuit described above, introduce changes, view waveforms, and study component stress.

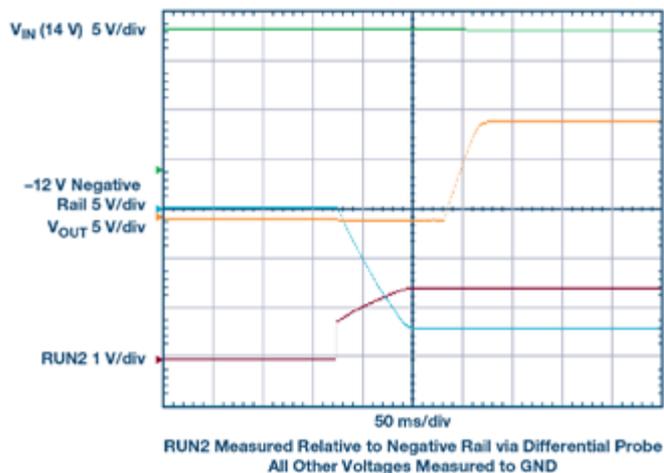


Figure 2: Start-up waveforms into resistive load.

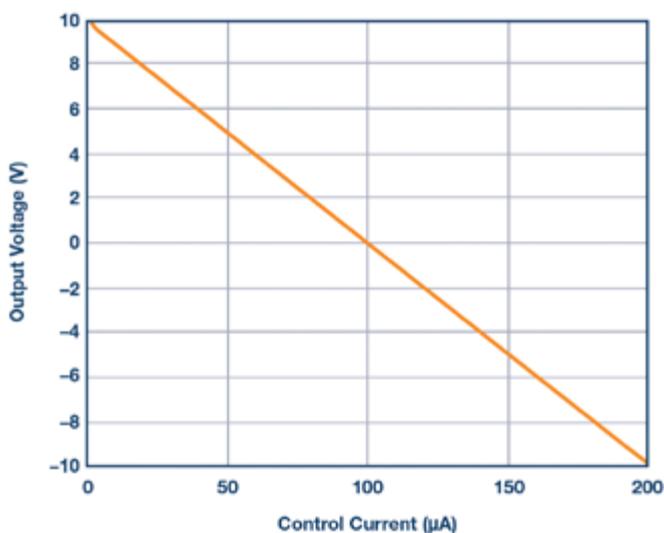


Figure 3: V_{OUT} as a function of control current I_{CTRL} . As I_{CTRL} increases from 0 A to 200 μA , the output voltage drops from +10 V to -10 V.

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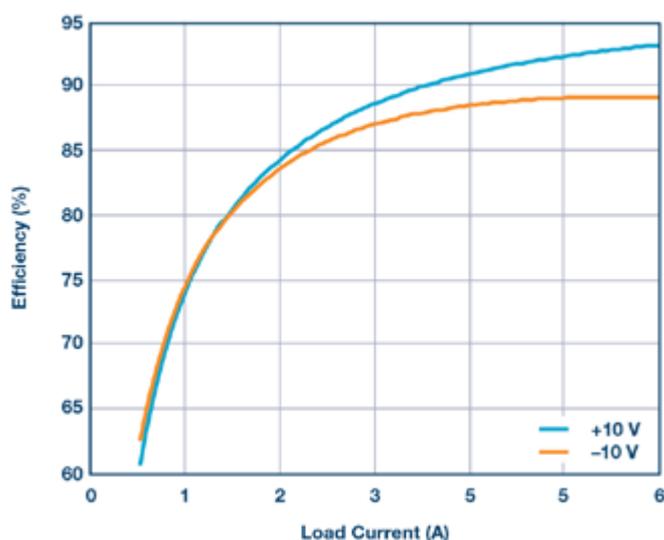


Figure 4: Efficiency curves for positive and negative output.

Essential Formulas and Expressions Describing this Topology

This approach is based on the negative rail, V_{NEG} , generated by the buck-boost section of the design.

$$V_{NEG} = V_{OUT} + V_{OUT} \times K_m \quad (1)$$

Where V_{OUT} is the absolute value of maximum output voltage and K_m is a coefficient ranging from 0.1 to 0.3. K_m limits the minimum duty cycle of the step-down converter. V_{NEG} also sets the minimum value of V_{IN} :

$$\begin{aligned} V_{IN} &\geq |V_{NEG}| \\ V_{BUCK} &= |V_{NEG}| + V_{IN} \end{aligned} \quad (2)$$

Where V_{BUCK} is the input voltage for the step-down section and thus presents the maximum voltage stress on the converter's semiconductors:

$$\begin{aligned} V_{BUCK(MAX)} &= |V_{NEG}| + V_{OUT} \\ V_{BUCK(MIN)} &= |V_{NEG}| - V_{OUT} \end{aligned} \quad (3)$$

$V_{BUCK(MAX)}$ and $V_{BUCK(MIN)}$ are the maximum and minimum voltages of the step-down section of this topology, respectively. The maximum and minimum duty cycles and inductor current of the step-down section can be described by the following expressions, where I_{OUT} is output current:

$$\begin{aligned} D_{BUCK(MAX)} &= V_{BUCK(MAX)} / V_{BUCK} \\ D_{BUCK(MIN)} &= V_{BUCK(MIN)} / V_{BUCK} \\ I_{L(BUCK)} &= I_{OUT} + \Delta I_1 \end{aligned} \quad (4)$$

The duty cycle of the buck-boost section of the PS:

$$D_{BB} = |V_{NEG}| / (V_{IN} + |V_{NEG}|) \quad (5)$$

The input power of the step-down section and, correspondingly, output power of the buck-boost:

$$P_{OUT(BB)} = (V_{OUT} \times I_{OUT}) / \eta \quad (6)$$

The converter power and input current.

$$\begin{aligned} I_{OUT(BB)} &= P_{OUT(BB)} / |V_{NEG}| \\ I_{L(BB)} &= I_{OUT(BB)} / (1 - D_{BB}) + \Delta I_2 \end{aligned} \quad (7)$$

The output voltage changes are executed by injecting current into the feedback resistor divider of the step-down section. Setting up the output voltage control is illustrated in the output voltage control circuit section of Figure 1.

If R_B is given, then

$$\begin{aligned} P_{BB} &= P_{OUT(BB)} / \eta \\ I_{BB} &= P_{BB} / V_{IN} \end{aligned} \quad (8)$$

where V_{FB} is the feedback pin voltage.

When the current source I_{CTRL} injects zero current into R_A , the output voltage of the buck converter is the maximum positive value ($V_{BUCK(MAX)}$) relative to the negative rail and maximum output voltage ($+V_{OUT}$) relative to GND. To produce a negative output voltage to the load (relative to GND), the output voltage is reduced to its minimum value, $V_{BUCK(MIN)}$, relative to the negative output voltage ($-V_{OUT}$), by injecting ΔI into resistor R_A of the buck's voltage divider.

Numerical Example

By using the previous equations, we can calculate voltage stress, current through the power train components, and the parameters of the control circuit for the bipolar power supply. For instance, the following calculations are for a supply generating ± 10 V at 6 A from a 14 V input voltage.

If K_m is 0.2, then $V_{NEG} = -12$ V. Verifying conditions of minimum input voltage $V_{IN} \geq |V_{NEG}|$. The voltage stress on the semiconductor's V_{BUCK} is 26 V.

The maximum voltage of the step-down section is $V_{BUCK(MAX)} = 22$ V, relative to negative rail, setting the output voltage $+10$ V relative to GND. The minimum voltage, $V_{BUCK(MIN)} = 2$ V, corresponds to the output voltage of -10 V relative to GND. These maximum and minimum voltages correspond to the maximum and minimum duty cycles, $D_{BUCK(MAX)} = 0.846$, $D_{BUCK(MIN)} = 0.077$, and $D_{BB} = 0.462$.

Power can be calculated by assuming an efficiency of 90%, producing $P_{OUT(BB)} = 66.67$ W, $I_{OUT(BB)} = 5.56$ A, $I_{L(BB)} = 10.37$ A, and $P_{BB} = 74.074$ W.

For an output voltage of $+10$ V (as per Figure 1), the control circuit current, ΔI , is $0 \mu\text{A}$, whereas for an output voltage of -10 V, $\Delta I = 200 \mu\text{A}$.

Conclusion

This article presents a design for bipolar, two terminal power supplies. The approach discussed here is based on step-down converter topology, which is a staple of modern power electronics, and thus available in a variety of forms, from simple controllers with external components to complete modules. Employment of step-down topology gives the designer flexibility and an option to use prequalified parts, which saves time and cost.

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Preserved Echoes Diagnose Component Failures

The failure may involve a military system, medical equipment, or any other application where sudden shutdown is undesirable and serious. A subsystem fails electrically, and the immediate cause is pinpointed as the unexpected failure of a single component. This component, and the unit it is installed in, both have good track records, so there is interest in learning the precise cause of the failure, since it seems possible that the present failure might involve some type of internal structural failure within the component.

By Tom Adams, consultant, Nordson SONOSCAN

Acoustic micro imaging (AMI) tools can nondestructively image internal structural anomalies such as cracks or delaminations, but in some cases the component is not available for imaging to determine the cause of the failure. The component may be irretrievable because it is traveling in space, or if earthbound it may have been entirely destroyed by the failure.

In such cases the outlook will be brighter if precautions have been taken against such an event. Before a component is mounted onto its board, all echoes from the entire volume of the component can be collected and preserved by the Virtual Rescanning Mode™ (VRM), one of the imaging modes in the C-SAM® line of acoustic micro imaging tools from Nordson SONOSCAN.

These tools pulse ultrasound into a sample and collect the return echoes, which are produced only by material interfaces. A pulse sailing through featureless silicon or mold compound sends back no echoes, but when it strikes the interface between the current material and another material, it sends back to the transducer that launched the pulse an echo containing information about the two materials that meet at the interface.

Before they are mounted on boards, loose components may be mass screened by an automated acoustic micro imaging tool to prevent components having structural defects from being used in assembly and causing eventual field failures. The tool typically images a specific depth of interest - the bonding of the solder bumps to a die face in a flip chip, for example. Gating means that only echoes from the selected depth are used to make the acoustic image, and to classify the component as accept/reject. Routine automated inspection for structural defects may therefore look at only part of the thickness of a sample, and in that gate it will use techniques for finding the most common or most critical structural defects.

VRM vastly supplements this process by scanning and collecting all of the raw echoes received from all depths at each of the thousands of x-y locations where a pulse is launched into the sample. This method collects echoes returned from the entire volume of the component. The result is a large amount of data - amplitude, polarity, arrival time and frequency - that can be analyzed as desired. (Standard C-mode imaging, by contrast, selects at each x-y location only the amplitude of a single echo. The user cannot later recapture the additional values from the amplitude data.)

The VRM echoes are preserved in a 'matrix' file. Because echoes are generated only at material interfaces, most of the volume of the component will produce no echoes because it consists of homogeneous material such as silicon. But VRM generates and records all of the echoes from all of the material interfaces in the entire x-y-z volume of the component - far more than is collected by standard mass acoustic inspection.

When a component that has been archived by VRM fails in service, the matrix file of echoes is retrieved and scanned as though it were the physical component in order to gain insight into what may have caused the failure. Matrix file scanning is typically more comprehensive than the original mass scan: it contains all echoes, and not just the echoes from a depth where failures most often occur. What VRM is looking for is an anomaly, possibly quite small. The anomaly may, for example, have been buried in a larger echo and thus not have been detected earlier. VRM scanning may involve all depths within the component, and may use any of the 15 or so C-SAM imaging modes. The anomaly that caused the field failure may be identified, imaged and analyzed, for example, by using the non-destructive cross-sectioning mode, the three-dimensional mode, the thin slice mode, or any other mode.

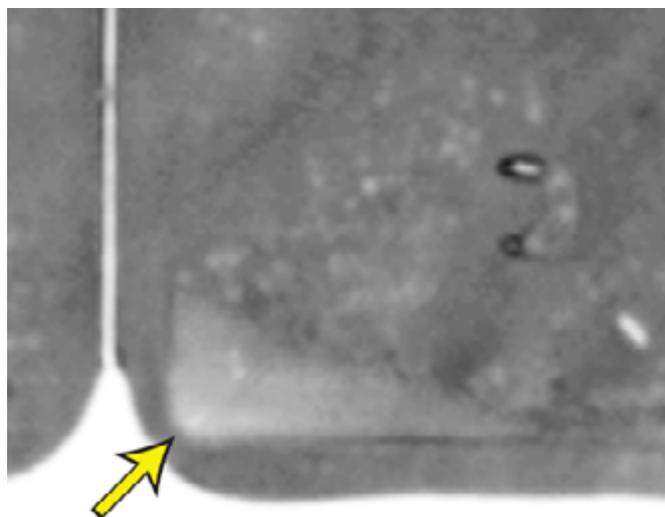


Figure 1: The appearance of a tiny corner of this IGBT's raft - barely within the gate being imaged - indicates that the raft is tilted rather than flat.

Figure 1 is the acoustic image constructed from the VRM matrix file of an IGBT module. The die of an IGBT can be damaged by contamination left by evaporating water. High voltage current may traverse contaminated areas and cause the IGBT to fail. IGBT modules are therefore typically imaged from the bottom side by using an inverted imaging tool to pulse ultrasound through the heat sink and collect the return echoes. In this way the die is kept away from the coupling fluid.

It was thought that the eventual failure of the IGBT module may have been related to voids in the solder bonding the heat sink to the ceramic raft, so gating encompassed almost the entire calculated depth of solder, while avoiding the heat sink above the solder and the ceramic raft below the solder. Figure 1 displays about 3% of the area of one die. Because the solder itself is homogeneous, it returns no echoes, and the ideal image in this situation would be featureless and solid gray, meaning "no return echoes received." In Figure 1 there are a few tiny features which are probably tiny voids at varying depths within the solder.

Near the lower left corner, however, is a pale gray feature much larger than the voids. The pale gray feature is a corner of the tilted raft that moved into the gate. Its brighter hue indicates that it is the interface between two solid materials - the solder and one corner of the ceramic raft. But the gate from which echoes were used for making this image was at a depth that should encompass only the solder layer. Deeper imaging revealed that the ceramic raft was irregularly distorted, and this corner of the raft was the highest point (when viewed through the heat sink) and the only part of the raft imaged within the whole area of the gate used to make Figure 1.

The module may have failed because the uneven thickness of the solder resulted in a temperature gradient that put mechanical stress on the raft. In conducting the post mortem on the module from the matrix file, the small corner of the raft in Figure 1 was the first clue.

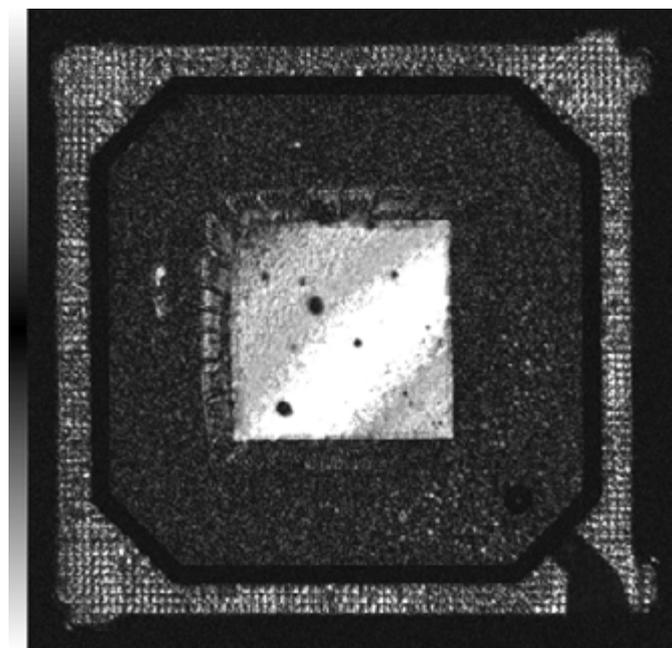


Figure 2: A very narrow (vertically) gate was used to reveal die tilting inside this plastic BGA package.

A BGA that had failed in service is shown in the VRM image in Figure 2. When the usual C-mode imaging was used on the matrix file and had not identified any pre-existing condition that could have led to an electrical failure, the same mode was used but with a much narrower (vertically) gate to accept only echoes reflected from a sequence of thin "slices" of the BGA package.

In this thin slice, one can see that the die is not flat. The lower right corner of the die is tilted downward and lies below the gate; the upper left corner is above the gate. The black features on the die are the acoustic shadows of voids in the underfill above the gate.

The tilt would put some degree of stress on wire bonds. Given time and thermal cycling, one or more wires may have broken to cause the failure that generated the need to examine the component's matrix file. In planar imaging, as used during pre-mounting inspection, a thicker gate would have been used, with the result that all of the die would have the same color and would therefore appear to be horizontal.

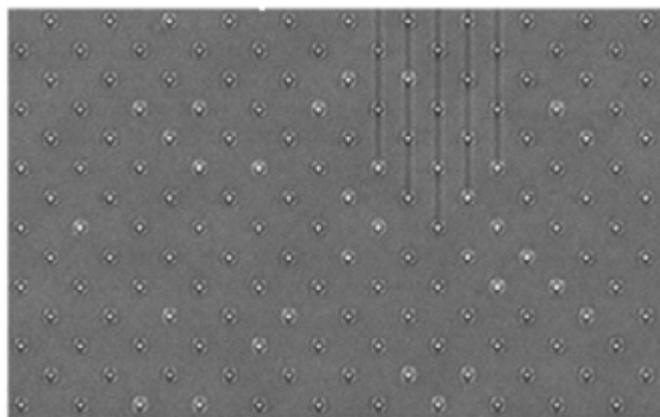


Figure 3: Variations in the brightness of the bumps indicate some disbonds in this flip chip.

The image in Figure 3 was produced from the matrix file of a flip chip, and was imaged through the die at a frequency of 230 MHz to achieve high resolution. The images are gated on the depth of interest: the bonding of the solder bumps to the die.

The bumps themselves range from bright to dark, bright suggesting some degree of disbond from the die because there is an air gap reflecting nearly all of the arriving ultrasound. Surrounding each bump are four copper pads, whose shades also range from bright to dark, and for the same reason.

In each of the absent devices described here, VRM was able to extract from the preserved matrix file an anomaly that might have caused the component to fail electronically. The data in the three images does not conclusively prove that these were the existing internal anomalies that led to failure. But if VRM investigation reveals no other candidates matching the manner and extent of failure that occurred, these are very good candidates. It should be mentioned that recent advances in automated acoustic scanning may find an anomaly that otherwise might be found only after it has caused a failure. Thin-slice imaging, for example, can now be performed by automated tools. If the tilted die in Figure 2 had been imaged in this manner, it might never have become a field failure.

Universally Accessible Education in Power Electronics

Python Power Electronics is a free and open source circuit simulator for power engineers. A question often asked is what is the need for another circuit simulator when there are numerous simulators already available? The answer is that when I started this project, I was not attempting to build a circuit simulator but rather to understand the process of circuit simulation to eventually create educational resources.

By Dr. Shivkumar V. Iyer, Python Power Electronics

Currently, I am an online instructor with three courses in electrical engineering with several more planned in the near and distant future. Power electronics is a domain that has immense capability to solve some of our most significant challenges – climate change, mobility, and many more. Besides infrastructure, government policies and investment, one of the major factors that can influence how strongly power electronics can transform our future is the opportunities to learn. In a domain like power electronics, education cannot merely be limited to universities and colleges but has to be accessible to an engineer throughout his professional life. This requirement of life-long access to education applies to every domain. However, the challenge in learning power electronics after entering the workforce is compounded by the fact that learning power electronics requires specialized software as well as laboratory facilities to implement hardware. Access to laboratory facilities and equipment is a hurdle that is quite difficult to overcome, particularly in developing countries, though with the emergence of online marketplaces, the procurement of equipment and components is much easier than it was ten years back. Access to software is still restricted as most software are specialized enterprise software that are proprietary and expensive. The explosion of free and open source software that has been witnessed in software domains such as web development and artificial intelligence has not occurred in the core engineering domains. The open source software that are available are very few and limited and do not have the same level of aggressive development seen in the software domain where a new version of a package is available as often as every six months.

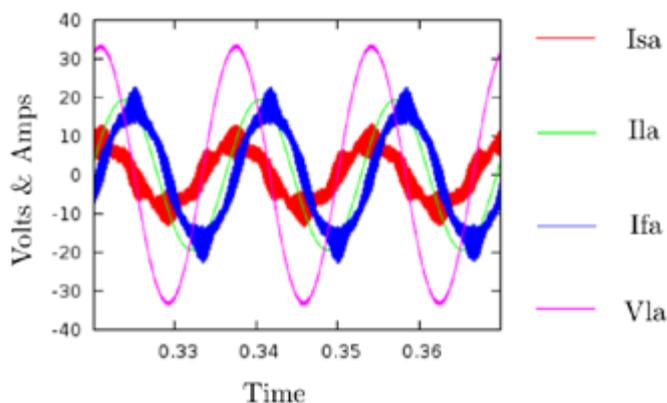


Figure 1: Simulation of a reactive power compensator using Python Power Electronics

This limitation of free and open source software in power electronics is particularly detrimental to engineers in developing countries who find proprietary software too expensive to purchase. This has in turn led to other problems such as software piracy. One of the major motivations into creating a free and open source circuit simulator for power electronics was to be able to provide every power engineer the opportunity to access educational material without licensing restrictions. By creating online courses on power electronics that contain theory and simulation examples, engineers can learn about new technologies using simulations. It can be argued that without hardware implementation, no learning in power electronics is complete. That may very well be true. However, theory and simulations can take an aspiring engineer a significant distance in becoming proficient in a new and emerging technology.

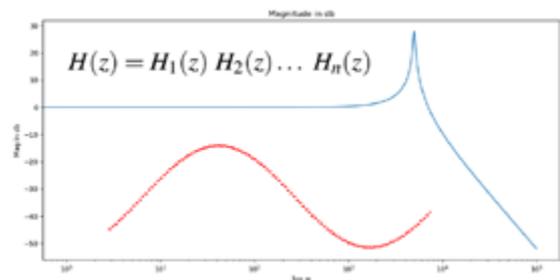
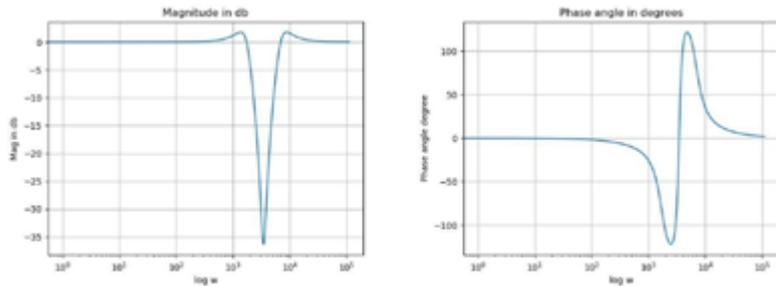


Figure 2: Course poster for the online course on digital signal processing

The next question is what is new in my courses that is not already there online and in texts? The only difference is the approach. In all my courses, I choose the Feynman technique of teaching. The first step, pick a topic. I have started with basic topics so far – simulating basic power electronic circuits, designing digital filters and simulating transformers. I am familiar with these topics. But I have never taught them before nor would I consider myself an expert. I don't consider that to be a problem, but rather welcome the need to open my eyes wide to a new topic. The second step of the Feynman technique – explain the topic as if explaining it to a child who is unfamiliar with the topic and who would be put off by a mundane treatment of the topic. I start teaching a topic from the very basic laws of electrical engineering and of physics. As an example, while describing how to design and simulate an ac-dc diode bridge converter, I use the analogy of building a reservoir to store water. I add component after component to the converter circuit while gradually describing the equivalence to the reservoir. The third step in the Feynman technique – identify any gaps in your understanding. There have been many times when my

explanation of a concept in my online course was quite obviously vague. An example, in my digital filtering course, one of the things that perplexed me was trying to understand how performing Laplace Transform on a time varying function resulted in a frequency varying function. The fourth step of the Feynman technique – go back to literature to understand better. I went back to Euler's equation



(a) Magnitude plot

(b) Phase angle plot

Figure 3: Notch filter design is taught in the online course on signal processing

and the expression of a sinusoid as an exponential of a complex number. This resulted in several lectures in my online course where I meandered through basic mathematical concepts, describing the concept of angular frequency, the exponent of a complex number and the significance of the real and imaginary part of a complex frequency.

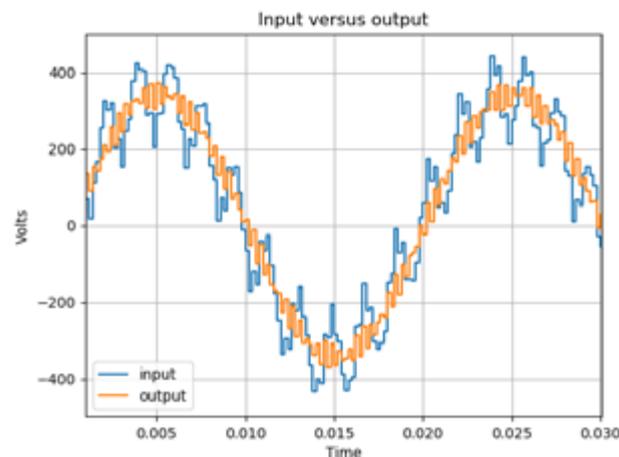


Figure 4: Implementation of a notch filter is taught in the online course on signal processing

Have students benefited? Two of my courses that have been available online for a few months are ranked as Bestseller courses on the online education platform Udemy. I have 850 students from 55 countries and every continent except Antarctica. Besides these courses, I also have my own YouTube channel by the name of Python Power Electronics. On this, I release weekly video lectures on simulation of power converters. I have

already uploaded 22 video lectures on six converters – buck converter, boost converter, buck-boost converter, Ćuk converter and SEPIC converter. I have close to 500 subscribers to the YouTube channel.

One of the reasons why these numbers are significant is that they point to a growing community of online learners in power

electronics. Once again, I try to copy over the community led development and education in the software domain where online forums and repositories like Stack Overflow or GitHub are thronging with developers asking and answering each others questions and sometimes even going so far as to solving a developer's problem completely. Numerous

developers have their blogs and newsletters where they describe in depth how to they achieve a particular task. To be able to mimic a growth comparable to the software industry, the power industry needs to build a community that is just as vibrant and willing to share information. The road ahead for Python Power Electronics is to continue on this journey. At present, I am writing a book on digital filtering for power engineers based on my second online course. After which, there will courses on

grid connected converters, voltage stabilizers, microgrids, renewable energy integration and many more. I am not an expert on any of these, but the Feynman technique that I have used so far does not need me to be one. One of the best parts of being an educator is that you embark on a journey of continuous learning.

www.pythonpowerelectronics.com

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September 2020

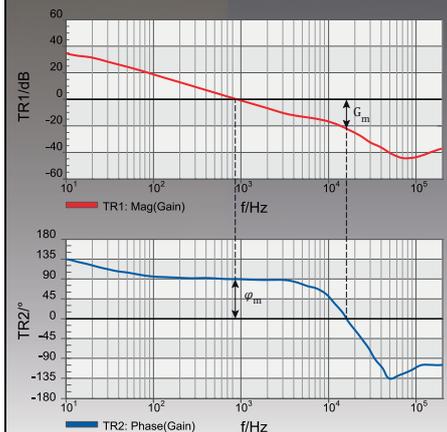
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Littelfuse announced a series of PPTCs designed to help make the next generation of today's most-used consumer electronics smaller and more reliable. The PolySwitch® zeptoSMDC series provides robust overcurrent and overvoltage protection on the signal lines for both the lithium ion battery pack ICs and fuel gauge. These PPTCs are for high voltage (13 VDC) applications. Available in the small 0201 surface-mount size, they are ideal for increasingly smaller mobile and wearable product designs. Part of the Littelfuse PolySwitch family of resettable overcurrent protection devices, the



series is best suited for consumer electronics applications such as Smartphones, Notebook PCs, Tablets, and e-Readers, Wearables (Smartwatches, Fitness Trackers), Wireless speakers, Portable game players,

Portable medical equipment and Mobile point-of-sale (POS). "The zeptoSMDC is smaller than any currently available components in its class," said Jin Xu, Product Manager at Littelfuse. "This enables electronics designers to more easily reduce the overall size of their portable, mobile, and wearable products while providing exceptional protection for the battery fuel gauge and battery management IC."

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2-Phase Stepping Motor Driver IC

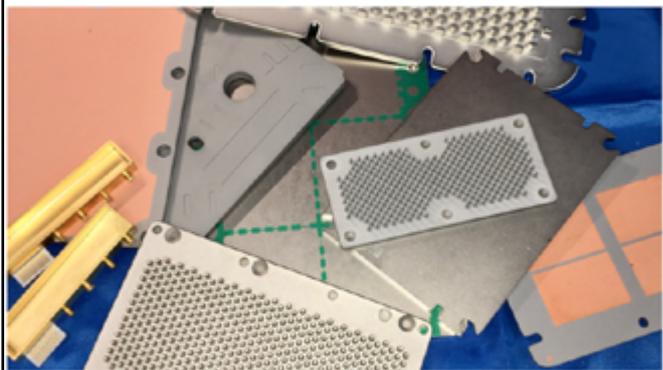
Toshiba Electronics Europe has introduced the TB9120AFTG. This constant-current 2-phase bipolar stepping motor driver, which is designed for automotive use, can significantly streamline motor system implementations. It delivers a sine-wave output signal (with up to 1/32 incremental steps supported) while requiring only a simple clock input. The need for a sophisticated microcontroller unit (MCU) or dedicated software is thereby avoided. Each of the AEC-Q100-compliant TB9120AFTG driver ICs incorporates low on-resistance DMOS FETs, and can deliver a 1.5A (maximum) current. Thanks to the large number of micro-steps they support, motor noise can be significantly reduced, with smoother operation and more precise control being benefited from. The built-in mixed decay mode helps to stabilize the current waveforms. Numerous protection mechanisms are incorporated, these include over-current and over-temperature detection, plus thermal shutdown. There is also a stall detection function. These devices are supplied in compact VQFN packages (with 6.0 mm x 6.0mm dimensions) featuring wettable flanks to allow the use of automated optical inspection (AOI) for ensuring the quality of solder joints. They support an operational temperature range covering -40°C to 125°C. Key applications include battery management systems, or refrigeration circuit expansion valves for air conditioning.

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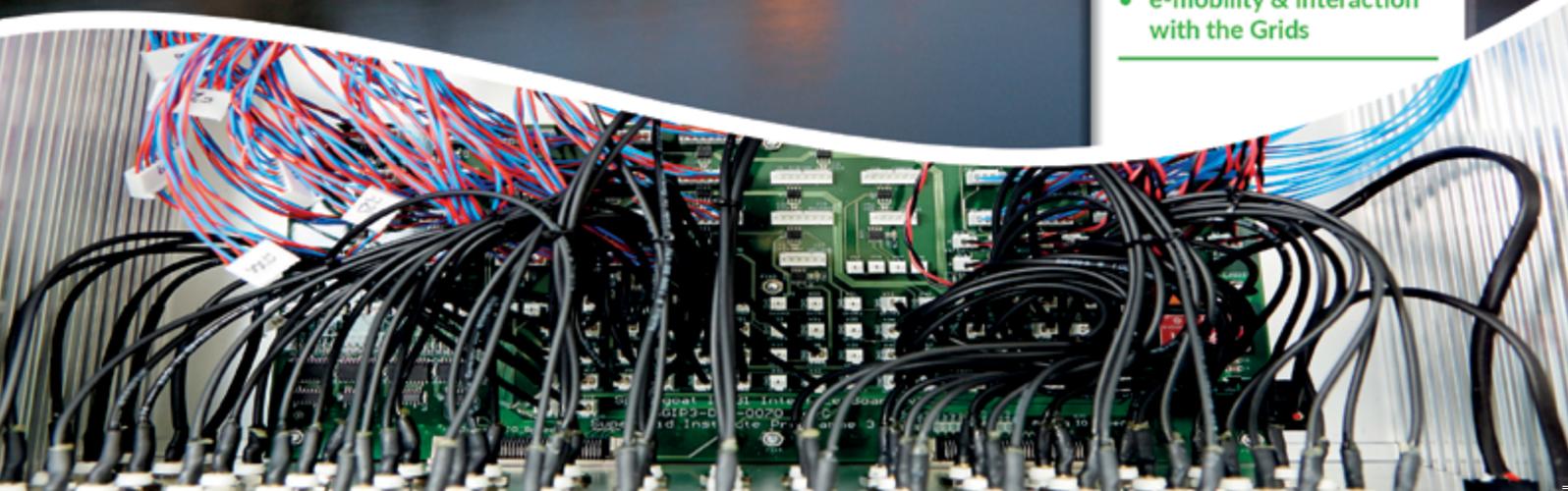


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Power Electronics Product Line

Proton-Electrotex continuously works to improve the current product line and develops new solutions in the field of power electronics. So, the company is ready to present its latest developments:

- IGBT module MIHA housing with a base width of 62 mm and an increased rated insulation voltage of 9500V. The module has several configuration schemes: half-bridge, lower and upper chopper. A special feature of this design is a wide range of operating temperatures - from -55... + 125 °C. The modules are designed for switching high-power loads and are used as part of converters and drives of small and medium-power electric motors.



- Press-Pack IGBT - module in tablet version with two-way cooling-the sealed design of the module housing makes it possible to work in explosive and aggressive environments. The module has a uniform pressure contact of the active elements, which improves the thermal cycle resistance; in emergency mode, it acquires a stable short-circuited state. The module is applicable for sequential switching circuits

and has an operating temperature range - from -60... + 125 °C. The modules are used in flexible AC transmission systems (FACTS), static synchronized compensators (STATCOM), static reactive power compensators (SVC), high-voltage DC power lines (HVDC), wind power plants, voltage inverters for solar panels, railway transport, marine electric drive, electric drive of mining and transport machines.

- Inverter Power Stack - three-phase IGBT inverter with high energy density (9 kW/kg) and high overload capacity. The block contains three half-bridge IGBT modules 1200V/400A. The main features are the IP67 enclosure, the possibility of liquid cooling, the presence of a DC link capacitor and a gate driver with protection (OC, OU, OT, UV). Inverter Power Stack directs current from the vehicle's energy storage battery to three-phase alternating current to power the engine, and is intended for use in: road and off-road electric (EV) vehicles and hybrid (HEV) vehicles.
- Single component module B0 housing has a pressure-tight design and an insulated base at voltage. The modules are designed for use in energy converters, as well as in other DC and AC circuits of various power electrical installations.

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compact design – these are the requirements for state-of-the-art electronic devices. The filters of the FMBB EP family are particularly suitable wherever such equipment is

confronted with stubbornly high EMI interference signals. Highly clocked semi-conductors generate increasingly strong interference frequencies. This massively increases the requirements for compliance with EMC. Typical applications include test and measurement equipment, professional kitchen equipment, medical and critical industrial applications. The filters use the same housings as the proven FMBB NEO filter series. These housings are spot welded, thus completely closed, resulting in significantly improved attenuation behavior. Thanks to top-quality components (generously dimensioned film capacitors, chokes with highly permeable cores), an exceptionally broad-band attenuation is achieved. The FMBB EP filter series has 6.3 x 0.8 mm plug-in connections or threaded connections for quick and easy wiring. Thanks to a metal flange, excellent ground connection is ensured when screwed to the chassis. The standard versions can be used over a temperature range from -40 °C to 100 °C.

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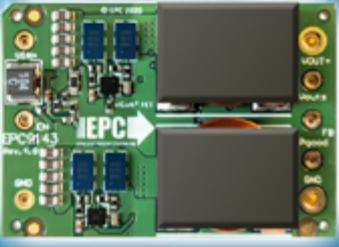
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DC-DC Converter Demonstration Board

EPC announces the availability of the EPC9143, a 300 W DC-DC voltage regulator in 16th brick size. The EPC9143 power module integrates Microchip's dsPIC33CK digital signal controller (DSC) with



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the latest generation EPC2053 eGaN FETs from EPC to achieve 96% efficiency in a 48 V input to 12 V output conversion at 25 A. The switching frequency of 500 kHz enables the 300 W in the very small 16th brick format which is just 33 mm x 22.9 mm (1.3 x 0.9 in). Additional phases can be added to this scalable 2-phase design to further increase power. The flexibility of the Microchip digital controllers allows the input voltage to be adjusted from 8 V – 72 V and the output voltage from 3.3 V – 25 V.

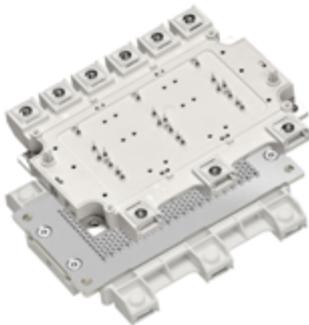
Brick DC-DC converters are widely used in data center, telecommunication and automotive applications, converting a nominal 48 V to a nominal 12 V distribution bus among other output voltages. The main trend has been towards higher power density given the form factor is fixed. A main application is high density 48V to 12V point-of-load (POL) converters, where a regulated 12V output voltage is required, like those used for commodity PCIe cards and storage.

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Power Module for Mid-Power Electric Vehicle Traction Inverters

Infineon Technologies introduces an IGBT power module tailored to the needs of electric vehicle traction inverters in the 80 kW to 100 kW power class: the HybridPACK™ DC6i. This six pack module is optimized to deliver an excellent fit of system cost and performance



to hybrid and small battery electric vehicles. It combines Infineon's established EDT2 IGBTs with package technologies for compactness, very good thermal management at reduced material cost, and an easy installation.

The global boom of vehicle electrification puts the design of cost-effective

traction inverters into focus. In this context, selecting the power module plays an important role; system designers are looking for the best-sized module with the optimal silicon area for the required performance. Within Infineon's portfolio, the HybridPACK DC6i is positioned between the HybridPACK1 family and the more powerful HybridPACK Drive family. The module has the same compact footprint (7.2 cm x 14 cm) as the HybridPACK1 – 25 percent smaller than the HybridPACK Drive – but the available output power is more than 50 percent higher. While the HybridPACK1 uses Infineon's IGBT3 technology, the HybridPACK DC6i is equipped with the latest EDT2 IGBTs. Furthermore, the module has six screw connectors to the DC-link capacitor compared to two in the HybridPACK1 family. This enables a low-inductive design with a stray inductance of 15 nH.

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Advertising Index

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Amantys	33	Hitachi	9	SEMI	C3
Asahi Kasei	39	Infineon	41	Semikron	51
Broadcom	15	LEM	5	Sirio Elettronica	47
CPS	61	Mersen	55	sps	53
EA Elektroautomatik	63	Mitsubishi Electric	17	Texas Instruments	29
Electronic Concepts	1+25	MUECAP	10	UnitedSIC	19
EPC	C4	OMICRON Lab	59	Vincotech	31
EPE	62	PEM UK	61	Wolfspeed	21
EV Tech Expo	49	Plexim	13	Würth Elektronik eiSos	3
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