

Electronics in Motion and Conversion

March 2022

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Houston, We Have a Problem



We probably wouldn't have travelled to Texas by spaceship but somehow that popular but slightly incorrect quote from the Apollo 13 crew came to mind when Bodo and I

made the final decision not to attend the APEC show this year. It was a very difficult decision as we both enjoy the special spirit of this event. We always welcome the opportunity to meet our customers and partners in North America in person and at the same time learn about the latest trends. But on the other hand, we are running a monthly magazine, and it's these clients, and our readers of course, who deserve a reliable and timely delivery of Bodo's Power Systems. That wouldn't be guaranteed if we had to quarantine or were unable to return home for some reason. We are a small team and can't handle downtime too well. So, for this year our magazine will be present at the show and at the trade press booth. I hope that we can all meet in person for next year and Florida doesn't sound too bad either! For this year, I wish APEC a successful show and a great time in Texas to all attendees!

Over the last I would say 12 to 18 months, we have published several announcements about companies increasing their production capabilities by either building new fabs or by increasing available capacities and this issue contains more of this news. Of course, power-related news only, that's what we stand for. Now the EU announces the "European Chip Act to confront the semiconductor shortage and to strengthen Europe's technology leadership" and it sounds great, doesn't it? €43 billion euros of public and private investments over the next years is planned, and the official press release also communicates a goal: Europe wants to double its market share to 20% in 2030. Considering that some of the continents are not necessarily famous for semiconductor industries, that leaves Asia, North America, and Europe as the main players and to me this means that Europe wants to catch up to the other two in volume. That's an ambitious goal, but it's also a chance and 8 years is not a long time, so we will soon see how much substance was in this announcement from Brussels. You can read it here: https://ec.europa.eu/commission/presscorner/detail/en/IP_22_729

Historically, R&D is a European subject while volume is produced in Asia, but nowadays semiconductor production is highly automated and can be at any place in the world. Europe had projects in the past with memory fabs that failed badly, such as Siemens' when Heinrich von Pierer opened the Newcastle fab. 12 years later it was demolished with lots of public money having been wasted.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive of my magazine with every single issue is available for free at my website bodospower.com.

My Green Power Tip for the Month:

Spring is coming and it's time to let the rain fill your water reservoirs for the garden. Especially the freshly planted need lots of water in the beginning. Don't waste tap water, use rain and contribute to the natural cycle!

Kind regards

Holy Martal

Thermal Management Innovation 2022

Online March 14 – 18 www.ev-manufacturing.com/ webinars-btm-innovation CIPS 2022

Berlin, Germany March 15 – 17 www.cips.eu

APEC 2022 Houston, TX, USA March 20 – 24 www.apec-conf.org

Events

SEMI THERM 2022 San Jose, CA, USA March 21 - 25 www.semi-therm.org

DesignCon 2022 Santa Clara, CA, USA April 5 – 7 www.designcon.com

EnerHarv 2022 Raleigh, NC, USA April 5 – 7 www.enerharv.com FORTRONIC 2022 Bologna, Italy April 12 – 13 www.fortronic.it

EXPO Electronica 2022 Moscow, Russia April 12 – 14 www.expoelectronica.ru

Smart Systems Integration 2022 Greneoble, France April 26 – 28 www.smartsystemsintegration.com

Miniature current sensor

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Packaged as S016 surface-mount device with a height of just 6 mm, HMSR current sensor is adapted to the power electronics world for a perfect integration thanks to its SMD automatic assembly and space saving. As a reinforced insulation level, cost effective and miniature solution for current sensing, HMSR provides solutions to photovoltaic, white goods, windows shutters, air-conditioning, high switching frequencies drives applications.

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GaN-on-Si FET Producer Opens Locations in the USA and Europe

Innoscience Technology announced the official launch of its international operations in the USA and Europe. Headquartered in Suzhou, China, Innoscience is now poised to support customers through the addition of design and sales support facilities in Santa Clara, California, and Leuven, Belgium.

Founded in December 2015, the company has currently a capacity of 10,000 8-inch wafers per month which will ramp up to 14,000 8-inch wafers per month later this year and 70,000 8-inch wafers per month by 2025. The company has a wide portfolio of devices from 30V to 650V and has shipped more than 35 million parts for use in applications including USB PD chargers/ adapters, data centers, mobile phones and LED drivers. Innoscience produces high-



performance, normally-off e-mode GaN FETs. By introducing a stress enhancement layer, the company has significantly reduced RDS(on) without affecting other parameters including threshold voltage and leakage. Both epitaxy as well as device processing have been optimized to obtain high reproducibility and yield. Parts have passed quality and reliability tests in excess of JEDEC standards.

Comments Dr. Denis Marcon, General Manager, Innoscience Europe: "The time is right for GaN, and Innoscience is ready to supply the world. We will surpass anyone on price for an equivalent device and our huge manufacturing capacity means that our customers are assured of security of supply, which is often uppermost in people's minds given the shortage of chips at the moment. We look forward to working with any company in order to proliferate GaN throughout the global electronics industry."

www.innoscience.com

Program Amplifies Gallium Nitride Speed, User-Experience and CO₂-Reduction Benefits

Navitas Semiconductor has announced a GaNFast Global Marketing Program with consumer electronics and accessory specialist UGREEN. The program builds on the companies' successful technology partnership to create awareness of GaN and education for global consumers. In-person and on-line events emphasize the significant capability of GaN technology to set standards in fast charging, with miniaturized form-factors, and sustainability benefits to reduce energy consumption and carbon emissions. Additional cooperation to increase global consumer awareness of GaN and associated charger products include enhanced product promotion via the companies' official websites, social media channels, conference/trade show booths, and video displays on the Nasdaq building in Times Square, New York.

Commenting on the GaNFast Global Marketing Program, Charles ZHA, VP and GM of Navitas China stated: "We have already established a highly successful relationship with UGREEN at the product technology level. This program builds on that success and takes it to a new level by strengthening the depth of cooperative marketing. Together, we will offer more in-depth knowledge for the mar-



ket and consumers and also strengthen the link between the power semiconductor industry and the 3C digital product industry."

www.navitassemi.com

GaN-Valley Founded in Belgium

BelGaN Group BV has completed the acquisition of all shares of ON Semiconductor Belgium BV from the onsemi group. BelGaN will transform into a leading GaN (Gallium Nitride) automotive semiconductor foundry in Europe. BelGaN will form the foundation for a GaN-Valley, a growing and innovative ecosystem for GaN-based chips and power electronics with applications, amongst others, in Electrical Vehicle, Mobile, Industrial, Data Center and renewable energy markets in Europe and beyond. This is well aligned with the European ambition for greater chip autonomy (European Chips Act) and a carbon-neutral society (Green Deal). BelGaN's vision is to



become a leading 6 inch and 8 inch GaN Foundry in Belgium, at the heart of Europe, developing GaN technologies and manufacturing GaN products. Going forward an extensive and rich roadmap of new GaN technologies will be developed and qualified for the high demands of the automotive market, amongst others.

Within a few years, the site in Oudenaarde will be transformed from a Silicon site to a GaN site. This will give an innovation-driven growth boost to the region and provide employment opportunities in Oudenaarde with multiple career opportunities in R&D, operations and various service departments.

GaN-Valley targets a growing industry for electronic systems in which energy supply and usage of electrical energy will become increasingly more efficient (less energy waste), smaller, lighter and lower cost. BelGaN and GaN-Valley are driven by energy and climate mega-trends on increased electrification for higher sustainability and carbon neutrality (solar- and wind-energy, electric cars etc.), at affordable energy costs. E.g. according to industry experts, every GaN device shipped would save 4kg CO2 compared to its Silicon counterpart.







POWER THE FUTURE ROHM'S GEN 4 SIC POWER DEVICES

As a technology leader ROHM is contributing to the realization of a sustainable society by focusing on the development of low carbon technologies for automotive and industrial applications through power solutions centered on SiC Technology. With an in-house vertically integrated manufacturing system, ROHM provides high quality products and stable supply to the market. Take the next development step with our Generation 4 SiC power device solutions.

Industry-leading low ON resistance

Reduced ON resistance by 40% compared to previous generation without sacrificing short-circuit ruggedness.

Minimizes switching loss

50% lower switching loss over previous generation by significantly reducing the gate-drain capacitance.

Supports 15V Gate-Source voltage

A more flexible gate voltage range 15 -18V, enabling to design a gate drive circuit that can also be used for IGBTs.

Capital Investment for Increase in Production of SiC Power Semiconductors

Fuji Electric is pleased to announce that it has made a decision to carry out capital investment in Fuji Electric Tsugaru Semiconductor Co., Ltd. (Goshogawara City, Aomori Prefecture), one of their power semiconductor production bases, for an increase in the production of SiC power semiconductors. Mass production is planned to begin in fiscal 2024. In the Five-Year Medium-Term Management Plan ending in fiscal 2023 (fiscal 2019 - fiscal 2023), FE announced that it will carry out capital investments totaling 120 billion yen toward power semiconductors. Although our capital investments currently focus on front-end process production lines for 8-inch Si (silicon) wafers, our amount of investments in power semiconductors, including this investment in SiC power semiconductors, is expected to expand to 190 billion yen, set against conditions of increased demand for electrified vehicles and renewable energy.



SiC power semiconductors are next-generation power semiconductors that use SiC (silicon carbide) materials. Currently, power semiconductors that use Si materials are the most common, but SiC power semiconductors can make it possible to conserve energy and reduce the size and weight of Power Electronics Equipment they are installed in. FE predicts that the power semiconductor market (the market targeted by FE) will account for 2 trillion yen in fiscal 2024, with SiC power semiconductors making up approximately 8% of this. The market growth rate of SiC power semiconductors is expected to be 17% or more from fiscal 2021 to 2024.

www.fujielectric.com

Chinmaya Joshi Appointed Global Automotive Segment Director



Vicor Corporation announced the appointment of Chinmaya Joshi ("CJ"), as Global Automotive Segment Director. Chinmaya joins Vicor from the Jaguar Land Rover group where he served as a Senior Manager for powertrain power electronics. Chinmaya brings deep automotive industry experience with over ten years leading DC-DC converter design and development teams for HEV, PHEV and BEV vehicle platforms. His primary role at Vicor will be to support the expansion of the OEM customer base, tier-one suppliers and automotive system partners through high density modular solutions for electrification. "To address fleet electrification with a robust funnel of OEM and tier-one opportunities, Chinmaya will add significant bench strength to our global automotive team," said Patrick Wadden, Global Vice President of the automotive business unit. Chinmaya earned a Bachelor of Technology in Materials Science and Engineering (Semiconductor Physics) at the College of Engineering, Pune India and a Masters of Science degree at Cornell University.

www.vicorpower.com

Asia-Pacific Power Supply Product and Technology Exhibition



With gathering the foremost power supply brands in China, Asia-Pacific Power Supply Product and Technology Exhibition, August 10 – 12, 2022 in Guangdong, China, is a strategic platform not only for domestic and international manufacturers to display their advanced power supply products as well as technology but also for professional distributors to import quality products. Having been held for a consecutive 11

years, the event is highly recommended by insiders, professional institutions and media at home and abroad and helps overseas power supply companies to find their first pot of gold in China! The Ministry of Industry and Information Technology of China predicts that the country's power supply market will grow from 232.1 billion yuan in 2017 to another all-time high of 257.6 billion yuan by 2022. China is also home to 5000+ power supply manufacturers, mainly spreading across the Pearl River Delta, the Yangtze River Delta and the region near Beijing. Co-organized by the Power Supply Committee of Guangdong Lighting Association, Shenzhen Electronic Chamber of Commerce, and Shenzhen Association for the Development Promotion of Semiconductor Lighting Industry, Power Supply Exhibition is one of the leading trade shows for power supplies in China. The 2022 show is expected to gather 500+ exhibitors on a 40,000 sq.m show floor.

www.bspexpo.com

One Sample Order = One Tree Planted

In 2022, one tree will be planted for every sample order placed in the United States, Canada, and Latin America. To make this possible, Würth Elektronik is partnering with One Tree Planted, a nonprofit organization focused on supporting reforestation throughout the world. One Tree Planted also helps educate people on the many benefits of trees, including that they provide clean air and water, habitats for wildlife, and a positive social impact. To let customers know about the initiative, sample orders will be packed with recyclable paper tape and stickers featuring "One Sample Order = One Tree Planted" and a QR code linked to more information. As a way to further include employees, customers, and partners in the initiative, a fundraiser page has also been created where anyone is able to donate directly to One Tree Planted. This is a way for anyone to feel inspired to contribute to the cause. It will also serve as



a benchmark to see how how many trees have been donated; both from the sample orders and individual donations. This partnership is another way in which Würth Elektronik is taking steps to improve sustainability and care for the environment.



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More Information: pdd.hitachi.eu / pdd@hitachi-eu.com

Sam Maddalena CEO of TDK-Micronas



TDK Corporation announces that effective March 01, 2022, Sam Maddalena (45) has been named Chief Executive Officer (CEO) of TDK-Micronas GmbH. "We are very happy to appoint Sam Maddalena as the new CEO of TDK-Micronas. He joined the management team in 2021 and showed great ambitions and commitment to grow the business of TDK-Micronas. His experience within the industry and his management skills will be a strong support for TDK-

Micronas and the Magnetic Sensor and embedded motor control business of TDK to achieve further growth in our target markets", says Noboru Saito, CEO of TDK's sensor business company. Mr Maddalena has gained more than 20 years of experience within the Automotive semiconductor industry. He started his professional career at Melexis, after graduation as an MS EE (Master of Science in Electrical Engineering) at the University of Gent, Belgium. He held a number of technical, business and executive roles at Melexis. From 2016 to 2019 he was the Vice President Corporate Strategy and Global Marketing. During 2020 he supported various projects as a consultant for XenomatiX and IMEC. In 2021 he joined TDK-Micronas, where he held the position as Chief Strategy Officer (CSO). "I am looking forward to my future tasks as CEO of TDK-Micronas GmbH and I am sure to contribute to the future growth of TDK's sensor and motor control business and expand our market position in the Automotive industry and other target markets. We can offer a strong product portfolio that we will optimize further in order to offer the best solutions for our customers", says Sam Maddalena.

www.micronas.tdk.com

300-Millimeter Wafer Fabrication Facility

Toshiba Electronic Devices & Storage Corporation ("Toshiba") announced that it will construct a 300-milimeter wafer fabrication facility for power semiconductors at its main discrete semiconductor production base, Kaga Toshiba Electronics Corporation, in Ishikawa Prefecture. Construction will take place in two phases, allowing the pace of investment to be optimized against market trends, with the production start of Phase 1 scheduled for within fiscal 2024. When Phase 1 reaches full capacity, Toshiba's power semiconductor production capacity will be 2.5 times that of fiscal 2021.



Power devices are essential components for managing and reducing power consumption in every kind of electronic equipment, and for achieving a carbon neutral society. Current demand is expanding on vehicle electrification and the automation of industrial equipment, with very strong demand for low-voltage MOSFETs (metal oxide semiconductor field effect transistors) and IGBTs (insulated-gate bipolar transistors) and other devices. To date, Toshiba has met this demand growth by increasing production capacity on 200-milimeter lines, and expediting the start of production on 300-milimeter production lines from the first half of fiscal 2023 to the second half of fiscal 2022. Decisions on the new fab's overall capacity and equipment investment, the start of production, production capacity and production plan will reflect market trends.

The fab will have a quake absorbing structure; enhanced BCP systems, including dual power supply lines; and the latest energy saving manufacturing equipment to reduce environmental burdens. It will also aim to achieve the "RE100" goal of 100% reliance on renewable energy. Product quality and production efficiency will be improved by introducing artificial intelligence and automated wafer transportation systems.

https://toshiba.semicon-storage.com

European Distributor of the Year 2021 Award

Avnet Abacus announced that it has received the "European Distributor of the Year 2021" award from Harwin. Michael Clarner, Head of Distribution Sales EMEA at Harwin, said: "Our partnership with Avnet Abacus is exceptionally strong across Europe at all levels of our business. During 2021, revenue grew beyond the market av-



erage, and the number and value of new design-wins pave the way for a bright future." This latest award follows on from Avnet Abacus' recent success in Harwin's 5 Star Awards, which recognised two individuals from Avnet Abacus for their highly creditable efforts in supporting Harwin's business. Jose Ramon Blazquez played a key role in securing Harwin design wins in a variety of markets, and Dieter Kuhn contributed invaluable technical support to a series of high-profile customer projects. Hagen Götze, Senior Director Marketing at Avnet Abacus, said: "By having a strong focus on customer service, excellent technical support and a great collaboration with Harwin we were able to once again strengthen our position as the number 1 distributor in Harwin's network in EMEA during 2021. I'd like to thank the entire Harwin team for the great support."

Avnet Abacus distributes a broad portfolio of Harwin high reliability interconnect products for use in industries including industrial IoT and aerospace & defence, and for EMC shielding.

www.avnet.com



All-SiC Trench gate MOSFET – 2nd Generation

MAIN FEATURES

- Significantly lower loss operation and higher power density
- New internal design accomplishes very low inductance package
- Enables much higher switching frequency compared to Si-IGBT
- Fully compatible package to conventional Si-IGBT module

Comparison of All-SiC 300A/1700V with Si-IGBT





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 Case Size

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- 250 Watt / 500 Watt
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 Isolation Voltage 7 kV or 12 kV
 - High Pulse Load

PR Spezial

- Up to 3 resistors per case
- Adapted terminals or cable connection
- Partial discharge tested

info@muecap.de www.muecap.de

International Conference on Integrated Power Electronics Systems

CIPS 2022 will be held in Berlin, Germany and Online from March 15th to 17th. Basic technologies for integrated power electronic systems as well as upcoming new important applications will be presented in interdisciplinary invited papers. In the next decades, power electronic system development will be driven by energy saving systems, intelligent energy management, power quality, system miniaturization and high reliability. Monolithic and hybrid system integration will include advanced device concepts including wide bandgap devices, new packaging technologies and the overall integration of actuators/drives (mechatronic integration). In 2022 the successful story of



CIPS will continue as the conference focus is today more important than ever – increasing functionality, energy efficiency and system reliability while decreasing cost.

www.cips.eu

EPE'22 and Future ECCE Europe Conferences: New Submission Policy



The EPE executive council has decided to change the submission policy. Authors, from now on, are invited to submit a provisional 6-8 page full paper to the review committee. The new deadline is, as of now, the 31st of March. This will be valid for 2022, but also for future years. You are, of course, MOST WELCOME to upload NEW WORK in the form of a nearly-ready 6-8 page full paper before the 31st of March 2022. If you already have uploaded a synopsis for EPE'22 ECCE Europe, then it currently is in the reviewing/evaluation process, and you will be notified about the result on the 2nd of March 2022.

www.epe2022.com

PLECS Conference 2022 Postponed

The first PLECS Conference is entitled "Real-Time Simulation of Power Electronics". The event brings together engineers from industry and academia who are eager to learn about current applications in this field. In addition to the technical aspects, the conference offers a good opportunity to connect with other engineers. As this is an on-site only event, there will be no virtual replacement. The conference was originally scheduled for March 8 & 9 but had to be postponed to September 20 & 21 due to the extended Covid measures in Switzerland.

www.plexim.com





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Baoxing Chen Named IEEE Fellow



Analog Devices' Technology Fellow Dr. Baoxing Chen has been named a 2022 IEEE Fellow for his contributions to integrated signal-power isolation and integrated magnetics. IEEE Fellow is the highest grade of IEEE membership and is recognized by the technical community as a prestigious honor and an important career achievement. The total number selected in any one year cannot exceed one-tenth of one- percent of the total voting membership. "I am incred-

ibly humbled and honored to be named an IEEE Fellow," said Dr. Chen. "This is a testament to Analog Devices' leadership in digital isolation technology, which is only made possible through decades of dedication from our isolation team. I am extremely fortunate to work in such a collaborative environment where innovation is nurtured and valued." Dr. Chen, who joined Analog Devices in 1997, was named an ADI Fellow in 2010. As the chief technologist for the Isolation Group, he pioneered iCoupler® and isoPower® digital isolation technology from inception through today's innovations, enabling over 4.4 billion isolation channels shipped. He also heads chip scale thermoelectric harvester developments at ADI. Dr. Chen has published more than 40 papers and holds 52 US patents. Additionally, he is an adjunct professor in Northeastern University's Electrical and Computer Engineering Department and also serves as associate editor for IEEE Transactions on Power Electronics. Dr. Chen holds a Ph.D. in Physics and a M.S. in Electrical Engineering from the University of Michigan as well as a B.S. in Physics from Nanjing University in China.

www.analog.com

APEC 2022 Taking Steps to Assure Safe and Healthy Conference Environment

For the first time since 2019, APEC 2022, being held in March, will once again be a face-to-face conference and exhibition. To assure a safe and healthy environment for all APEC participants at the inperson event, the conference organizers are taking special precautions by requiring proof of full vaccination or a negative COVID-19 test (obtained within 72 hours of attendance) as a condition of entrance. To facilitate this screening, APEC has partnered CLEAR Health Pass, enabling attendees to show their vaccination using a free mobile app. According to local current guidelines, face masks while indoors also will be encouraged at the event. Attendees can use the QR Code (shown here) to download the CLEAR app.

"Although conditions are improving," said Omer Onar, APEC 2022 General Chairman, "the APEC 2022 Conference Committee recognizes the unique and changing impact the pandemic has had on our practices, families and plans over the last two years. Since the health and safety of APEC attendees is of utmost importance to us, we are providing a CLEAR Health Pass app free to all attendees. Additionally, we are working closely with the George R. Brown Convention Center, as well as federal, state and local public health officials, to incorporate best practices to ensure the highest level of protection at APEC 2022." Health Pass by CLEAR provides secure, digital proof of COVID-related health insights via the CLEAR mobile app. Attendees are encouraged to download the CLEAR app and complete the process at least 24 hours prior to arrival at the event.



The QR Code and further details can be found at http://apec-conf.org/exposition/health-and-safety.

www.apec-conf.org

Reflecting on Past Achievements and Embarking on Future Opportunities

Nexperia celebrates five years since entering the semiconductor industry as an independent entity. During this time, the Nexperia brand, while still relatively young, has become firmly established in the marketplace by building on the foundations of a strong track record in semiconductor manufacturing over several decades. Right from the start back in 2017, Nexperia combined passion with pro-



fessionalism and set about growing with its customers by providing them with the innovative products that they need. It now celebrates five years of forward thinking, growth, and market-leading products. During this time Nexperia has also developed industryleading capacity that consistently meets the highest automotive standards, while also providing the widest range of discrete components, power, and Logic ICs.

While justifiably proud of its past achievements, Nexperia is a future focused company with renewed ambition and commitment to further innovation and progress, both for itself and its customers. With a world-class team that includes a visionary CEO and forwardthinking leaders, Nexperia is aggressively targeting an increased market share by seizing on new opportunities as they emerge. "We will have record investments into our facilities, people and into innovative products in 12 inch. This will enable Nexperia to transition into a world leader in essential semiconductors with a revenue of more than USD \$10bn by 2030", says Xuezheng Zhang, CEO of Nexperia. "We will achieve this by becoming the number one supplier in the market segments that we serve."

www.nexperia.com



ONE vinc NOVERTER TO SOLVE IT ALL

Can one inverter cover all your single-phase solar system needs?

Trying to choose an easy-to-use solution for your next single-phase PV and ESS systems? Our multi-sourced *flow*PACK 1 H6.5 family has it covered. Optimized for PV systems with active or reactive loads, Vincotech's latest additions extends the family for bidirectional ESS applications. Engineered for applications from 3 kW up to 10 kW, these modules are housed in 12mm, low-inductance *flow* packaging.

Main benefits

- Optimized for single-phase solar PV and ESS applications
- / Highly efficient three-level H6.5 topology maximizes ROI
- Common footprint lowers development costs
- Compact, integrated solution reduces weight and increases power density
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UK Startup Dares to Innovate GaN Differently

I had the chance to interview Co-Founder and CEO Giorgia Longobardi and spoke to her about Cambridge GaN Devices' work in Gallium Nitride technology.

By Bodo Arlt, Publishing Editor, Bodo's Power Systems

Bodo: Please tell us a little bit about Cambridge GaN Devices and how the company was founded!

Giorgia: Cambridge GaN Devices, or CGD, is a fabless semiconductor company created in 2016 to exploit the power of Gallium Nitride-based technology by delivering greener electronics. The company was spun-out of the engineering department at Cambridge University by myself and Professor Florin Udrea, which came about after 10 years of research into GaN. I was the first person in the department researching GaN alongside Florin in his group. At the time, he had more than 30 years of experience in power devices, not only in research, but also collaborating with some of the major semiconductor companies. Together we had a clear understanding of the technology and the challenges involved, such as reliability issues, and we had some ideas that could help solve this and more. Additionally, with the strong ecosystem in Cambridge, we decided that we had to start the company because of the impact GaN and its efficient technology could have on saving energy and improving power electronics going forward.

Bodo: What are some of CGD's biggest accomplishments since the company was founded?

Giorgia: Our goal was to explore and develop a number of unique opportunities in power electronics, and our team was able to accomplish that via our proprietary application of GaN to the silicon-based semiconductor transistor manufacturing process. Over the last few years, our engineers have developed GaN transistors that are over 100 times faster, lose 5 to 10 times less power, and are 4-times smaller than existing silicon equivalents. I'm so proud of the highly driven, committed, and knowledgeable team that we've built on our journey from a few sketches of ideas on pieces of paper to actively working to deliver the highest quality and highest performance semiconductor devices and integrated circuits for a new generation of power systems.

I'm also proud of the number of projects CGD has been involved in, including GaN Next, a ≤ 10.3 m Europe-wide initiative devel-



Giorgia Longobardi

oped through a consortium of 13 partners and led by our company. When we won the project, we had more partners than employees in the company, and that goes to show how ambitious we have been from the very beginning. We've quickly grown in numbers, and in terms of our IP portfolio we have now made 36 patent applications, including our proprietary ICeGaN[™] technology.

Bodo: Can you tell us more about your ICe-GaN™ technology and how it works? Giorgia: Our patented ICeGaN[™] (Integrated Circuit Enhancement Mode GaN) technology, which is integral to our first product release due in the first half of 2022, is an integrated solution based on GaN with an intelligent and self-protecting mechanism that enhances the functionality of logic gates within a transistor. This merit is noteworthy on its own, for the reliability and scalability the technology offers, effectively enhancing the power efficiency of the devices.

ICeGaN[™] allows us to drive CGD's GaN transistors with available gate drivers, normally utilised for Silicon transistors, while GaN-specific gate drivers and RC networks are needed to drive other GaN transistors. Moreover, CGD embeds into its GaN transistors dedicated ICs which deliver additional essential functions for the power supply such as overcurrent protection, temperature sensing and over temperature protection. This is why we refer to an ICeGaN[™] powered product as a GaN power IC rather than simply a GaN transistor.

Bodo: What makes CGD different from other semiconductor companies?

Giorgia: One of the key factors that differentiates us from others is how we've identified what is called the 'third way' in GaN power devices and has been made possible by doubling down on our ICeGaN™ technology. Our company has been able to integrate the smartness needed for the transistor and make it easy to use, while giving any customer the flexibility to use any gate



Team Cambridge GaN Devices

driver. Basically, ICeGaN[™] technology merges the positive of Cascode configuration (ease-of-use) with the beauty of eMode HEMTs (single chip, normOFF), as well as a number of integrated smart sense and protection features. This is quite unique as it provides a reliable transistor, but it is also scalable in power and in voltage. ICeGaN[™] technology is deployed into a portfolio which will grow to cover Consumer and Industrial applications, from 30W mobile chargers all the way to multi-kW servers, telecom rectifiers and PV inverters, with an eye towards Automotive applications at the right point in time. We're the only company that has such flexible technology right now.

We're also different thanks to the innovative approach to everything that we do and having a constant eye on the future. Our expertise in GaN is strong thanks to our deep knowledge of the material, the device physics, as well as the system and market requirements which puts us in the unique position of being flexible and able to move quickly once we have shared with the market and our customers. We're extremely committed to not only delivering a green product, but to be a company that has embedded sustain-

ability in its own culture with the entire team committed to the journey ahead.

Bodo: Which applications/markets do you intend to make your products available for?

Giorgia: We're in the process of developing a range of energy-efficient GaN-based power devices using ICeGaN[™] technology and are looking to deploy it in several key market segments such as consumer electronics, lighting, data centres, telecoms, solar and automotive electric and hybrid electric vehicles. Our company recently commenced an Innovate UK (the UK government's innovation agency) project with the goal of developing a product for the automotive market as this is a key market to meet our business objectives. We've also just launched ICeData, a project aiming to develop and commercialise a highly efficient GaN-based IC for use in data centre server power supplies. The primary goal of this project will be to deliver state-of-the-art GaN power IC technology to boost the efficiency of data centre server power supplies to more than 97 percent, which will contribute to the saving of more than 8 megatons of CO2 emissions annually in 2030.

Our GaN-based transistors can provide other power saving benefits, such as decreasing the amount of power needed for typically power-hungry data centres, or when it comes to consumer electronics opening up the potential for smaller, energy-efficient components, changing the game in a positive way for the world at large. As sustainability is a core tenet of our business, the idea here is to bring our innovative solution with the aim of continuously lowering power losses in the electronic power industry to benefit a wide community of customers and end users.

Bodo: What can we expect from CGD in 2022 and beyond?

Giorgia: 2022 is set to be a big year for the company. We've already unveiled a rebrand of the company to better communicate our approach in changing GaN technology. We also launched the ICeData project, and at

APEC we'll be announcing the launch of our first product for the market. We also have a number of client engagements in the pipeline, including partnerships with major companies that are soon to be finalised. We are also in ongoing discussions with various customers, including some that have expressed interest in our technology with some initial design-in work taking place, from which there will be soon-to-be-announced business wins.

CGD will continue to invest heavily in R&D across the various markets we've targeted as we aim to become the market leader in GaN power integrated circuits and wish to demonstrate to all that efficient power electronics is a key piece of the puzzle for the world to reach its net zero targets. We also plan to significantly expand our team over the next few years as we continue to innovate and push forward on R&D activities via strategic partnerships that will take the company to the next level.

Bodo: Thank you very much, I will keep my eyes open for more to come from CGD!

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Lowest On-resistance SiC FETs Offer Rugged Short-Circuit Performance

The largest growth area for silicon carbide FETs is expected in the electric vehicle traction inverter, offering extended range, lower battery costs and higher power density. UnitedSiC (now Qorvo) has recently released low on-resistance SiC FETs, 750V/6mOhm in a standard TO247-4L package.

By Pete Losee, Anup Bhalla, Xueqing Li, Jonathan Dodge, Vineeth Krishna, Ke Zhu, Qorvo, Princeton, NJ, USA

The FETs are compelling for inverters designed with 400V-500V bus voltage, offering superior conduction losses and switching losses compared to their Si IGBT or WBG alternatives. In addition to low losses, it is also essential for power switches in motor drive inverters to offer short-circuit protection to allow detection and safe shut down to avoid catastrophic system failure. These 6mOhm/750V SiC FETs offer a useable short-circuit widthstand time of 5 microseconds. In this article, we discuss the importance of this feature and why these 4th generation SiC FETs are uniquely positioned to meet this demand without compromising on $R_{DS(on)}$.

Introduction

Silicon carbide FETs have established themselves in many applications including on and off-board charging of EVs, datacenter power supplies, solar inverters etc. The largest growth area for silicon carbide FETs is expected in the EV traction inverter, offering extended range, lower battery costs and higher power density [1,2]. Already introduced in 400V battery system, SiC FETs have perhaps an even more compelling case with higher bus voltages (500V or 800V) [1,2]. The drivetrain inverters in these systems are conventionally 3-phase, 2-level voltage source inverters operating at frequencies below 20kHz. In this application, it is paramount for the switch to offer low conduction and switching losses across the full load range. SiC FETs are a great candidate with their absence of knee voltage (improved light load efficiency), and low conduction and switching losses. However, one area where silicon carbide switch options have not met the application need until now is short-circuit ruggedness. In this article we will discuss why UnitedSiC/Qorvo's 4th generation cascode SiC FET is an ideal candidate to minimize on-resistance while maintaining a useful (up to 5 microsecond) short-circuit widthstand time for designers.

Short-circuit ruggedness is an especially important feature for power semiconductor switches in motor drive inverters to possess, requiring some fault ride-through protection allowing for the system to detect and safely shut down avoiding catastrophic system failure. Figure 1 depicts the various short-circuit faults that commonly occur in a motor drive inverter system. The system can experience a direct short of the DC-bus when there is a shoot-through condition of one of the inverter phase legs. This can happen if one of the phase leg switches fails short while the other switch's gate drive remains functional. Alternatively, a shoot-through condition can occur if an erroneous signal from the gate driver is applied to one of the phase leg FETs. A short-circuit across phase legs (phaseto-phase) can occur when insulation in the windings of the motor fails. Finally, a phase-to-ground failure can occur if there is a failure in the motor winding insulation such that a short is created to the motor casing. In each of these failure modes, the power semiconductor switch must endure a direct short-circuit of the entire DC bus voltage or share bus voltage in short-circuit with the complementary switch in the phase leg. Under these harsh conditions, it is the power semiconductors which catastrophically fail first (within microseconds), rendering the entire system inoperable.



Figure 1: Schematic of traction inverter showing location of commonly encountered short-circuit faults, Phase leg shoot-through, Phase to Phase short, or Phase to Ground failure

Multiple methods of detecting a short-circuit have been proposed, but most fall into either current measurements or de-saturation (deSat) detection of the switch Drain-to-Source voltage (or collector-emitter voltage of IGBTs). Figure 2 depicts a standard deSat approach on the low-side switch of a phase leg. A fast, high-voltage deSat diode is used to allow monitoring only during the switches on-time. In the event that the voltage across the switch is higher than expected while the switch is gated on, a threshold level is tripped (typically 7-9V) indicating an overcurrent or short-circuit event. The state of the deSat signal is used to shut down the gate driver output and the switch is turned off before catastrophic failure. However, care must be taken to prevent false tripping of the deSat signal. A blanking time is used to censor the time between the start of turn-on and the switch reaching its nominal Drain-to -Source voltage during conduction. Additionally, avoiding spurious deSat trips often includes filtering (RC etc.) of the input to avoid noise induced trips, which can further increase the practical minimum detection time. Thus, a trade off exists between noise immu-



Figure 2: Schematic of commonly employed desaturation detection

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nity and short-circuit detection and shutdown time. Designers can find these constraints challenging to implement in systems without several microseconds of assumed ride-through capability. To date, wide bandgap devices, with their low on-resistance and smaller die sizes, have underperformed their traction IGBT counterparts which have historically offered more than 10 microseconds of short-circuit ride-through capability. However, as Si IGBTs have continually lowered V_{ce,on} and switching losses, along with improved gate drivers, short-circuit ride-through ratings have decreased to below 10 microseconds [3].

There are several characteristics associated with a power semiconductor switch that impact its ability to handle short-circuit faults. To understand these characteristics, we can first look at the typical failure mechanisms that occur when FETs are subjected to shortcircuit conditions as represented in Figure 3. In the figure, a typical I-V characteristic of a Type-1 short-circuit is represented with the bus voltage being applied across the device. There is a small dip/ overshoot in the otherwise constant voltage associated with the drop across the power loop stray inductance under the high di/dt portion. In the figure, the device's short-circuit current (black curve) increases rapidly as the FET's impedance is low in the on-state. During this phase, the device's junction temperature is heating rapidly as the high instantaneous power is contained in the FET's active layer. As the junction temperature and current rises, eventually the FET reaches its current saturation regime limiting the peak shortcircuit current (lsc-peak). The large instantaneous power dissipation continues to heat the FET and the short-circuit current begins to decrease from the self-heating and the resultant decrease in saturation current.



Figure 3: Typical short-circuit I-V waveforms (top) and resulting temperature rise (bottom) exhibited by a power FET under short-circuit

If the device's junction temperature reaches a thermally unstable level prior to the gate driver shutting off the channel of the FET, a runaway event can occur as illustrated by bubble1 in Figure 3. In the case of conventional SiC MOSFETs, failure prior to shut down can also occur if the gate oxide ruptures in the presence of high electric field and high junction temperatures [4,5]. The failure mode 2 depicted in the figure represents thermal runaway after the FET is turned off. In this mode, the device's leakage current at high temperature (can be more than 600°C) can lead to thermal runaway or latch the device's internal parasitic transistor causing catastrophic failure to occur. Finally, in the case of mode 3, the device can safely shut down the short-circuit fault and the device's junction temperature slowly returns to its nominal running temperature. In state of the art SiC FETs operating with practical bus voltages, the shortcircuit period on the microsecond scale can be thought of as an adiabatic process. Silicon carbide's 3-6x smaller die sizes and associated reduced thermal capacity results in a larger temperature rise for a given short-circuit energy than their Si counterparts.

SiC FETs Offer Breakthrough Performance

From the discussion around Figure 3, it is clear that the optimum power switch is one that can reduce I_{sc-peak} without compromise of on-resistance, thereby keeping the short-circuit energy low, reducing temperature rise and avoiding thermal runaway. The switch should also avoid secondary failure modes such as gate-oxide rupture and avoid any parasitic bipolar transistor latch up. While p-n junction leakage at high temperature is unavoidable, the optimal switch should also maintain a sufficiently high threshold voltage versus temperature to diminish channel leakage components that adds to thermal runaway.

These characteristics are all found in vertical SiC JFETs. SiC JFETs offer the lowest specific on-resistance of any technology from 650V-2kV+, while also offering good current saturation. The vertical JFET device structure has no internal parasitic transistor in its primary leakage path (Drain-to-Gate) in the off state. There is no gate oxide in the device structure and the threshold voltage versus temperature is flat compared to Si or SiC MOSFETs. When configured with a low voltage Si MOSFET, the normally-off cascode SiC FET offers a superior trade-off between on-resistance and short-circuit ruggedness [6]. It can also be shown that during the short-circuit fault (up to 10 microseconds), the heat is concentrated in the SiC JFET and



the low voltage Si MOSFET in the stacked cascode FET does not see significant temperature rise. Figure 4 illustrates an electrothermal TCAD simulation of a SiC stacked cascode FET under short-circuit. Up to 10 microseconds, the temperature rise (up to >700°C) is primarily contained in the SiC JFET bulk and topside metallization. Here, the Si MOSFET, which does not enter the current saturation regime remains well below its maximum junction temperature. Thus, it is the SiC JFET that determines the short-circuit capability of a SiC cascode FET.

UnitedSiC (now Qorvo) has exploited these features with its 4th generation of SiC FETs. The new UJ4SC075006K4S product boasts the industry's lowest on-resistance of 6mOhm in a standard discrete package. The device offers a voltage rating of 750V which allows plenty of design headroom for 400V or 500V bus applications. The superior on-resistance (less than half of the nearest competitor) is offered with all the additional advantages that users have grown accustomed to with UnitedSiC FETs such as the easy 0-12V or 0-15V gate drive, excellent integral diode, and low switching losses afforded by the lower device capacitances (C_{oss}).

For the first time with a SiC power switch, rugged short-circuit performance is achieved without compromising cost or efficiency. The 750V rated SiC JFETs boast a specific on-resistance less than 1/3rd of their 650V SiC MOSFET competitors. The UJ4SC075006K4S 750V/6mOhm SiC FET has also been designed with a useable short-circuit withstand time of greater than 5 microseconds. Figure 5 shows the Type-1 short-circuit characteristics of a typical UJ4SC075006K4S SiC FET with a bus voltage of 400V. The device safely shuts off after a 10 microsecond short-circuit when the starting junction temperature is 25°C and passes 8 microseconds even when starting from the devices' $T_{j,max}$ =175°C. The devices are designed with current saturation (800A shown at $T_{j,start}$ =25°C, 600A at $T_{j,start}$ =175°C, respectively) between 5-10x nominal, which is sufficient to allow for overcurrent surge events but low enough to achieve adequate short-circuit withstand time for safe shut down.



Figure 5: Short-circuit waveform of UJ4SC075006K4S 750V/6mOhm SiC FET, Vgs=15V, Vbus=400V, starting temperature = 25°C (grey) and 175°C (blue)

The UJ4SC075006K4S can be safely shut down with commercial gate drivers offering deSat protection. In the Figure 6, we've illustrated a phase leg short-circuit with UJ4SC075006K4S in both switch positions. The short-circuit detection and safe shut down with a commercial (ADuM4136) gate driver from Analog Devices [7] occurs when the V_{DS} of the low-side switch was above the deSat threshold (9.2V) after the blanking time of 312ns. In the test, the short-circuit current reaches a peak of 880A, respectively, before the device's self-heating reduces the fault current to approximately 500A prior to turn-off. The deSat protection safely shuts down the short-circuit within 2.7 microseconds, well below the UJ4SC075006K4S short-circuit withstand time rating of 5 microseconds.



Figure 6: DeSat detection and shutdown example of UJ4SC075006K4S half-bridge w/ 400V dc-bus using commercial gate driver ADuM4136. Short-circuit turned off after 2.7us with low-side switch deSat engaged. Tested with Rg,ext=33ohms, V_{GS} =-5V/15V, Each FET has device snubber RsCs = 4.7ohm/680pF.

Conclusion

UnitedSiC (now Qorvo) has recently released the industry's lowest on-resistance 750V, 6mOhm SiC FET leveraging its 4th generation technology with breakthrough performance. By virtue of the excellent ruggedness afforded by its internal SiC JFET, this new FET offers designers a useable 5 microseconds of short-circuit withstand time, even at high temperature, without sacrificing on-resistance. The new UJ4SC075006K4S allows designers to use deSat protection found in standard drivers and is a great choice for 400V or 500V bus applications.

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High Performance 1 kW per Phase 48 V/12 V Converter Using GaN ePower Stage

How integrated GaN technology drives superior performance, simpler design, and reduced cost in 48 V/12 V automotive mild hybrid applications.

By Yuanzhe Zhang, Director, Applications Engineering, Efficient Power Conversion Corporation

Introduction

Automotive 48 V/12 V converters are essential in modern hybrid electric vehicles, as the energy is exchanged between the 48 V and 12 V buses. This two-voltage system accommodates legacy 12 V systems and provides higher power for 48V to loads such as vacuum and water pumps, electric super chargers, steering, and audio systems. Among all the requirements for the 48 V/12 V converter, efficiency, power density, size and cost are on the top of the list. This article addresses these design criteria by employing the GaN ePower Stage, EPC23101, and compares it with a previous design using discrete EPC2206 devices.

GaN ePower Stage Chipset

GaN FETs used in 48 V applications are rated between 80 V and 100 V, and usually have a 4 times better figure of merit (A_{Die} ·R_{DSon}) compared to equivalent MOS-FETs [1]. For the same gate voltage of 5 V, GaN FETs have at least 5 times lower gate charge than equivalent MOSFETs. Other important advantages of GaN FETs include lower C_{OSS}, faster voltage transition, zero reverse recovery Q_{RR} and are physically smaller.

Monolithic integration of GaN power FET and gate drivers has already been established [2], but with limited power ratings, mainly due to die size. To accommodate applications with high power and also provide more design flexibility, the new EPC23101 integrates only the upper GaN FET of a half bridge with a complete half bridge gate driver, as shown in Figure 1.



Figure 1: EPC23101 concept diagram.

The on-resistance of the integrated power FET is 3.3 m Ω , with a maximum voltage and current rating of 100 V and 65 A respectively. The gate driver can be supplied with 5 V and the PWM inputs can accept 3V3 logic levels. In addition, the EPC23101 includes an enable pin allowing the gate driver to be placed in low quiescent power mode when disabled. It is available in an exposed-top QFN package that measures 3.5 mm by 5.0 mm with solder bars that comply with IPC-2221 creepage and clearance requirements for its rated voltage.

To form a half bridge, an external low side GaN FET is required. The EPC2302 is the good choice for this example application. The EPC2302 is a 100 V rated 1.8 m Ω device that is available in a similar QFN package as the EPC23101. This asymmetrical half bridge yields an optimal balance between switching and conduction losses for 48 V/12 V converter [3]. A photo of this chipset (EPC23101 and EPC2302) and a functional block diagram is shown in Figure 2.

the 12 V bus. Furthermore, the design is scalable, so two boards can be paralleled for a 4 kW system.



Figure 3: Simplified schematic diagram.

The PCB layout of the power stage plays a critical role. Parasitic inductance can affect efficiency and voltage overshoot. A good layout contributes to high reliability. This design utilizes the internal vertical layout technique [1] to minimize parasitic inductance by placing the decoupling capacitors



Figure 2: Photo of EPC23101 and EPC2302 chipset with functional block diagram.

Converter Design

A 2-phase synchronous buck converter topology was selected for the demonstration of the ePower stage technology. This converter can also operate as a boost in reverse. A simplified schematic diagram is shown in Figure 3 that includes the power stage and support functions such as current sensors, temperature sensor, digital controller and 5 V and 3.3 V auxiliary power. Each phase is designed to carry up to 70 A current on the 12 V bus. This equates to 1 kW at 14.3 V. The total maximum output power of this design is 2 kW, or 140 A into close to the FETs with a solid ground plane beneath. Symmetrical layout between the two phases is also important for current balancing and minimizing the effects from mismatch, such as switching transition, overshoot, etc.

Compared to the design using discrete EPC2206 [4], the layout with GaN ePower stage chipset is much simpler, as shown in Figure 4. The majority of the gate driver components on the bottom side of the PCB is eliminated. This results in a reduction of the occupied area from approximately 1.5 cm^2 to 0.9 cm^2 , or 40%.

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There is limited selection for off-the-shelf high-current automotive grade inductors. This design uses the 1 μ H inductor with 65A saturation current rating from Vishay IHTH-1125KZ-5A series.



Figure 4: Layout comparison of discrete GaN FET with gate driver and integrated ePower stage chipset.

To ensure accurate phase-current balancing, current sensing using a precision shunt resistor is used, together with digital average current mode control and an active current balancing algorithm. Using a Microchip dSPIC microcontroller with high resolution PWM (250 ps), the inner current loop bandwidth is set to 8 kHz, and the voltage loop to 800 Hz.

Performance Evaluation

Figure 5 shows a photo of the converter (EPC9170). With the heatsink installed and 2000 LFM airflow, the converter was operated at 48 V input, 14.3 V output and 500 kHz switching frequency. The measured efficiency is shown in Figure 6, compared with the converter built with discrete EPC2206 and external gate driver [4]. By



Figure 5: Photo of the EPC9170 with EPC23101 and EPC2302 ePower stage chipset.

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using integrated solution, this converter achieved higher peak efficiency, at 96.7%, and also higher full load power. At full load of 1 kW/phase, the efficiency is 95.8%. With the reduced occupied area, this also leads to higher power density.

Conclusion

GaN FETs have demonstrated superior performance in automotive 48 V/12 V applications over equivalent MOSFETs. With the integrated ePower stage chipset of EPC23101 and EPC2302, designers can further improve the converter performance, while reducing size and cost through reduced component count. This design example used the chipset in a 2-phase synchronous buck converter and demonstrated significant performance gain compared to the previous design using discrete EPC2206, achieving peak efficiency of 96.7% and full load efficiency of 95.8% at 2 kW, when converting 48 V to 14.3 V and switching at 500 kHz.



Figure 6: Measured efficiency of EPC9170 (integrated EPC23101 and EPC2302) compared with discrete EPC2206.

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Achieving Fast Load-Transient Response and Low EMI with the AECM DC/DC Control Topology

No single control topology is a good fit for all applications. Designers requiring low electromagnetic interference (EMI) and fast load-transient response should consider advanced emulated current mode (AECM) – a new, constant-frequency and inductor-based control topology with smart loop-bandwidth control.

By Vincent Zhang, Systems Applications Manager Buck Switching Regulators, Texas Instruments

What is AECM control?

There are many types of control topologies addressing specific design challenges for non-isolated switching DC/DC converters and controllers [1], including peak current-mode control (PCM), voltage-mode control, constant on-time (COT) control, D-CAP2[™] control topology and all of their derivatives. In accordance with the implementation of duty cycle, it's possible to separate these control topologies into two categories: the pulse-width modulation (PWM) technique and the pulse-frequency modulation (PFM) technique. The PWM technique is common in DC/DC converters used to power communications, audio and automotive equipment. It has a fixed and predictable switching frequency, which is convenient when designing the output filter for low electromagnetic interference (EMI).

The PFM technique is common in DC/DC converters used to power digital applications such as graphic engines, memory, digital signal processors and field-programmable gate arrays because of its fast load-transient response. Control topologies do affect DC/ DC converter design and may vary based on system-level requirements such as ripple, solution size, load-transient response, fixed frequency and light load efficiency. No single control topology is a good fit for all applications.

In this white paper, I am introducing a constant frequency and inductor current-based control topology with smart loop-bandwidth control called advanced emulated current mode (AECM). This new control topology combines the benefits of PFM and PWM techniques, showing a fast load-transient response with a true fixed switching frequency operation. AECM can help enhance the performance of applications currently using both the PCM and PFM techniques.



Figure 1: PCM control scheme block diagram.

РСМ

PCM is a popular fixed-frequency control topology for DC/DC converters given its overload protection, accuracy and ease of compensation. Figure 1 illustrates PCM control of a buck converter.

The power stage consists of the power switches and output filter. The compensation block includes the output voltage divider network, error amplifier, reference voltage and compensation components. The pulse-width modulator uses a comparator to compare the inductor current information with the slope compensation ramp to the error signal, creating an output pulse-train that has a width controllable by the level of the error signal.

As shown in Figure 2, the internal clock initiates one pulse, and the high-side field-effect transistor (FET) turns on, with current increasing in the inductor. When the sensed current reaches the control voltage, the high-side FET turns off and the low-side FET turns on until the next rising edge of the clock. The next PWM pulse is generated at the next clock pulse. Thus, the switching frequency depending on the clock is truly fixed.



Figure 2: PCM control scheme waveform.

PCM control introduces one inner current loop, which transforms the inductor into a voltage-controlled current source. The power stage can be approximated as a current source feeding the parallel combination of the output capacitor and the load resistor, and produces a single low-frequency pole. The power stage also consists of a higher-frequency zero set by the output capacitor and its equivalent series resistance (ESR). Type-II compensation normally introduces one zero and one pole to compensate the output pole and output zero.

Engineers designing with traditional PCM control devices prefer external compensation to achieve good loop performance for wide output-voltage-range applications. However, external compensation complicates loop design and requires more external components. To simplify the design, a growing number of integrated



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circuit (IC) manufacturers have developed internally compensated PCM control devices that integrate Type-II loop compensation with Rc, Cc1 and Cc2. Rc and Cc1 generate a fixed internal zero to compensate the output pole, while Rc and Cc2 produce a fixed internal high-frequency pole to compensate the output zero. Both the effective output capacitance and load resistance have an impact on the output pole, however. In order to support a wide output-voltage range or wide output-capacitance range, you must set the fixed internal zero relatively low to get good stability. What's more, the cross-frequency (fc) of PCM control is designed to meet fsw/5 < fc < fsw/10. Therefore, the error amplifier introduces some delay, which limits the load-transient response.

PCM also has these drawbacks:

- The lower the output voltage, the lower the load resistance under a certain output current. Getting the output pole close to the fixed internal zero requires a large output capacitance, resulting in a higher bill-of-materials cost.
- Some PCM devices that clamp the control voltage to achieve high efficiency at a light load may face multipulse issues, resulting in a large output ripple.

D-CAP2 control scheme

The D-CAP2 control scheme is a variation of adaptive COT control with an emulated ramp-generator circuit integrated inside the IC. This control scheme is popular in buck converters because of its simplicity and improved load-transient performance. Figure 3 shows the block diagram for D-CAP2 control of buck converters, while Figure 4 shows the corresponding control waveforms.

The ramp generator (ripple injection generator) emulates the inductor current information and brings this information back to the comparator.



Figure 3: D-CAP2™ control scheme block diagram.



Figure 4: D-CAP2 control scheme waveform.

When the emulated ramp voltage and feedback voltage are lower than the reference voltage, the comparator output goes high to initiate an on-time pulse. The width of the on-time pulse (Ton) is constant, since it is calculated by the adaptive on-time generator based on the input voltage, output voltage, output current and frequency setting. The off-time relies on the voltage ripple, which has some variation during a line or load transient. As a result, the switching frequency is pseudo-fixed. During the on-time, the high-side FET turns on and the inductor current increases to charge the output voltage. After the on-time, the high-side FET turns off and the lowside FET turns on. The output voltage goes down until the generation of the next on-time pulse. Because D-CAP2 control topology doesn't integrate an oscillator or clock, the on-time may be affected by a propagation delay from logic to driver, resulting in poor jitter performance. That is the main reason why it is not easy for IC manufacturers to design high-switching-frequency buck converters (2.1 MHz) with D-CAP2 control topology. Additionally, there are different offset voltages of the emulated ramp-generation circuit under different load conditions, resulting in poor output-voltage accuracy.

The D-CAP control topology requires some ripple on the output where low ESR capacitors can become a problem. That's why engineers need D-CAP2 control. There is some limitation to the internal emulated ramp-generator circuit of the D-CAP2 buck converter as well, so the traditional D-CAP2 buck converter can only support an output up to 7 V. There is a minimum off-time requirement as well because of the valley voltage detection; thus, D-CAP2 control is not recommended for large duty-cycle applications.



Figure 5: Bode plot of a D-CAP2[™] buck converter.

Reference [2] proposed an open-loop transfer function of the D-CAP2 control topology. Figure 5 shows the corresponding Bode plot. The emulated ramp-generation block introduces one internal zero, which can eliminate the double pole set by the output inductor and capacitor, thus making the gain plot crossing the horizontal line 0 dB with a slope of -20 dB per decade, and boosting the phase margin at the crossing frequency. Equation 1 expresses the DC gain of the open-loop transfer as:

$$G(0) = A \times H(0) = A \times V$$
 (1)

where
$$Acp = (R1 + R2)/R2$$
.

Since Acp and Vref are constant, the DC gain is an inverse proportional of VOUT. As shown in Figure 6, if VOUT1 > VOUT0 > VOUT2, then the DC gain trend is Gain1 < Gain0 < Gain2. For a certain device, the internal zero is fixed. Assuming that the double pole for different outputs is the same, the bandwidth trend is fBW1 < fBW0 < fBW2. Therefore, for a D-CAP2 buck converter, a higher output voltage would have a lower bandwidth.

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www.kikusuiamerica.com kikusui@kikusuiamerica.com Kikusui America, Inc. 3625 Del Amo Blvd, Ste 160 Torrance, CA 90503 Tel: 310-214-0000 Additionally, because the duty cycle cannot change with COT control, the on-time generator will produce a delay factor in the loop, causing a phase drop at high frequency. A larger duty cycle means a longer on-time, resulting in a bigger phase drop.



Figure 6: Bode plot with different VOUT conditions of a D-CAP2^m buck converter.

AECM control benefits

AECM is a new topology based on a fixed-frequency modulator with emulated current information for the loop control, combining the fixed frequency of PCM control and the fast load-transient response of the D-CAP2 control topology. The key features and benefits of AECM include:

True fixed-frequency modulation that can simplify EMI filter design and make it easy to achieve high-frequency modulation such as 2.1 MHz.

An emulated ramp-generator circuit with smart loop-bandwidth control that can adjust the DC gain smartly, supporting wide-output and high-duty-cycle applications with good load-transient performance.

It is possible to simplify AECM control for a buck converter, as shown in in Figure 7. There are two basic operation modes, PWM mode and PFM mode, selectable by the mode-detection block. The integrator in the voltage loop can improve output-voltage accuracy issues.



Figure 7: AECM control block diagram.

The integrated oscillator generates the fixed clock. Implementing slope compensation in the modulator avoids subharmonic oscillation when the duty cycle is higher than 50% in PWM mode. The emulated ramp generator with the smart loop-bandwidth control circuit can adjust the DC gain to achieve high bandwidth over all output rails. And even though there is an integrator, unlike PCM

control, the integrator in AECM control can improve output-voltage accuracy with no direct impact on loop response speed.

How AECM control works

PWM operation mode

The PWM mode control scheme is similar to PCM control. As shown in Figure 8 on the following page, the internal clock initials one onpulse; the high-side FET then turns on, with current increasing in the inductor. When the emulated ramp voltage, feedback voltage and slope compensation voltage reach the integrated reference voltage, the high-side FET turns off and the low-side FET turns on until the next clock cycle. Therefore, in PWM mode, the switching frequency is truly fixed.



Figure 8: AECM control scheme waveform: PWM operation mode (a); PFM operation mode (b).

Figure 9 shows the load-transient behavior of the AECM device. The duty cycle increases or decreases with a decrease or increase of VOUT.

PFM operation mode

AECM control implements PFM mode to achieve high efficiency under light loads. With a load current decrease, the device enters into discontinuous conduction mode (DCM) from continuous conduction mode (CCM). In both modes, the switching frequency is fixed; the width of the on-pulse (Ton) depends on the load current. Lighter loads have a shorter Ton. AECM has an on-time generator like the D-CAP2 control topology, but that generator is disabled in PWM mode.



Figure 9: Duty-cycle changes with the load current: load step-up (a); load step-down (b).

With the load current further decreasing, the Ton decreases down to the internal clamped on-time, while the AECM device steps into PFM mode with the internal clock blocked and the on-time generator enabled. As shown in Figure 8, the control scheme of PFM mode is similar to the D-CAP2 control scheme. Figure 10 on the following page shows the transition waveform between PWM mode and PFM mode.



Figure 10: Transition waveform between PWM mode and PFM mode of AECM: PWM mode to PFM mode (a); PFM mode to PWM



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Smart loop-bandwidth control

Unlike PCM control, where direct inductor current information is in the loop, AECM uses emulated inductor current information. The output filter of AECM control introduces one double pole like the D-CAP2 control topology. Thus, the Bode plot of AECM control is similar to the D-CAP2 control topology.

In D-CAP2 control, the Acp is constant and the DC gain of the openloop transfer function changes with VOUT. While in AECM control, the Acp adapts to the changing value of R2 per the VOUT setting to keep the Acp × VOUT a constant value for a fixed DC gain. As shown in Figure 11, assuming that the double poles for different outputs



Figure 11: Bode plot under different VOUT conditions of AECM.

	Traditional PCM buck converter (internal compensation)	AECM buck converter
Load- transient response	 Slow. The fixed internal zero is set relatively low. Error amplifier delay. 	 Fast. Smart loop-bandwidth control provides a relatively high internal zero. No error amplifier delay.
Light Ioad pulse	 Single or nonsingle. Pulse controlled by the clamping control voltage. 	Single. Pulse controlled by the on-time under PFM operation mode.
Wide output stability	 Difficult. The fixed and relatively low internal zero makes it hard to support a wide output range. 	Easy. Smart loop-bandwidth control provides an adjustable bandwidth.



Figure 12: Measured Bode plot of 5-V and 1.05-V outputs.

are the same, the loop bandwidths under different outputs should be much closer to each other when compared to the loop bandwidths of D-CAP2 control.

Figure 12 on the following page shows the measured Bode plot of AECM control under different VOUT conditions. The DC gains are almost the same. The crossing frequency and phase margin have slight differences because of the output double-pole shift.

Table 1 compares a traditional PCM buck converter with an AECM buck converter. Table 2 on the following page compares a D-CAP2 buck converter with an AECM buck converter.

Conclusion

Devices with the AECM control topology for DC/DC converters can achieve a fast load-transient response with a true fixed frequency, while maintaining a wide output voltage and low design cost. This new control topology has been implemented in several products with good performance, ease of use and small solution size.

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Table 1: Comparing PCM and AECM buck converters

	D-CAP2*** DUCK CONVERTER	AEGWI DUCK CONVERIER
Frequency	 Pseudo-fixed and hard to support high frequencies. Frequency depends on the on-time generator, resulting in a large frequency variation. 	 Truly fixed and easy to support a high frequency. The frequency depends on the internal clock, resulting in a small frequency variation.
High V _{OUT}	 Less than 7 V. Limitation from the internal emulated ramp-generator circuit. 	 Higher than 7 V. Improved internal emulated ramp-generator circuit and smart loop-bandwidth control.
Large duty cycle	 Difficult. Limitation from the internal emulated ramp-generator circuit. Requires a long minimum off-time. 	 Easy. Improved internal emulated ramp-generator circuit and smart loop-bandwidth control. Requires a short minimum off-time. On-time extension function.

Table 2: Comparing D-CAP2™ buck converters and AECM buck converters

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Pulsed Inductance Measurement on Magnetic Components from 0.1A to 10kA

Pulse measurement with IGBT power stages using the Power Choke Tester DPG10/20 series was presented in detail in the first and second parts of this series of articles on inductance measurement. The third part shows how the measurement principle can also be used to measure the inductance of 3-phase chokes with the help of a 3-Phase Extension Unit and what significant advantages it has over conventional measurement with mains voltage and mains current.

By Hubert Kreis, Chief Executive Officer, ed-k, Germany

Introduction

3-phase chokes are used in many applications such as output filters and input filters for frequency converters and commutation inductors for line-commutated converters. Normally, they are made of electrical steel sheets with three legs of the same cross-section. They are specified by their inductance and rated current at 50 or 60 Hz. Due to the asymmetrical, flat structure, the inductance of the two outer legs is usually lower than the inductance of the middle leg.

Conventional measuring method

In the conventional measuring method, the choke is connected to an adjustable 3-phase, sinusoidal, high-current, 50 or 60 Hz power supply in order to determine the inductance. The current is then adjusted to the rated RMS current for all three windings and the RMS voltage is then measured on each winding. The secant inductance (often called amplitude inductance) of each phase k can then be calculated according to the common alternating current theory with the following equation, neglecting the ohmic resistance:

$$L = \frac{Urms}{2\pi f * Irms}$$

Taking the ohmic resistance into account, this results in:

$$L = \frac{\left(\sqrt{\left(\frac{Urms}{Irms}\right)^2 - R^2}\right)}{2\pi f}$$

In addition to the 3-phase high-performance power supply, the test setup requires 3 RMS current meters and 3 RMS voltage meters. Normally, only one measurement is performed at the rated current. The difference between the middle leg and the two outer legs (3 - 9%) is mostly neglected.

Pulse measurement principle on 3-phase chokes

If the measuring pulse of the Power Choke Tester DPG10/20 series is only fed into one winding of a 3-phase choke, then completely different flux conditions are obtained in the core than with a 3-phase sinusoidal feed. The measurement result would be useless.

However, if a few points are considered, the pulse measurement method of the Power Choke Tester DPG10/20 series is also suitable for measuring the inductance of 3-phase chokes.

- The windings of the 3 legs must be interconnected in a suitable way so that a flux distribution in the core results that corresponds to that with the 3-phase sinusoidal current feed.
- For the independent characterisation of all three legs, several measurements must be carried out.

- All legs must have the same core cross-section.
- The secant (= amplitude) inductance measurement L_{sec}(i) is to be used, from which the corresponding inductance of the middle and outer legs is to be calculated.
- In order to be able to scale the current axis with the corresponding RMS value, as is also specified in conventional measurement with 50/60 Hz mains voltage, a corresponding correction is required.
- Frequency effects due to excitation with a rectangular pulse not equal to 50 or 60 Hz must be corrected.



Figure 1: 3-Phase Extension Unit EXT1

In order to enable automatic and simple operation without manual reconnection of the windings, ed-k has developed special additional units for the Power Choke Tester DPG10/20 series: the 3-Phase Extension Units. In conjunction with sophisticated software algorithms, they provide a result that is equivalent to a conventional measurement with 3-phase sinusoidal voltages and currents. A correction to a reference frequency of 50 Hz or 60 Hz can be made if the pulse width has not corresponded to this frequency.



Figure 2: Inductance curves of a 3-phase inductor L1(I_{RMS}), L2(I_{RMS}) and L3(I_{RMS})

As opposed to conventional measurement, the measurement result not only provides the inductance at one measuring point, but a complete inductance curve $L1(I_{RMS})$, $L2(I_{RMS})$ and $L3(I_{RMS})$ for each individual winding of the 3-phase choke. Thus, the usually higher inductance of the middle leg can be seen immediately.



Figure 3: Current waveforms in the linear range CH1-CH3: 20A/div



Figure 4: Distorted current waveforms in the non-linear range CH1-CH3: 20A/div

It is worth noting that only 4 measuring pulses are necessary for this.

Advantages of the pulse measurement principle

Compared to conventional measurement, the pulse measurement principle has decisive advantages.

Conventional measurement only provides correct results in the linear range. Due to the extremely non-linear behaviour of the core materials (saturation), the currents and/or the voltages are distorted and no longer sinusoidal. This is especially true for iron-based core materials, which have a much lower permeability at both very small and large magnetic field strengths H than in the normal working range. If sinusoidal currents are applied to the 3-phase inductors, a non-sinusoidal voltage results on the test specimen. Conversely, non-sinusoidal currents result if a sinusoidal voltage is applied.

In practice, neither sinusoidal currents nor sinusoidal voltages result. The normally round sine peaks become pointed. In extreme cases, there may even be steep, needle-shaped pulses on the peaks. The measured variables feature considerable harmonic contents.

The above equations come from the common alternating current theory and are valid only for linear conditions. They are therefore no longer permitted for the calculation of the inductance in the non-linear range (saturation)!

Another problem of conventional measurement is the RMS value measurement of voltage and current. In RMS value measurement, by definition, the measured variable is evaluated quadratically and integrated over a period (same heating of an ohmic resistance as a direct current with the same value). The RMS value measurement of distorted measured variables containing harmonics therefore provides a result that obviously has nothing to do with the physical relationships of magnetism.

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For these two reasons, therefore, conventional measurement systematically provides incorrect measurement results with non-linear conditions. Due to the principle, however, the pulse measurement method also provides correct measurement curves $Lk(I_{RMS})$ even with non-linear conditions. Each inductance determined at overload currents is just as accurate as at the rated current!



Another significant advantage of the pulse measurement method is that the measurement can be carried out more easily and very much faster than the conventional measurement. With the help of the 3-Phase Extension Unit, the measurement curves L(I_{RMS}) for all 3 legs are already available after about 5 secs.

Even in the case of measurements in the overload range with measurement currents that are significantly larger than the rated current, the measurement result is not influenced by thermal effects, as the short measuring pulses do not cause any heating.

Safety

In order to characterise inductive power components under real operating conditions, the Power Choke Tester DPG10 series must operate with high voltages and currents. A very large pulse energy must be available for large components.

In order to be able to guarantee maximum safety for the user and compliance with all safety-relevant regulations and standards at all times, the DPG10/20 series is based on a comprehensive, sophisticated safety concept. It includes extensive safety and monitoring circuits. All safety-relevant circuit parts such as charging circuit, discharge circuit and monitoring circuits are subjected to a self-test after switching on the device. If the self-test fails, the device is placed in an energy-free, safe state within <100 ms.

The device is similarly placed in an energy-free, safe state within milliseconds if a monitoring circuit detects a fault. Particularly critical monitoring circuits are redundantly implemented. Of course, the DPG10/20 series also meets the EN 61010 safety standard, which also includes the safety requirements under fault conditions. For inductance testing in series production, the DPG10/20 series has a safety lock interface, to which a safety contact of a protective cover or a light curtain can be connected. If the safety contact is interrupted, measuring pulses are immediately blocked and the outputs are switched off within milliseconds.

Summary

The 3-phase test system based on the proven DPG10 technology can not only rationalize inductance testing in series production. Due to the complete inductance curves, it is also an efficient and high-precision engineering tool that can be used for the development and selection of optimised components for various applications. This is the case in particular when the inductance must be taken into account for overload currents, as the conventional measuring method with mains voltages and mains currents in the nonlinear range provides inherently incorrect results.

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Modified Standard, Semi-Custom and Full-Custom Designs

RECOM offers over 25,000 standard portfolio DC/DC and AC/DC products, but still at times, a non-standard converter is needed. This article explores the difference between modified standard, semi-custom and custom power converters.

By By Steve Roberts, Innovation Manager, RECOM



One of the reasons RECOM has the broadest power converter portfolio in the industry is the sheer number of variations available within our standard product range. If we take a classic 5W isolated and regulated DC/DC converter in a DIP24 case, the REC5 series (for example), then the datasheet explains that it has five input and nine output voltage range options, including single and dual outputs. There are three different isolation voltage options from 2kV up to 6kV and three different pinning options to make it a pincompatible alternative to the competition, including a version with a remote on-off pin. Additionally, the board mounting pins can be through-hole or SMT. The case material can be plastic or metal. Finally, the series is available with either tube or tape-and-reel packaging options. Overall, for this one DC/DC converter series, there are well over two thousand permutations as standard!



Figure 1: Simplified shunt regulator circuit (in this circuit, Vset would be Vref(1+(R1/R2)) + Voptodiode)

Modified standard power converter

It would seem that all possible customer requests would be covered with such a wide portfolio of catalog products, but still sometimes specific characteristics requested by customers are not included in these options. An example would be different pin lengths (shortened or over-long) or a 5.7V output voltage instead of the usual 5V output voltage so that an OR-ing diode could be included in the output circuit. Such requests are very easy to implement and fall under the umbrella of 'modified standard' products.

To understand why a modified output voltage is so simple, it helps to look at the most common way of regulating the output voltage in a DC/DC or AC/DC converter – an output shunt regulator based on a precision programmable reference IC (Figure 1).

On each switching cycle, the output voltage rises until the shunt regulator set voltage, Vset, is exceeded, upon which the optocoupler is energised and the cycle reset. Although very simple, this circuit accurately regulates the output voltage for both load and line voltage variations. The switching duty cycle and hence output voltage is decided by combining the turns ratio of the transformer, the Vref voltage (typically 1.22V) and the two programming resistors R1 and R2. Modifying this converter to offer 5.7V instead of 5.0V would require fitting alternative R1 or R2 values to create a different programming divider ratio, a simple modification that could be carried out at little to no extra cost. RECOM has its own SMD assembly lines, so creating a batch of converters with a modified output voltage would mean changing only the production SOP and the laser-printed label.

We can also optimise the choice of component values to fit the specific requirements of the customer's end application, rather than



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relying on a standard converter. If we take an unregulated DC/DC converter as an example, then the output voltage depends on both load and input voltage. Typically, we adjust the component values so that the nominal output voltage is delivered with the nominal input voltage and 80% load, as shown in the diagram of the output voltage tolerance envelope (Figure 2).



Figure 2: Example of an unregulated converter voltage tolerance diagram (R1SX series)

This standard configuration fulfils the most common requirements for the output voltage tolerance for unregulated DC/DC converters, which typically operate at slightly less than full load. The compromise is that the output voltage is lower at full load and higher at low loads. Should a customer demand that the output voltage rise to less than +7% under low load conditions, then we can modify the design to keep the output voltage under, say, +5% by modifying the component values so that the Vnom voltage is delivered at 70% load instead of 80%, effectively shifting the tolerance envelope downwards. The disadvantage would be a lower output voltage at full load but may not matter in this particular application.

However, the amount of output voltage modification that can be achieved by optimising the component values to better match the requirements of the end application is limited. The nominal output voltage depends on the turns ratio of the transformer, so if the required output voltage deviates too far away from the standard, then a modified transformer with an adjusted turns ratio could be required. This would entail not only a custom transformer part number but also a re-certification of the safety standards. We will now move away from a modified standard converter to describe a 'semi-custom' design.

Semi-custom power converter

The boundary between a semi-custom and a modified standard power converter is not always obvious, so a useful definition is whether safety re-certification is needed. Modifications that influence safety-critical components or separations - such as the transformer construction, choice of optocoupler or Y-capacitor, or creepage or clearance distances - will almost certainly require a new certification process. However, the safety test reports typically allow a ±10% variation in the output voltage and current rating to accommodate production tolerances, leaving some scope for flexibility. The input voltage rating also has at least a ±20% tolerance and often more. If the required modification can respect these tolerance bands, then safety re-certification may not be required. The same applies if the original safety test report lists 'alternate construction' options for certain components or the potting materials. We have customer applications where silicone potting material is unacceptable, either because of the possibility of outgassing, which could affect other parts or because silicone could emit smoke in a fire, so although silicone is an excellent encapsulation material with high thermal conductivity and good adhesion, we could offer these customers epoxy potting as a modified standard.

It may seem surprising, but the label design and text are considered part of the safety documentation and are very carefully controlled by the certifying bodies. We regularly receive requests for a custom label design with, for example, the customer's own brand name and part number instead of RECOM's standard label. Although physically the two parts would be identical, we would need to apply for a copy certificate with the new label, part number and customer logo to manufacture this modified part with valid safety certification. However, we have experience in handling such requests and we strive to make the process as fast, simple and unbureacratic as possible.

Once we enter the realm of semi-custom power converters, then we can offer much more flexibility than simply tweaking the specifications, such as using alternative PCB layouts to change the shape of the converter or matching the pinout to replace a competitor's part that has been rendered obsolete. The changes do not need to be physical; we have made semi-custom converters that use higher-rated components to extend the operating temperature range or harder epoxy to allow the converter to meet specific environmental conditions. All of these modifications are based on standard designs, so although a semi-custom product meets individual customer requirements for form, fit or function, it can still be manufactured quickly and cheaply on our standard production lines with a short time-to-market.

Semi-custom power converter examples

In 2010, a US competitor abruptly stopped manufacturing a series of switching regulators, leaving their existing customer base 'in the lurch.' One customer approached us, asking if we could modify our standard R-78 series to be pin-and-function compatible with these end-of-life products, even though the format was completely different from our existing design. In only 12 weeks, we released the R-78T series with three different open-frame SMD pinning options, designed to be pin-compatible with these no longer available parts. The reason we could react so swiftly was that we did not need to start from ground zero – we already had extensive experience in designing and manufacturing switching regulator modules and could use this as a base for the semi-custom design.



Figure 3: The three different formats (/AC, /AL and /FC) of the R-78T series



Figure 4: The semi-custom RAC20-K/X6 with IEC 62477-1 certified OVC III

More recently, we received a request for a 20W board-mount AC/ DC module to be used as an auxiliary power supply in an EV charging station. As the charging station is hard-wired to the electricity supply, it is classed as an OVC III (Over Voltage Category III) installation and has to satisfy additional safety requirements concerning





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overvoltage surges, isolation ratings and creepage and clearance distances. We were able to manufacture a semi-custom product, the RAC20-K/X6 with a revised PCB layout and transformer construction to meet the IEC 62477-1, OVC III requirements with 4kVAC/1 minute rated reinforced isolation instead of the standard 3kVAC/1 minute rating. This feat was achieved without changing the dimensions, pinout or other important specifications such as the wide input voltage range, wide operating temperature range and <40mW no-load power consumption.

With many semi-custom designs, other customers also need similar parts, and they can become standard off-the-shelf options in our portfolio.

Full-custom power converter

A full-custom power converter differs from the modified standard or semi-custom variants because it is not based on an existing product, but it obviously uses proven and tested building blocks and existing production infrastructure where appropriate. Typical requirements that would make a custom power converter project viable would be that no existing product can fulfil the need, that the costs (R&D, testing and production) are viable for both partners, and that the project volume justifies the investment in resources.

The typical custom power converter project stages are shown in Figure 5:



Figure 5: Custom power converter project stages

Project Proposal: The initial request from the customer detailing the technical requirements of the custom power converter (functional specifications, performance requirements, technical standards and physical dimensions) as well as the commercial factors (budget, expected volume, target cost, etc.)

Project Evaluation: Analysis of the technical requirements (suitability, manufacturability, resource availability, etc.). Is the project viable?

Project Plan: The project plan details the project schedule, resource allocation and milestones that need to be achieved at each stage of the project.

Prototype: Prototypes will be built to verify compliance with the functional specifications. A change in specifications at this stage is common. RECOM understands that even when the initial custom power converter requirements are clear and well-defined, the specifications may need to be occasionally updated or further modified, usually reacting to changes in the market. This is normal. As long as the communication channels between the customer and the RECOM design team are open, we aim to be as flexible as our customers.

After approval of the initial prototypes, the next stage is the manufacture of pre-production prototypes (at least 50 units) so that statistically valid performance and stress testing can be conducted.

DVT/PVT: The design verification tests and production verification tests are critical to the success of the project. RECOM needs to provide datasheets and test documentation that will inspire in the customer a high level of confidence that the custom design is fit for purpose and will function reliably under all foreseeable operational and fault conditions. To do this, RECOM has an automated test lab with networked test stations to allow rapid testing and evaluation, whether it be electrical testing, environmental testing in climate chambers, reliability testing (electrical and thermal stress tests, safe operating area tests, long term soak tests, shock and vibration, etc.) or production tolerance testing.

Production and Certification Plan: As soon as the DVT testing is advanced enough to initiate a design freeze, then the production plan can be started, entailing purchasing of the necessary components from primary and second sources and ordering the custom housing, printing and packaging. The production-ready prototypes can be sent off for agency approval (UL, IEC, EN, CB Reports, etc.).

Production: An assembly line will be set up to manufacture, test and ship the final product to the customer.

Change Management: As mentioned previously, change is a fact of life and needs to be managed. Technical standards are updated on average every three years, and sometimes this requires a modification to the custom design to stay compliant with any new regulations. Changes to the availability of key components may require notification to, and agreement from, the customer, with a Product Changer Notice (PCN). The Product Life Cycle (PLC) documentation is maintained over the lifetime of the product until the eventual end-of-life decision by the customer.

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Туре	Customisation level	Complexity	Speed	Added Cost
Modified Standard Product	restricted	Simple	Several weeks	Low or no added cost
Semi-Custom	flexible, but limited	medium	A few months	Low NRE costs, but may involve re-certification fees.
Full Custom	open	complex	Several months	Product-dependent, but NRE charg- es and new certification costs are significant

As can be seen by this brief introduction, a RECOM power converter can be offered as a modified standard, semi-custom or full-custom product to the customer in several ways. Each variant has advantages and disadvantages (Figure 6), so the simplest way to decide is to escablish a dialog with us so we can advise and work together with you to offer the optimum solution.

Figure 6: Summary of the advantages and disadvantages of modified standard, semi-custom and full cus- to offer the optimum solution.

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How To Design Reliable Multilevel Bridgeless Totem-pole PFC

This article discusses key design guidelines to implement safe operating conditions for power switches, enabling delivery of higher reliability and greater robustness for multilevel totem-pole PFC.

By Dr. Trong Tue Vu and Rytis Beinarys, ICERGi

Multilevel totem-pole PFC offers the designer market appealing advantages over 2-level designs including a significantly smaller inductor, much lower dv/dt's and reduced switching losses. The inherent reduction in switch operating voltage enables the multilevel PFC to be optimally implemented by low-cost standard multi-sourced 150V MOSFETs with minimal reverse recovery time and charge. This implementation enables best-in-class efficiency > 99.2% at much lower system cost compared to existing wide-band gap (WBG) solutions in the market.

Multilevel Implementation of Totem-pole PFC



a) Topology



b) Phase-shifted PWM modulation for two switching cells

Figure 1: Bridgeless Totem-pole PFC Design using 150V MOSFETs

Due to the lowest conduction losses, the bridgeless totem-pole arrangement is a preferred PFC topology for single-phase AC/DC applications [1], [2]. The high frequency switching leg can be implemented in either a 2-level fashion using 650V WBG devices [1] or a multi-level arrangement based on readily available 150V MOSFETs [2]. The latter implementation illustrated in Figure 1(a) allows for optimal power conversion with 75% smaller magnetics and 50% lower BOM costs. These substantial benefits are a direct result of how power is digitally modulated and converted from AC to DC. Specifically, 8 x 150V MOSFETs (Q_1 to Q_8) and capacitor C_2 are ar-

ranged to form two 2-level switching cells. The inner cell including Q_3 , Q_4 , Q_5 and Q_6 is controlled to be 180-degrees phase shifted to the outer cell composing of Q_1 , Q_2 , Q_7 , and Q_8 . Serially connected MOSFETs in each cell, e.g. Q_3 and Q_4 , are driven on and off together by isolated low-cost gate drive circuits based on ICERGi IC70001. Exemplary drive signals for the two switching cells are demonstrated in Figure 1(b).

Since the two switching cells are cascaded and phase-shifted, the multilevel topology processes power more efficiently and quietly than a conventional 2-level solution. In particular, power conversion happens at half of the output voltage and twice the switching frequency of power devices, which results in:

- 4 x reduction in the volt-seconds product for the main inductor. This allows for a 4x smaller inductor design using low-cost standard Sendust toroidal cores and solid enamelled wire, enabling 50% BOM cost reduction. In addition to cost and size benefits, a smaller inductor is more efficient at low-line operation, which improves converter efficiency further.
- Lower switching losses
- Reduced dv/dt which is of value in limiting EMI effects

As similar to any PFC topologies, the reliability of the multilevel totem-pole design is dictated by the life span of power switches, particularly 150V MOSFETs. Therefore, keeping these devices well within their electrically and thermally safe operating areas is required for long life and reliable applications. The next part of the article will discuss how to meet such requirements in a real-word design.

Voltage Balance is Key

Capacitors C₂ and C_{bulk} shown in Figure 1(a) define the operating voltage for each pair of serially connected MOSFETs in a switching cell. However, the operating voltage of each MOSFET may not be well defined depending on its switching characteristics as well as how it is driven [2]. Such sensitivity is fully addressed by adding two flying capacitors C₁ and C₃ to the switching cells as illustrated in Figure 1(a). Maintaining the operating voltage level for all switching devices within their specifications is achieved by controlling the voltage across three flying capacitors C₁, C₂, C₃ and output capacitor C_{bulk}.



Figure 2: Flying capacitor voltage monitoring and control

The PFC output voltage V_{Cbulk} is measured and regulated by a digital PFC controller. The phase-shifted modulation naturally forces the voltage of C₂ to settle at a half of the output voltage V_{Cbulk}. Even though natural balance is sufficient to address most device and manufacturing tolerances, the flying capacitor voltage V_{C2} should be actively monitored and controlled for greater protection. Such a control feature is incorporated in ICERGi PFC controller IC70101 as illustrated in Figure 2. The voltage across C₂ is first buffered by a differential amplifier whose output is then fed to the PFC controller IC70101 for ADC measurement and software protection. An additional analogue circuitry with fast comparators can be used to provide an extra layer of over voltage protection for switching components.

Precise drive delay matching for serially connected MOSFETs is required to minimize the energy absorbed by C₁ and C₃ during turnoff transitions. Such a requirement can be met by using miniature isolated drive transformers in conjunction with ICERGi gate driver IC70001. Since C₁ and C₃ do not have to handle any significant power during operation, their values can be small, e.g. around 47nF. Consequently, their voltage can be effectively controlled by using 4 x TVS devices T₅, T₆, T₇, and T₈. For minimal power losses, the



Start-up: V_{line} = 230V_{ac}, No load



Steady State Operation: $V_{line} = 230Vac$, $P_{load} = 3kW$



2kV L-to-N Differential Surge, $V_{line} = 230V_{ac'}P_{load} = 2kW$

Figure 3: Flying capacitor and output voltage during start-up, steady state, and line voltage surge conditions. $(V_{C1} = BLUE, V_{C2} = RED, V_{C3} = GREEN, V_{Cbulk} = ORANGE)$

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norwe.de | norwe.eu norwe.com clamping level is chosen to be above 115V and only triggers one of the TVS devices when V_{C1} and V_{C3} drift away from their balance points of V_{Cbulk}/4 and 3*V_{Cbulk}/4, respectively.

It should be noted that capacitor voltage V_{C2} is well controlled during all operating conditions while the output voltage V_{Cbulk} could experience fast transients during power-up and line voltage surges. Therefore, two additional TVS devices T_1 and T_2 shown in Figure 1(a) are included in the outer cell to provide adequate voltage clamping preventing MOSFETs from entering avalanche mode.



Figure 4: Recommended PCB layout for switching cells of multilevel totem-pole PFC

Figure 3 demonstrates the behaviour of V_{C1}, V_{C2}, V_{C3}, and V_{Cbulk} during different operating conditions. Evidently, the voltage balance is well maintained not only at steady state but also during transient responses. The worst-case scenario for the outer cell occurs during a differential-mode surge as demonstrated in Figure 3(c). The converter quickly increased V_{C3} in response to the fast variation in V_{Cbulk}, which maintains the operating voltage for the outer cell MOSFETs well within the 150V limit.

Mind The Loop

In addition to the operating voltage, the overshoot during MOS-FET turn-off transitions needs to be controlled in order to meet the design requirement. Turn-off overshoots in general are a function of parasitic inductance and reverse recovery current. Most commercial 150V MOSFETs already have excellent reverse recovery characteristics intended for hard switching applications; hence, minimizing parasitic inductance through PCB layout optimisation is a necessary step. Using SMD components and low ESR ceramic capacitors for loop size reduction is recommended. Figure 4 exemplifies a PCB design in which 8 x SO8 MOSFETs and SMD flying capacitors are arranged to minimize 4 loops formed by (Q_4 , Q_5 , C_1), (Q_6 , Q_3 , C_1 , Q_2), (Q_7 , Q_2 , C_2 , C_3), and (Q_8 , Q_1 , C_3 , C_{bulk} , R_{cs}). The two film-type PTH capacitors in parallel with C_2 are not included in Figure 4 for ease of demonstration.

Thanks to low loop inductance and excellent reverse recovery performance, the switching waveforms of MOSFETs Q_1 , Q_2 , Q_7 , and Q_8 exhibit clean transitions with minimal overshoots. Even for the maximal loading condition as illustrated in Figure 5, the overshoot is less than 10V and all switching components in the outer cell experience less than 120V. This suggests an operating margin of 30V or 20% which is very desirable for hard-switching applications.

Similarly, the Drain-to-Source voltage of other 4 MOSFETs Q₃, Q₄, Q₅ and Q₆ also undergoes minimal overshoot and ringing, resulting in maximal voltage stress of less than 120V. Due to space limit, the experimental data for the inner cell is not included in this article but can be provided upon request.



(c) Q₇

Figure 5: Drain-to-Source voltage of switching devices in the outer cell. The testing condition is 115Vac and 1.5kW. Experimental data were collected by a floating oscilloscope and a 300MHz single-ended probe. The 20MHz bandwidth limit function is disabled.

(d) Q₈

Stay Cool Stay Reliable

In addition to electrical stress, high operating temperatures greatly affect the life span of switching components in general and in particular 150V MOSFETs. A reliable design should be able to limit component temperatures while delivering maximal power to the load. This target is not easy to achieve if the converter is inefficient and the heatsink size is constrained.

Multi-level totem-pole PFC is thermally more advantageous than 2-level solutions thanks to more efficient power conversion and greater loss distribution. In particular, the 3kW multi-level totem-pole PFC prototype as shown in Figure 6 can achieve > 99.2% efficiency at 230Vac for 30% to 50% load, and has a total loss of < 38W at 100% load. The overall losses present in the switching leg is in the order of 20W which is distributed evenly between 8 MOSFETs. Therefore, each MOSFET has to dissipate around 2.5W at full load, which can be achieved by bottom-side cooling working in conjunction with thermal vias and thermal interface material.



Figure 6: 3kW multilevel totem PFC prototype and efficiency data

Figure 7 shows a thermal image of 4 MOSFETs in the inner cell. The remaining outer cell MOSFETs are covered by the control card and cannot be seen in the image. The thermal data suggests that the maximal absolute temperatures of the 4 switches are well below 50 degrees Celsius at full load and minimal air flow. The temperature rise above the ambient temperature is 30 degrees Celsius. This ties in well with the efficiency data and the estimation of power loss per MOSFET. It is important to stress that having the power switches running cooler is the most effective way to improve the product reliability.



Figure 7: Temperatures of Q_3 , Q_4 , Q_5 , and Q_6 captured at $V_{line} = 230V$ and $P_{load} = 3kW$. Measurements were taken after 20 minutes running at the ambient temperature of 20 degrees Celsius. Air flow is < 0.3m3/min.



Summary

Using 150V MOSFETs for 400V power conversion does not make the design less reliable if all switching devices are controlled to operate well within their electrical and thermal ratings. As demonstrated in the article, multilevel bridgeless totem-pole PFC can be designed to operate well within their safe operating area with significant margins at extreme conditions and be as reliable as any other topologies. By controlling the flying capacitor voltages, the voltage stress for 8 x 150 MOSFETs remains within 120V at steady state and 150V for line voltage surges and transients.

Thermally, the multilevel totem-pole PFC offers advantages over 2-level solutions because multilevel power conversion is more efficient (>99.3% efficiency), leading to lower power losses and heat generated. Additionally, multiple switching components spread the losses over more switches, minimizing the risk of thermal hotspots commonly associated with a 2-level design.

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The Interleaved Inverting Charge Pump – Part 1: A Topology for Low Noise Negative Voltage Supplies

Analog Devices offers a wide variety of solutions for producing low noise power. Most of these solutions are designed to produce positive voltage rails, with fewer dedicated ICs for generating negative voltages. This can be particularly limiting when the negative voltage needs to power low noise devices, such as RF amplifiers, switches, and data converters (ADCs and DACs).

By Jon Kraft, Senior Staff Field Applications Engineer and Steve Knoth, Product Marketing Manager, Analog Devices

Introduction

Noise must be minimized in precision instrumentation or radio frequency (RF) circuits, but reducing noise comes with a number of challenges due to the nature of these systems. For instance, these systems must often operate over a wide input voltage while meeting strict electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements. Furthermore, systems are crowded with electronics, making them space-constrained and heat sensitive. The increasing complexity of integrated circuits (ICs) has led to an increase in the number of power supply voltage rails that these systems require. Generating all these rails, meeting the above requirements, and keeping the entire system low noise can be daunting.

In Part 1 of this article series, we introduce a method to generate this low noise negative rail from a positive supply. It starts with a general understanding of how negative rails are typically generated and where they are used. Then we discuss the standard inverting charge pump before introducing an interleaved inverting charge pump (IICP) topology. A short derivation of the input and output voltage ripple for the IICP emphasizes its unique advantages for low noise systems.

Part 2 of the series gives a practical example of an IICP implementation with Analog Devices' ADP5600. We first compare this part to a standard inverting charge pump by measuring voltage ripple and radiated emissions. Then we use the equations from Part 1 to optimize the IICP performance and develop a complete solution for powering a low noise RF circuit.

Traditional Negative Voltage Generation Methods

To create a negative voltage, one of two methods is commonly employed: use an inductive switching regulator or use a charge pump. Inductive switchers use an inductor or transformer to generate the negative voltage. Examples of these magnetic converter topologies are: inverting buck, inverting buck-boost, and Ćuk. Each of these has its own set of advantages and disadvantages regarding solution size, cost, efficiency, noise generation, and control loop complexity.1, 2 In general, the magnetics-based converters are best suited when higher output currents are required (> 100 mA).

For applications requiring less than 100 mA of output current, charge pump positive-to-negative (inverting) dc-to-dc converters can be very small and feature low EMI because no inductors or control loops are required. They simply require moving charge between capacitors via switches—supplying the resulting charge to the output.

Because charge pumps use no magnetics (inductors or transformers), they typically feature lower EMI than inductive switching topologies. Inductors tend to be much larger than capacitors, and unshielded inductors act like antennas by broadcasting radiated emissions. In contrast, the capacitors used in a charge pump do not produce any more EMI than a typical digital output. They can be easily routed in short traces to reduce antenna area and capacitive coupling, resulting in lower EMI.

Table 1 compares inductor-based switching regulator and switched capacitor inverting topologies.

Features	Inductor-Based Switching Regulator	Switched Capacitor Voltage Converter
Design Complexity	Moderate to high	Low
Cost	Moderate to high	Low to moderate
Noise	Low to moderate	Low
Efficiency	High	Low to moderate
Thermal Management	Best	Moderate to good
Output Current	High	Low
Requires Magnetics	Yes	No
Limitations	Size and complexity	V _{IN} /V _{OUT} ratio

Table 1: Comparison of Magnetic and Inverting Charge Pumps

Traditional Inverting Charge Pump

The configuration of the traditional inverting charge pump is shown in Figure 1.



Figure 1: Inverting charge pump schematic.

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The output impedance, ROUT, of the charge pump is defined as the equivalent resistance of the charge pump mechanism from input to output. It is found by measuring the input to output voltage difference and dividing by the load current:

$$R_{OUT} = \frac{V_{IN} - GAIN \times V_{OUT}}{I_{LOAD}}$$
(1)

where GAIN = -1 for an inverting charge pump.

Alternatively, the equivalent output resistance can be calculated as a function of switching frequency, switch resistance, and flyback capacitor size—generally simplified as:

$$R_{OUT} = \frac{1}{f_{OSC} \times C_{FLY}} + 2 \times \sum_{1}^{4} R_{ON}$$
⁽²⁾

Where **Where** is the summation of the four switches' resistance.

Each of the four switches operates at the same frequency, f_{OSC} , and they are on for one half of the switching period, T, where T = 1/ f_{OSC} . Operation can be separated into two phases based on the two halves of the switching period, as shown in Figure 2.



Figure 2: Inverting charge pump during each phase of operation.



Figure 3: Timing diagram for inverting charge pump.

Figure 3 gives the voltages and currents for each phase of the charge pump's operation. In Phase 1, S1 and S2 are closed and S3 and S4 are open. This charges the flying capacitor (C_{FLY}) to a voltage of + V_{IN} . In Phase 2, the energy from C_{FLY} is discharged into the output by opening S1 and S2 and closing S3 and S4. The two distinct phases of operation means that discontinuous current flows into C_{FLY} from V_{IN} , and discontinuous current flows out of C_{FLY} into C_{OUT} . This leads to voltage ripple on C_{IN} and C_{OUT} , which can be

calculated:

$$I_{LOAD} = C_{OUT} \frac{\Delta V_{OUT}}{\Delta t}$$
(3)

Solving for output voltage ripple gives:

$$\Delta V_{OUT} = \frac{I_{LOAD}}{C_{OUT} \times 2 \times f_{OSC}}$$
(4)

Similarly, the input voltage ripple is:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_{IN} \times 2 \times f_{OSC}}$$
(5)

Equation 4 and Equation 5 illustrate that, for a standard inverting charge pump, the voltage ripple is a function of switching frequency and input (or output) capacitance. Higher frequency and higher capacitance reduce this ripple in a 1:1 relationship. However, there are practical impediments to increasing frequency: namely increasing current consumption of the chip, which decreases efficiency.

Similarly, cost and PCB area often restrict the maximum input and output capacitance of an inverting charge pump. Also note that the flyback capacitor plays no role in the charge pump's voltage ripple.

To reduce ripple, input and output filters could be constructed around the charge pump, but this again increases complexity and the charge pump's output resistance. However, these issues can be addressed with a novel improvement to the standard inverting charge pump inverter: an interleaved inverting charge pump (IICP).

Interleaved Inverting Charge Pump (IICP)

Phase interleaving is widely used in inductive switching regulators (that is, polyphase operation) to reduce output voltage ripple.3 A 2-phase buck converter interleaved at exactly 50% duty cycle produces, in theory, 0 mV of output voltage ripple. Of course, the duty cycle of a regulated buck converter changes with input and output voltage, so the 50% case is only realized when $V_{IN} = 2 V_{OUT}$. Charge pumps usually operate at exactly 50% duty cycle, so an interleaved charge pump inverter is interesting to consider.



Figure 4: Interleaved inverting charge pump.

Interleaving charge pumps are sometimes used within ICs when a very low current negative rail is required on the die, but right now there is no commercially available dedicated IICP inverting dc-to-dc converter. The construction of an IICP requires two charge pumps and two flying capacitors. The second charge pump operates the switches 180° out of phase with the first charge pump. Let's look at the setup and the output ripple of an IICP and highlight how to optimize its performance. The setup is shown in Figure 4 with the timing diagram in Figure 5.



Figure 5: Timing diagram for interleaved inverting charge pump.

In each phase of the oscillator, one of the flying capacitors is connected to $V_{\rm IN}$ and the other is connected to $V_{\rm OUT}$. At first glance, one might think that the addition of the second capacitor would only reduce the voltage ripple by half. However, this is an inaccurate oversimplification. In fact, the input and output voltage ripple can be far less than a standard inverter, because a capacitor is always charging from the input and discharging to the output. This can be better understood from the derivation of the IICP's output voltage ripple.

IICP Output Voltage Ripple Derivation

Since the IICP always has one of the flying capacitors supplying current to the output, its output stage can be simplified, as shown in Figure 6.



Figure 6: Simplified IICP output stage.

Furthermore, the IICP's output resistance, as defined in Equation 1, can be approximated by:

$$R_{OUT} \approx \frac{1}{8 \times f_{OSC} \times C_{FLY}} + 0.5 \times \sum_{1}^{8} R_{ON}$$
(6)

Where $\frac{1}{1}$ is the summation of the switch resistances.

Summing the currents into I_{LOAD}, we arrive at:

$$I_{LOAD} = C_{OUT} \frac{dV_{OUT}}{dt} + C_{FLY} \frac{dV_{CFLY}(t)}{dt}$$
(7)

Where dt is equal to a quarter of the switch period (T/4, or 1/(4 × f_{OSC})). The output voltage ripple, ΔV_{OUT} , is dV_{OUT} and $V_{CFLY}(t)$ is the voltage difference across C_{FLY}. We can make the reasonable assumption that output voltage ripple is small relative to the flying capacitor voltage ripple. Then to calculate ΔV_{OUT} , we need an un-

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$$C_{FLY} \frac{dV_{CFLY}(t)}{dt} = \frac{V_{CFLY}(t) - |V_{OUT}|}{2 \times R_{ON}}$$
(8)

To solve this differential equation for V_{CFLY}(t), at least one initial condition must be known. This condition can be found via inspection of the timing graphs in Figure 5. Note that from t = 0 to t = T/4, both C_{FLY} capacitors contribute current to I_{LOAD} and charge C_{OUT}. Then, from t = T/4 to t = T/2, C_{FLY} and C_{OUT} contribute to the output load current. So, right at t = T/4 (and similarly t = 3/4 T), the contribution to I_{LOAD} from C_{OUT} is exactly 0. Therefore, at this moment, I_{LOAD} is equal to I_{FLY}, and the voltage of V_{CFLY} is given by:

$$V_{CFLY}(t = T/4) = |V_{OUT}| + I_{FLY} \times 2 \times R_{ON}$$
where $V_{OUT} = -V_{IN} + R_{OUT} \times I_{LOAD}$
(9)

Using Equation 8 and Equation 9, we can differentially solve for $V_{\mbox{CFLY}}(t)\!\!:$

$$V_{CFLY}(t) = |V_{OUT}| + |I_{LOAD}| \times (R_{OUT} - 2 \times R_{ON}) \times \beta^{1.5}$$
where $\beta = e^{1/8/RC}$
where f is f_{OSC} . R is R_{ON} , and C is C_{FLY}
(10)

To find the delta in V_{CFLY} for Equation 7, take two points (for example, t = 0 and t = T/4), and solve Equation 10 for each of those points. The result simplifies to:

$$\Delta V_{CFLY} = I_{LOAD} \times (R_{OUT} - 2 \times R_{ON}) \times \frac{\beta - 1}{\sqrt{\beta}}$$
(11)

Combining Equation 11 and Equation 7, and solving for ΔV_{OUT} gives:

$$\Delta V_{OUT} = \frac{I_{LOAD}}{4 \times f_{OSC} \times C_{OUT}} - I_{LOAD} \times (R_{OUT} - 2 \times R_{ON}) \times \frac{C_{FLY}}{C_{OUT}} \times \frac{\beta - 1}{\sqrt{\beta}}$$
(12)

The impact of Equation 12 may not be initially obvious. It may help to first simplify it by considering the case of an ideal switch ($R_{ON} = 0$ Ω). Doing so brings the second term to nearly zero, leaving only the first term. That first term is very similar to the standard inverting charge pump ripple (Equation 4), but the dual flying capacitors of the IICP increase the denominator by 2×. Twice the charge pumps yields half the ripple. This result is consistent with intuition.

However, the important part of Equation 12 lies in the second half. Note the minus sign for the second term, meaning that this portion reduces the output voltage ripple. Focus on the switch resistance (R_{ON}) and the flying capacitor (C_{FLY}). In a standard inverting charge pump, these terms play no role in reducing the output voltage ripple. But in an IICP, the switch resistance acts to smooth out the charge and discharge current. The dual flying capacitors allow this charge/discharge action to happen uninterrupted.

Output Voltage Ripple Confirmation

We can use circuit simulation to check the accuracy of Equation 12 and the validity of the assumptions used to derive it. This is easily accomplished using LTspice[®]. The schematic for this simulation is shown in Figure 7, and the file is available for download.

A comparison was performed for a variety of conditions, with a summary of the results in Table 2.

Table 2 shows that Equation 12 closely matches simulation, validating the assumptions made in simplifying the equations. Now we can use that equation to make trade-offs in the IICP implementation.

						V _{OUT} Ripple (mV)	
V _{IN} (V)	I _{LOAD} (mA)	f _{OSC} (kHz)	C _{OUT} (μF)	C _{FLY} (µF)	R _{ON} (Ω)	Equa- tion	LTspice
10	50	1000	4.7	2.2	2	0.038	0.038
5	100	1000	4.7	2.2	2	0.076	0.075
5	50	1000	1	1	2	0.393	0.390
5	50	1000	1	1	3	0.261	0.260
7.8	37	532	2.4	0.5	4	0.430	0.425
5	100	1000	10	2.2	3	0.024	0.024
5	50	200	4.7	1	10	0.418	0.415
12	50	500	10	1	10	0.031	0.033
12	20	500	4.7	1	3	0.089	0.089

Table 2: Comparison of Theoretical vs. LTspice Simulation Results for Various Configurations

It's also instructive to compare the voltage ripple between an IICP and a standard charge pump. In Part 2 of this series, we will show bench test data of these differences. But for now, our LTspice model in Figure 8 can illustrate the difference in output voltage ripple.



Figure 7: Interleaved inverting charge pump in LTspice.



Figure 8: Output voltage ripple of an IICP vs. a regular charge pump: $V_{IN} = 12 V$, $I_{LOAD} = 50 mA$, $C_{FLY} = 2.2 \mu F$, $C_{OUT} = 4.7 \mu F$, $R_{ON} = 3 \Omega$. To make the comparison fair to the regular charge pump, its R_{ON} was halved and C_{FLY} was doubled.

Optimization of IICP Topology

Having derived the IICP equations and proved their validity, there are two primary conclusions: For the IICP, the switch resistance (RON) reduces both input and output voltage ripple, a desired result. In contrast, in a standard inverting charge pump, the switch resistance is entirely undesirable, as it increases the R_{OUT} of the charge pump and provides no ripple voltage reduction. In fact, we could further augment the switch resistance by placing a resistor in series with the flyback capacitor. This gives us a knob to reduce

input and output voltage ripple at the expense of increased charge pump resistance. We'll explore this knob further when we discuss use cases of the IICP in Part 2 of this series.

Secondly, the value of the flying capacitors, and their ratio with COUT, can be optimized to further optimize the ripple. For example, a large output capacitor value may be difficult to find in a small package, and subject to a significant capacitance derating at higher voltages. But by reducing COUT, and then increasing CFLY,

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the same output voltage ripple can be obtained for more attainable values of capacitance. For example, instead of CFLY = 1 μ F and COUT = 10 μ F, if they were all set to 2.2 μ F, then nearly the same output voltage ripple is attained. 2.2 μ F/25 V capacitors are more readily available in small packages than 10 μ F/25 V capacitors. An example application in Part 2 explores this.

Conclusion

This concludes Part 1 of the 2-part series on the interleaved inverting charge pump topology. This part covers the general concepts behind an IICP topology, including input/output voltage ripple calculations. The derivation of the equations governing input/output ripple yields important insights into how to optimize the performance of an IICP solution.

In Part 2 of the series, we unveil the ADP5600, an integrated solution for the IICP topology. We measure its performance and compare to a standard inverting charge pump. Finally, we'll put it all together to power a low noise phased array beamforming solution.

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Acknowledgements

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Protecting the Health of the Battery: The Importance of Rugged Design and the BMS

With the growing rise in the use of batteries for a range of applications, it is crucial that the battery is designed in a manner that protects the safety of the user and the battery itself. Incorrect construction of the battery greatly increases the risk of damage to the internal battery cells which can have serious consequences.

By Jake Schmalz, Director of Engineering at Briggs & Stratton

When it comes to designing a battery there are two core elements (among many others) that need to be considered: the battery casing and the batteries internal structure. Getting these two elements correct reduces the chance of risk, protecting both the health and safety of the battery and its user.



Figure 1:

Internal structure of Vanguard's 5kWh Commercial Battery Pack

Designing the Battery Casing

The outer structure of a battery design is often an afterthought to the internal structure that generates the power output required. With a focus on generating power that can compete with petrol and mains-powered machinery, ensuring that the battery is stored in a secure casing is fundamental in allowing it to withstand the demanding conditions placed on machines.



Heavy duty machinery often experiences severe vibrations that can impact the user of the machine, something that is greatly improved by the introduction of battery power. Whilst there is often a significant reduction in sound pressure in decibels, there is also likely to be a reduction in harsh operation of the equipment. Because the demands of the machine are still the same, the battery needs to be designed to withstand these forces.

This starts with a heavy Aluminium base to absorb the pressure and to work alongside the internal structural supports to keep the battery cells in place during operation. Once the battery cells are secure it is imperative to protect the electrical componentry from impact and dust and water ingress by sealing the battery casing, all while allowing critical venting for the battery cells. The addition of heavy-duty busbars, connections and contactors support the matrix for the cells and allow the pack to be able to withstand the physical conditions while providing long-lasting, powerful performance.

Once they have been carefully designed, batteries must go through rigorous modelling and testing protocols, including impact and vibration, to ensure that the battery performs under the demanding conditions needed for use with various machinery. Briggs & Stratton's Power Application Centre has been carefully developed so its team of experienced Application Engineers can model, build, and test actual customer products to provide real-world development support and validation for equipment of all types.

Taking the approach of designing from the ground up in this manner allows Briggs & Stratton's Vanguard batteries to be used in commercial applications that have high vibration, impact, temperature shocks, and environmental exposure requirements.



Figure 3: Scanning the Individual Battery Cells



Focusing on the outside demands and the expected use of the battery is crucial to understanding the size of the casing needed and its structure to protect the internal cell structure. A poorly designed battery casing will greatly impact the health of the battery and its power capabilities.

The Internal Battery Structure

Within premium Lithium-ion batteries, the battery management system (BMS) plays a crucial role in protecting the health and safety of both the user and the battery itself, ultimately reducing risk. Attached to the battery within the battery casing, the BMS is constantly able to run diagnostics on the internal mechanisms of a battery. The data collated can be recorded and relayed to the user on different elements including temperature, charging speed, and charge status. Combined the statistics gathered by the BMS can ensure the safety of the battery for the user and protect the battery health.

The role of the BMS is fundamental beyond collecting data, it is essentially the brains that control all the functions of the battery. At its most basic, it evaluates the battery in relation to the equipment or charger; only allowing the flow of energy when properly connected and when environmental conditions and charge/discharge parameters are met. Combined with thermistors that constantly monitor individual cell and pack temperatures, the BMS logic works to prevent exceeding safe limits for charging or discharging the battery.



Figure 4: Building the Circuitry

The BMS "Power Map" governs all the rules and boundaries for safe, long-life battery operation. The Power Map works to optimize the charge and discharge rates based on ambient and pack temperature, state-of-charge (SoC) and state-of-health (SoH). This prevents the pack from operating in fringe areas where the Lithiumion battery life is most compromised.

Operating windows for Lithium-ion batteries have been greatly increased by the data that is collected by the BMS. It allows them to be used in temperatures as low as -20°C by carefully adjusting the discharge rate to counter for the extreme temperature. Ambient temperatures cause the chemical reactions that take place need to produce the desire power output to occur at a slower rate. A highly efficient and intelligent BMS will be able to compute the lower temperatures and carefully control the rate of discharge to avoid damaging the anode of the cell. Without an effective BMS, use at low temperatures can cause damage to the battery cells which can reduce their long-term battery life.

This too applies to charging in ambient temperatures. If the charging rate is not controlled, the battery can be damaged as lithium ions build up on the anode in a process known as lithium plating. An effective BMS works to slow the rate of charge in extreme temperatures to protect the internal cell to avoid impacting on the rate of performance. Whilst this can result in longer charge times for the user, the health of the battery is maintained allowing for its power capacity to remain constant regardless of the change in external conditions.

Overall, it is the BMS that is crucial to protecting the internal health of the battery as it is always in control. By constantly monitoring a multitude of criteria, the BMS keeps the battery operating in the most safe, efficient, and healthy mode protecting both the battery and the user.

In summary

To summarise, it is imperative to create a battery that is not just a bundle of cells formed together in an enclosure. Instead, batteries need to be engineered specifically to keep users productive and safe. Whilst many elements of Briggs & Stratton's Vanguard batteries are hidden from view, they play a crucial role in constantly monitoring a multitude of factors to keep the user safe and the battery healthy for long, reliable life.

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to meet PD specifications. The device incorporates cable-drop compensation with an internal voltage-feedback resistor divider, to ensure the load receives the correct voltage unaffected by losses in copper tracks and the attached output cable.

The STPD01 includes protection against over-voltage, over-current, and over-temperature. Additional built-in features include embedded discharge circuitry, soft-start, under-voltage lockout, and a programmable watchdog timer that help ensure a robust and safe system.

ST has also launched the STEVAL-2STPD01 USB Type-C[™] Power Delivery dual-port adapter kit, to accelerate development of solutions based on the STPD01. Created as an expansion card to be used with the NUCLEO-G071RB STM32 Nucleo-64 development board, the STEVAL-2STPD01 board contains two Type-C ports with two STPD01 programmable buck converters. Two TCPP02-M18 protection ICs for USB Type-C and PD Source applications are also on-board, and the associated software package, STSW-2STPD01, contains a sample application to run on the STM32G07 microcontroller.

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Silicon Power MOSFET for High Efficiency Power Conversion

SkyWater Technology and Applied Novel Devices announced a transistor technology that offers significant benefits for fast switching power conversion applications. The power MOSFETs offer 2x lower output charge, near-zero reverse-recovery and ultra-low Qoss enabled by AND's proprietary channel engineering technology. In addition, these power MOSFETs offer superior specific on-resistance (< 5 mOhm-mm2 @ 30V BVDSS) at gate drive as low as 2.5V as well as low leakage currents and near-ideal sub-threshold slope made possible by AND's device architecture. These characteristics can substantially reduce parasitic losses incurred in power management systems. This will improve power management and conversion efficiency in numerous applications including data centers, automotive, electric motor drives, microinverters for renewable energy systems and many others in industrial and consumer markets. In applications such as DC-DC power conversion, AND's technology offers unique advantages enabled by its novel device architecture. Near-zero reverse recovery and low output capacitances eliminate the need for integrated or standalone Schottky clamp diodes. These efficiency enhancing characteristics make the technology attractive for higher frequency voltage conversion applications not typically supported by conventional Si MOSFETs. The high frequencies enabled by these power MOSFETs, in turn, drive reduction of passive component sizes to achieve small form factor power modules that support further system level efficiency gains.



AND will offer wafer scale and standard package products ranging from 15-80V for industrial and consumer applications. AND plans to expand the offering to span the 200-1000V range with a family of products produced at SkyWater for electric vehicle, renewable energy and various industrial applications.

www.skywatertechnology.com

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ICs Feature Energy Measurement, Dimming and Relay Control

The SY7T501 and SY7T502 are Silergy's latest single-phase energy measurement ICs for cost-sensitive IoT applications such as smartplugs, dimmers, power-strips, intelligent lighting, and other points of load. The devices feature a line voltage zero-crossing comparator with dedicated state-machine. A relay control-block with user-programmable on/off delays for latching relays (single and dual coil) and non-latching types. The relay control-block includes relay's contact sensing, allowing timing adjustment to compensate for relay's delay variation due to wear and other conditions.

9777988 (90-4) 1 input (Single (indet) 1 input (Offerential) Line Voltage W Comparator with configurable Filters ad	5977592 (MSQP-18) 2 (Single (nded) 1 (Differential) Line Voltage
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Logic)	(HW Comparator with configurable Filters and Log- ic)
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Programmable ON & OFF Delays Latching (single-coil) and Non-Latching	Programmable ON & OFF Delays Relay Contact Feedback (Cosed Loop Control) Latching (Single/Dual-Coll) and Non-Latching Continuous relay status monitoring
Leading Edge and Trailing Edge Control	Leading Edge and Trailing Edge control
1 (multi-function, user programmable and configurable)	2 (multi-function, user programmable and configurable)
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The devices also include a dimming control block for trailing and leading-edge controls and configurable digital I/O's. A 32-bit signal processing unit with a delta-sigma converter, precision bandgap reference and analog front-end allow accurate energy measurement (Vrms, Irms, Power, Energy, Line Frequency etc.). The UART interface allows communication with the host processor, includes communication protocol with data integrity check and auto-baud function. The devices are available in SO8 and MSOP10 packages.



www.silergy.com

Standard Non-Hybrid Space-Grade Power Converters

Space system designers cannot easily support non-standard voltages or add functions with traditional hybrid-style power converters. Microchip Technology has eliminated the cost, complexity and customization challenges of these hybrid solutions by offering a discrete-component-based, space-grade DC-DC power converter family that now includes 28V-input, 50-watt (W) radiation-tolerant options.

"Our latest 28V-input SA50-28 products greatly simplify and accelerate system development," said Leon Gross, vice president of Microchip's discrete product business unit. "They are easier to customize than alternative space-grade power converters so they can meet specific voltage, current and other needs. Customers gain flexibility while reducing the size, cost and complexity of their space system designs."

Microchip's SA50-28 family is an off-the-shelf, 28V-input, radiation-tolerant power converter offering that is based on discrete components with surface-mount construction and non-hybrid assembly processes. Delivering more capabilities than alternative off-the-shelf, space-grade power converters, a single SA50-28 device with customized parameters eliminates the volume, weight and complexity problems of using hybrid solutions with their multiple devices and surrounding circuitry.



Microchip's comprehensive SA50-28 product line is a 20V- to 40Vinput, 50W family with nine standard outputs of 3.3V, 5V, 12V, 15V and 28V in single- and triple-output configurations. The devices can be tailored to a system's exacting power needs in a relatively short time with minimal additional costs as compared to hybridstyle power converter products. bodospower.com

High-Voltage Switcher ICs with 1700 V SiC MOSFET

Power Integrations announced the addition of two AEC-Q100 qualified, 1700-volt rated ICs to its InnoSwitch[™]3-AQ family. The devices are automotive-qualified switching power supply ICs to incorporate a silicon carbide (SiC) primary switching MOSFET. Delivering up to 70 watts of output power, the ICs are targeted for use in 600- and 800-volt battery and fuel-cell electric passenger vehicles, as well as electric buses, trucks and a wide range of industrial power applications.

Highly integrated InnoSwitch ICs reduce the number of components required to implement a power supply by as much as 50 percent, saving significant circuit-board space, enhancing system reliability and mitigating component sourcing challenges. Devices from the InnoSwitch family are now available with a choice of cost-effective silicon, high-efficiency gallium nitride (GaN) and high-voltage SiC transistors, permitting designers to optimize their power solution across a broad range of consumer, computer, communications, industrial and automotive applications.

Peter Vaughan, director of automotive business development at Power Integrations, said: "800-volt batteries are becoming standard for EVs. Multiple vehicle systems are connected to this powerful electrical source, yet delicate electronic control circuits



require just a few volts for operation and communication. Inno-Switch devices allow the electronics to safely sip from the firehose of energy available on the main bus, using minimal board area and without wasting energy. Most exciting is the opportunity to dramatically simplify the emergency power supply for the main traction inverter, which may be called upon at a moment's notice to operate from any voltage between 30 volts and 1000 volts. Our SiC-based InnoSwitch3-AQ devices handle this vast range with incredible ease."

www.power.com

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Current Sensor in a Laboratory Device

The engineering office Jochen + Georg Frank in Stuttgart was commissioned by a manufacturer of laboratory equipment to develop an electronic control unit for a laboratory device for experiments



with chemical substances. The project involves a boiler, in which a temperature profile with narrow tolerances must be run over time. It is heated by a grid fed heating element, which is activated via a computer output. Since the computer is powered independently of the heating system, they need to ensure that the heating output is actually present. Any unintentional tripping of the heating circuit fuse or significant deviation from the nominal heating current must be detected as guickly as possible. Furthermore, the correct switching of the high-power relay must be monitored.

Angst + Pfister Sensors and Power (APSP) offered the best solution with a potential-isolating AC current sensor. The simple wiring is a major plus. A fully insulated conductor of the mains-fed heating cable is threaded through the current sensor. The current detection electronics in the control module normalize the sensor signal. Heating current 0...25A (ACeff) corresponds to 0...2.5Vdc at an analog input of the control unit. It was possible to implement the project in a linear and timely manner thanks to the technical expertise and project-related support from APSP, including the delivery of corresponding sample sensors. The equipment manufacturer is pleased to have a simple, inexpensive and robust solution.

https://sensorsandpower.angst-pfister.com

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