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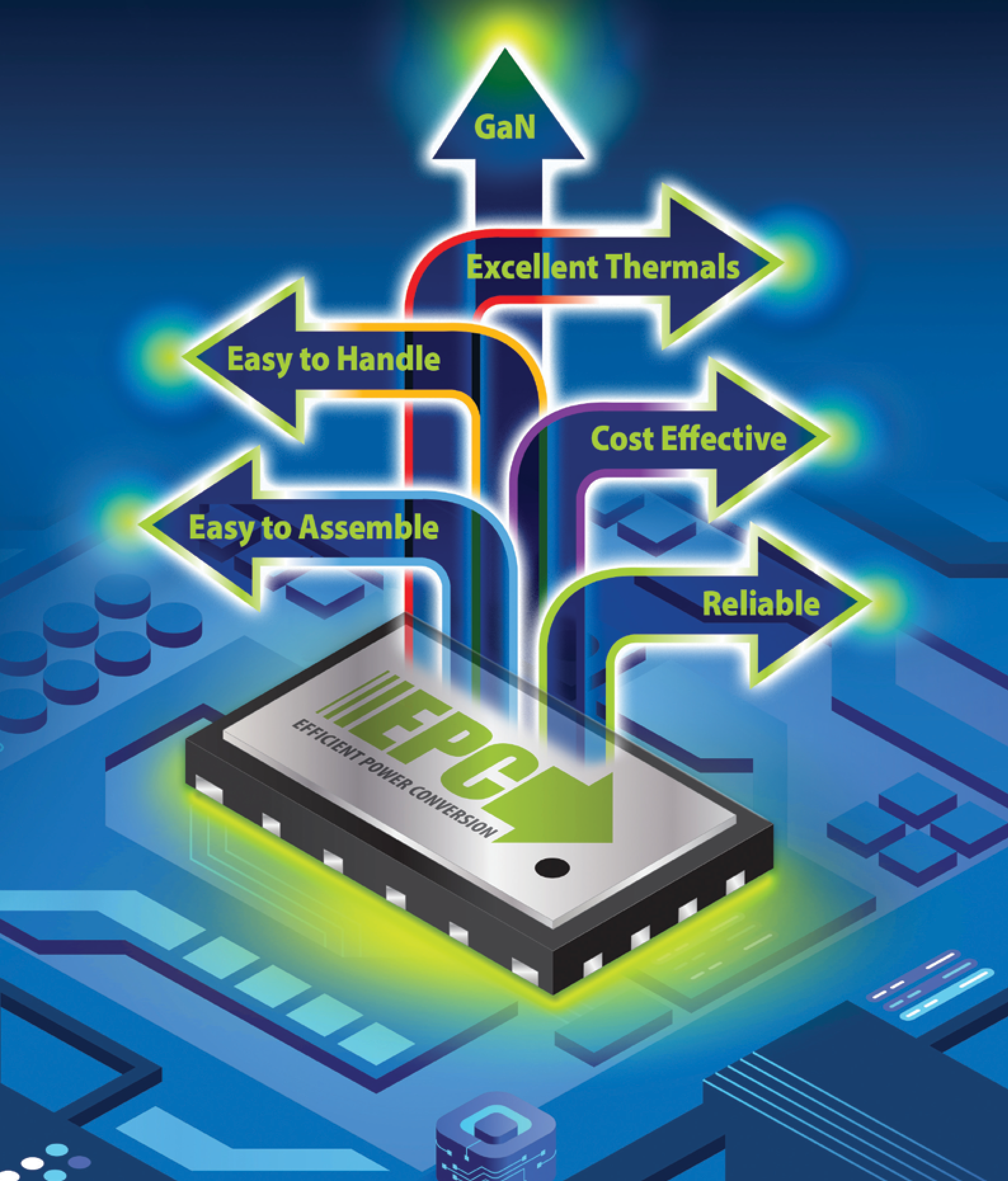
Bodo´s Power Systems®

Electronics in Motion and Conversion

March 2023



PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the

- **Incremental inductance** $L_{inc}(i)$ and $L_{inc}(\int U dt)$
- **Secant inductance** $L_{sec}(i)$ and $L_{sec}(\int U dt)$
- **Flux linkage** $\psi(i)$
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** B(i)
- **DC resistance**

Also suitable for 3-phase inductors

WIDE RANGE OF MODELS

7 models available with maximum test current from 100A to 10000A and maximum pulse energy from 1350J to 15000J

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

APPLICATIONS

Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**

- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

Technological leader in pulsed inductance measurement for 18 years

www.ed-k.de

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Let's Meet in Orlando!

March is here and traditionally the time for the APEC trade show. Bodo and I considered the pros and cons for a very long time, before finally deciding that I would make the trip to Florida this month to attend the event. It's still a little strange imagining being on a plane for so long, especially now that all the restrictions are lifted. But then again, I've traveled a few times now, I'm fully vaccinated and no one can stop me from wearing a mask if I feel uncomfortable. Maybe some will look irritated, who knows! But, let's face it, for me, as for most Europeans, it is still exciting traveling to the US. Having visited PCIM Europe and Electronica last year, I am eager to discover what is trending at the Orlando show. Sure, the technical approaches will be similar and the products exhibitors showing will often be the same, but it's the feeling you get when walking in the aisles and talking to other visitors, who are always both professionals on one side, but also normal consumers on the other. It's hard to describe, but somehow applications and technical approaches are perceived differently, and people expect something else from their equipment on the various continents. Often you talk about other topics and hear different stories abroad, and that's one of the advantages of working internationally. What can I say, I'm really looking forward to meeting our US customers and friends again in person, many who haven't made it to Europe during the past three years. And of course, I am also looking forward to meeting lots of new people.

During the next few months, we are planning our next episode of "Bodo's WBG Expert Talk" on April 12th. This will be the 9th edition already. If you are wondering what to expect, you can find all previous episodes on our website: www.bodospower.com/wbg.aspx. I may also take a short trip to the Hannover Messe. I've never visited this event before, but I understand that it is a very interesting trade show. And since Hannover is just around the corner, compared to Orlando, the time away from my desk will be shorter.

My Green Power Tip for the Month:
It is now common for suppliers such as airlines or even trade fairs to offer the option of an ecological upgrade, e.g. electricity from renewable sources for your stand or a CO2 bonus for your flight. Opt for this whenever you can!

Kindest regards,

Holger Moscheik

Events

embedded world 2023
Nuremberg, Germany March 14 – 16
www.embedded-world.de

APEC 2023
Orlando, FL, USA March 19 – 23
www.apec-conf.org

AMPER 2023
Brno, Czech Republic March 21 – 23
www.amper.cz

Smart Systems Integration 2023
Bruges, Belgium March 28 – 30
https://smartsystemsintegration.com

emv 2023
Stuttgart, Germany March 28 – 30
https://emv.mesago.com

electronica China 2023
Shanghai, China April 13 – 15
www.electronica-china.com

PE International 2023
Brussels, Belgium April 18 – 19
www.pe-international.net

FORTRONIC Power 2023
Bologna, Italy April 19 – 20
https://fortronic.it

Battery Tech Expo 2023
Silverstone, UK April 20
www.batterytechexpo.co.uk

Silicon Carbide Device Manufacturing Facility in Saarland, Germany

Wolfspeed announced plans to build a 200mm wafer fabrication facility in Saarland, Germany. The company's first fab in Europe will be its most advanced, creating a development and production facility in the European Union to support growing demand for a wide variety of automotive, industrial and energy applications. The European fab announcement is an important part of the company's broader $6.5 billion capacity expansion effort, which includes opening of the company's 200mm Mohawk Valley device fab in April 2022, and the construction of The John Palmour Manufacturing Center for Silicon Carbide, a 445-acre (180 hectare) Silicon Carbide materials facility in North Carolina, which will expand the company's existing materials capacity by more than 10x. "This new fab represents a big step forward for both Wolfspeed and our regional customers, as we enhance the ecosystem for semiconductor production and innovation," said Gregg Lowe, President and CEO of Wolfspeed. "Silicon Carbide devices offer greater energy efficiency and are essential in the global shift toward sustainable electrification. This new facility will be crucial to supporting our expansion in a capacity constrained industry that is growing very rapidly, especially across the EV marketplace. It was important for us to have a facility located in the heart of Europe, near many of our customers and partners, to foster collaboration on the next generation of Silicon Carbide technologies."

The announcement was made at an event on the 35-acre (14-hectare) site of the planned fab, a former coal-fired power plant in Saarland, Germany.

www.wolfspeed.com

Aly Mashaly Appointed Director Application and Technical Solution Center in Europe

As of January 1st, Aly Mashaly has succeeded Günter Richard as Director of ROHM's European Application and Technical Solution Center (ATSC). Günter Richard has retired after 32 years working for ROHM.

Before having joined ROHM in 2015, Aly Mashaly has gained more than 20 years of experience in the electronics industry. He is an expert in power electronics, especially in the field of automotive applications. Also, he has worked as a development engineer and project manager in the fields of e-mobility and aerospace applications for several years.

Mashaly is also a regular speaker at various conferences, including PCIM, ECPE, EPE and CS International. He holds degrees from the Ain Shams University Cairo and Leibniz University Hanover where he has studied electrical engineering.

For his new role at ROHM, he has set himself ambitious goals: "With our highly skilled team, technical services and high quality products we strive for excellence to be a competent partner to our customers. On top, we want to be a supplier and partner for innovative solutions to help our society to overcome some pressing challenges of our time," states Mashaly. "I would also like to express my gratitude to my predecessor Günter Richard who has established the Application and Technical Solution Center back in 2019 and who has made the transition very easy to me," adds Mashaly.

Aly Mashaly is now directly reporting to Wolfram Harnack, President of ROHM Semiconductor Europe: "Based on his huge amount of proven technical experience as well as his demonstrated leadership skills and commitment towards ROHM, I'm convinced that Mr. Mashaly will bring the ATSC and the technical customer service involved to the next level," concludes Wolfram Harnack.

www.rohm.com

PCIM Asia Conference 2023 Call for Papers now Open

As part of PCIM Asia, held from 29 – 31 August 2023 at the Shanghai International Expo Center, the conference is inviting interested individuals to submit abstracts to be incorporated into the conference proceedings and published in scientific databases. The call for papers closes on 15 March 2023.

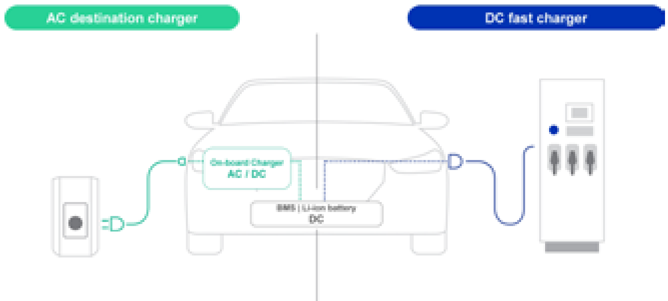
The submissions will be reviewed by the PCIM Asia Advisory Board, and upon their acceptance will be considered for a 20-minute talk or poster session. Successful submissions will also be included in the PCIM Asia conference proceedings, as well as in the Ei Comendex, IEEExplore, IET Inspec-Direct and Scopus scientific databases.

As always, there will be three awards honouring the most outstanding achievements and contributions of researchers, with all winners receiving an attractive prize. Awards include "The Best Paper Award" for the best overall submission, "The Young Engineer Award", which recognises an engineer under the age of 35 for an outstanding paper and "The University Scientist Award" for universities best promoting the development of the power electronics industry.

www.pcimasia-expo.com

Solution Enables Accurate Billing for Electric Vehicle Charging

A major step forward in supporting the deployment of fast electric vehicle (EV) chargers in North America, the bi-directional DCBM will enable makers of electric vehicle charging stations (EVCSs) to accelerate their certification for DC metering requirements following Certified Test and Evaluation Professional/National Type Evaluation Program (CTEP/NTEP) certification. The DCBM will simplify the process of the manufacturers having to qualify their own charging stations for UL listed certification and, for extra peace of mind, will undergo a fresh audit every quarter.



Capable of monitoring current, voltage, temperature and energy, the meter has been designed with data security, e-mobility, digitization and flexibility in mind and is a UL recognized component for the United States and Canada. The DCBM 400/600 complies with the standards UL 61010 and UL 810 with its certification in the FTRZ category for EV applications. To achieve this certification, the meter had to pass reinforced insulation tests, temperature testing of all its components and sub-assemblies, testing for protection against electric chock, durability of markings tests, equipment temperature limit tests and resistance to heat/fire risk tests. Says Claude Champion, General Manager at LEM USA Inc.: "The US and Canadian markets for EVs are continually expanding but this growth could be held back by insufficient access to rapid DC charging stations. LEM understands exactly what the sector needs and has worked closely with EVCS manufacturers and installers when developing solutions like the DCBM 400/600. We are ready to help make a zero-carbon future possible for North America."

www.lem.com

Accelerating Solar Adoption with Silicon Carbide MOSFETs

Navitas and KATEK GROUP announce that KATEK's coolcept fleX family of Steca solar inverters have adopted GeneSiC power semiconductors for improved efficiency, size, weight and cost, with significant market size expansion. GeneSiC 'trench-assisted planar-gate' SiC MOSFET technology delivers high-temperature, high-speed performance, resulting in up to 25°C lower case temperature, and up to 3x longer life than alternative SiC products. With the highest-published 100%-tested avalanche capability, 30% longer short-circuit withstand time, and stable threshold voltage for easy paralleling, GeneSiC MOEFTs are ideal for high-power, fast-time-to-market applications.

Steca – A KATEK Brand – develops and produces power electronics for grid inverters and energy storage as well as control technology for photovoltaic systems and fuel cell systems. The Steca coolcept fleX model solar inverter converts DC power from a string of solar panels into 4.6 kW AC power for use in the home, returning to the grid, or being stored locally for later use – to smooth demand and/or support power during an outage.

Each 4.6 kW Steca coolcept flex inverter uses 16x SiC MOSFETs. These devices are used in a two-level converter, with bi-directional boost converters and an H4-topology for AC voltage output. Increased switching frequency shrinks the size and weight of 'passive' components, which optimizes the KATEK unit in size and weight compared to legacy silicon-based inverters.

www.navitassemi.com

Addition of GaN Technology Strengthens Distributors Range of Power Technologies

Anglia Components PLC has expanded its portfolio of power solutions following the signing of a distribution agreement for the UK and Ireland with EPC (Efficient Power Conversion).

Anglia offers its customers a full portfolio of the mainstream power technologies, including Silicon MOSFET and Silicon Carbide, and GaN, allowing them to select the solution that is most appropriate to their design from a size, efficiency, and cost perspective. The addition of EPC enhancement mode gallium nitride (eGaN) FETs and ICs strengthens Anglia's range particularly in the low voltage (sub-400V) end of the market. In many applications, EPC eGaN devices deliver lower system cost, higher performance and greater power density.

John Bowman, Marketing Director of Anglia, explained, "Power is attracting considerable focus from our customers at the moment. Their concern is driven both by environmental and economic considerations. EPC impressed us as a company that is pro-active in its approach to the market, anticipating customers questions about adopting this technology and helping them on the design journey to a smaller, more efficient system design. Our FAE team is benefitting from this approach as they undergo comprehensive and in-depth training on the range."

www.anglia.com
www.epc-co.com

Chae Lee Appointed Chief Executive Officer

Tagore Technology announced the appointment of Chae Lee as Chief Executive Officer. Chae Lee brings more than 35 years of experience to Tagore Technology. Prior to joining Tagore, Mr. Lee was President and CEO of Insyte Systems. Before that, Mr. Lee was Senior Vice President and General Manager of NXP's Secure Interface and Power Solutions Business Unit where he grew the business unit's revenue to $1B. Prior to NXP, Mr. Lee spent 16 years at Maxim Integrated Products where he developed multiple new product lines at Maxim and as Senior Vice President and General Manager of the Mobility Group, grew its revenue from $350M to $1B. Mr. Lee graduated from the University of Missouri-Rolla with a Bachelor of Science degree in Electrical Engineering.

"I am pleased to welcome Chae to Tagore," said Oleg Khaykin, Tagore Technology's Chairman.

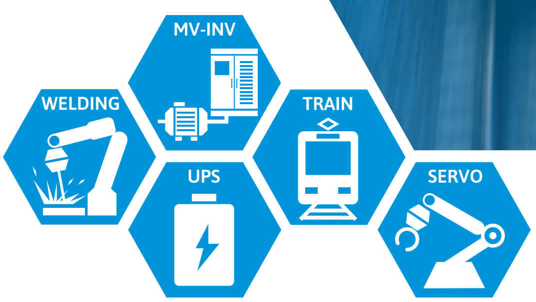
"Chae is an accomplished technology leader with an impressive track record." Mr. Khaykin added, "The Board feels Chae is an excellent choice to leverage our recent progress and lead the company to achieve our aggressive growth strategy and expanded profitability." CEO and co-founder of Tagore Technology, Amitava Das added: "As co-founders of Tagore, Manish Shah and I are delighted to welcome Chae to the Tagore family as we take the company to the next level in its growth trajectory."

www.tagoretech.com

Vertical GaN Sample Shipments to Customers

Odyssey Semiconductor announces product sample fabrication is complete with shipments to customers commencing in Q1 2023. "Our backlog of customers has been eagerly waiting for these vertical GaN product samples. I'm proud to report that fabrication was completed as planned in Q4 2022 and now the samples are being prepared for shipment to customers later this quarter," said Mark Davidson, Odyssey's Chief Executive Officer. "We will work closely with these initial customers to gain valuable feedback on their product features. We expect to secure product development agreements with customers by the end of Q2 2023." Odyssey's approach to vertical GaN will offer even greater commercial advantages over silicon than silicon carbide or lateral GaN. Vertical GaN offers a 10x advantage over silicon carbide (SiC) at performance and cost levels unattainable by the competing technologies. The market the Company is pursuing is large and fast growing. The 650 volt segment is the larger market today, expected to grow at a 20% compound annual growth rate. The 1200 volt product market segment is expected to grow faster at 63% CAGR and will become the larger market in the second half of this decade. Together, the 650 and 1200 volt power device market is expected to exceed $5 billion in 2027, a 40% combined CAGR according to Yole Group, a French market research firm.

www.odysseysemi.com

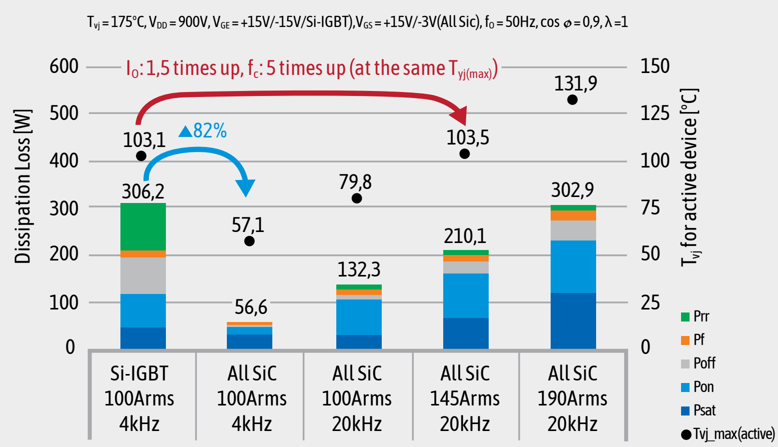


All-SiC Trench gate MOSFET – 2nd Generation

MAIN FEATURES

- Significantly lower loss operation and higher power density
- New internal design accomplishes very low inductance package
- Enables much higher switching frequency compared to Si-IGBT
- Fully compatible package to conventional Si-IGBT module

Comparison of All-SiC 300A/1700V with Si-IGBT



www.fujielectric-europe.com
www.americas.fujielectric.com/semiconductors

Fuji Electric
Innovating Energy Technology

Provider of Charging Solutions for EVs Expands Porsche's Investment Portfolio

Porsche has invested a double-digit million euro amount in ABB E-mobility, Baden, Switzerland, in a private placement. Lutz Meschke, member of the board of management responsible for investment management at Porsche SE: "With the fast growth that we are seeing in electromobility, the need for the expansion of the corresponding charging infrastructure is increasing. We expect that the demand for chargers will continue to increase rapidly in the years to come. As a leading provider of charging solutions for electric vehicles, ABB E-mobility will participate significantly in this market growth."

ABB entered the e-mobility market in 2010, and today has sold more than one million electric vehicle chargers across more than 85 markets. With over 50,000 DC fast chargers sold, the company has the largest installed base of fast chargers in the market. In addition to electric vehicles chargers, ABB E-mobility's product portfolio also comprises services in the area of life-cycle management as well as software solutions for the planning and operation of electric vehicle fleets. The total volume of the private placement that has now been completed amounts to approximately 525 million Swiss francs. The proceeds will be used to further accelerate the rapid organic growth of the company as well as for acquisitions.

www.porsche-se.com

Haviv Ilan to Become Next President and CEO

Texas Instruments announced that Haviv Ilan will become the next president and chief executive officer (CEO) of Texas Instruments, effective April 1. A 24-year veteran of TI, Haviv succeeds the current president and CEO, Rich Templeton, who will remain chairman of the board. The transition is a well-planned succession that follows Haviv's promotion to senior vice president in 2014, executive vice president and chief operating officer in 2020, and election to the board of directors in 2021. Haviv has served in a variety of senior management roles at TI, including leading businesses in both analog and embedded processing. He joined TI in 1999 through the acquisition of Butterfly, a wireless start-up company in Israel. Haviv earned bachelor's and master's degrees in electrical engineering from Tel Aviv University. He also earned a Master of Business Administration from the Joint International Executive MBA Program at Northwestern University's Kellogg School of Management and Tel Aviv University's Leon Recanati Graduate School of Business Administration.

"I am honored to lead TI during this amazing time for our company and our industry," said Haviv. "The combination of our broad portfolio of products, strong foundation of manufacturing and technology, reach of market channels and diverse and long-lived positions all put TI in a unique class of companies. Our ambitions and values will continue to be integral to how we build TI stronger and when we are successful, our employees, customers, communities and shareholders all benefit."

www.ti.com

Multi-Year Agreement for Delivery of Silicon Carbide Materials

Infineon is extending its cooperation with silicon carbide (SiC) suppliers. The German-based semiconductor manufacturer has signed a multi-year-supply and cooperation agreement with Resonac Corporation (formerly Showa Denko K.K.), complementing and expanding the announcement of 2021. The set of contracts will deepen the long-term partnership on SiC material. According to the agreement, Resonac will supply Infineon with SiC materials for the production of SiC semiconductors, covering a double-digit share of the forecasted demand for the next decade. While the initial phase focuses on 6" SiC material supply, Resonac will also support Infineon's transition to 8" wafer-diameter during the later years of the agreement. As part of the cooperation, Infineon will provide Resonac with intellectual property relating to SiC material technologies. The Infineon - Resonac partnership contributes to supply chain stability and will support the rapid growth of the emerging semiconductor material SiC. "The business opportunities in the area of renewable energy generation and storage, electromobility and infrastructure are enormous for the years to come. Infineon is doubling down on its investments into SiC technology and product portfolio, to proliferate the most comprehensive product offering to its customers. We are very happy that our partnership with Resonac will strongly support our market-leading position," said Peter Wawer, President of Infineon's Industrial Power Control division.

www.infineon.com

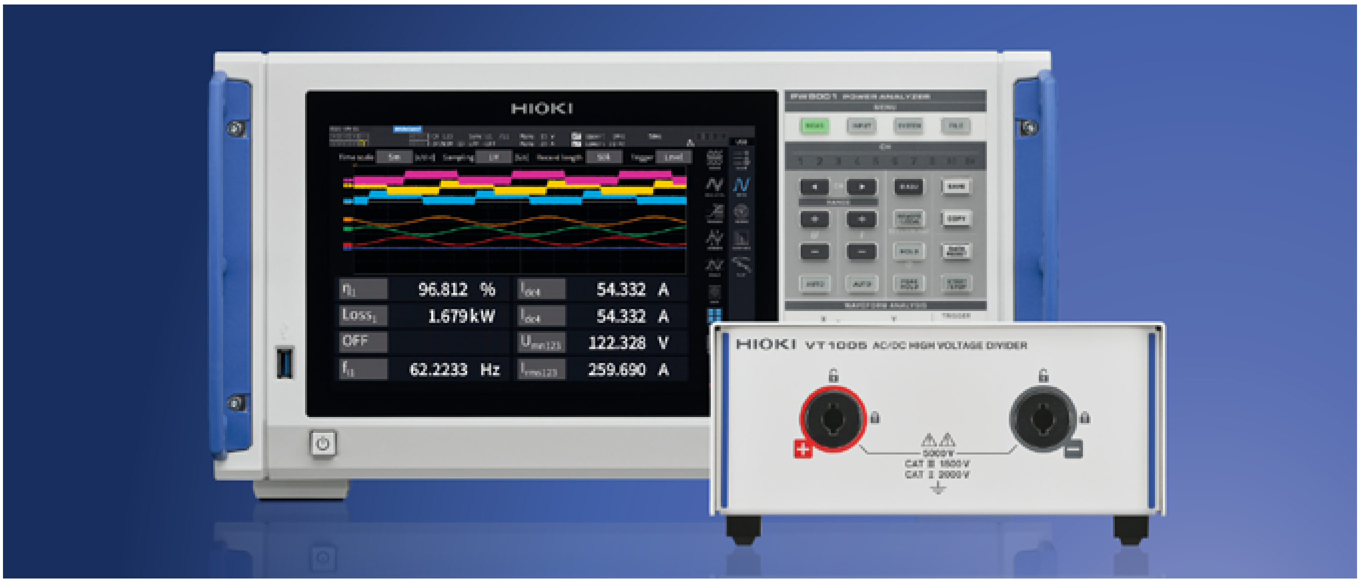
Elif Balkas Appointed Chief Technology Officer

Wolfspeed announced the promotion of Elif Balkas to Chief Technology Officer, succeeding the late Dr. John Palmour, a co-founder of Wolfspeed. In her role as Vice President of Research and Development in Wolfspeed's Materials organization, Balkas shaped the company's technical strategy on wide bandgap materials and drove its development execution to maintain Wolfspeed's position as a leader in Silicon Carbide for Power and RF device applications. She has overseen multiple significant technology milestones during her tenure at the company, including the development of 150mm and 200mm boule growth systems and processes, the dramatic reduction in crystal defect levels that saw higher device yields, and advancements in wafer processing. "I'm excited to continue building upon the legacy that John created and unlock new innovations and applications for Silicon Carbide," said Balkas. "It's an exciting time of growth at Wolfspeed and I look forward to the new challenge of finding greater efficiencies as we continue to expand the reach of our technology." Balkas brings more than 20 years of experience in the technology industry. Prior to Wolfspeed, she served in a variety of leadership positions in R&D and operations, focusing on developing Silicon Carbide crystal growth and GaN technologies that are scalable for manufacturing purposes and that enable more efficient and powerful electronic systems.

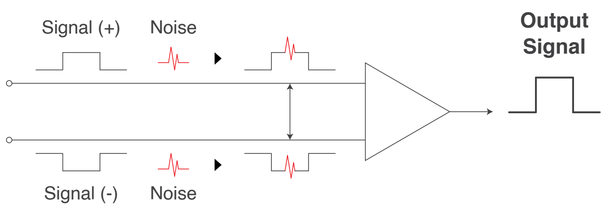
www.wolfspeed.com

Accurate High Voltage Power Measurement

The High Voltage Divider VT1005 is an important addition to the HIOKI power measurement solutions. The VT1005 in combination with one of the HIOKI Power Analyzers enables to accurately measure power up to 5 kV. This means a huge improvement in accuracy especially for high frequency applications such as SiC based solutions or loss measurement of HV coils and transformers.



With the ongoing electrification of our society there is a rapidly growing need for more electrical power. One of the ways to meet this demand is to increase the system voltage. Obvious applications are ultra-high-speed chargers for EV's and solid-state transformers that help to increase the flexibility and reduce the losses of the power grid. For the development of these high voltage systems accurate power measurement is essential. A high accuracy power analyzer like the HIOKI PW8001 can measure power up to a voltage of 1500 V. In combination with the VT1005 High Voltage Divider you have the solution for accurate voltage and power measurements from 1500 V up to 5 kVrms. To guarantee such accurate power measurement results, a HV divider needs to have two main features: high noise resistivity and excellent frequency flatness.



High Noise Resistivity

The VT1005 is highly resistant to both high-frequency noise and common-mode noise (see Figure 1), allowing it to measure voltage accurately even in noisy environments. Since conversion devices like inverters are sources of noise, this level of noise resistance is important to ensure accurate efficiency evaluation.

SiC power devices are characterized by a fast voltage response, and their output waveforms contain numerous high-frequency components. If you check the output voltage of SiC power devices, the VT1005 shows no ringing effect and ensures accurate power measurement.

Frequency Flatness

Frequency flatness defines the gain and phase error of a power measurement system over a defined frequency range. As the VT1005 High Voltage Divider and the current sensors are developed and produced by HIOKI, these devices are optimized for the HIOKI power analyzers and offer outstanding performance both in gain and phase accuracy over the entire frequency measurement band.

To further increase the efficiency of high power systems, SiC semiconductors have become popular switching devices. As the switching frequency of these semiconductors is 50 kHz or higher, power needs to be measured accurately over a broad frequency spectrum, from DC to several hundred kHz. This can be a challenge because not only voltage and current need to be measured accurately at high frequencies, but the phase angle as well. HIOKI power measurement systems, including HV Dividers and Current Sensors, offer an excellent frequency flatness that ensure accurate measurements. To guarantee this at higher voltages, the VT1005 delivers a gain error of just ±0.1% up to 200 kHz, and a phase error of just ±0.1° up to 500 kHz. (after phase correction by the power analyzer)

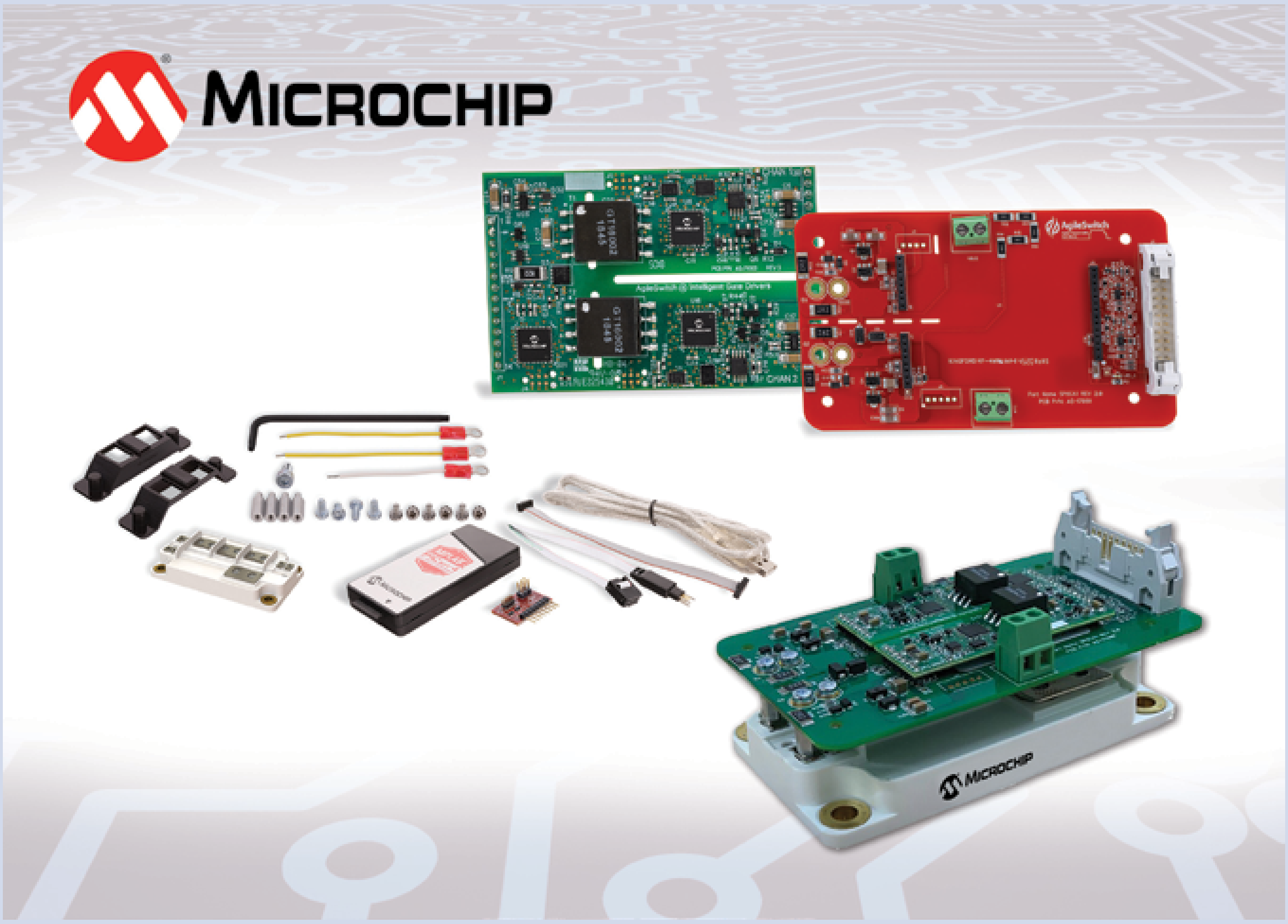
Loss Measurement of HF reactors and transformers

HIOKI provides a solution to measure loss of high voltage HF reactors and transformers used in inverter drives and solid-state transformers. Both the noise resistivity and the frequency flatness make the combination of the VT1005 High Voltage Divider, PW8001 Power Analyzer and the CT6904A Current Sensor ideal for these applications. With this setup accurate loss measurements can be guaranteed even at a frequency of 300 kHz.

www.hioki.eu

Win an Accelerated Silicon Carbide (SiC) Development Kit

Win a Microchip Accelerated Silicon Carbide (SiC) Development Kit (ASDAK-MSCSM70AM025CT6LIAG-01-DK) and accelerate your power system development and performance.



Microchip's Accelerated Silicon Carbide Development Kits can reduce power system development times by up to six months and include the hardware and software elements required to rapidly optimize the performance of Silicon Carbide power modules and systems. Helping you adopt SiC with ease, speed and confidence.

This kit incorporates configurable multi-level, digital gate drive control (Augmented Switching™) to optimize the performance of your SiC power modules and systems. Rapidly configure and adjust system performance through software settings using the AgileSwitch® Intelligent Configuration Tool (ICT). Small changes to the Augmented Switching profiles can yield dramatic improvements in switching efficiency, overshoot, ringing and short-circuit protection. No soldering is required.

The Accelerated SiC Development Kit includes:

- 1× MSCSM70AM025CT6LIAG – 700V SiC Power Module
- 1× AgileSwitch 2ASC-12A1HP – 1200V Configurable Digital Gate Driver Core
- 1× SP6CA1 – 1200V SP6LI Module Adapter Board
- 1 x PICKit™ 4 Programming Kit
- Intelligent Configuration Tool (ICT)
- Mounting Hardware
- Cabling

For your chance to win an Accelerated Silicon Carbide (SiC) Development Kit visit https://page.microchip.com/Bodo-SiC.html and enter your details in the online entry form.

www.microchip.com

Power Packaging for the GaN Generation of Power Conversion

Since the launch of GaN-on-Si enhancement mode power transistors in March 2010 there has been a slow but monotonic shift towards adoption and replacement of silicon-based power MOSFETs. Initial adoption came from risk-taker visionaries in applications such as lidar, high-end audio amplifiers, robots, vehicle headlamps, and high-performance DC-DC converters.

By Alex Lidow, Michael de Rooij, and Sam Sundaram, Efficient Power Conversion (EPC)

These were companies that had much to gain from the performance of these new-technology devices. EPC was the first company to go into mass production with our eGaN® FETs, all of which were in a controversial wafer level chip scale (WLCS) format such as in figure 1.

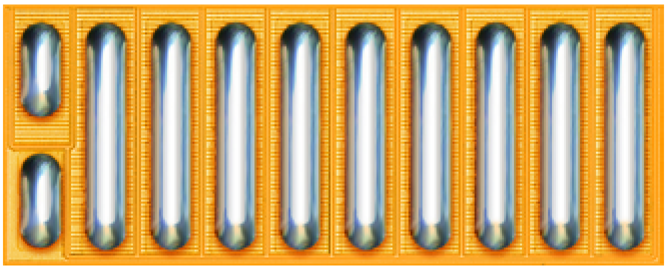


Figure 1: The 7 mm2 WLCS EPC1001 was among the first GaN-on-Si products introduced in March 2010 by EPC.

The reasoning behind the elimination of the packaging was that GaN devices were initially targeted at the highest performance requirements from early-adopter companies. These companies were primarily looking for speed and size reductions. Traditional power semiconductor packages had significant internal inductance and added a lot of size to a final design in addition to the actual GaN chip.

Over the next several years the applications and volume expanded by factors of hundreds and then thousands. The customer base for WLCS eGaN devices, which started to include integrated circuits in 2014, rose to over 1,000 active users in over 60 countries. Adoption rates, however varied depending upon the manufacturing capabilities of the companies purchasing the products. In some circumstances, particularly in lower volume applications, the small pitch between terminals as well as the brittle nature of the WLCS caused unwanted design iterations and increased manufacturing cost. For the expansion of GaN for power conversion to get beyond the early adopters, a more user-friendly format needed to be developed. This format, however, needed to preserve the key attributes of small size, low RDS(on), high speed, excellent thermal conductivity, and low cost. In other words, the best package would be the least amount of package technically possible.

Enter the PQFN

The Power Quad Flat No-Lead (PQFN) package was the logical starting point. EPC's PQFN design encases the GaN device with a minimum amount of epoxy along the sides of the device to protect against chipping during handling but leaves an exposed substrate that can be used as a thermal pad on the upper surface as shown in figure 2. This upper surface is designated "case" and is connected to source potential for discrete devices. For power stage integrated circuits it is tied to the source of the low-side FET. The opposite side of the device contacts with the printed circuit board (PCB) in the same manner as for WLCS devices and is designated "board".

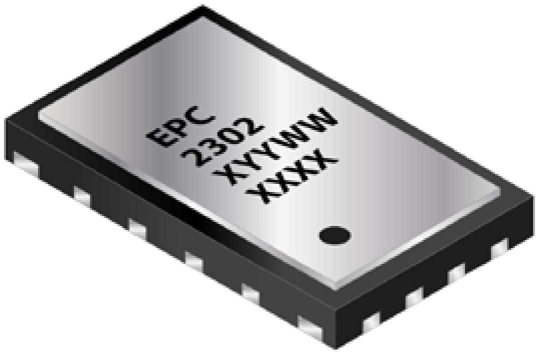


Figure 2: eGaN FET in a PQFN package.

Figure 3 shows a cross section comparison between the WLCS and PQFN devices and highlights some key differences and similarities together with the thermal paths from junction to board and case.

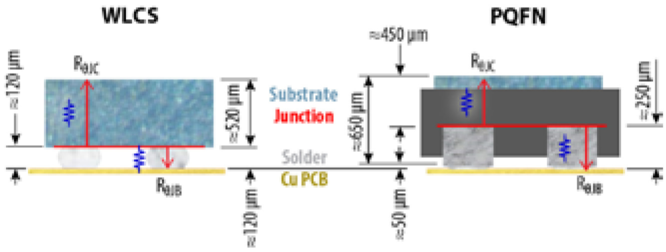


Figure 3: Cross-sectional view comparison between the WLCS and PQFN eGaN FETs with junction to board and case thermal resistances highlighted.

At its best, the size adder from this packaging approach is about 20%. For the largest GaN device in a 3mm x 5 mm the PQFN increases the outside dimension from 12.5 mm^2 to 15 mm^2. There is no significant increase in package inductance or resistance compared with a WLCS device and therefore there is no measurable impact on conduction losses, switching speed, or EMI-generating ringing.

Thermal performance is also quite comparable to WLCS devices. A comparison between the thermal resistances of eGaN FETs and Si MOSFET in various packages can be made with junction-to-board ($R_{\Theta JB}$) shown in figure 4 and junction-to-case ($R_{\theta JC}$) shown in figure 5. The metric used for the device areas is the outer dimensions of the packaged part.

Figure 4 shows that the PQFN packaged eGaN FET has higher thermal resistance of junction-to-board compared to WLCS devices, but the difference is small due to the high thermal conductivity of the materials in this path and larger device area. The overall area for eGaN FETs, however, is smaller than packaged MOSFET devices and the best method to overcome this is by PCB design that effectively increases the heat-spreading area of the GaN FETs [2,3,4]. All PCB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layout and thermal techniques applicable to WLCS devices remain applicable to PQFN devices too. Thus, when all the devices, eGaN FETs and Si MOSFETs, are compared on a PCB level from junction to ambient, the thermal differences become negligible [3]. When relying on PCB only cooling, the key converter performance improvements are driven by eGaN FETs superior electrical characteristics over that of Si MOSFETs [5].

Figure 5 shows that the PQFN packaged devices have *lower* thermal resistance of junction-to-case compared to WLCS devices due mainly to the thinner substrate that improves the ability to cool the devices when using a heatsink [1,4,5,6]. The difference in comparison with Si MOSFETS becomes even greater, including dual sided cooling packages such as Super SO8 Dual Cool [7].

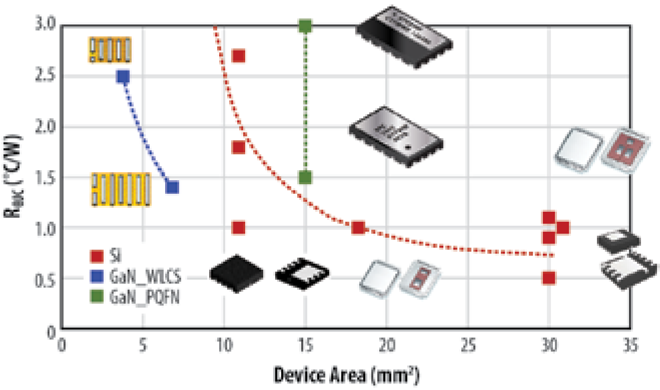

Figure 4: Junction to board thermal resistance comparison of various devices and packages.

Additional PQFN Advantages

One of the key reasons GaN power devices are so small is the lateral conduction of electrons through a two-dimensional electron gas (2DEG) [5]. This lateral conduction mechanism results in a significant contribution to the final device $R_{DS(on)}$ coming from metal layers deposited during wafer processing. The farther apart the WLCS bumps or bars, the higher the $R_{DS(on)}$ of the final device. This is the basic reason for the tight pitch found on WLCS devices. With the addition of a copper leadframe in the PQFN package, the spacing between the terminals can be expanded to meet IPC-2221A [3] creepage and clearance requirements without sacrificing device conductivity. In addition, by extending the leadframe to the edge of the device the flanks become solderable, leading to improved thermal cycling capabilities and easier manufacturing process controls that visually inspect for thorough solder coverage.

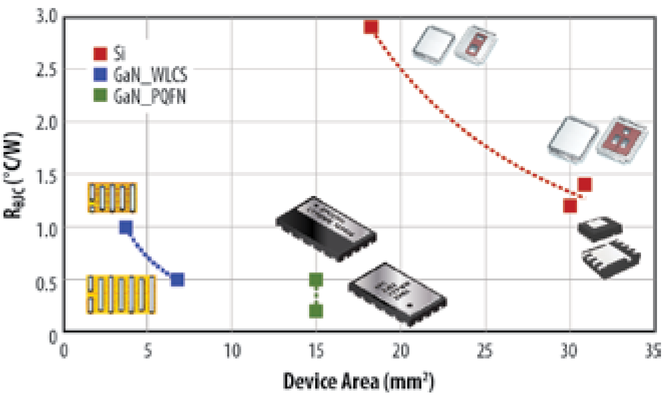

Figure 5: Junction to case thermal resistance comparison of various devices and packages.

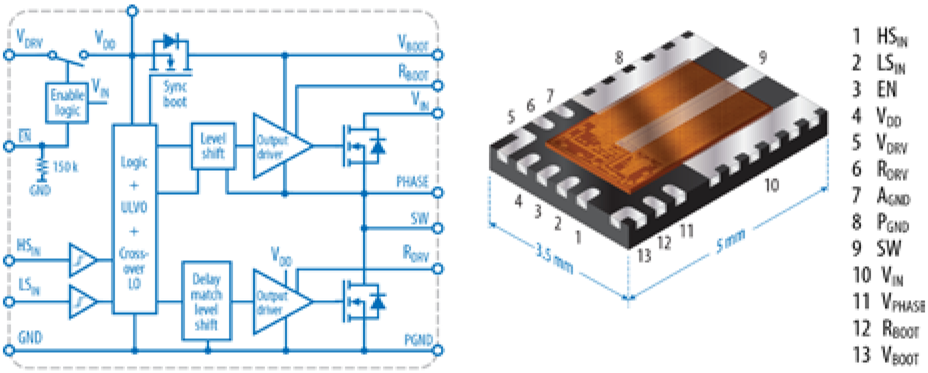

Figure 6: Detailed block diagram symbol and photo with pin assignments of the EPC23102.

For integrated circuits there is the added advantage of enabling more output pins without significantly increasing die area. Figure 6 shows a block diagram and a see-through illustration of the EPC23102 GaN monolithic power stage IC in a PQFN [8].

Summary

GaN transistors and ICs in PQFN packages maintain the performance and size advantages of WLCS GaN devices that are in widespread use in demanding applications such as automotive, satellites, enterprise computing, and e-mobility. Advantages include ease of manufacturing, excellent thermal performance, wider lead spacing in conformance with IPC-2221A standards, and, in the case of integrated circuits, the ability to accommodate a higher pin count. Indications are strong that this highly optimized package is attracting a broader group of customers with faster design cycle requirements.

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1200 V Discrete SiC MOSFETs with Enhanced Interconnection Technology Enable Energy Efficient Welding Machines

In recent years, the demand for more energy efficient products for better natural resource sustainability has led to mandatory efficiency regulations for welding machines. The improved silicon carbide CoolSiC™ MOSFET 1200 V in a TO-247 package with .XT interconnection technology and the unconventional assembly and thermal design methods offer improved designs that increase efficiency and power density[1].

By Jorge Cerezo, Sr. Applications Engineer, Infineon Technologies

In the welding machine industry trends such as improved power efficiency, reduced costs, and enhanced portability, i.e., reduced size and weight, have been the driving force behind continuous development. For instance, specific power source efficiency levels for welding machines have become, or will soon become, mandatory in standard regulations. One example of this is the latest European Union (EU) regulation for welding equipment [2] that came in force on 1 January 2023. Therefore, meeting the trends for welding machines in the medium power range of around 10 to 40 kW, where using power modules is the typical solution, has now become very demanding.

Infineon's CoolSiC MOSFET 1200 V in a TO-247 package using .XT interconnection technology for packaging significantly enhances the thermal performance and reliability of the device. Together with a specific cooling design ("in which discrete devices are directly mounted on the heat sink without any electrical isolation with the purpose of increasing the heat dissipation" [3]) it offers an improved solution for discrete devices (figure 1). It enables higher output power levels with increased efficiency and power density, and reduces the cost of medium power welding machines.

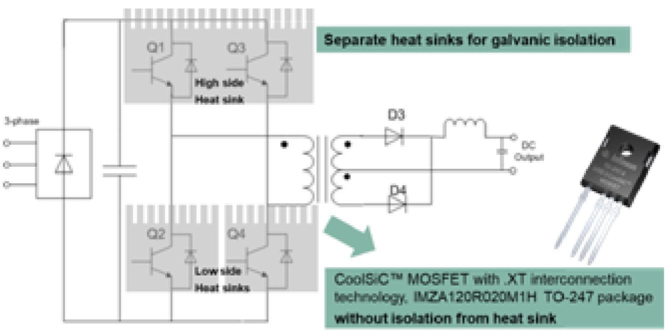


Figure 1: Welding machine power supply with 1200 V CoolSiC MOSFET discretes not isolated from the heat sink

CoolSiC MOSFET discrete with .XT interconnection technology

The enhanced CoolSiC MOSFET 1200 V takes advantage of the improved TO-247 package that uses Infineon's .XT interconnection technology. This technology features an advanced, diffusion-soldering, die attach process. The main benefit of this packaging technology, discussed at length in [4], is the significant reduction in the bond line thickness (figure 2), which, in combination with specific intermetallic alloys, results in a significantly higher thermal conductivity. This property reduces the junction-to-case thermal resistance ($R_{thj\text{-}case}$) and thermal impedance ($Z_{thj\text{-}case}$) of the device.

The reliability of the device also improves because it prevents die tilt and solder bleed-out during the die attach process, and offers practically a void free interface. Furthermore, it improves performance under thermo-mechanical stress, which means better performance during active and passive thermal cycling test conditions. Basically, the CoolSiC MOSFET 1200 V in the TO-247 package with .XT interconnection technology enables welding machine power supply designs with better thermal and reliability performance.

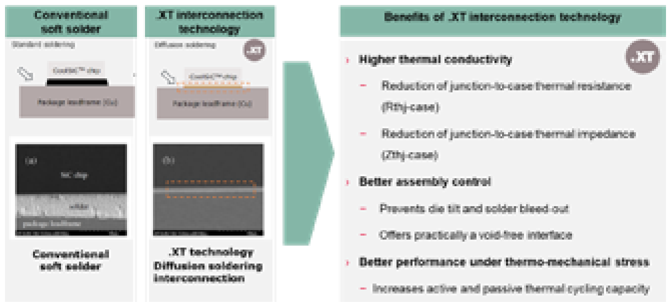


Figure 2: Infineon's .XT interconnection technology versus the conventional soft solder process

500 A welding machine power supply inverter design using CoolSiC MOSFET discrete device

The improved solution for medium power welding machines using CoolSiC MOSFET 1200 V in a TO-247 package with .XT interconnection technology was demonstrated using a unique 500 A power supply inverter design of a welding machine from a major manufacturer. It uses the cooling concept previously discussed and shown in figure 1, in which devices are mounted without electrical isolation on the heat sinks. Also, to confirm its enhanced performance, it was compared against a main competitor's SiC MOSFET under the same test conditions.

The welding machine power supply consisted of a three-phase, full-bridge topology inverter using four Infineon 20 mΩ 1200 V CoolSiC MOSFETs with .XT interconnection technology (IMZA120R020M1H) in a TO-247 4-pin package device. The basic specifications of the power supply inverter are listed in Table 1:

Parameter	Value
Input supply voltage	3-phase, 400 V, 50 Hz
Output current	500 A_{DC}
Output voltage	40 V_{DC} at 500 A_{DC}
Duty cycle	60%
Switching frequency	50 kHz
Operating $t_{ambient}$	40°C
Operating $T_{heat\ sink}$	80°C

Table 1: Basic specifications of the welding machine power supply inverter

Note that compared to the typical IGBT module solution of medium power welding machines operating at 10 to 20 kHz switching frequency, the ultra-high switching speed of the SiC MOSFET enables a significant increase in the typical operating switching frequency. This helps in reducing the size of the magnetic and passive components and thus of the inverter.

Furthermore, to meet the requirements listed in Table 1, the heat sink and air flow were selected to have the proper thermal time constant. All the heat sinks reached the thermal steady state condition in about five minutes, and thus the cooling system design (figure 3). As a result, during the 60% welding duty cycle of maximum operating requirement the SiC MOSFET devices reached the thermal steady state condition.

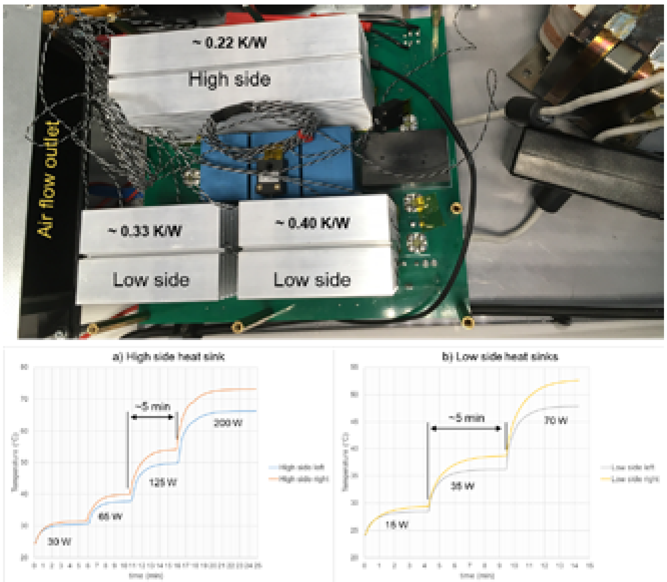


Figure 3: Thermal steady state condition and power dissipation capability of heat sinks

The power supply inverter tests were performed at the following test conditions:

- Output power: 408 A at 47.7 V, ~19.5 kW. Target 20 kW, 500 A at 40 V
- Welding duty cycle: 60%, 6 min ON, 4 min OFF
- DC bus voltage of the inverter: 530 V_{DC}
- Switching frequency: 50 kHz
- VGS, 20 mΩ CoolSiC MOSFET: 18/-3 V
- VGS, competitor 20 mΩ SiC MOSFET: 20/-4 V
- Low side heat sink R_{th}: ~0.36 K/W
- High side heat sink R_{th}: ~0.22 K/W
- Paste thermal conductivity: 6.0 W/mK
- Mounting clip force: 60 N (13.5 lbs.)
- Ambient temperature: Room temperature
- Forced air cooling
- RCL load.

As expected, because of the proper gate driver, RC snubber, and PCB layout design, there was not a significant difference between Infineon's CoolSiC MOSFET and the competitor's SiC MOSFET, both of which showed similar waveform performance (figure 4).

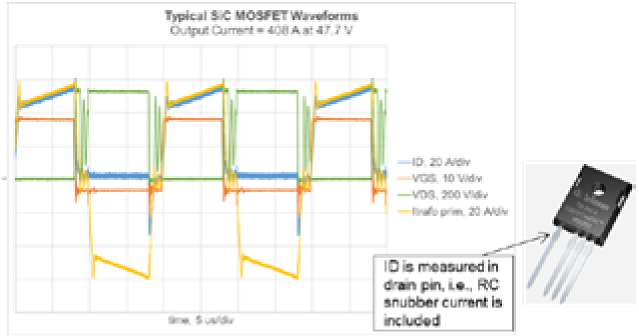


Figure 4: Typical SiC MOSFET waveforms during a welding machine power supply inverter operation

However, the thermal and power loss results demonstrated an enhanced performance of the CoolSiC MOSFET. The temperature profiles (figure 5) showed significantly better performance of the 20 mΩ IMZA120R020M1H CoolSiC MOSFET as opposed to the competitor's device. On average, the CoolSiC MOSFET showed about 6 percent lower heat sink temperature, 17 percent lower estimated power losses, and 14 percent lower case temperature than the competitor's device.

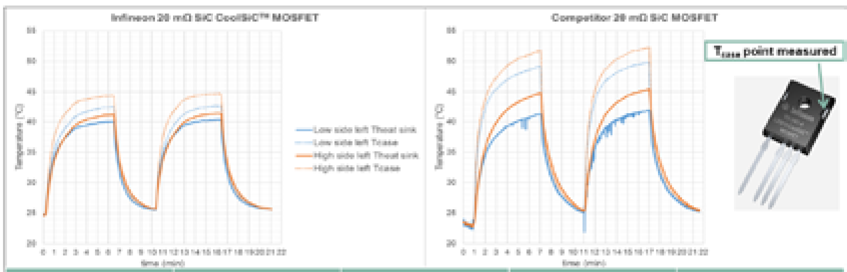
Moreover, as expected from the cooling design's data information, the CoolSiC MOSFET reached the thermal steady state condition after five minutes of operation. The competitor's SiC MOSFET, on the other hand, never reached the thermal steady state condition, implying that its power losses continue increasing after six minutes of system operation.

Lastly, the requirement of 80°C maximum heat sink temperature is easily meet by this SiC MOSFET discrete solution, even if the maximum ambient temperature of 40°C is considered.

In summary, the test results confirmed and demonstrated that the CoolSiC MOSFET discrete solution, using a cooling concept in which devices are mounted without electrical isolation on heat sinks, enables the design of inverters for medium power welding machines ranging from 20 kW and above, where power module solutions are the typical choice.

Conclusion

An improved power supply for welding machines using CoolSiC MOSFET 1200 V in a TO-247 package with .XT interconnection technology, and a well-known but unconventional cooling design, has been substantiated. The design significantly enhances heat dissipation, enabling higher output power levels typically achieved by



Inverter Position	SiC MOSFET	Maximum $T_{heat\ sink}$	Maximum T_{case}	Estimated P_{loss}
Low side	Infineon	40.4°C	42.7°C	47.6 W
	Competitor	42.0°C	49.8°C	54.3 W
High side	Infineon	41.4°C	44.7°C	42.0 W
	Competitor	45.4°C	52.3°C	53.2 W

Figure 5: 20 mΩ 1200 V SiC MOSFET's thermal and power losses performance at 60 percent welding DC operation, Infineon CoolSiC MOSFET IMZA120R020M1H versus the main competitor's device

power module solutions. The benefits of Infineon's .XT interconnection technology enables better thermal, and therefore, reliability and lifetime performance for the inverter. The proposed discrete solution enables higher efficiency and power density, helping fulfill the demand for more energy efficient welding machines and meeting welding machine industry trends such as cost, weight, and size reduction.

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High-Voltage Discrete Silicon MOSFETs (≥ 2 kV) and their Applications

The role of high-voltage (HV) discrete power semiconductor devices has become increasingly important in the world of power electronics today. Littelfuse addresses this development with an extensive portfolio of discrete HV Silicon (Si) MOSFETs featuring improved overall device performance, reduced losses, increased avalanche robustness, and reliable operation. This article focuses on the Littelfuse offering of HV discrete Si MOSFETs ≥ 2 kV.

By Sachin Shridhar Paradkar, Product Marketing Engineer; Raymon Zhou, Product Marketing Manager; José Padilla, Director Product Marketing, Littelfuse

Market Comparison of Discrete HV Si MOSFET Portfolios

Figure 1 represents Littelfuse's leadership in the HV discrete Si MOSFET market, notably above 1700 V. Being the only manufacturer developing the industry's highest voltage blocking capability of up to 4700 V, Littelfuse is the one and only supplier and thus the market leader of HV discrete Si MOSFETs above 1700 V. No other manufacturer provides discrete Si MOSFETs at this HV level. A portfolio with rugged and reliable devices, competitive product performance, patented packaging technology, and leading technical expertise have enabled Littelfuse to successfully support customers in developing demanding applications.

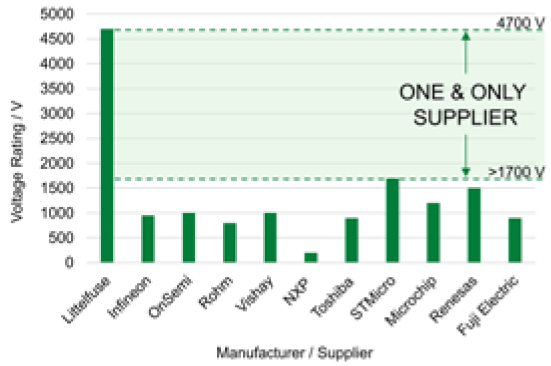
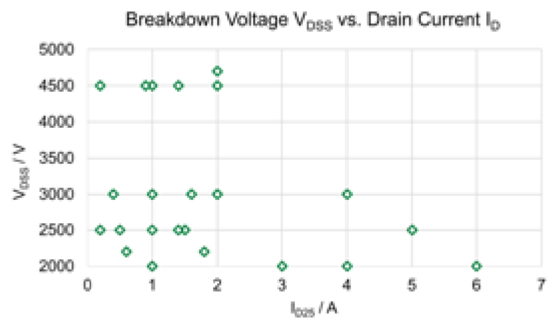


Figure 1: Market comparison of discrete HV Silicon MOSFET portfolios



V_{DSS} / kV	I_{D25} / A	$R_{DS(ON)}$ /Ω	P_D / W
2, 2.2, 2.5, 3, 4.5, 4.7	0.2 - 6	4 - 625	78 - 960

Figure 2: Littelfuse portfolio of discrete HV Silicon MOSFETs

Littelfuse Portfolio of Discrete HV Si MOSFET

The distinct and broad portfolio of discrete HV Si MOSFETs by Littelfuse from 2000 to 4700 V is depicted in Figure 2. A key highlight is the availability of these n-channel discrete HV MOSFETs in both, standard and unique packages with current ratings ranging from 200 mA to 6 A and power dissipation capability ranging from 78 to 960 W. These HV MOSFETs are capable of withstanding high avalanche energies and are specifically designed to address demanding, fast-switching power conversion applications requiring very high blocking voltages. The HV MOSFETs represent an optimal solution in applications such as laser and X-ray generation systems, HV power supplies, pulsed power applications, and are particularly of interest for auxiliary power supplies in medium voltage motor drives, photovoltaic (PV) inverters, high-voltage direct-current (HVDC) grid converters, traction, and uninterruptable power supplies (UPS).

Moreover, the HV discrete Si MOSFETs are suitable for parallel device operation due to the positive temperature coefficient of their on-state resistance. These HV discrete devices provide a more reliable and cost-efficient solution than employing series-connected, lower-voltage MOSFETs. Figure 3 enumerates the main advantages of implementing a HV design with Littelfuse's HV discrete Si MOSFETs in comparison to a series-connection of low-voltage (LV) MOSFETs.

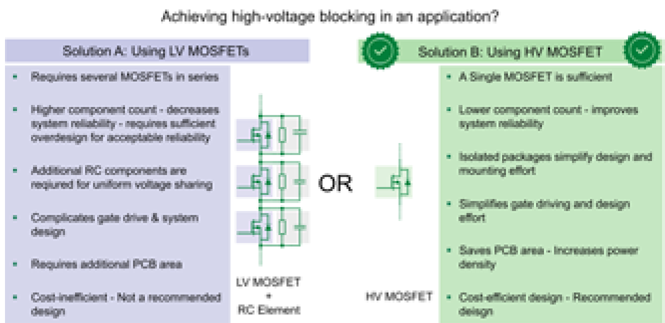


Figure 3: Key advantages of building a HV design utilizing Littelfuse's HV Si MOSFET in comparison to LV MOSFETs

Packaging – Unique HV and Proprietary Isolated Packages

Littelfuse offers unique high-voltage and patented isolated packages with several benefits resulting in value addition for the customer. At high voltage and power levels, the heat dissipated in the power device becomes critical. Packaging significantly influences the thermal behavior of the power device and could become a limiting factor. The unique high-voltage and proprietary ISOPLUS™ packages developed by IXYS-Littelfuse support to deal with critical concerns of isolation and thermal management in HV applications. Figure 4 highlights some differences between Littelfuse HV packages and standard packages.

The high-voltage versions of the standard packages offer increased creepage distances as an essential benefit. The HV discrete Si MOSFETs from Littelfuse ≥ 2 kV are available in unique HV packages such as:

- TO-263HV and TO-268HV for surface-mount-device (SMD), and
- TO-247HV and PLUS247HV for through-hole-technology (THT) PCB assembly.

HiPak
Next generation 3300 V and 6500 V

HiPak IGBT modules are renowned for their high performance in traction, industrial or renewable energy applications. Now the performance has moved up a gear with the arrival of the Trench TSPT+ for 3.3 kV 1800 A and Enhanced Planar SPT++ for 6.5 kV 1000 A IGBTs. With TSPT+, Hitachi Energy offers the next generation IGBT cell featuring a further 30 percent reduction in losses and opening up the possibility to increase current density.

Hitachi Energy

The removal of the middle drain pin in TO-263HV and TO-268HV packages, as well as the larger distance between the drain and source pins of the TO-247HV package result in increased creepage distances. This supports customers to ease the prevention of possible arcing conditions in their HV applications. For instance, the lead-to-lead creepage distance of the TO-263HV and TO-268HV has approximately doubled to 4.2 mm and 9.5 mm, respectively, compared to the standard packages. Another critical concern in HV applications is the electrical isolation itself. Littelfuse proprietary isolated discrete ISOPLUS™ packages are an excellent choice for implementing HV designs. As illustrated in Figure 5, the design incorporates a direct-copper-bond (DCB) substrate instead of the usual copper lead frame onto which the Si chip is soldered.

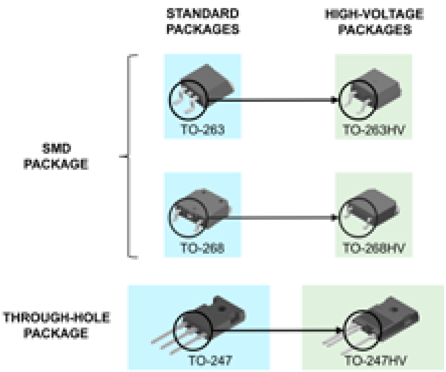


Figure 4: Increased creepage distances (lead-to-lead) offered by Littelfuse HV packages in comparison to standard packages

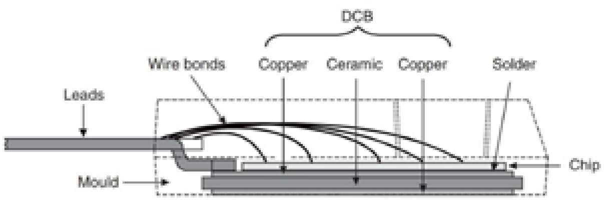


Figure 5: Cross section of Littelfuse isolated discrete package showing the direct-copper-bond (DCB) substrate

The electrically isolated tab is provided for heat sinking. DCBs provide a high isolation capability, of 2500 V_{RMS} for up to 60 s. This potentially eliminates the need for external tab isolation and additional insulator-mounting steps in the final assembly, depending on the isolation and grounding concept of the heatsink. This in turn results in cost savings for the customer in the system assembly stage. Littelfuse isolated packages offer an overall lower thermal resistance of the junction-to-heat sink path, R_{thJH}, compared to non-isolated packages with external insulation pads. This significantly improves the thermal performance of the device. Furthermore, the lower coupling capacitance between the die and heat sink in these isolated packages helps the customer to improve the EMI shielding. The HV discrete Si MOSFETs available in the ISOPLUS i4-PAC™ and ISOPLUS i5-PAC™ (ISOPLUS264™) packages display the aforementioned qualities. Figure 6 depicts the various standard, HV and proprietary isolated packages offered by Littelfuse for HV discrete Si MOSFETs.

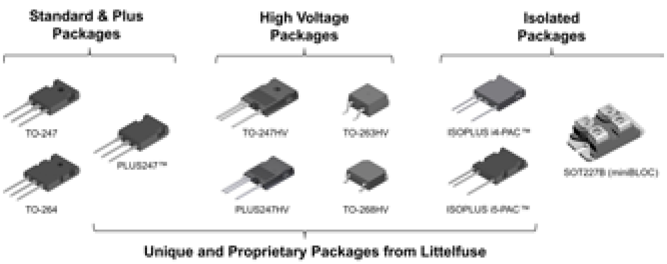


Figure 6: Standard, HV and proprietary isolated packages offered by Littelfuse for HV discrete Si MOSFETs

Applications

Figure 7 a) illustrates an example, where a HV auxiliary (AUX) power supply is used. It is a sub-component of a larger system to power gate-driver units, measurement and monitoring systems, as well as other safety-critical functions. Typically, less than 100 W of output power and output voltages between 5 and 48 V are required. Therefore, the flyback circuit, as depicted in Figure 7 b), is widely utilized.

The input to the AUX power is usually the HV DC link voltage of the power converter. An inherent requirement of the HV flyback is a power device with a very high blocking voltage rating to withstand the reflected voltage from the transformer's secondary side. Littelfuse HV discrete Si MOSFETs are a perfect fit for HV AUX power supplies in HVDC grids, electric vehicle (EV) chargers, solar inverters, medium voltage drives, UPS, and HV battery applications.

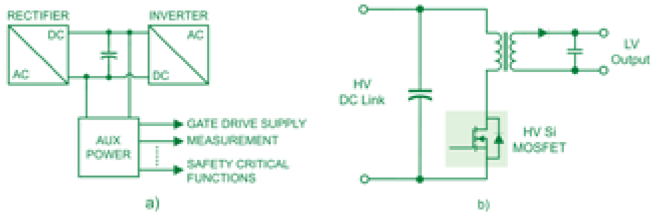


Figure 7: a) Block diagram of an inverter with the auxiliary power supply b) Flyback topology typically used for HV AUX power supplies

Pulsed power is another potential application for Littelfuse HV discrete Si MOSFETs. Pulsed power consists of releasing stored energy quickly, in a fraction of a second to apply a well-defined amount of power. Figure 8 a) depicts the simplified schematic of a pulsed power application utilizing a HV MOSFET to transfer the energy from the HV DC input capacitor to the load within a short period of time. Pulsed power is utilized in different applications such as high energy density plasma generators, intense electron beam radiography, high power microwave, medical equipment, food pasteurization, water treatment, and ozone generation, to name a few. An example of a pulsed power application illustrated in Figure 8 b) is an ultrasound-based diagnostic imaging used in medical diagnosis and treatment of patients.

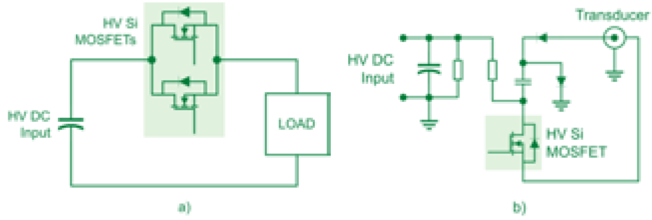


Figure 8: a) Simplified schematic of pulsed power application b) Ultrasound-generation as an example of pulsed power application

Summary

Littelfuse portfolio of unique HV discrete power devices is supporting the development of modern HV applications which have witnessed an unprecedented demand in recent times. With a broad portfolio of HV discrete Si MOSFETs in innovative, distinct packages such as the high-voltage and ISOPLUS™ types, these MOSFETs from Littelfuse have become the choice for design engineers developing novel high-voltage applications. With its uniquely positioned portfolio, Littelfuse discrete HV Si MOSFETs are particularly well-suited for AUX power solutions across a wide range of applications.

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Practical Application of Middlebrook's Filter Criteria

In this article, we will revisit a very old topic and apply practical rules to the problem. The subject is the stability of a system where an input filter interacts with a switching power supply. We will discuss how defining the input filter incorrectly can lead to inaccurate conclusions about the system stability or lead to systems that are far from optimal.

By Dr. Ray Ridley, President, Ridley Engineering

We will show the need to properly identify which components are part of the input filter and which are part of the power supply. Middlebrook's input filter stability criteria only apply to the system measured with the filter components in the correct location.

Then, we will talk about the practical way to measure the system. Complex and difficult measurements can be avoided with a pragmatic and simple lab approach to ensure a stable system.

Input Filter Impedance Interaction

An input impedance measurement or prediction gives information about the characteristics of the power supply input terminals. Knowledge of the input impedance characteristic is very useful for anyone who must add components to the basic power supply design to complete the power system. This can include an input EMI filter or another power supply that preconditions the input voltage rail.

Figure 1 shows a block diagram of a switching power supply connected to an input filter. Dr. Middlebrook, in his paper on input filter interactions [1], said that if the input impedance of a converter, Zin, is always greater than the output impedance of the filter, Zout, then a stable power supply will remain stable when the filter is connected.

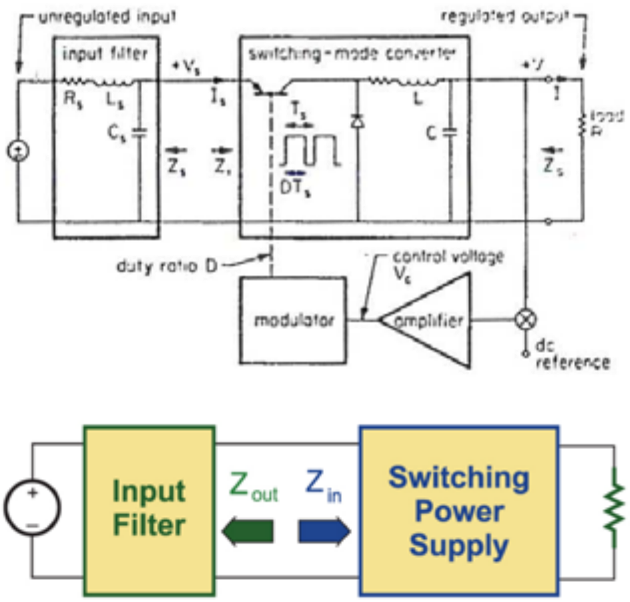

Figure 1: Power supply with input filter module. (Middlebrook's original Figure 1 is shown for reference.)

Conceptually, the impedances can be measured with the setup shown in Figure 2. An AC voltage source is connected in series between the filter and the switching power supply. The input impedance of the power supply is measured from the ratio of the input voltage of the switching power supply and the current into the terminals. While this measurement is easy to conceive and implement in a theoretical circuit or simulation, it is an awkward measurement to make in the lab. As we will see in this article, it will often result in erroneous results if you don't measure in the right place.

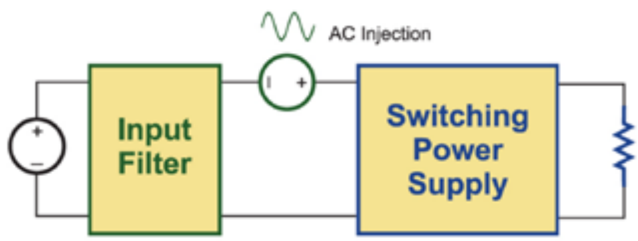

Figure 2: Voltage injection into the power rail for impedance interaction measurements.

Measuring in the Right Place

The Middlebrook criteria requires that the switching power supply block of Figure 2 contains ONLY the switching cell, and none of the input filter components, as shown in his original Figure 1. However, it is usually a practical necessity that at least one filter component is included in the power supply block to filter high-frequency pulsating currents. Without this, measurements can be too noisy, and the converter may not operate properly. Also, in many cases, the internal circuit nodes for measurement are inaccessible, and the power supply input impedance measurement will naturally include several filter components.

Figure 3 shows a measurement setup where a small input bypass capacitor is included in the power stage measurements. This has a significant impact on the input impedance measurements, greatly reducing the impedance at higher frequencies. We cannot use this measurement to apply the Middlebrook criteria.

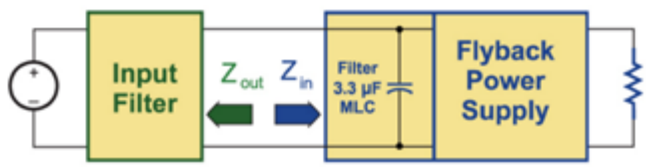

Figure 3: Flyback converter with input filter capacitor. In most cases, practical measurements require some input filter components to be included in the impedance measurement.

Figure 4 shows the proper location for application of the Middlebrook criteria. The filter capacitor is moved into the input filter block and is NOT included in the switching power supply block. However it is included in the filter block.

Now we have a problem. Proper application of Middlebrook's rule requires that we measure the system of Figure 4, but it may be practically impossible to measure the input impedance. If we just measure the input impedance of the power supply with filter com-

ponents inside, Middlebrook's rule has no relevance. What to do? The answer is considered next in this article.

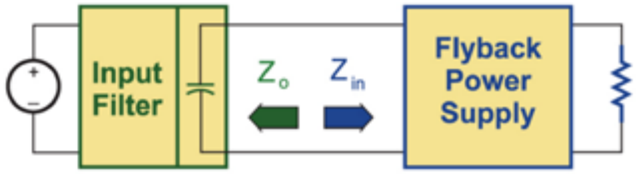

Figure 4: Proper characterization of the impedance interaction requires the input filter capacitor to be moved to the filter module.

Plot the MEASURED Output Impedance of the Unpowered Input Filter

Measure the output impedance of the input filter, including ALL filtering components, with a device such as the [AP310](), or the [RidleyBox](). This measurement can be done with the filter unpowered, making sure that the input of the filter is shorted. This is an easy measurement to make since there is no switching noise present.

Figure 5: Use the AP310 or the RidleyBox to measure the unpowered input filter. This measurement is essential since filter vendors may not provide accurate data or measurements. Make sure the input of the filter component block is shorted.

We don't recommend that you just model the input filter in a circuit simulator – always confirm the impedance with measurement. It is common for filter designers to use core loss and damping components to stop the input filter impedance from peaking. The damping mechanisms require advanced circuit models that are unlikely to be provided by a filter vendor. There is no problem in using your circuit simulator to verify the results, but you should always make a hardware measurement.

Plot the CALCULATED Ideal Input Impedance of the Power Supply

There is no need to measure the input impedance of the power stage. This can be plotted as a theoretical quantity. For simplicity, and to be conservative in the design, we will assume an infinite bandwidth control loop which will provide a fixed negative input impedance.

The two impedances are plotted on the same graph as shown in Figure 6. Make sure there is good separation (10 dB) between the two quantities.

You can see from Figure 6 that this is a poor design without good separation of input and output impedance. Even if there is good separation, it is a good idea to damp the ringing of the filter to prevent ringing at the output of the power filter. I remember Middlebrook stating at a conference that it's probably not a good idea to run with an undamped filter.

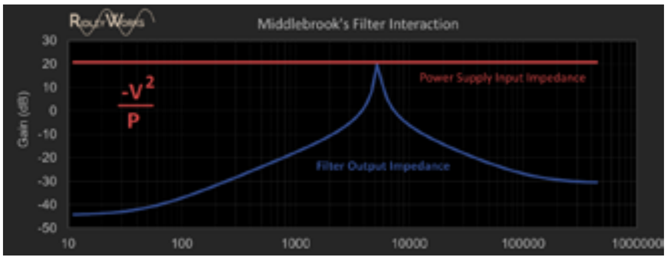

Figure 6: Measured filter output impedance plotted with calculated power supply input impedance. The example shown here is NOT a good design case. It will probably oscillate.

Notice that in the practical world, there is no need to consider the open-loop input impedance of the power supply. Middlebrook devoted a lot of time in his paper to talking about this, but I have never seen it applied in the field.

Summary

Middlebrook's original paper is quite complicated to follow. However, bear in mind that it is an academic paper. Simplify for practical application. There are six steps to a successful system design:

1. Identify the components that are part of the input filter.
2. Identify the components that form the switching power supply. Do NOT include any filter components in the power supply.
3. Place a short circuit on the input to the filter.
4. Measure the output impedance with a device such at the AP310 or RidleyBox. Use the impedance attachment. This is a passive, two-terminal measurement that does not require power applied to the input filter.
5. Plot the CALCULATED input impedance of the power converter on the same graph as the filter output impedance. Ensure good separation between the two curves.
6. Check that the filter is well damped to prevent ringing. Failure to do this can cause dynamic range loss in the operation of the power system.

Following these steps will bring confidence in rendering a stable system.

References

You can read more information on this topic in each of these references.

- [Input Filter Considerations in Design and Application of Switching Regulators]() 1976 paper by Dr. R.D. Middlebrookk
- [Impedance Measurement for Switching Power Supplies]() using the AP310 or RidleyBox frequency response analyzers.
- [Input Filter Design and Measurement,]() and other related article in the Ridley Engineering Design Center.

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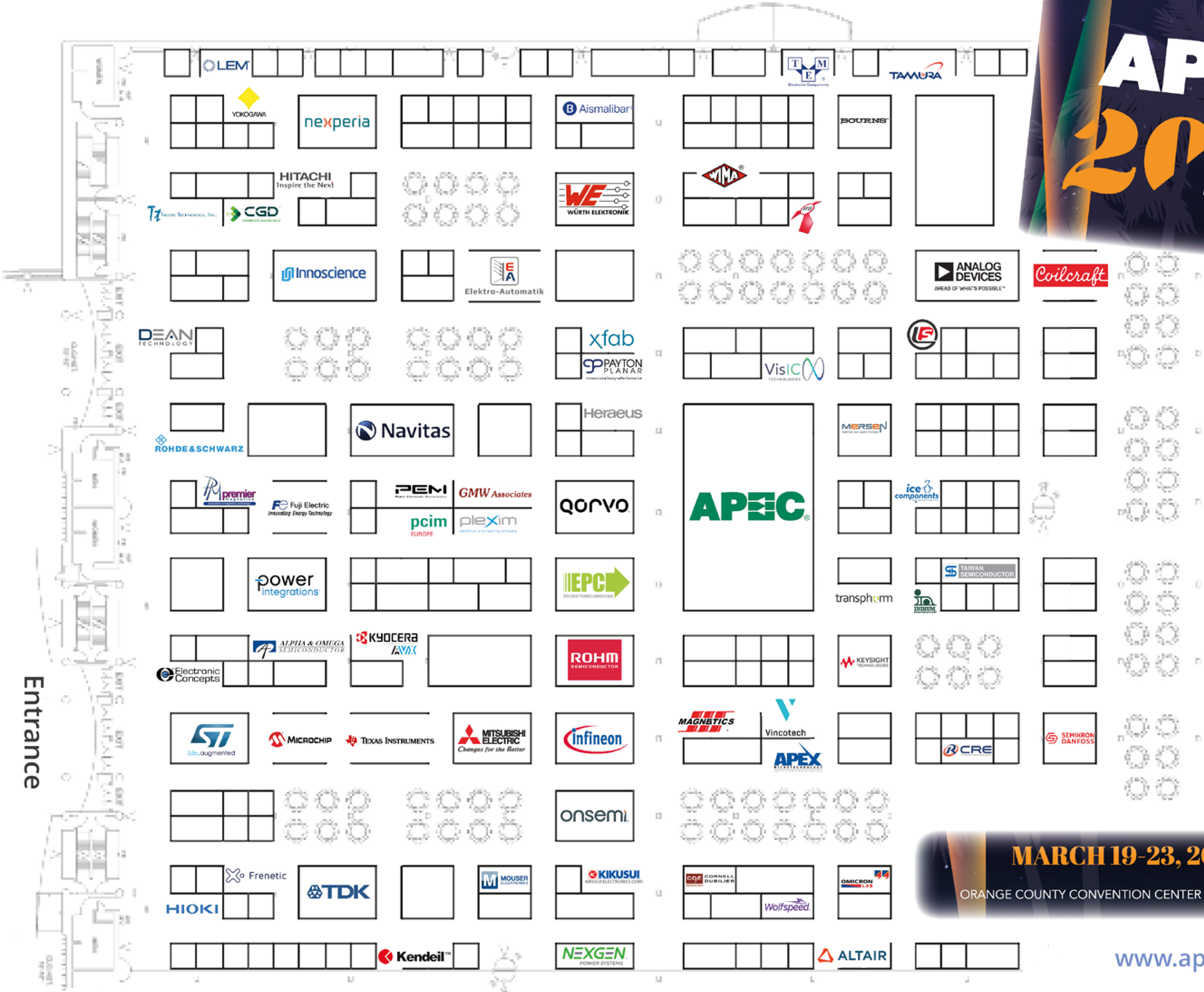

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10 Tips for Designing with High Voltage Resistors

Optimised strategies prioritise definition and testing of these key components early in the design cycle

"High voltage" is a term that can have several meanings, but here we are considering circuits with voltages from 1 to 100kV. An example from the lower end of this scale is an automatic external defibrillator, in which a capacitor is charged to up to 5kV before delivering a potentially life-saving, precisely calibrated electrical surge to a patient.

By Stephen Oxley, Business Development Engineer, TT Electronics

Staying with the healthcare theme but at the other end of the scale, we have medical X-rays, which are generated by accelerating electrons with around 70kV, then abruptly stopping them with a metallic target. Carefully controlled variation in this voltage allows the system to be adjusted to capture the image of soft tissue or different bone thicknesses. These are just two examples of high-voltage applications in which resistors, usually the simplest of commodity components, are elevated in importance to provide critical protection and accurate control in demanding applications. This article presents ten tips based on support given over many years to designers needing high-voltage resistors, not just in medical, but also in industrial, transportation, and scientific sectors.

Ten Tips

1. Understanding voltage ratings

The primary voltage rating of a resistor is its limiting element voltage (LEV), sometimes called the working voltage. This is the maximum continuous voltage that may be applied across a resistor whose ohmic value is greater than or equal to the critical resistance. Below this value, the maximum voltage is restricted by the power rating (P_r) to $\sqrt[2]{P_r . R}$. Generally, it is DC or AC rms, but the datasheet for high voltage parts may define it as DC or AC peak. Associated with this is the overload voltage rating, which is generally 2 or 2.5 times the LEV for 2 to 5 seconds. Often, much higher peak voltages can be withstood for short durations, as indicated in the pulse performance section of a datasheet. The final rating is the isolation voltage, which is the maximum continuous voltage that may be applied between the resistor and a conductor in contact with its insulated body.

2. Voltage division with discrete resistors

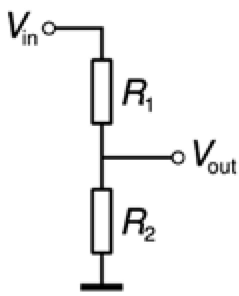

Figure 1: Voltage Divider

Voltage division requires a high-value resistor R_1 in series with a low-value resistor R_2 as shown in Figure 1.

The voltage ratio is given by

$$\frac{V_{in}}{V_{out}} = {(R_1 + R_2)}/{R_2} = {R_1}/{R_2} + 1$$

It should be noted that the voltage ratio is not the same as the resistance ratio R_1 / R_2 but is offset by one. For example, to obtain a voltage ratio of 1000, it is necessary to define a resistance ratio of 999. For a discrete resistor design, it is preferable to select standard values, and some examples for decade voltage ratios are presented in Table 1.

Target Voltage Ratio	R_1 / R_2	R_1 (E12)	R_2 (E24 or E96)	Actual Voltage Ratio	Nominal Error
10	9	82K	9K1	10.01	+0.1%
100	99	470K	4K75	99.95	-0.05%
1000	999	1M0	1K0	1001	+0.1%
1000	999	6M8	6K81	999.5	-0.05%
10,000	9999	10M	1K0	10,001	+0.01%

Table 1: Decade Voltage Ratios using Standard Resistor Values

Having selected nominal values, the next consideration is the tolerance required. The tolerance in resistance ratio is simply the sum of the individual resistance tolerances. These are not necessarily the same; often it is most economical to select a tighter tolerance on the low-voltage part. For example, high voltage R_1 at 1% and low voltage R_2 at 0.1% results in a resistance ratio tolerance of 1.1%. For voltage ratios exceeding 50:1, the tolerance on the voltage ratio is effectively the same as that of the resistance ratio.

3. Specifying integrated voltage dividers

High-voltage dividers that integrate R_1 and R_2 into one three-terminal component are available, illustrated by TT Electronics' HVD series (Figure 2). There are a number of precision advantages to this approach. For example, the target voltage ratio may be defined precisely, without the constraint of choosing standard values.

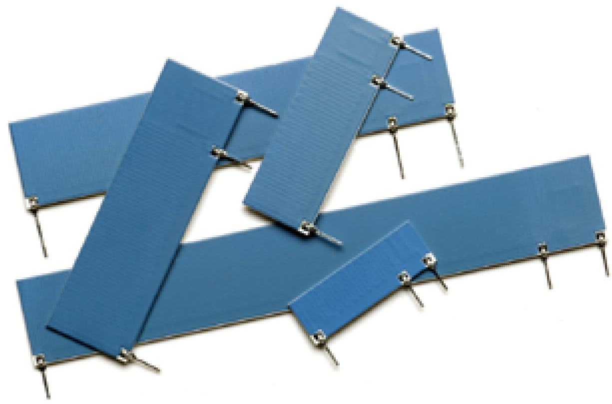

Figure 2: Integrated Voltage Dividers

The values specified for integrated dividers are normally the low value R_2 and the total value R_1 + R_2. Also, the tolerance on the voltage ratio can be controlled directly by the trimming process and so can be made considerably tighter than the absolute tolerances on the resistor values. For example, R_1 and R_2 can be defined with


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2% absolute tolerances, but the voltage ratio may be adjusted to a 0.5% tolerance.A similar advantage can apply in relation to the temperature coefficient of resistance (TCR), with the tracking TCR, which determines the temperature stability of the voltage ratio, being potentially lower than the absolute TCR of the resistor elements. Further, it is possible to design dividers that extend this element of matching to the areas of life drift and voltage coefficient of resistance (VCR), although this will typically call for a customised design.

4. Evaluating TCR and VCR errors in dividers

Provided the R_1 value is sufficiently high, and the voltage sufficiently low, there will be a low level of self-heating in the divider. If this is the case, it is relatively easy to measure the TCR and VCR effects separately. TCR effects are calculated using a temperature chamber, and the resulting figure of merit is defined as Temperature Coefficient of Voltage Ratio = $\frac{1E+6.\frac{VRht-VRlt}{VRlt}}{HT-LT}$ in ppm/°C where $VRht$ and $VRlt$ are the voltage ratios at high and low temperatures, and HT and LT are the high and low temperatures.

The corresponding figure of merit for VCR effects is similarly defined as Voltage Coefficient of Voltage Ratio = $\frac{1E+6.\frac{VRhv-VRlv}{VRlv}}{HV-LV}$ in ppm/°V where $VRhv$ and $VRlv$ are the voltage ratios at high and low voltages, and HV and LV are the high and low voltages.

If self-heating is not negligible, then in the TCR test, the chamber temperature should be adjusted to give the correct HT figure, and time should be allotted for the temperature to stabilise. The VCR test should be short in duration to minimise temperature rise. Alternatively, one can use a temperature chamber to measure low voltages at higher temperatures and vice versa, thereby cancelling out temperature-related resistance changes.

5. Calculating the value of a bleed resistor

Bleed resistors are used to discharge capacitors to safe voltage levels after power is removed. A bleed resistor may be either switched across the capacitor for rapid discharge without quiescent dissipation, or permanently connected for high reliability and low cost. In the latter case, there is a trade-off between the time to reach safe discharge and the quiescent power loss. Selecting a maximum suitable ohmic value is achieved from an exponential discharge calculation:

$$R_{max} = {}^{-T_d}/_{C.Ln(V_t/V_o)}$$

where T_d is discharge time, C is capacitance value assuming maximum positive tolerance, V_t is the safety threshold voltage, and V_o is the initial voltage. The highest standard value, which, allowing for tolerance, lies below R_{max} should be used.

For a selected value R, the initial power is given by $P_o = V_o^2/R$. For a switched bleeder, this is the peak power. For a permanently connected bleeder, it is the continuous dissipation, and the resistor chosen must be rated accordingly.

6. Selecting the right balancing resistor

All aluminium electrolytic capacitors exhibit a leakage current when a DC voltage is connected across them. This may be modelled by a leakage resistance connected in parallel with the capacitor. This resistance is non-linear, that is, its value is a function of the applied voltage. In this case, the value is poorly defined, having a large degree of variation from one capacitor to another. When building a capacitive reservoir for a high-voltage DC bus, it may be necessary to use a series combination of two capacitors, each rated at half the bus voltage. If the capacitors are identical, the bus voltage will be shared equally between them. However, in practice, the leakage resistances will differ, leading to uneven sharing and possible voltage overload on the capacitor with the higher leakage resistance.

Figure 3: TT Electronics' WPYP series is designed for direct mounting on capacitors

The solution is to use balancing resistors, such as that shown in Figure 3, in parallel with each capacitor. These are high-value resistors rated at the appropriate voltage and matched in value to within a few percent. The value needs to be as high as possible to minimise power dissipation, but is generally chosen so that it is no more than 10% of the lowest value of leakage resistance at the rated voltage of the capacitor. By this means, the effect of the unbalanced internal capacitor leakage resistance is swamped by that of the balancing resistors, and the voltages are approximately equalised.

7. Withstanding high voltage surges

It is sometimes the case that designers looking at high-voltage resistors are doing so because their circuit must withstand high-voltage transients. If the continuous voltage stress does not call for a high-voltage rating, it may well be the case that a low-voltage but surge-tolerant part is the best solution. For example, TT Electronics' 5W wirewound high surge resistor, WH5S, does not have a high-voltage rating but can withstand a 1.2/50µs up to 10kV peak, whilst the surge tolerant 2512 chip resistor, HDSC2512, has an LEV of 500V but can withstand a peak voltage of up to 7kV.

8. Designing to meet safety standards

When designing equipment to meet the requirements of electrical safety standards such as IEC 60664, it is necessary at an early stage to consider the relevant creepage and clearance requirements. These will not only affect PCB layout design but also, in some cases, component selection. Where a resistor connects to a high-voltage level, it is important to check the distance between its terminations, and, in the case of heatsink-mounted parts, between the resistor and a metallic thermal interface. This is defined in two ways. Firstly, the creepage is the shortest distance across an insulating surface. This reduces the likelihood of humid and contaminating conditions enabling surface scintillations with energy high enough to entail tracking. Secondly, the clearance is the shortest distance in air. This addresses the risk of flashover. These two dimensions, if not apparent from datasheets, should be available from the manufacturer.

Another piece of information that may be needed is the material forming the insulating surfaces, as this determines the comparative tracking index (CTI), which classifies an organic material's propensity to support processes leading to tracking. If a resistor bridges the isolation barrier in a design, for example, to provide a galvanic connection to prevent excessive electrostatic charge build-up, the IEC 60065 safety standard requires resistors to withstand a specified high-voltage surge test. As this is becoming a legacy standard, ongoing certification of resistors is no longer relevant. Still, designers following the hazard-based safety engineering approach of IEC 62368-1 will be helped in knowing that there are still products that meet the requirements of IEC 60065.

Figure 4: TT Electronics' T44TUH is suitable for oil immersion, which doubles its LEV to 28kV

9. Optimising the PCB layout

PCB layout is crucial to maintaining the safety of a high-voltage design, and this is most obvious where high-voltage resistors are miniaturised and in surface mount device (SMD) form. A good example is TT Electronics' HVC series which includes a 2512 size chip resistor with a 3kV rating. Tracks or vias beneath or very close to the component should be avoided, as should any features likely to trap or encourage ionic contamination during manufacture or use. One special measure which may be used to increase creepage distance and avoid trapped contamination is the cutting of a slot in the PCB beneath the component.

10. Designing for potted and oil-filled assemblies

Two limiting factors in high voltage designs can be the tendency of contaminated organic surfaces to support tracking and the risk of electrical discharge in the air, particularly around small radius surfaces. Both of these constraints can be tackled by potting or immersion in mineral oil, which prevents the ingress of contamination and replaces air with a substance of higher dielectric strength. This in turn reduces creepage and clearance constraints allowing an assembly to be reduced in size. When choosing resistors for such an assembly, it is essential to select parts that are insulated in a manner that avoids the risk of outgassing. Any air incorporated with the component can form a void in which partial discharges can occur, leading to the long-term degradation of insulating materials. This rules out the use of parts with insulation sleeving or with rough or porous coating finishes. An epoxy coating, either printed or powder dipped, is often ideal, and a manufacturer can advise on suitability.

Conclusion

In many cases, resistors can be regarded as the simplest of components in a circuit and need no special attention from designers beyond selecting an appropriate ohmic value and power rating. However, high-voltage circuits often call for a specialist component from a manufacturer who can provide experience and expertise. The designer is well advised to prioritise these as critical components for definition and testing at an early stage in the project, and to check whether a custom or semi-custom approach can add significant value.

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A Novel Half-Bridge GaN Device for Enhanced System Performance

Gallium Nitride (GaN) power switches continue to make inroads in diverse power conversion applications. One of the facilitators for this growth has been the responsiveness of GaN device manufacturers to diverse end-user requirements by providing targeted products that fit well into a given application.

By Asif Eqbal, Manager Design; Rajesh Ghosh, Chief Power Electronics Engineer; and Dhaval Dalal, Systems Applications Architect, Tagore Technology

When it comes to half-bridge (HB) power conversion topologies, there is a clear distinction between high-power, efficiency-driven applications and low-power, cost-driven applications. For the first type, Tagore Technology offers a set of devices with integrated-driver functionality. These devices interface very well with digital controllers as well as with dedicated analog controllers, while offering a number of benefits from driver integration, including, but not limited to efficiency improvements, better reliability, and a higher level of programmability.

However, at the other end of the spectrum, the low-power, cost-driven applications already have an existing ecosystem where there are well-established highly integrated controllers and drivers that meet the customers' requirements when used with Silicon MOSFETs. For these applications, what is needed is a GaN solution that leverages this existing ecosystem and complements it by providing a highly integrated, compact GaN switching device.

A novel Half-Bridge GaN device

As shown in Figure 1, the TP44xx0HB, recently introduced by Tagore Technology, fulfills these requirements. The device is available in a 30-pin, 8×10×0.8 mm QFN package. It integrates two GaN switches: high-side (HS) and low-side (LS) needed for HB applications. The two switches are internally connected (the source of the HS switch to the drain of the LS switch), offering extremely low parasitics (both power loop parasitic inductance and parasitic junction capacitance). Additionally, thermal pads for both the sources ensure low thermal-impedance cooling paths. Each of the switches is equipped with its own gate ESD structure to provide added protection. Finally, and most importantly, Kelvin connections for both the switches ensure separation between the power loop and the gate drive loop for the HS and the LS, providing a safeguard against the Miller turn-on and the degradation in gate reliability. The TP44xx0HB is available in three different flavors, featuring GaN switches with Rds-on of 90 + 90 mΩs (TP44110HB), 180 + 180 mΩs (TP44220HB), and 360 + 360 mΩs (TP44440HB).

Ease of layout and associated circuit benefits

The TPS44100HB has been specifically designed to simplify the circuit board layout and offer a slew of associated circuit performance benefits. The integrated package allows the shortest possible loop between the HS drain and the LS Source adjacent to the package as shown in Figure 2. The suggested layout in Figure 2 also depicts that the required creepage distance of 2.8 mm is maintained in the IC as well as on the board. When using discrete switches, designers are often forced to make compromises between the optimum electrical layout and meeting creepage distances. The integrated device alleviates that concern. Further, the area of the pad connecting the drain of the LS to the source of the HS, which is the switched node of the half-bridge, is small enough to minimize parasitic capacitance to other planes, but large enough for effective thermal performance.

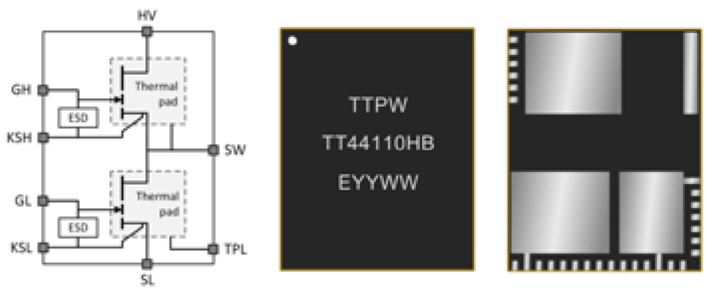

Figure 1: TP44xx0HB – Functional Block Diagram (Left) and Device Image (Center, Right)

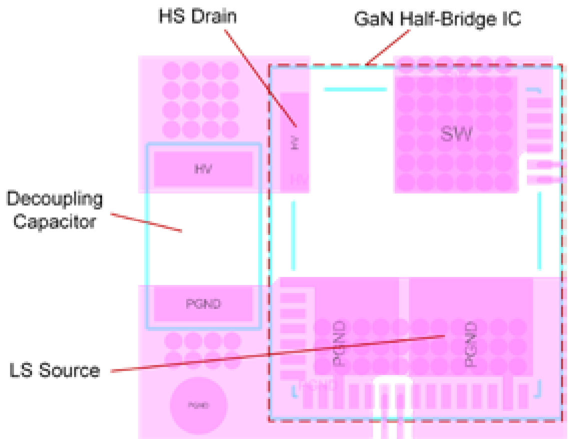

Figure 2: PCB layout diagram showing the suggested placement of the DC bus decoupling capacitor

The pin-out of the TP44xx0HB has been carefully designed to provide ease of layout and significant flexibility. A number of pins and a large thermal pad are not electrically connected—allowing the flexibility to connect them to appropriate nodes/traces or leaving them unconnected, as desired. The most important feature here is the low voltage (± 20 V) isolation between the thermal pad and the source pins of the LS switch. This isolation allows one to place current sense resistors between the source pins and the power ground without compromising the connection between the thermal pad and the PCB of the power ground.

Ease of interface with popular controllers

In time-, space-, and cost-constrained product designs, there is a major incentive to use tried and tested components and a disincentive to make big changes to the system architecture. In such cases, the GaN device needs to be as easy to retrofit into the traditional silicon MOSFET -based designs as possible. While the integrated HB offers space and cost savings as opposed to discrete devices, it also offers a very easy interface with popular controllers (e.g., TEA2016 from NXP or NCP13992 from onsemi). These controllers typically include drive circuits for driving silicon MOSFETs, so the drive signal voltage levels are high and cannot be used directly with GaN

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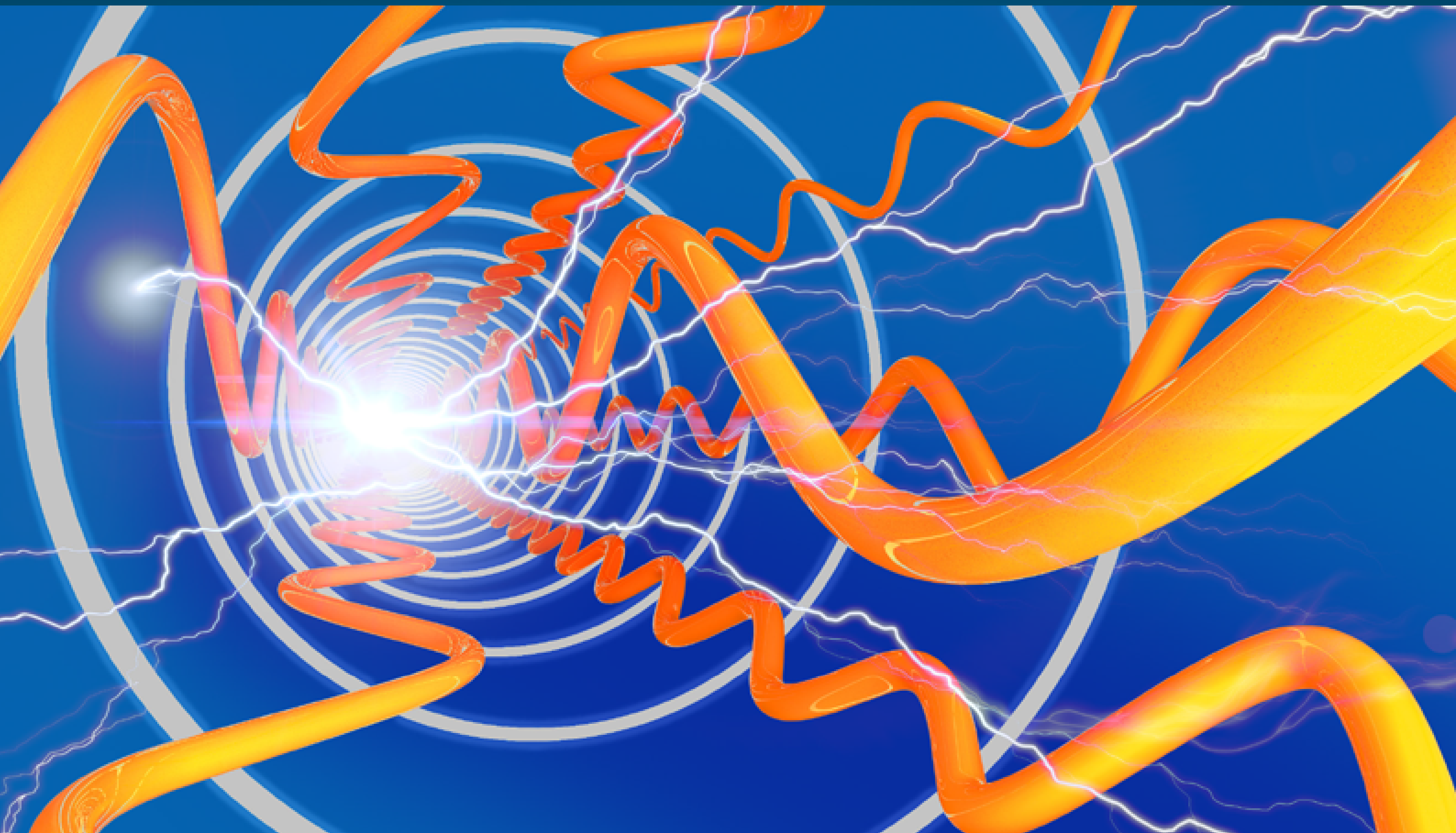

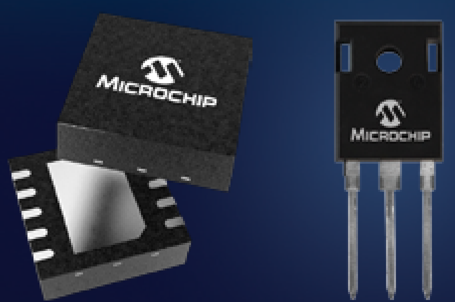

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switches. It is impractical to expect their interface to GaN to include a dedicated driver for GaN FET driving – that would be space and cost prohibitive.

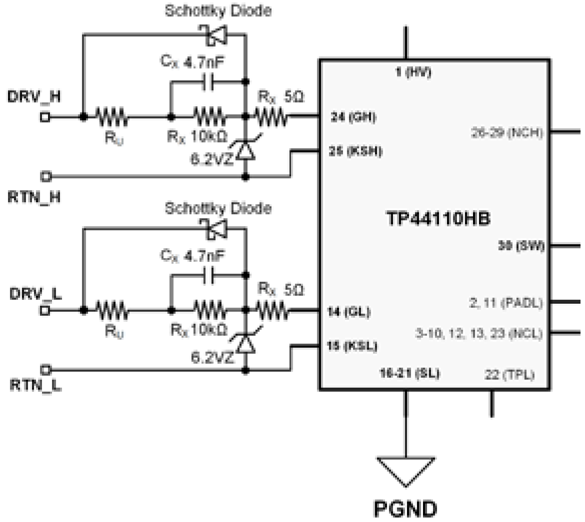

Figure 3: Interface circuit for driving GaN switches from a PWM controller/driveR

Instead, Tagore Technology offers an extremely simple interface circuit as shown in Figure 3. Here, DRV_H and DRV_L are the original gate drive signals with respect to their respective return signals RTN_H and RTN_L, coming out of the controller IC for the HS and LS switches. These signals are, however, of +12V/0V levels. On the other hand, the performance of the GaN switches greatly depends on the gate drive voltage levels. The interface circuit provides the optimal (reliable and efficient) drive levels for GaN switches (+6.2V/0V across the Gate and Source terminals). The 6.2V Zener diode clamps the gate-to-source voltage of each GaN switch to 6.2V ensuring the reliability of the device. The resistors RU control the turn-on switching times of the GaN switches. The reverse Schottky diodes help speed up the turn-off times and avoid cross-conduction between the high- and low-side switches. The rest of the components either provide required biasing for the Zener diode or damping against any oscillations that might arise in the gate drive path. The separate Kelvin source of each GaN switch completely decouples the gate drive circuit from the power circuit.

Additionally, the pinout of TP44xx0HB has also been optimized for a direct interface to the TEA2016 and other similar controllers/drivers. Since the TEA2016 is a combo controller (PFC+LLC), it is the most challenging to interface with and will be used as an illustrative example. The utilization of a combo controller and an integrated device offers the highest level of integration and the lowest parts-count that can be significantly beneficial to many cost- and space-constrained designs. The overall system reliability can also improve due to a reduction in the component count. By positioning the gate drive pins orthogonally on the package, the traces to each of the GAN switch gates from the TEA2016 can be kept separate. This results in a single-layer layout of the complete gate circuitry (HS and LS) without the use of any vias as shown in Figure 4. There are multifold benefits of the single-layer layout: reduction in loop inductances, decoupling of gate signals from power signals, reduction in board size, and most importantly, better thermal design. Multiple vias can compromise any heat-spreading efforts through the PCB layers and increase thermal impedances. The power trace layout is also simplified for both power stages as shown in Figure 4, resulting in lower loop inductance and better noise immunity.

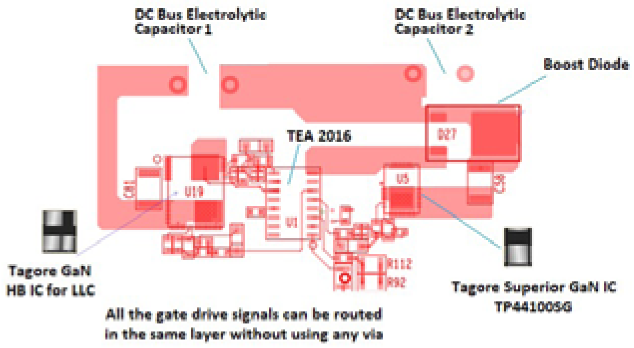

Figure 4: Layout of a PFC+LLC using TP44xx0HB(U19) and TEA2016 (U1)

Conclusions

The TP44xx0HB fills a much-needed gap for time-, space- and cost-constrained power converter designs by offering a unique highly integrated, flexible, easy-to-use, and easy-to-interface GaN device. The system-level benefits accrued using this device include lower parasitics, higher reliability, better electrical performance, and improved thermal performance.

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Understanding the Theory Behind Transient Thermal Impedance

Transient thermal impedance is a measure of how a device behaves when pulsed power is applied to it. Transient thermal impedance is an important parameter, as it determines how the device behaves under low duty cycles and low-frequency pulsed loads.

By Christophe Vaucourt, Senior Technical Marketing Engineer, Monolithic Power Systems (MPS)

IC packages have many thermal metrics, such as θ_{JA} and Ψ_{JT}. These parameters make it simple to estimate junction temperature in steady state. This article discusses thermal transient behaviors and presents the basic theory regarding thermal impedance.

Thermal Parameters Overview

The thermal properties of flip-chip IC packages are characterized by their θ_{JA}, Ψ_{JT}, and Ψ_{JB} parameters. θ_{JA} is the junction-to-ambient thermal resistance (in °C/W), which is a system-level parameter that significantly depends on system properties, such as the design and layout of the PCB on which the part is mounted. The board acts as heatsink that is soldered to the leads of the device. For natural convection heat transfer, more than 90% of the heat is dissipated by the board, and not from the surfaces of the package. θ_{JA} can be calculated with Equation (1):

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \quad (1)$$

Where TJ is the junction temperature (in °C), TA is the ambient temperature (in °C), and PD is the device's heat dissipation (in W).

Ψ_{JT} is the characterization parameter that measures the temperature change between T_J and the temperature on the top of the package (in °C/W). Because the heat flowing from the die to the top of the package is unknown, Ψ_{JT} is not the true junction-to-top thermal resistance, but it is assumed by the circuit designer to be the total power of the device. Although this assumption is invalid, Ψ_{JT} is still a useful parameter since its characteristics are similar to that of the IC package's application environment. For example, thinner packages have smaller Ψ_{JT} values.

Note that Ψ_{JT} varies slightly due to both board construction and airflow conditions. Ψ_{JT} can be estimated with Equation (2):

$$\Psi_{JT} = \frac{T_J - T_C}{P_D} \quad (2)$$

ΨJB can allow system designers to calculate the device's junction temperature based on a board's measured temperature. The ΨJB matric should be close to θ_{JB}, as the PCB dissipates most of the heat of the device. T_J can be calculated with Equation (3):

$$T_J = T_{PCB} + (\Psi_{JB} X P_D) \quad (3)$$

Where T_{PCB} is the board's temperature close to the package's exposed pad (in °C).

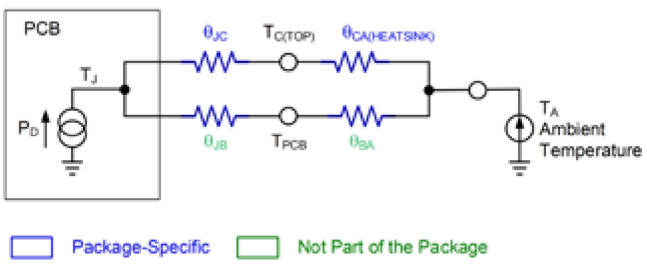

Figure 1: Junction-to-Ambient Thermal Resistance

Figure 1 shows a diagram that explains the junction-to-ambient thermal resistance.

A lower θ_{JA} is mainly achieved by reducing the resistance from the PCB's thermal plane. In applications where conduction is the primary method of heat transfer (meaning that convection cooling is restricted), the PCB's power plane area has the most significant effect on θ_{BA}.

Thermal Properties

In applications such as motor drivers, the high-power pulse width is limited to a few tens or hundreds of milliseconds, which means designers must consider the effects of thermal capacitance. If the thermal capacitance is sufficiently large, it can limit the junction temperature to remain within the device's ratings, even in the presence of high dissipation peaks. Proper thermal management improves the device's performance and reliability.
There are three mechanisms by which heat can be transferred: conduction, convection, and radiation.

Conduction

Conduction is important because it is the surface area that eventually dissipates the heat. Through conduction, heat spreads out the required surface area. Heat transfer through conduction is governed by Fourier's law, which states that the rate of heat flow through a material is directly proportional to the material's cross-sectional area and the temperature difference across the material; conversely, the heat flow is inversely proportional to the material's thickness. Some materials (e.g. copper) conduct heat more effectively than others (e.g. FR4). Table 1 shows the thermal conductivity factor (K) for different materials. These common materials have significantly different thermal conductivity factors.

Materials	Conductivity (W/m.K)
Air	0.025
FR4 PCB dielectric	0.35
Mold compound	1
Solder	62
Silicon (die)	148
Aluminum	247
Copper	398

Table 1: Material Thermal Conductivity

Convection

Convection is the method of moving heat from a material's surface to the air. The temperature rise is a function of the power dissipated, and it is inversely proportional to the surface area and the heat transfer coefficient (h). h is a function of the air speed and the temperature difference between the board and the ambient air.

Radiation

Thermal radiation involves the transfer of heat via electromagnetic waves. The rate of heat flow is directly proportional to the surface area and to the temperature of the radiating element (e.g. board, component) to the fourth power.

Heat transfer via conduction is most applicable to semiconductors in high-power applications. The standard description of the IC package's thermal performance, θ_{JA}, is of little help in pulsed applications, and leads to a redundant and prohibitive thermal design.

Instead, the complete thermal impedance of a device can be modeled by combining two elements: the thermal resistance and the thermal capacitance.

Thermal capacitance (C_{TH}) is a measure of a component's ability to accumulate heat, similar to how a capacitor accumulates a charge. For a given structural element, C_{TH} depends on the specific heat (c), volume (V), and density (d). C_{TH} (in J/°C) can be estimated with Equation (4):

$$C_{TH} = c \times d \times V \qquad (4)$$

The electrical analogy for a given application's thermal behavior (consisting of an active device, package, PCB, and external ambient) is a chain of RC cells, each having a characteristic time constant (τ). τ can be calculated with Equation (5):

$$\tau = \theta \times C \qquad (5)$$

Figure 2 shows how each cell contributes to the transient thermal impedance of a packaged device using a simplified electrical model.

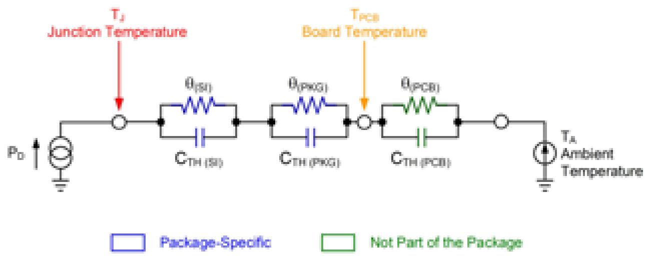

Figure 2: Simplified Equivalent Thermal Circuit

Pulse Power Operation

When a power device is subjected to a pulsed load, it can support higher peak power dissipation. Power packages have a definite thermal capacity, which means that the critical T_J is not reached immediately, even when excessive power is being dissipated in the device. The power dissipation limit may be extended for intermittent operation. The time length of the extension depends on the duration of the operation period (also known as the pulse duration) and the frequency during which operation occurs (also known as the duty factor).

If power is applied to a device, the die immediately starts to warm up (see Figure 3).

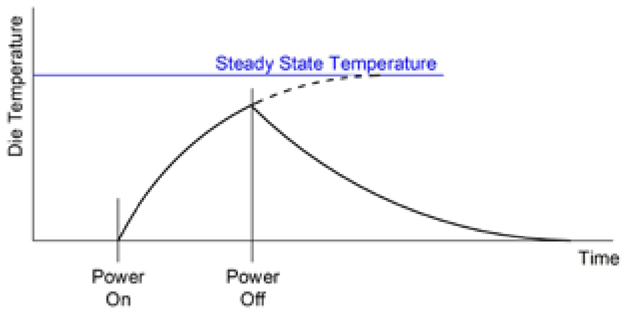

Figure 3: Die Heating/Cooling: Single Pulse

If the power continues dissipating, a balance is struck between heat generation and heat removal, which stabilizes T_J. Some heat energy is stored by the device's thermal capacity. The stable conditions are determined by the thermal resistances, which are associated with the transistor and its thermal environment.

When power stops dissipating, the device cools down, and the heating and cooling laws are identical (see Figure 3). However, if power dissipation stops before the transistor's temperature stabilizes, then the peak values of T_J are below the values that are reached for the same level of continuous power dissipation (see Figure 3).

If the second pulse is identical to the first, then the peak temperature attained by the device at the end of the second pulse is greater than the peak temperature at the end of the first pulse. Additional pulses build up until the temperature reaches a new, stable value (see Figure 4). Under these stable conditions, the device's temperature fluctuates above and below the mean.

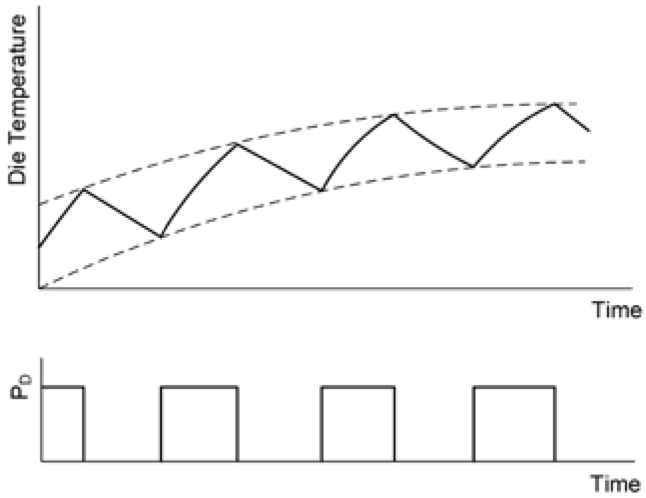

Figure 4: Die Heating/Cooling: Repetitive Pulses

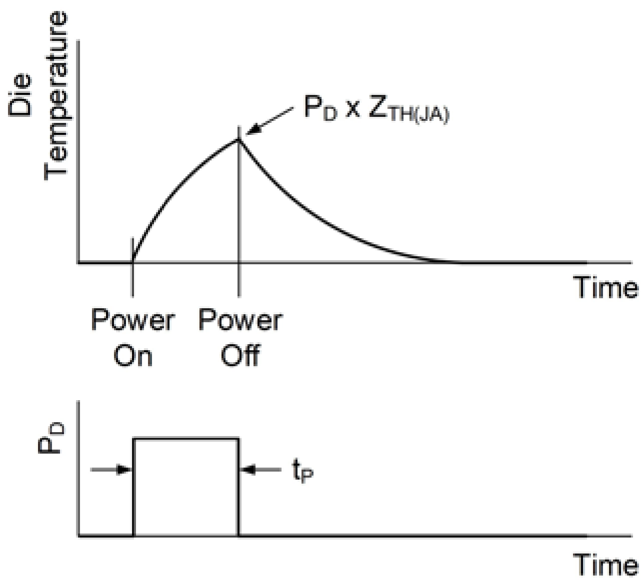

Figure 5: Short Single Power Pulse

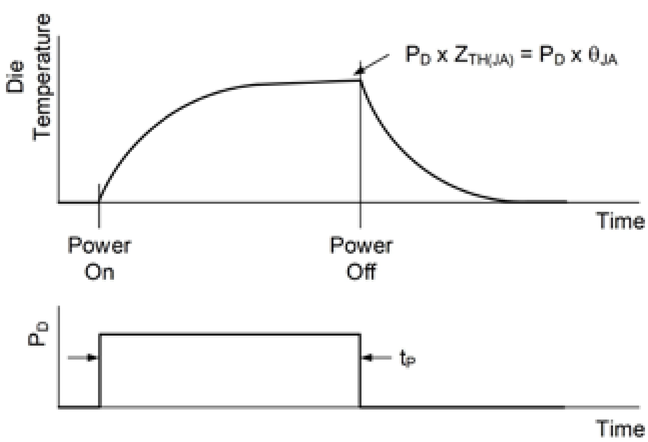

Figure 6: Long Single Power Pulse

If the junction temperature following a series of pulses becomes excessively high (e.g. T_J > 125°C), then the device may experience reduced electrical performance and life expectancy. This can occur with high-power pulses with low duty cycles, even when the average power is below the device's DC rating. Figure 5 shows a short, single power pulse.

As the pulse duration increases, TJ approaches a stationary value toward the end of a pulse (see Figure 6).

The thermal impedance ($Z_{TH(JA)}$) reflects the temperature rise produced by time-limited power pulses. This thermal impedance offers a simple way to estimate the device's junction temperature under transient power dissipation conditions.

The transient thermal impedance tends to become equal to the thermal resistance for continuous power dissipation, estimated with Equation (6):

$$\lim_{t_P \to \infty} Z_{TH(JA)} = \theta_{JA} \tag{6}$$

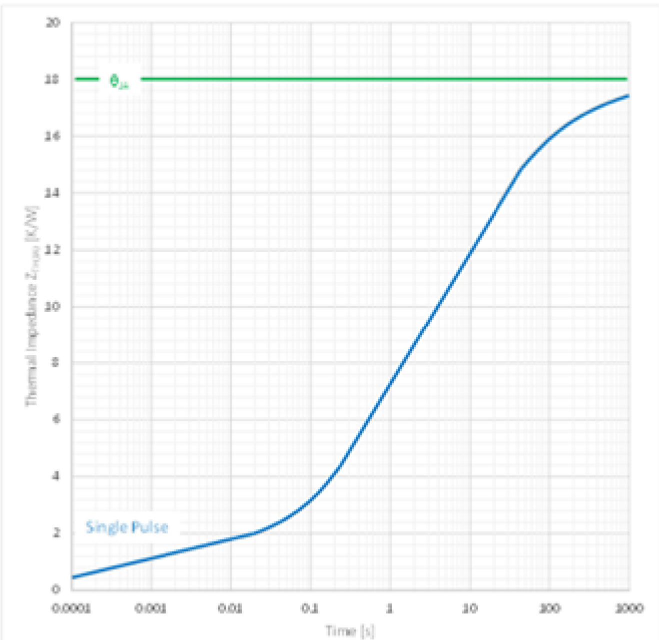

Figure 7: Transient Impedance $Z_{TH(JA)}$ vs. Time

As the repeat rate becomes smaller, the junction tends to cool down completely between pulses, so that each pulse can be treated individually.

For power packages, transient thermal effects die out within approximately 0.1 to 100 seconds. This time depends on the chip size, the package type, and size. In addition, it is greatly affected by the PCB stack-up and layout.

A PCB acts as a heatsink, providing path(s) for the IC package to effectively transfer heat to the board and the adjacent environment. Therefore, maximizing the area of the metal traces where the power and ground pin(s) of the package are located is important for effective heat transfer.

The package's thermal performance is not greatly affected by T_A and P_D. Power pulses with excessive durations during this time have an effect that is similar to a continuous load.

Conclusion

The junction temperature influences many operational parameters, as well as the device's operational lifetime. The most challenging aspect of designing a high-power circuit is determining whether a specific device can support the relevant application requirements.

The effective transient thermal impedance is influenced by many factors, including copper area and layout, heating from adjacent devices, the thermal mass of adjacent devices on the PCB, and airflow around the device. To accurately estimate temperature rise, it is best to characterize the thermal impedance directly in the application circuit.

If you want to learn more join Monolithic Power Systems´ webinar on 22nd of March 2023!

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Characterizing High Voltage Inductors and Magnetic Material via Triangular Flux Excitation

Measuring power inductors to obtain real-life, application relevant data is a challenge. The challenge further increases when using high voltages, such as in offline applications like PFC, electric vehicle inverters, fast-chargers.

By Mike Wens, CEO & Co-Founder, Jef Thoné, CTO & Co-Founder, and David Czajkowski, Strategic Business Development Manager MinDCet NV

The DC-losses are relatively easy to predict when the operating temperature and DC resistance are known. But to what extent are losses caused by the AC-component of the current? How do these AC-losses contribute to self-heating? Does the applied voltage cause other issues that impact reliability and lifetime? These questions can only be solved when measurement data is available. Generating such data in-turn requires a system that can apply real-life switching waveforms. HIGH-VOLTAGE MADMIX is the measurement system capable of characterizing such power inductors.

Figure 1 below shows the hardware of the HIGH-VOLTAGE MADMIX equipment, a software controlled, fully-automated test-bench for power inductors. A closeable cavity houses the inductor under test (LUT), protecting the environment and user from high-voltages and EMI.

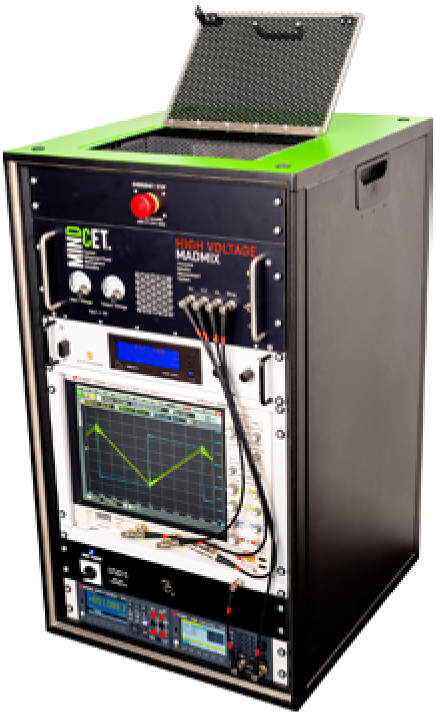

Figure 1: The HIGH-VOLTAGE MADMIX equipment

The HIGH-VOLTAGE MADMIX Principle

The principle of operation is shown in figure 2. It consists of a full-bridge DCDC converter, where the inductor L is the device under test (LUT).

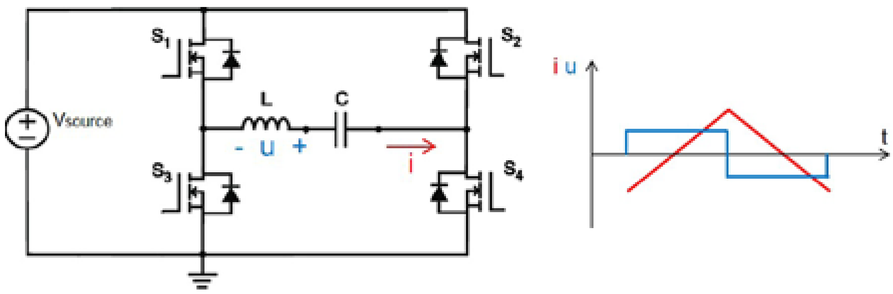

Figure 2: The HIGH-VOLTAGE MADMIX principle.

The LUT is subjected to a hard-switched, square-wave voltage which results in a triangular current and hence magnetic flux. The amplitude of the ripple current depends on the inductance, source voltage, frequency and duty-cycle according to the equation:

$$Irip = \frac{2 \cdot V_{source} \cdot \delta(1-\delta)}{f \cdot L}$$

Where V_{source} is the voltage source, δ is the duty cycle, f is the switching frequency and L is the inductance of the inductor under test.

In normal operation, a DC bias voltage is built across the series capacitor when the duty-cycle is lower or higher than 50%:

$$V_{DC} = V_{source}(2\delta - 1)$$

As a result, the inductor may see a voltage higher that the supply voltage according to:

$$\max(V_L) = V_{source} + \mathrm{abs}(V_C)$$

where V_L is the voltage across the LUT and V_C is the voltage experienced by the series capacitor.

By measuring the voltage over and current through the LUT in a very accurate fashion and by using a high-bandwidth, high-resolution digital oscilloscope, various parameters of the LUT can be revealed. Key parameters including the inductance, total AC losses, core loss, winding loss, saturation current, core breakdown voltage. As an example, the total AC losses are determined by calculating the integral of the LUT voltage and current and averaging them over multiple periods for higher accuracy.

$$P_{ac} = \frac{1}{T}\int_0^T i(t)\, v(t)\, d(t)$$

Key Specifications

The HIGH-VOLTAGE MADMIX uses state-of the art GaN switching technology and in-house developed drivers to enable switching the LUT with the following parameters:

- Voltage range across the inductor: 50V-800V
- Ripple current through the inductor: 50mA-60Aptp
- Frequency: 10kHz-2MHz
- Duty-cycle: 50%-95%
- Ambient temperature: -60°C-225°C

Very fast voltage transients up to 60V/ns are generated in this way, resembling state-of-the-art wide-bandgap applications, as shown in figure 3.

The above parameters allow for stressing even large inductors up to their limits. An example is a 75µH, 150A rated inductor, weighing about 3kg. Switching this part at 85kHz, 500V and 40Aptp, yields an AC power loss of 140W. This significant AC power loss is enough to reach a surface temperature of the inductor case to over 100°C in under 5 minutes, where the inductor had not yet reached thermal steady state.

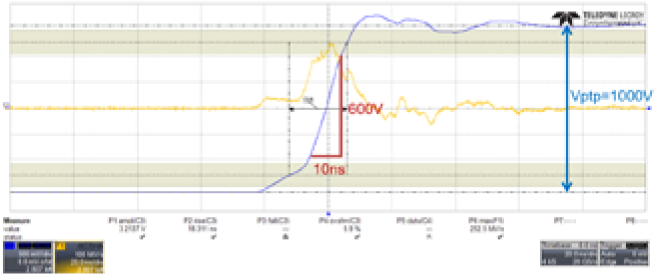

Figure 3: A real-life example of the fast switching transients that are used in HIGH-VOLTAGE MAMDIX, up to 60V/ns.

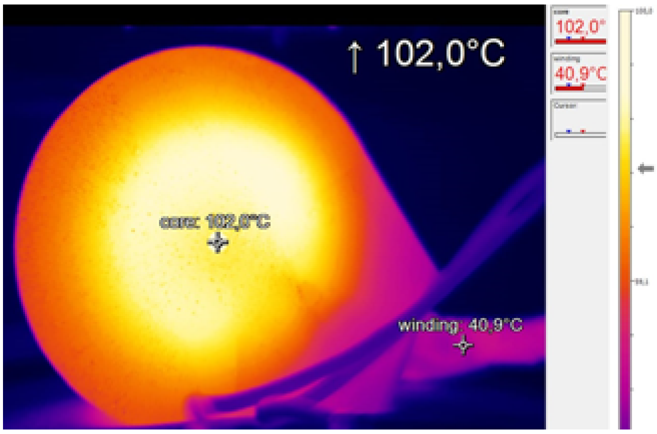

Figure 4: A 75µH, 150A rated inductor heated to 102°C in under 5 minutes by switching with the HIGH-VOLTAGE MADMIX equipment at 85kHz, 500V and 40Aptp.

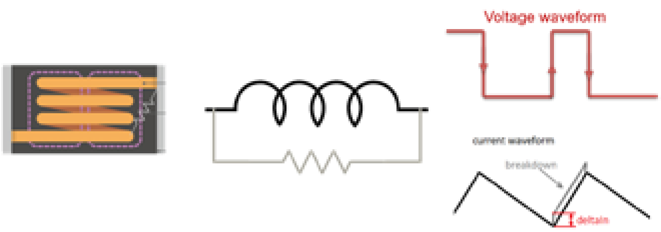

Figure 5: Inductor under core breakdown visualized by a leakage resistor to the inductor terminal (left) translated to an electrical equivalent model (middle) and the step effect visible on the triangular current (right).

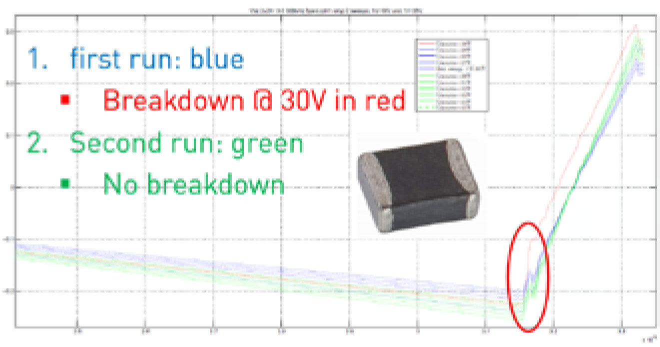

Figure 6: A real-life measurement showing a step in the LUT current from 30V onwards, indicating core breakdown.

Core Breakdown Voltage

An effect that is until today little known and understood is the breakdown of the inductor magnetic core as a result of the induced voltage differences within it. Indeed, under certain circumstances the magnetic core may start to conduct current. This effect can be modeled by imagining a parallel "leakage resistor" across the terminal of the inductor. As a result when excited under triangular flux, a step in the current waveform starts to show. This is depicted in figure 5.

The HIGH-VOLTAGE MADMIX is able to reproduce this core breakdown effect by applying hard switching while an incremental voltage is applied to the inductor to detect the moment of breakdown. An example of such a measurement is shown in figure 6. The current through the LUT starts to show a distinct step response from a certain voltage onwards, 30V in this case. Clearly, this is crucial information for both manufacturers and end-users.

The Added Value

The HIGH-VOLTAGE MADMIX measurement system allows performing an accurate prediction of the efficiency and overall performance of power inductor components in a wide range of growing applications like EV inverters, fast chargers, PFC and more. This way the performance of various commercial inductors and new inductor designs can be determined beforehand. HIGH-VOLTAGE MADMIX provides a clear insight into the important trade-off in designs, specifically cost, size, efficiency and overall performance. Furthermore, in some niche applications, there is often no standard off-the-shelf inductor that fulfills the application requirements. In such a case, HIGH-VOLTAGE MADMIX allows to prototyping power inductors with specific form-factors and large temperature ranges (up to 225°C). Additional capabilities such as core breakdown voltage detection bring deep insights to power inductor manufactures and researchers alike.

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How Thermal Efficiency Is Helping Data Centers Run More Sustainably

Innovative semiconductor design and packaging technologies are improving efficiencies in data centers as server power demands increase

Every time we stream the latest movie, talk to AI-driven voice assistance or attend a business meeting from home using a laptop computer, we're pushing large amounts of digital information through data centers and using resources that consume vast amounts of electricity. And that usage is only increasing.

By Les Stark, Director of QFN and SOT Package Development, and Robert Taylor, Applications Engineer, Texas Instruments

In 2022, the world created and consumed nearly 100 zettabytes – 100,000 billion gigabytes – of data. That incomprehensibly vast ocean of bits is projected to almost double by 2025.1 And increasingly, that data is running through hyperscale data centers, each filled with thousands of servers.

Estimates by the U.S. government place the energy demands of data centers at 70 terawatt-hours per year.2 Increases in blockchain mining alone have more than doubled that figure since then. Current data center consumption is likely accounting for at least 2% of total U.S. electric power consumption, according to the Center of Expertise for Energy Efficiency in Data Centers.3 That's enough to have a significant impact on the environment, which adds urgency to the goal of enabling data centers to run more sustainably.

As servers in these centers evolve to handle and process the exploding flow of data, the electric power consumed by each server is growing as well — from an average 1,500 watts per server in previous years to 3,000 watts in newer servers, said Robert Taylor, a systems manager with our company who specializes in industrial power management.

Achieving higher power densities and thus improved efficiency in server power supply units (PSUs) is one way to achieve more efficient data center operations.

There's an additional urgency to upgrade server PSUs, Robert said. The growing power demands of data centers are bumping up against a bottleneck: Most hyperscale data centers can't bring in more than 50 megawatts of electric power.

"Because the total amount of power is limited in these data centers, they need to waste as little power as possible on cooling and on losses due to inefficiencies in the electronics," Robert said.

At the same time, he said, the server industry is demanding smaller printed circuit board footprints to fit more computing power in each rack. That means the power components in servers have to become smaller and more efficient without producing excessive heat.

Our company has taken the lead in producing innovative semiconductor power products that meet the daunting performance, efficiency and thermal management demands of the current and future generations of leading-edge data centers. The resulting power supplies are helping keep even the largest data centers running smoothly with more sustainable footprints.

Handling higher power and temperatures

The key to high-performance, energy-efficient semiconductor power supplies is to achieve ever-higher levels of power density — that is, to pack more power-handling capacity into smaller volumes. But higher power densities also pack more heat into that reduced volume, and that requires advanced thermal management techniques to sustain performance and protect components.

The need for higher power density isn't unique to data centers. Electric systems from grid and communications equipment to electric vehicles and personal electronics also need the performance and efficiencies offered by denser, thermally efficient power chips.

Produce less heat with efficient packages

Our company is stepping up to the challenge of providing higher power density in server power supply chips. Small outline transistor (SOT) packages with integrated switches are expanding the boundaries of power densities and performance while lowering cost.

Advances such as these wouldn't be possible without innovative approaches to thermal management. There are three key areas we focus on to optimize thermal performance and break through power density barriers at the chip level: process technology, circuit design techniques and thermally optimized packaging.

Much of the heat produced in servers has come from power losses due to the conversion of incoming AC power at 400V down to DC power at 6V or less. Products such as the TLVM13630 power module use our Enhanced Hotrod™ Quad-flat No Lead (QFN) package technology with integrated field-effect transistors (FET) that deliver fast switching speeds and lower resistance to sharply cut those power losses, boosting chip efficiency and thus trimming heat.

"Any resistance in the silicon is inefficiency, and that's wasted power and extra heat," said Les Stark, director of QFN and SOT package development at our company.

To further cut losses that produce extra heat, our company is taking advantage of industry-leading capabilities such as integrating more components into power chips, including FETs and capacitors. That integration provides faster, more efficient switching with less noise, as with the TPS25985 eFuse with ultra-low on-resistance, delivering better thermal performance while achieving as much as 80A of current. In some cases, our company achieves higher integration through 3-dimensional stacking of components on the chip.

Remove heat effectively with thermally enhanced packages

Our company also has taken the lead in getting heat off of chips with innovative device packaging. For example, our company pioneered HotRod and Enhanced HotRod QFN packages that use a flip-chip style package to directly bond the surface of the chip and its connectors to the circuit board, instead of relying on bond wires to get signals in and out of the chip. That more direct connection is highly efficient at moving heat off the chip onto the board.

"This package design provides large ground pads that weren't previously possible, allowing good thermal paths from the devices into the printed circuit board," Les said.

Our company's other advanced approaches to removing heat include more effective heat-sink placement to achieve improved top-side cooling. Our gallium nitride (GaN) FETs employ top-side cooled packages, which will become increasingly important in data center systems as the drive to pack more computing power into each server leads to new, denser component arrangements that require more ways to get heat off of the chips.

"As GaN enables us to achieve ever-higher power densities, this sort of flexible approach to cooling will become all the more important," Robert said.

Any one of these efficiency-increasing and heat-removing approaches in a tiny chip can make a big contribution to thermal management and efficiency. By optimizing packages for both size and efficiency, we are helping solve data-center customers' heat problems and reducing environmental footprints.

Ressources:

[1] Source: https://www.statista.com/statistics/871513/worldwide-data-created/

[2] Source: Center of Expertise for Energy Efficiency in Data Centers - https://datacenters.lbl.gov/resources/united-states-data-center-energy-usage

[3] Source: Center of Expertise for Energy Efficiency in Data Centers – https://datacenters.lbl.gov/who-we-are

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Power Optimization Techniques for Low Power Signal Chain Applications

This article presents precision low power signal chain solutions and techniques for attaining optimized power efficiency in low power signal chain applications. It will explain techniques (beyond selecting low power products, which isn't always sufficient) such as power scaling, power cycling, and duty cycling to further reduce system power consumption.

By Lluis Beltran Gil, Product Applications Engineer, Analog Devices

Introduction

To keep going and going was an obsession for that little drum playing bunny in the advertisements decades ago. When designing a battery-powered measurement system for applications such as field instruments (sensing temperature, pressure, or flow) or remote vital sign monitoring devices, low power signal chains are critical. Even for mains powered systems, minimizing the environmental impact or the energy costs pushes hardware designers to improve system power efficiency. A low power design may have indirect benefits like a smaller solution size, if enabling to reduce the number of battery cells in parallel. A further advantage to the low power design is the lower IC die temperature due to the lower energy the system consumes. This extends product lifetimes.

Precision low power signal chains are a great starting point for getting a low power hardware design done in a short time. Beyond choosing low power components, several power optimization techniques such as power scaling, power cycling, and duty cycling can be implemented to further reduce the system power consumption. Also, design choices like appropriate resistor values or the use of memories can be a great differentiator for achieving stringent low power targets and optimal battery life.

For example, identifying building blocks in the signal chain that can be eliminated or powered down momentarily when certain conditions are met makes it possible to implement low power techniques. This will require a good timing analysis[1, 2] and staging or duty cycling the operation. If several building blocks are idling for the greatest portion of the time, then these can be placed into shutdown mode or directly switched off. Note that fully power cycling a device will have some implications in terms of power and timing, compared to using shutdown modes when available.

Once this timing is properly implemented, major system-level power consumption improvements can be achieved even further by minimizing the microcontroller interaction. This will require the use of memories, either external or internal, that can store data while the host controller is shut down.

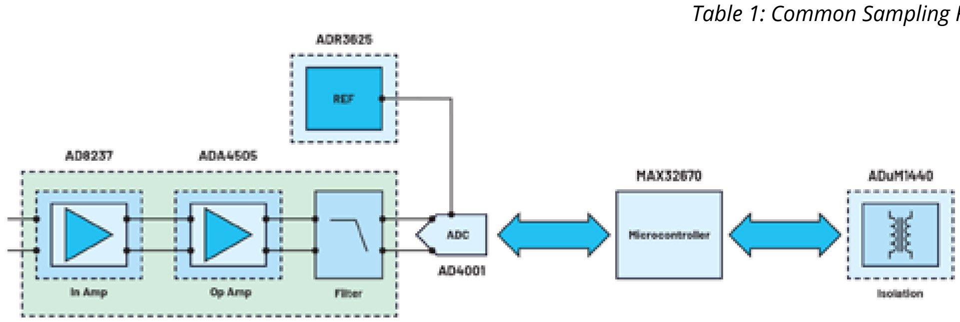

Figure 1: Single-channel voltage, current measurement in SAR ADC signal chain.

There are some differences on how to apply power saving techniques at the system level, depending on the type of ADC used for digitizing the sensor information, among SAR and sigma-delta, as detailed in the following sections. Also, hardware design decisions like digital comms pull-up/pull-down resistors, resistive dividers, and gain setting resistors will make a difference on the overall signal chain power consumption.

Pin naming may vary from device to device. For consistency, we will refer to AVDD for analog supply, VIO for digital supply, and VREF for reference voltage.

Power Optimization on a SAR ADC-Based Signal Chain

SAR ADCs perform conversions on demand—that is, they toggle from sample mode to hold mode[3] after assertion of the CONVERSION START command. The conversion process starts and, once completed, it toggles back to sample mode in order to acquire the signal. SAR ADCs like the AD4001 converter used in the signal chain shown in Figure 1 consume most of the power during the conversion phase, whereas consumption is minimal during the acquisition phase as shown in Figure 2. So, despite being capable of throughputs as high as a few MSPS, power can be greatly optimized by running these converters at the minimum speed required by the application.

SAR ADC: Power Scaling with Throughput

In many low power applications, sensor information is not needed continuously but at much lower rates, in the order of kSPS or tens of kSPS. In these cases, power consumption of the SAR ADC can be scaled down with throughput, both for analog and digital supply rails.

Application	Common Sampling Frequency
Field Instruments	60 SPS to 600 SPS
Condition-Based Monitoring	1 kSPS to 10 kSPS
Vital Sign Monitoring	<1 kSPS

Table 1: Common Sampling Frequencies at Different End Applications

Most precision SAR ADCs have an internal clock that manages the conversion process, so the conversion time (t_{CONV}) is fixed. With t_{CONV} being fixed, the lower the throughput and longer the cycle time (t_{CYC}), the longer the acquisition time (t_{ACQ}), which is the period where the ADC minimizes its power consumption. In other words, the lower the throughput rate, the lower the power consumption per sample acquired.

As conversions are triggered externally through a digital signal, the conversion speed can be tightly controlled. A slower sampling rate results in a longer acquisition phase and therefore a lower average power consumption. This can be observed in Equation 1:

$$ADC_{POWER} = P_{V_{DD}} + P_{V_{IO}} + P_{V_{REF}} =$$
$$= V_{DD} \times \frac{I_{DD} \times t_{CONV} + I_{STDBY} \times (t_{CYC} - t_{CONV})}{t_{CYC}} + \quad (1)$$
$$+ V_{IO} \times I_{IO} \times \frac{n_{BITS} \times t_{SCLK}}{t_{CYC}} + V_{REF} \times I_{REF} \times \frac{1/max\_tput}{t_{CYC}}$$

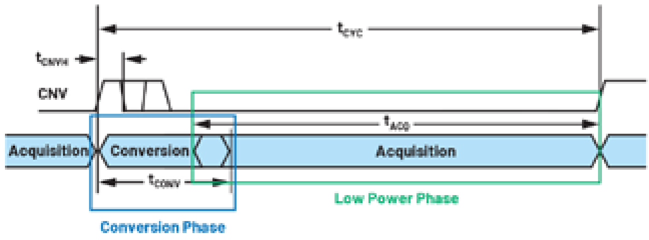

Figure 2: An SAR ADC timing diagram.

Where:
- t_{CONV} is the conversion time
- t_{CYC} is the inverse of the sampling rate
- V_{DD} is the analog supply
- V_{IO} is the digital supply
- n_{BITS} is the resolution of the ADC
- t_{SCLK} is the serial clock period time ($1/f_{SCLK}$)
- V_{REF} is the reference voltage and I_{REF} is the current at maximum throughput (max_tput)

So the ADC average analog power consumption will be inversely proportional to the sampling rate, according to Equation 1 and as seen graphically in Figure 4, if t_{CYC} is extended while t_{CONV} remains constant.

The power consumption of the ADC shown in Figure 1 is dominated by the analog supply during its conversion phase, as shown in Figure 2. For example, in a strain gage sensing circuit, the data acquisition rate can be as low as 1 kSPS, which allows the reduction of power consumption by 20-fold compared to running the AD4001 at maximum sampling speed.

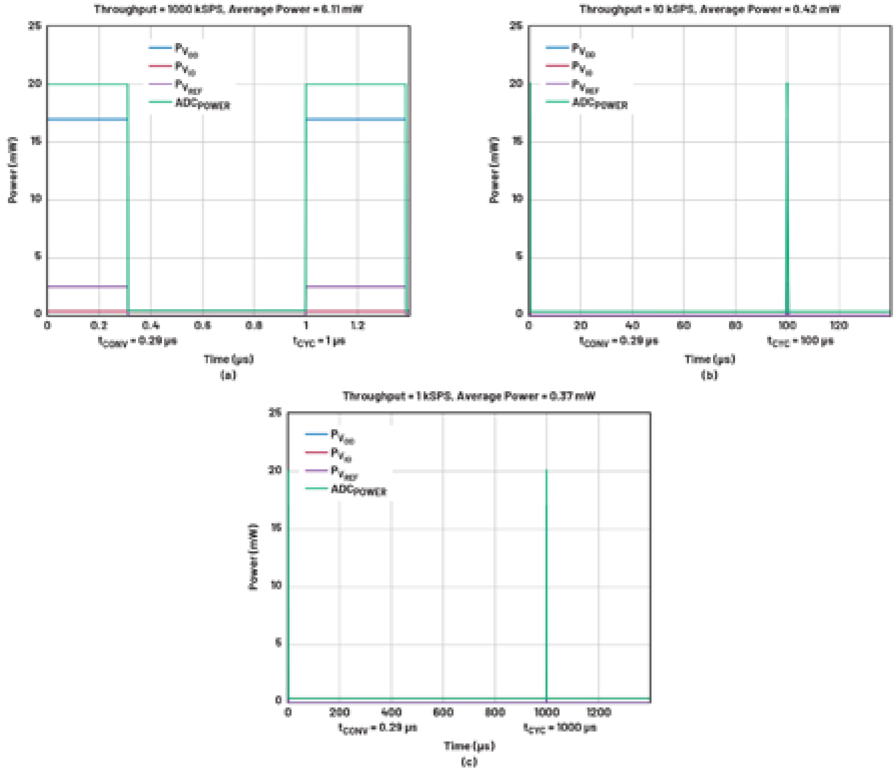

Figure 3: AD4001 SAR ADC timing diagram and power consumption during one cycle. The longer the cycle time, the lower the average power consumption: (a) avg. power = 6.1113 mW at 1 µs, (b) avg. power = 0.93756 mW at 10 µs, (c) avg. power = 0.36845 mW at 1 ms

AD4001 Throughput Rate	Total Power Consumption
1 kSPS	300 µW
10 kSPS	400 µW
1 MSPS	6 mW

Table 2: AD4001 Power Scales with Throughput

A graphical representation of Equation 1 shows how the power increases exponentially with throughput, as shown in Figure 4.

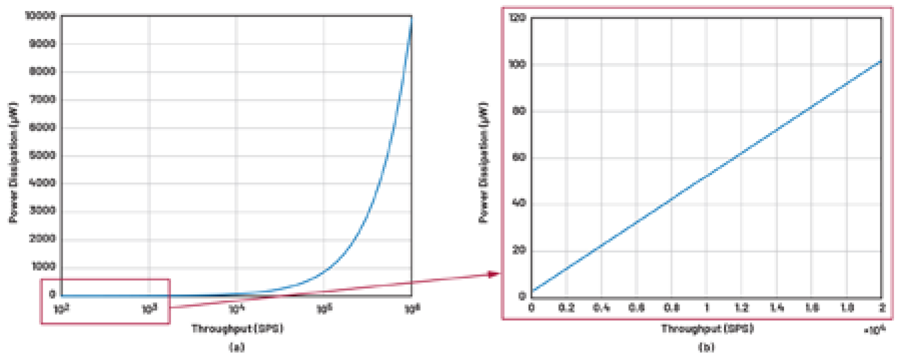

Figure 4: (a) AD4001's power scaling with throughput, graphical representation of (b) zooming in for the frequency range of interest—that is, under 10 kSPS.

Reducing the ADC sampling rate results in longer acquisition time, which reduces the bandwidth requirements of the ADC driver amplifier, allowing a larger base of devices to choose from. Lower bandwidth amplifiers tend to have comparatively lower quiescent current. So lower ADC sampling rates not only lower ADC power consumption but also lower power requirements for companion amplifiers.

$$P_Q = I_Q \times (V_+ - V_-) \quad (2)$$

Op Amp	Bandwidth	I_Q	e_N
ADA4897-1	90 MHz	3 mA	1 nV/√Hz
ADA4610-1	16 MHz	1.6 mA	7.3 nV/√Hz
MAX40023	80 kHz	17 µA	32 nV/√Hz

Table 3: Operational Amplifier Bandwidth vs. Current Consumption and Noise Performance; Bandwidth and Power Are Inversely Proportional

However, selecting a lower bandwidth operational amplifier has its trade-offs. The lower bandwidth means a lower quiescent current (I_Q) but it comes at the expense of increasing the voltage noise density (e_N), as shown in Table 3. As a rule of thumb, lowering the quiescent current implies that the noise density increases at a ratio of $1/\sqrt{I_Q}$. However, note that the rms noise will be filtered by the adjusted bandwidth. In other words, a hardware designer might trade off power consumption (or battery life) vs. rms noise performance for the given sample rate, amplifier, and RC net bandwidth.

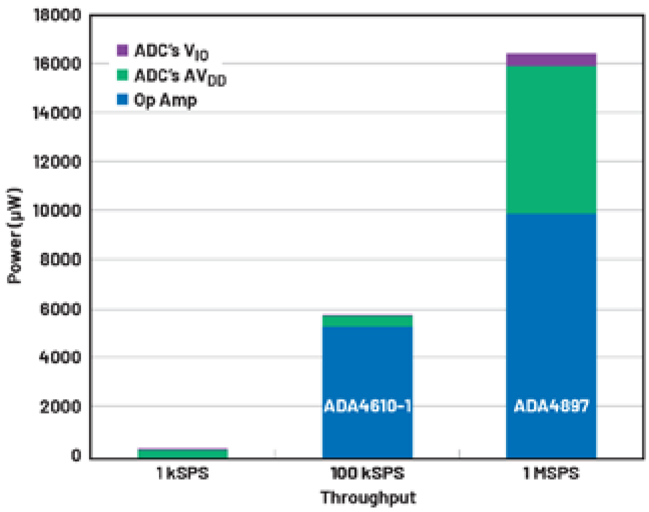

Figure 5: Power distribution per supply rail (op amp, analog, and digital rail), at various throughputs; different amplifiers were used depending on the bandwidth needs, as per Table 3.

Furthermore, the feedback resistors used to set the operational amplifier gain will impact power consumption as well: the larger these resistors are, the less power they will consume. This, again, comes with a noise trade-off as larger resistors generate more noise. A good design practice is to make the resistors as large as possible but not large enough that their contribution to the total noise is substantial. As individual noise contributions are root sum squared for obtaining total noise, following a common rule of thumb would lead us to set a maximum limit for resistor noise rms of 1/3 of that of the op amp, in order to keep their noise contribution less than 5% of the total. This would keep op amp noise dominant.

In some applications, where low frequency input signals are sampled at low throughput rates (a few kSPS), like the ones shown in Table 1, the driver amplifier could be removed, as long as no signal conditioning like a gain stage or low output impedance is needed. In higher speed applications, newer ADCs like the AD4000 or AD4696 families offer high input impedance (high-Z) modes that allow lower bandwidth (and lower power) amplifiers to drive the analog inputs, sometimes even eliminating the driver altogether. Removing this op amp will also contribute to minimizing total power consumption by eliminating its contribution, as indicated by the blue bar portion shown in Figure 5. This results in significant power savings compared to the use of traditional SAR ADCs that almost always requires a driver amplifier. In the case of the AD4696, a 16-channel device, this power savings is multiplied by 16 times. The reference high-Z mode feature also reduces the reference input current, and hence the overall system power consumption.

SAR ADC Signal Chain: AFE Dynamic Power Scaling

As described in the previous section, SAR ADC power consumption inherently scales with sample rate, but this is not true for other signal chain components. Amplifiers and voltage references consume constant quiescent current while they are powered up. Power cycling these components between ADC samples reduces the average power consumption of the signal chain. Having to wait for signals to be settled on every power cycle limits the time left for powering the system on and off. This is well explained in "What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 1" and "What Are the Most Important Timing Factors for Low Power Precision Signal Chain Applications? Part 2" (although an accurate analysis for each particular signal chain design is recommended).

Using highly integrated ADCs, with more analog front-end (AFE) blocks on chip, enables faster power-up and power-down transitions without compromising the performance. However, in many scenarios, a design may end up using discrete components for optimal performance. An example is shown in Figure 6.

This signal chain is multichannel and is comprised of one MAX41400 plus one antialiasing filter per channel, feeding into a 16-channel SAR ADC (the AD4696) with an ADR3625 precision reference.

As shown in the previous section, running the ADC at the lowest acceptable throughput reduces its power consumption. Beyond that, if the idle time is large enough, the MAX41400 can be put into shutdown mode during a portion of the acquisition time, given that for a multiplexed system like this, only one amplifier needs to be powered up at a time. The frequency at which the amplifier, MAX41400, needs to be powered up is t_{CYC}/L_{SEQ}, where L_{SEQ} is length of se-

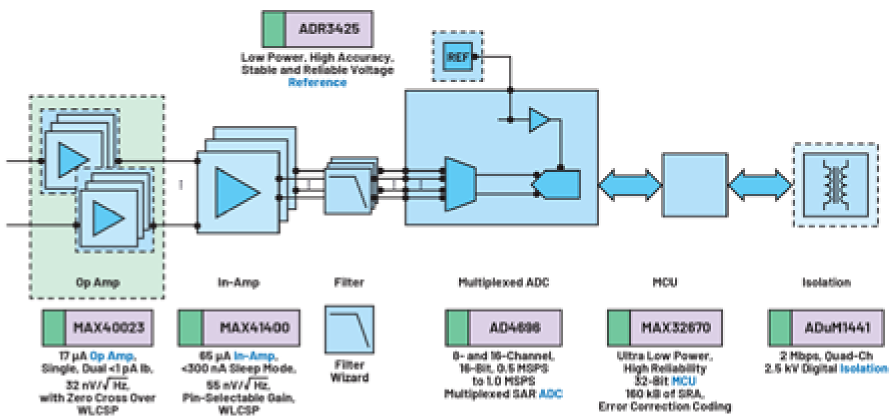

Figure 6: A multichannel measurement signal chain.

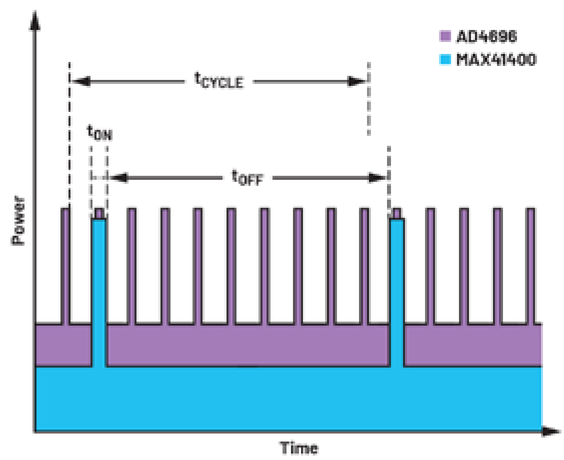

Figure 7: Power cycling the MAX41400 in a multichannel multiplexed application, based on the AD4696 ADC (assuming only 10 channels are in use for easier visualization).

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quence, which is 10 in the example given in Figure 7. For example, if running conversions at 1 kSPS per channel and the conversion time is a maximum of 415 ns, that means the MAX41400 on each channel can be placed into shutdown mode for around 10% of the cycle time.

The quiescent current (I_{Q_ON}) of the MAX41400 is 65 μA when fully powered up, but it can be reduced to 0.1 μA when placed into shutdown mode (I_{Q_OFF}). By powering it down in between samples, the average current consumed (IAVG) by the amplifier can be scaled with throughput.

$$I_{AVG} = I_{Q\_ON} \times \frac{t_{ON}}{t_{CYC}} + I_{Q\_OFF} \times \frac{t_{CYC} - t_{ON}}{t_{CYC}} \quad (3)$$

Once again, the slower the throughput, the higher the t_{CYC} and lower the I_{AVG}. t_{ON} is the time during which the amplifier is turned on. When the ADC switches from acquisition to conversion phase, the amplifier can be powered off, as extending t_{ON} longer than the minimum required does not yield any benefit. This off-time ($t_{OFF} = t_{CYC} – t_{ON}$) should be maximized for minimum power consumption, just not to the extent of compromising SNR or THD. Finding the right timing will depend on the application, the devices used, and the throughput rates. In fact, t_{ON} and throughput are maybe inversely proportional: lower throughputs lead to longer idle time, and longer idle time requires longer t_{ON} to power the amplifier back up. Based on the data sheet, the typical conversion time of the AD4696 is 415 ns. This conversion time plus the 100 μs required to power up the MAX41400 after shutdown will add up to the minimum t_{ON} time. So the average current consumption will be:

$$I_{AVG} = 65\ \mu A \times \frac{100.5\ \mu s}{1000\ \mu s} + 0.1\ \mu A \times \frac{899.5\ \mu s}{1000\ \mu s} = 6.62\ \mu A \quad (4)$$

Compared to an amplifier that is always enabled, the shutdown modes and fast power-up time of the MAX41400 result in a 10× reduction in current consumption.

For a more general view, besides power savings calculated on the examples shown so far at a given throughput rate, all these equations can be represented graphically as in Figure 9, with the specifications taken from the data sheets (assuming reference and analog input high-Z mode are enabled).

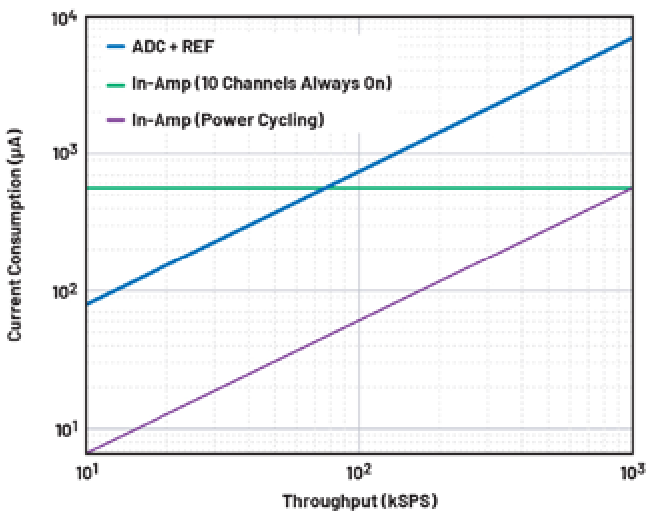

Figure 8: Signal chain power consumption vs. throughput, with and without power cycling at the front end.

This same analysis can be done for battery life, as opposed to power consumption, by dividing the battery capacity by the average current drawn.

Battery	Capacity (mAh)
CR927	30
2× LR44	158
2× AAA	1000
CR2354	560

Table 4: Batteries' Capacity

In this case, the relationship is inversely proportional—that is, the lower the throughput, the longer the battery will last.

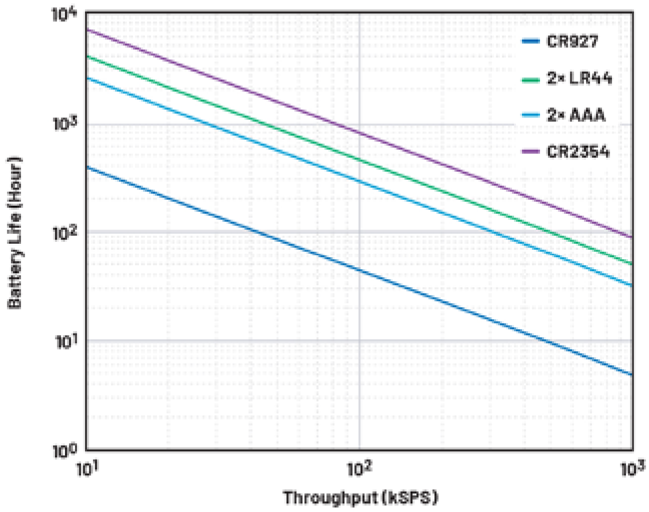

Figure 9: Battery life extends with power cycling/scaling.

Any amplifier, even if it does not have a shutdown mode like the MAX41400, can be power cycled like shown earlier. That is, powering it on and off completely instead of entering shutdown mode. However, care must be taken. On one hand, the wake-up time will be longer to get the amplifier ready, so the minimum t_{ON} will be longer. On the other hand, charging and discharging the decoupling capacitors over and over again will have implications on the current drawn to charge them up every power cycle, increasing the overall power consumption compared to using shutdown modes. Also, if the sensor is still driving the amplifier inputs while the rails are not powered up, this may lead to damage if they are unprotected.

SAR ADC-Based Signal Chain: Digital Supply Power Scaling

The previous section focused on reducing the analog supply power consumption, given it is the maximum contributor to the total power consumption. Reducing the throughput also has an impact on the digital power consumption as it allows the serial clock to run at a lower frequency:

$$I_{IO} = C_{SDO} \times V_{IO} \times f_{SCLK} \quad (5)$$

Equation 5 indicates that there are two extra potential steps we can take to minimize digital power consumption:

- Use a lower digital supply voltage (VIO)
- Minimize the trace capacitance of the serial data output line

Another point to note is the value of the pull-up/pull-down resistors used in the digital communication lines. These resistors are used to ensure a proper logical level at the digital input/output, and their value may have an impact on the overall system power consumption. Using too low a resistor value, also known as strong pull-up, will cause a high current to flow through it. Hence, unnecessarily low values should be avoided. On the other end, if the resistance is too high, the voltage drop caused by the leakage current could result in the interpretation of an incorrect logic level. In addition, the voltage drop impacts the propagation. So designers must use

the highest resistor value without compromising the voltage level (this will depend on the digital supply voltage and leakage current) or the signal integrity.

Sigma-Delta ADC-Based Signal Chain

In the case of sigma-delta ADC-based signal chains, the power scaling concept described in previous sections is not applicable straight away. This is because the conversions are not externally triggered, but rather they work from a free running clock.[4] So they cannot remain idle for a certain period of time as a function of an external conversion start signal.

However, many sigma-delta ADCs feature standby modes that can be used if the ADC does not need to convert continuously. As in previous sections, timing considerations[5] need to be taken into account as recovering the device from standby mode requires a wake-up time during which no samples can be taken.

Highly integrated sigma-delta ADCs like the AD4130 offer duty cycling modes in addition to standby modes. That way, the ADC powers up and down automatically without the need to interact with the host every cycle. The AD4130 offers two modes, 1/4 and 1/16, which means it is active during 1/4 or 1/16 of the time. That leads to significant power reduction compared to continuous conversion mode, as shown in Figure 10.

AD4130 Power Mode	Typical Current Consumption
Continuous Conversion	32 µA
Duty Cycling	5 µA
Shutdown Mode	0.5 µA

Table 5: AD4130 Current Consumption for Each Power Mode

Depending on the required throughput rate, techniques for optimizing power consumption can be either using one of the duty cycling modes, or just putting the part into standby mode for a given period. Indeed, the AD4130 has many operating modes that may impact power consumption of the ADC. The active functional model available in ACE[6] shows the power consumption and the expected battery life for the selected ADC configuration.

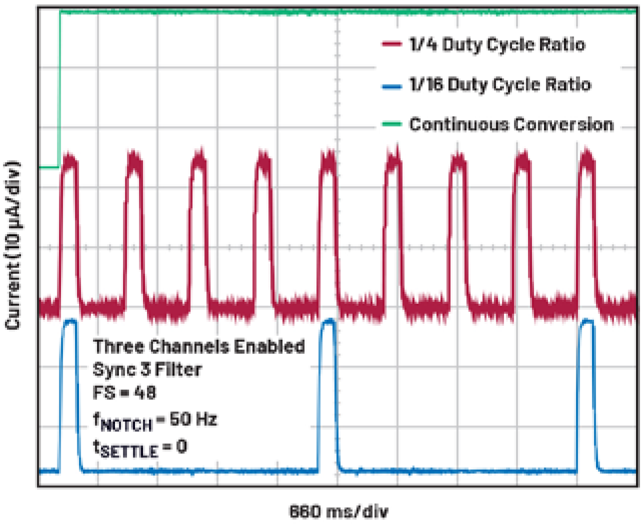

Figure 10: AD4130 current consumption under different modes of operation: continuous conversion, 1/4 duty cycle, and 1/16 duty cycle.

Sigma-Delta ADC-Based Signal Chain: AFE Dynamic Power Scaling with Duty Cycle

Just as with the SAR ADC-based signal chain, a sigma-delta-based signal chain can take advantage of the duty cycle to power down certain blocks during the time the ADC is placed into low power state (Figure 10). That would allow AFE power savings similar to the ones shown in Figure 9.

Sensor Excitation

Complete solution devices like AD4130 provide not only the core converter but also the internal programmable gain amplifier plus sensor biasing and excitation (selectable current source and precision voltage reference). This integration has implications in terms of ease of use, size, and optimization on the use of biasing, timing, or power cycling among the different building blocks. So, AD4130 on its own reduces the overall system power consumption by housing all these blocks on chip. Furthermore, it simplifies the design cycle thanks to its flexibility to be used in many different platforms like RTD, thermistor, or bridge sensors, to name a few. It also reduces the BOM count and the need for several power supply rails.

Other Power Optimization Techniques

Throughout this article, several ways for minimizing the signal chain power consumption have been presented. However, one portion of the signal chain has not been considered yet: the host controller. If the controller is powered up all the time because it needs to read and postprocess data from the ADC, it is going to sink a good portion of the power. Placing the controller into sleep mode while not in use will help achieve extra power savings.

ADCs with On-Chip FIFO

If the application does not need real-time data, but must read data points at much lower rate, ADCs with on-chip FIFO might play a role. The AD4130 incorporates such a block and this FIFO can store up to 256 conversions, so if the output data rate (ODR) is, for example, 2.4 kSPS, instead of reading every 416 µs, the microcontroller can be put to sleep mode and wake up every 100 ms to read the whole data memory in one go (see the Data Transfer section in Figure 11). In other words, having an ADC with memory that stores up to the latest 256 samples enables power cycling of the microcontroller too, thereby drastically reducing the overall system power consumption.

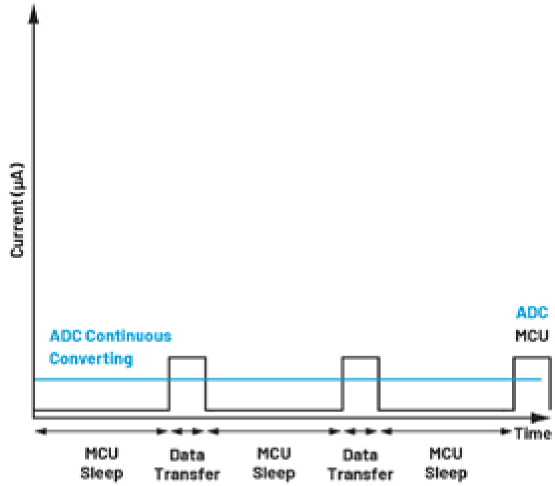

Figure 11: Microcontroller power reduction by using the ADC's on-chip FIFO.

Streaming ADC Data to Memory Through Direct Memory Access (DMA)

For ADCs that do not include on-chip FIFO, an alternative would be to use the direct memory access (DMA) available in most microcontrollers. DMA enables passing of data directly from a peripheral (in this case, the SPI) to memory (SRAM) without CPU intervention or interrupts for every single ADC sample received. The chosen microcontroller will have a direct impact on the achievable power savings. In many cases, the microcontroller will be able to stay in sleep mode most of the time and trigger an event only when an ADC sample is received. This event will then just briefly alert the DMA to start performing the SPI transactions and to return to sleep thereafter, thus minimizing the microcontroller power consumption compared to having the CPU fully awake for the whole SPI transaction. Note that using the DMA is only applicable if the format of the ADC data matches the destination memory. That is, for most microcontrollers, the DMA can be easily used only when the ADC data is 16 or 32 bits long.

Interrupt-Driven Programming

Many low power applications do not require the recording and processing of every single data point, but rather monitoring that the magnitude sensed is within certain thresholds. Traditionally, to do this, the host controller needed to be always awake in order to read each ADC sample and decide if the value was acceptable or not, then consequently, it would trigger an interrupt routine if need be.

Both the AD4696 (SAR ADC) and AD4130 (sigma-delta ADC) incorporate these threshold detection functions. Thresholds can be programmed such that a GPIO pin asserts only if the ADC output code is out of the user-defined bounds. This way, the host controller can stay in sleep mode most of the time and only wake up when the GPIO asserts, minimizing its power consumption given it will only be active when it is necessary to perform an action.

Conclusion

When designing a battery-powered measurement system, for applications such as portable field instruments, condition monitoring, or vital sign measurements (VSM), low power signal chains presented in analog.com/precisionlowpower are ideal for achieving power optimized solutions. Analog Devices' precision low power signal chains ease the journey for designers building low power measurement solutions, which offer the optimal combination of precision amplifiers, voltage references, ADCs, and isolation products. In these signal chains, power consumption is optimized while keeping noise performance, size, and ease of use as key vectors. These signal chains come in different flavors: single-channel, discrete multichannel (multiplexed), and also fully integrated multichannel solutions and ready-to-go power optimized designs, offering an excellent starting point for low power design.

Beyond presenting ADI's precision low power signal chains, this article demonstrated several system-level techniques that make the designed signal chains even more power efficient. Such techniques include power scaling, power cycling, duty cycling, or using on-chip features like FIFOs or interrupt-driven features like threshold detection.

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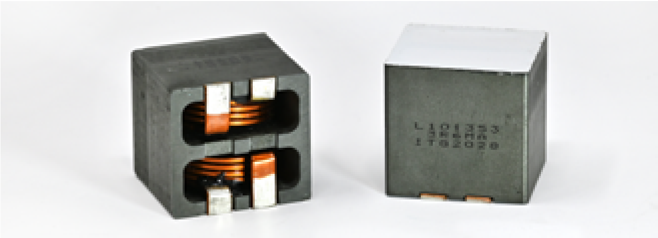
Non-Coupling Dual Inductors

ITG Electronics has introduced an updated version of its non-coupling dual inductors. The enhanced component is part of the company's L101353A Series of ferrite-based flat wire inductors, whose members range from 1.0-10.0uH. ITG Electronics' non-coupling dual inductor is designed for power conversion applications with current ratings from 14-170Amp at 25C and 20% inductance drop. The component has a low DC resistance (DCR) of 1.06mOhm, and IRMS up to 50Amp. The box-style surface mount device (SMD) inductors provide lower core loss and high current output – ideal for settings involving high density and limited board space. The non-coupling dual inductors are designed for 48-volt direct power conversion, offering high performance and premium efficiency in demanding data center environments. At a maximum height of 24mm, the component offers a low profile; it is also not particularly wide or deep, with a footprint of just 24.5 x 26mm.



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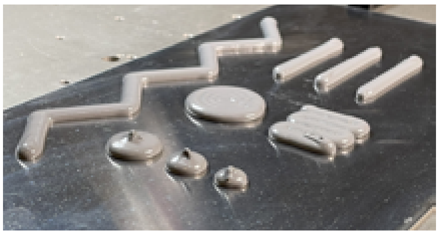
Non-Silicone, Dispensable Thermal Gels

The Chomerics Division of Parker Hannifin has unveiled THERM-A-GAP™ GEL 40NS, the next iteration in its line of silicone-free, thermally conductive gels. This one-component, low-outgassing material features a special formulation to meet the stringent requirements of silicone-sensitive applications such as optical equipment, camera modules, high-performance sensors and data storage devices. Offering heat-transfer performance of 4.0 W/m-K thermal conductivity, users of THERM-A-GAP™ GEL 40NS will discover a thermally reliability material in an ultra-low compression force package: it deforms easily under assembly pressure, minimising stress on components, solder joints and leads. The fully cured and dispensable product requires no mixing and maintains the traditional advantages of Parker Chomerics' line of thermal gels, providing seamless integration into high-volume, automated assembly applications, as well as rework and field repair situations. THERM-A-GAP™ GEL 40NS reliably conforms to rough surface irregularities, displaces air gaps and takes up manufacturing tolerances on heat-generating components. The product provides very low thermal impedance at bond lines as thin as 0.15 mm (0.006"). Requiring no secondary curing, THERM-A-GAP™ GEL 40NS is the ideal solution for applications that must reduce the risks associated with silicone oil migration or contamination, or for devices manufactured in silicone-free facilities.



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EMC Partner is offering an impulse insulation tester 1.2/50 µs from 500V to 30kV with integrated breakdown detection directly on generator or remote on the test object. Colour touch panel control with data collection and reporting are included. Optional impedances up to 5kΩ. The INS-1250 family of impulse insulation testers is designed for material insulation, components and electrical equipment safety in both development and production environments. The device features high accuracy internal or external measurement systems, programmable to detect breakdown with pass/fail criteria based on voltage and current impulse integral. Personnel safety is ensured through an emergency stop, warning lamp and test cabinet, disabling high voltage circuits when activated.

www.emc-partner.com

105 °C Prismatic Aluminum Electrolytic Capacitor Series

Cornell Dubilier has released a series of Flatpack, low-profile aluminum electrolytic capacitors, tested and rated for 10,000 hours at 105 °C. Type MLPS offers high capacitance density in a flat configuration, with voltage ratings up to 450 Vdc and a temperature range from -55 °C to 105 °C. Their rugged construction provides extraordinary life and reliability for the most robust, commercial, and military-grade power supplies.

MLPS capacitors are available in 4 sizes. All cases have a thickness (height profile above the board) of 0.6 inches and a width of 1.8 inches. Case lengths are available from 1.5 to 3.0 inches, with capacitance values ranging from 120 to 51,000 µF and voltage ratings spanning 7.5 Vdc to 450 Vdc. The larger case sizes are typically rated for several amps (RMS). Ripple current ratings can be significantly enhanced by adding one or more heat sinks to their flat sides. Unlike conventional electrolytics that have a rolled cover, MLPS covers are laser-welded, providing near-hermetic seals that resist electrolyte dry-out. They can be put into service at high altitudes of up to 80,000 feet and have excellent capacitance retention at low temperatures. Various lead types and mounting options are available.

www.cde.com

Space Level SMD Inductor

Ideal for space and aerospace applications, the S0603 inductor offers temperature stability, High Q and Ultra High SRF values, Low Outgassing Properties and an Operating Temperature Range of -55 to +125 C degrees (higher operating temperatures available) - all in a small rugged package. The company's environmental testing lab conducts load life, thermal shock, powdered burn-in, short time overload, real time x-ray, and extreme tempera- ture testing to guarantee the S0603's reliability in challenging environments. It's manufactured in a cleanroom and rigorously tested to MIL-STD-981 for the high performance criteria demanded in space flight.

www.delevan.com

Current Transducer for Automotive (EV) Test Benches & Battery Testing

Danisense announced the release of its latest current transducer mainly aimed at automotive (EV) test benches and battery testing & evaluation systems. Featuring a very large aperture of 41.2mm, the DN1000ID current transducer enables power cables with large power connectors to be easily fitted to EV test benches allowing for quick changeovers. The large aperture is an important advantage as test bench operators often face the issue that the power connectors fitted to the power cables are bigger than the diameter of the cable, making it difficult to fit them in the aperture of the current transducer and often requiring additional work to solve this issue. Comments Loic Moreau at Danisense: "Our new DN1000ID device now offers the best compromise between the 1000A nominal current and aperture size by keeping the best measuring performances in accuracy and phase shift."

Like all Danisense products the DN1000ID current transducers benefit from the high stability closed loop fluxgate technology. Further technical details include a linearity of 1 ppm, 5 ppm offset and a compact aluminium housing. Additional target applications for the product are power measurement and power analysis, MPS for particle accelerators, gradient amplifiers for MRI devices, precision drives as well as current calibration purposes.

www.danisense.com

Gate Driver IC Integrates Power Management Unit, Current Sense Amplifier, and Overcurrent Protection

To further expand its family for automotive and industrial motor control applications, Infineon introduces the MOTIX™ 3-phase gate driver IC 6ED2742S01Q. The 160 V silicon-on-insulator (SOI) gate driver features an integrated power management unit (PMU) and is available in a QFN-32 package with a thermally efficient exposed power pad. This makes the easy-to-integrate device ideal for battery-powered industrial BLDC motor control drives including cordless power tools, robotics, drones, and light electric vehicles (LEVs).

The 6ED2742S01Q has integrated bootstrap diodes that power three external high-side bootstrap capacitors. Through a trickle charge pump, they support 100 percent duty cycle operation. Protection features include under-voltage lock-out, overcurrent protection with configurable

threshold, fault communication, and automatic fault recovery. The output drivers integrate a high-pulse current buffer stage designed for minimal driver cross-conduction. In addition, a current sense amplifier (CSA) with selectable gain between the low-side supply voltage (V SS) and the low-side power ground return (COM) is integrated. The MOTIX gate driver provides a 1 A source and 2 A sink current with independent under-voltage lock-out (UVLO) for both high-side and low-side gate drives. The device offers a propagation delay of 100 ns and a minimum dead time of 100 ns with built-in delay matching. As a result, the driver enables high switching frequencies with reduced level shift losses.

www.infineon.com

Air Core Inductors Feature Miniature Size and Low Inductance

Richardson RFPD announced the availability and full design support capabilities for AL Series and AS Series of air core RF inductors from KYOCERA AVX. Part of KYOCERA AVX's wound air core inductor family, these devices feature SRF, high Q, high current, miniature size and low inductance. They are ideal for RF circuits, broadband I/O filtering, frequency selection and impedance matching.

The AS Series features a square cross section that provides better performance and offers manufacturing advantages over toroidal coils.

www.richardsonrfpd.com

Laser Driver IC for Lidar Systems

EPC announces the introduction of the EPC21701, a laser driver that monolithically integrates an 80 V, 40 A FET with gate driver and 3.3 logic level input into a single chip for time-of-flight lidar systems used in robotics, surveillance systems, and vacuum cleaners. It is tailored to lidar systems for gesture recognition, time of flight (ToF) measurement, robotic vision, or industrial safety. The EPC21701 laser driver uses 5 V supply voltage and is controlled using 3.3 V logic. It is capable of very high frequencies greater than 50 MHz and super short pulses down to 2 ns to modulate laser driving currents up to 15 A. Voltage switching time is less than 1 ns and delay time from input to output is less than 3.6 ns. The EPC21701 is a single-chip driver plus GaN FET using EPC's proprietary GaN IC technology in a chip-scale BGA form factor that measures only 1.7 mm x 1.0 mm x 0.68 mm. The wafer level packaging is small, low inductance, and lays out very well with the laser system. With this small form factor and the integration of several functions, the overall solution is 36% smaller on the printed circuit board (PCB) compared to an equivalent multi-chip discrete implementation.

www.epc-co.com

High Current Inductor for Automotive Applications

Würth Elektronik introduces another AEC-Q200 certified SMD inductor: WE-XHMA features a high current capability of up to 50.6 A saturation current and the ability to handle high current transient peaks. Its design with flat wire coil and a composite core material ensures low copper losses and stable behavior under temperature fluctuations.

WE-XHMA is particularly suitable for use in DC/DC converters for high current supply and field programmable gate arrays (FPGA), as well as filter applications. It is particularly useful when used in switching power supplies: In contrast to conventional core materials, the compact coil shows hardly any temperature-dependent fluctuations in terms of inductance and saturation current. The higher energy density and the compact design due to the use of flat wire also make WE-XHMA interesting for switched-mode power supplies. Flat wire also has the advantage that a larger cross-sectional area can be achieved with the same space requirement, thereby reducing resistance. Furthermore, it shows a lower skin effect at higher frequencies and the heat dissipation towards the circuit board is, because of the flat thermally conducting surface, also better than round wire.

The compact molded magnetically shielded coils are AEC-Q200 certified and have an operating temperature range of -40°C to +125°C. WE-XHMA is available from stock in SMT styles 6030, 6060, 8080, 1090, 1510 and with saturation currents from 9.3 to 50.6 A. Free samples for developers are provided.

www.we-online.com

AC-DC Power Factor Correction Module in a Full Brick Package

TDK announces the introduction of the TDK-Lambda brand PF1500B-360 full brick power module, capable of providing up to 1512W. The power supply has a 0.98 power factor and delivers a regulated 360Vdc non-isolated voltage from an AC input. The PF1500B-360 can be used to drive isolated high voltage input DC-DC modules in a distributed power architecture configuration, or loads requiring a high voltage DC input. Applications include semiconductor fabrication, LED lighting and custom power supply solutions using power modules.

With an input of 170 to 265Vac, the PF1500B-360 provides 1512W and 1008W when operated from 85 to 265Vac. The 96.5% efficiency ensures reliable operation with baseplate temperatures of up to +100°C and in ambient temperatures of -40 to +85°C. The module has the industry standard full brick package size, measuring 116.8mm in length, 61mm wide and 12.7mm high for low profile applications.

As standard, the PF1500B-360 provides a 10 - 16V 10mA auxiliary voltage, remote on/off and an inverter good signal. An enable function is available to activate isolated DC-DC converters when the output voltage is greater than 360Vdc to synchronise output rise times. Parallel connection with current sharing of up to three modules is possible for additional output power.

Input and output to baseplate isolation is 2,500Vac. The PF1500B-360 is certified to the IEC/EN/CSA/UL 62368-1 standards and is CE / UKCA marked to the Low Voltage, EMC and RoHS EU Directives and UK regulations. With external circuitry, the PF1500B-360 will meet radiated and conducted emissions and comply with the IEC 61000-4 immunity standards.

www.emea.lambda.tdk.com

All-in-One Hybrid Power Drive Module Solution Designed for Electric Aviation Applications

Microchip Technology announces a comprehensive hybrid power drive module, the first variant introduced in a product line of power devices that will be available in 12 different variants with either silicon carbide (SiC) MOSFETs or insulated-gate bipolar transistors (IGBTs).

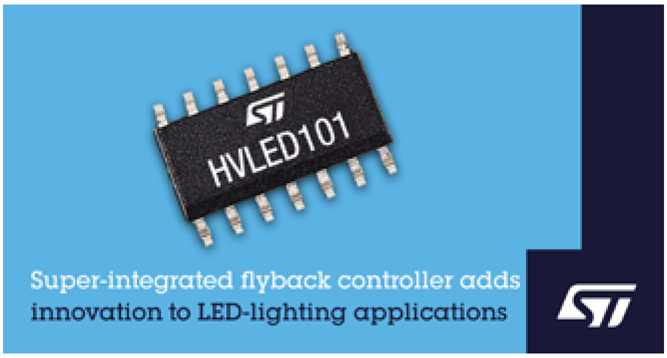
These hybrid power drive modules are highly integrated power semiconductor devices that reduce the number of components and simplify the overall system design. The configurable power devices include a three-bridge topology that are available in SiC or Si semiconductor technologies. Offering a compact design and low weight and profile, these high-reliability power devices help reduce the size and weight of MEAs.

Other key capabilities of these hybrid power drive modules include numerous auxiliary power devices that facilitate an inrush current limit function. Optional add-on capabilities include soft start, solenoid interface drive, regenerative brake switch and thermal sensors for external monitoring circuitry usage. The power modules also facilitate high-switching frequency power generation, which enables smaller and more efficient systems. The standard voltage of the power modules ranges from 650V to 1200V, with the option to customize up to 1700V on request. The device is designed for low inductances for high-power density with power and signal connectors that are solderable directly on the user's printed circuit board.

www.microchip.com

Integrated Flyback Controller Boosts LED Lighting Performance

STMicroelectronics' HVLED101 90-400V flyback controller for LED-lighting applications up to 180W enhances performance and simplifies design through extensive feature integration, patented control techniques, and support for primary-sensing regulation.



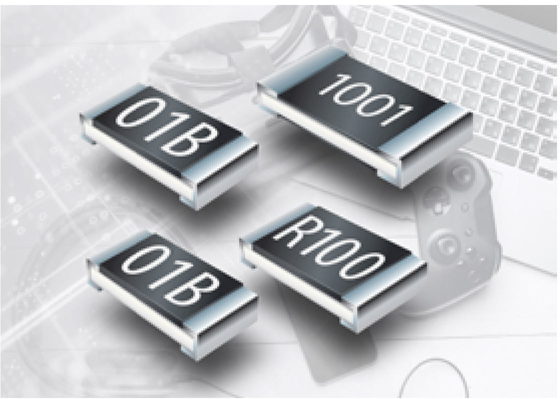
Joining ST's HVLED family of high-power-factor controllers, the HVLED101 contains 800V startup circuitry that cuts the LED turn-on time to less than 250ms. High-voltage input-sensing circuitry and a maximum power control (MPC) engine are also integrated to ensure consistent power output as the line voltage fluctuates. This lets designers choose smaller and lower-cost external passive components to handle worst-case line conditions. Primary-sensing regulation without isolated feedback further reduces the bill of materials and enhances reliability.

Among the patented innovations, ST's input-current shaping algorithm lowers total harmonic distortion (THD) and maximizes the power factor. Also, the HVLED101 is the first high-power factor flyback controller to implement ST's valley-locking technique to minimize audible noise, improve regulation, and reduce distortion. At steady state in quasi-resonant operation, valley locking fixes the number of valleys skipped until a significant change in output power or input voltage is detected. Together, current shaping and valley locking enhance the power factor and THD even at low and medium loads. Flyback converters controlled with the HVLED101 can achieve 5% THD at full load and 10% at 1/3 load to meet leading ecodesign codes.

www.st.com

AEC-Q200 Compliant High Power Thick Film Chip Resistor Line

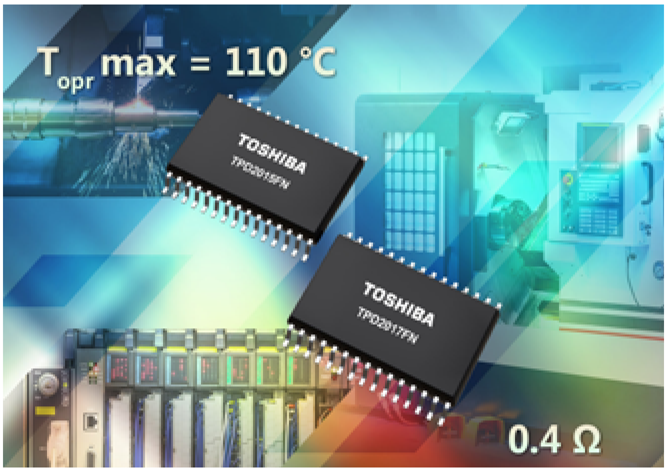
Bourns expanded its line of high power thick film resistors with four AEC-Q200 compliant product series. The Bourns® Model CRM-Q, CRS-Q, CMP-Q and CHP-Q Series are automotive grade and feature high rated power and pulse load surge capability. Manufactured using a thick film element printed onto a ceramic substrate enhances the four new resistor series' reliability. The features offered in Bourns' AEC-Q200 compliant resistors make them well-suited for current limiters and snubber circuits, as well as balancing and bleeder resistors in automotive, consumer electronics, industrial automation, power supplies, LED lighting and communication base station applications. Bourns® Model CRM-Q Series high power resistors and Model CRS-Q Series surge withstand resistors are available in three sizes from 1206 (3116 Metric) to 2512 (6432 Metric) with rated power from 0.5 to 2 watts. The Model CMP-Q Series pulse power resistors are available in five sizes from 0603 (1608 Metric) to 2512 (6432 Metric) with rated power from 0.25 to 1.5 watts. The Model CHP-Q Series ultra-high power resistors are available in five sizes from 0603 (1608 Metric) to 1206 (3116 Metric) with rated power from 0.33 to 0.75 watts.



www.bourns.com

8-Channel High- and Low-Side Switches for Driving Loads in Industrial Applications

Toshiba Electronics Europe has launched two intelligent power products to control the driving of resistive and inductive loads

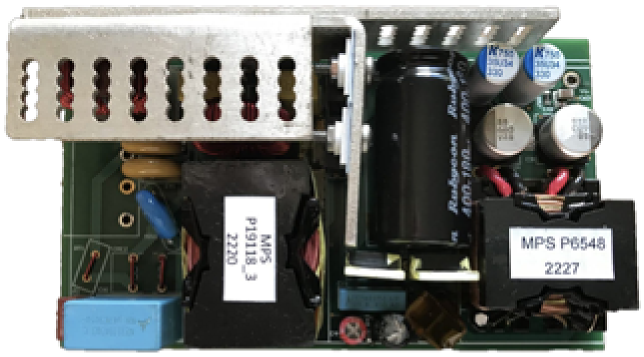


including motors, solenoids, and lamps in applications such as programmable logic controllers within industrial equipment. The power switch products both comprise 8 channels and are a high-side (TPD2015FN) and low-side (TPD2017FN) switches. Both devices benefit from Toshiba's latest analog device process (BiCD) that combines bipolar, CMOS, and DMOS technologies. Both of the products are housed in the small 0.65mm pitch SSOP30 package that measures just 9.7 ×7.6 ×1.2mm. This offers a reduction of around 29% in mounting area and 20% in height over the SSOP24 package (13.0 × 8.0 ×1.5mm) that is used for current products such as the TPD2005F and TPD2007F, thereby reducing the size of designs. With regard to the electrical performance, the on-resistance (RDS(ON)opr) from -40°C to +110°C with a junction temperature (Tj) as high as +150°C, ensuring their suitability for challenging industrial environments. In addition, both products have built-in over current protection circuits and over temperature protection circuits, thereby ensuring the reliability of equipment they are used in.

https://toshiba.semicon-storage.com

Power Adapter Reference Design with TO-220 GaN FETs

Transphorm announced availability of its 240W Power Adapter Reference Design. The TDAIO-TPH-ON-240W-RD deploys a CCM Boost PFC + Half-Bridge LLC topology to deliver a peak power efficiency of over 96 percent with a power density up to 30 W/in3. Transphorm's design uses three SuperGaN® FETs (TP65H150G4PS) each with an on-resistance of 150 milliohms. The GaN FET comes as a 3-lead TO-220, a well-known and long-trusted transistor package that offers superior thermals at lowline for higher current power systems running PFC configurations.



The reference design is intended to simplify and quicken power system development for applications such as high-power density AC-to-DC power supplies, fast chargers, IoT devices, laptops, medical power supplies, and power tools.

The TDAIO-TPH-ON-240W-RD is a 240W 24V 10A AC-to-DC power adapter reference design. It pairs the TP65H150G4PS GaN FETs with onsemi's off-the-shelf NCP1654 CCM PFC controller and NCP1399 LLC controller. The design uses a 25 millimeter heatsink that produces a power density of over 24 W/in3. The power density can increase by approximately 25 percent to 30 W/in3 depending on the heatsink design.

This high power density and efficiency range is primarily due to the FET's packaging as Transphorm offers the only high voltage GaN devices in a TO-220 today. Power adapters, along with all universal AC-to-DC power supplies, require high current at lowline (i.e., 90 Vac) which can require paralleling two PQFN packages (as typically seen with e-mode GaN) to achieve the desired power output. This method reduces a power supply's power density while requiring 2x part count. Transphorm's TO-220 packages mitigate this, thus providing unparalleled power density at a lower cost - a result not currently possible with e-mode GaN.

www.transphormusa.com

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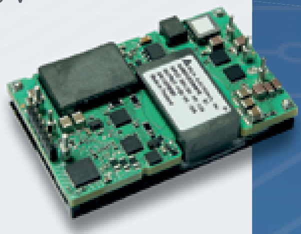

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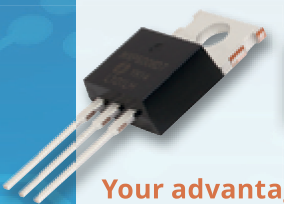

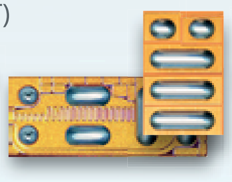

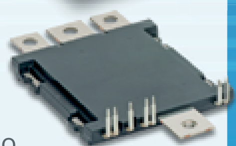

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