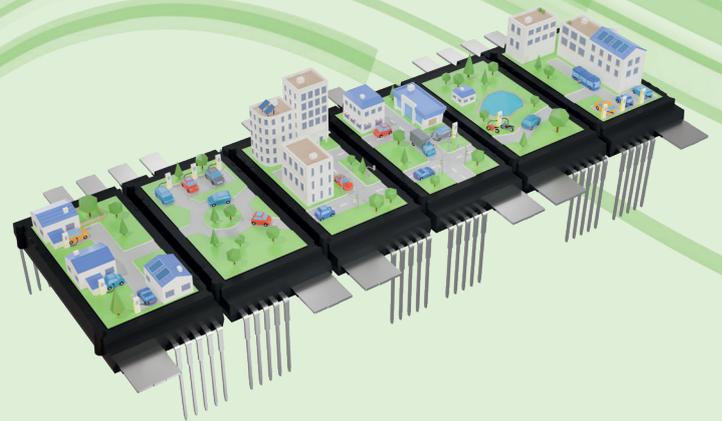
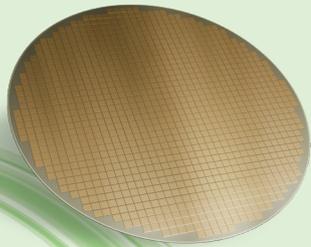
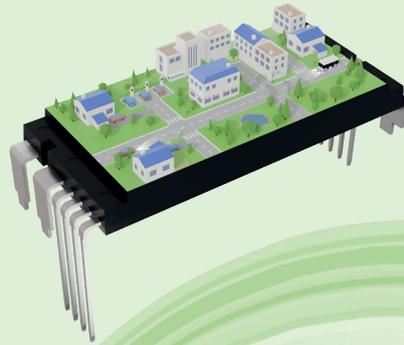


Bodo's Power Systems®

Electronics in Motion and Conversion

September 2025



YOU CAN BUILD ON IT.

Bare-Dies and Scalable T-PM for E-Mobility:
Advanced SiC MOSFET & Si RC-IGBT Devices



POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the

- Incremental inductance $L_{inc}(i)$ and $L_{inc}(\int U dt)$
- Secant inductance $L_{sec}(i)$ and $L_{sec}(\int U dt)$
- Flux linkage $\psi(i)$
- Magnetic co-energy $W_{co}(i)$
- Flux density $B(i)$
- DC resistance

Also suitable for 3-phase inductors

APPLICATIONS

Suitable for all inductive components from small SMD inductors to very large power reactors in the MVA range

- Development, research and quality inspection
- Routine tests of small batch series and mass production

KEY BENEFITS

- Very easy and fast measurement
- Lightweight, small and affordable price-point despite of the high measuring current up to 10000A
- High sample rate and very wide pulse width range => suitable for all core materials

AVAILABLE MODELS

Model	max. test current	max. pulse energy
DPG10-100B	0.1 to 100A	1350J
DPG10-1000B	1 to 1000A	1350J
DPG10-2000B	2 to 2000A	1350J <i>new model</i>
DPG10-2000B/E	2 to 2000A	2750J <i>new model</i>
DPG10-3000B/E	3 to 3000A	2750J
DPG10-4000B/F	4 to 4000A	8000J
DPG20-10000B/G	10 to 10000A	15000J

LH3 Series



BOOTH #403



Electronic Concepts
EST. 1969

ESL 7nH typical

- ✓ Film Capacitor Designed for Next Generation Inverters
- ✓ Operating temperature to +105°C
- ✓ High RMS current capability- greater than 400Arms
- ✓ Innovative terminal design to reduce inductance



ecicaps.com

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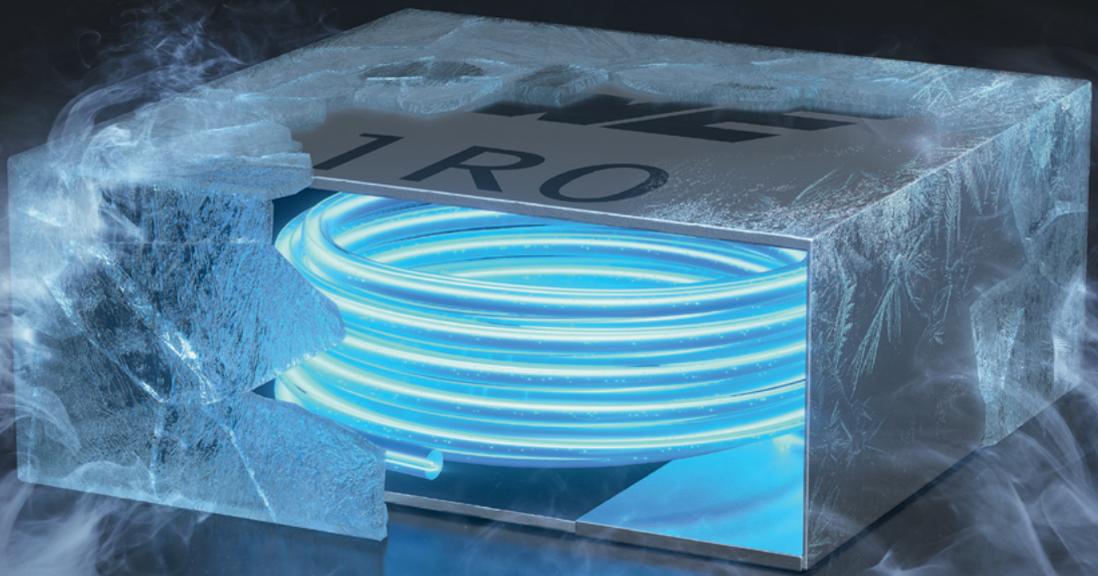
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With the WE-MXGI Würth Elektronik offers the newest molded power inductor series. It combines an innovative iron alloy material that provides high permeability for lowest R_{DC} values combined with an optimized wire geometry.

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Highlights

- Extremely high power density
- Ultra low R_{DC} values and AC losses
- Magnetically shielded
- Optimized for high switching frequencies beyond 1 MHz

#UltraLowLosses

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Free Subscription to qualified readers
Bodo's Power Systems is available for
the following subscription charges:
Annual charge (12 issues) is
150 € world wide · Single issue is 18 €
subscription@bodospower.com

**Printing by:**

Dierichs Druck+Media
GmbH & Co. KG
34121 Kassel, Germany

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The Power of Renewables



This August I took a few days off to experience the great outdoors with my son. This time, we took the train on a fully electrified route from Munich to Zurich to reach the Swiss mountains.

Afterwards, we crossed several mountain pass roads. I was overwhelmed when I saw how far the deployment of renewable energy generation has already progressed in this country. On the way up the mountains, we saw the past, the present time and the future of our electrical energy supply. Down in the valleys a lot of houses had photovoltaic panels on their roofs. In northern Switzerland in particular, many PVs were integrated into the facades or installed in place of roof tiles. However, this only applies to newer houses and not to the old, often listed, beautiful houses, of which there are still so many in Switzerland.

Climbing up just one valley – in this case the Grimsel mountain road – we saw numerous hydroelectric power stations (several of them pumped storage plants) at elevations of about 600 m, 1400 m and 2000 m. This year they are celebrating the 100th anniversary of hydropower generation in this valley while currently raising one of the lake's dams by 23 m to increase the storage capacity in this lake by more than 80 % which will increase the energy content from 270 GWh to 510 GWh.

At the dam wall of a reservoir, at an altitude of around 1,800 meters above sea level, I was amazed to see a 250 kWp PV system stretching across the entire crest of the wall. Together with another dam-mounted PV system in this area they can "harvest" 600 MWh every year. With snow reflecting from the frozen lake in wintertime the operator is able to "produce" almost 50 % of the PV energy during winter. Then we reached the Grimsel crest which also marks the continental divide between the North

Sea (Rhine River) and the Mediterranean Sea (Rhône River).

Slowly driving up the hairpin curves of the Nufenen Pass road (the highest mountain pass road purely within Switzerland) to its crest at 2500 m we additionally discovered several wind power plants – of course, in addition to hydropower. These are just two examples out of many that we saw. By the way: Only at the cobblestone! St. Gotthard mountain road we didn't encounter any trucks because there are three tunnels underneath the mountain: a road tunnel (17 km) and two train tunnels of 15 km (built in 1882 already!) and 57 km (completed in 2016 – the world's longest and deepest traffic tunnel). And on the St. Gotthard crest they have set up an educational hiking trail between the wind power plants.

On this vacation it became clear that we at Bodo's Power Systems made a good decision to dedicate a major part of this issue to renewable energies. But you may be assured that renewables will also play an important role at Bodo's Wide Bandgap event on December 2 and 3 in Munich/Germany. Please visit www.bodoswbg.com.

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive, of every issue of the magazine, is available for free at our website bodospower.com.

My green tip of the month:

Choose an electricity contract for your home which guarantees a 100 % supply out of renewables. I know that it is still slightly more expensive than the standard energy mix but it also shows your commitment to the future of our planet and enables your energy supplier to make the appropriate customer-demand driven decisions.

Events

electronica India 2025
Bengaluru, India September 17 – 19
www.electronica-india.com

PCIM Asia 2025
Shanghai, China September 24 – 26
www.pcimasia-shanghai.com

PwrSoC 2025
Seoul, Korea September 24 – 26
www.pwrsocevents.com

CIGRE 2025
Montréal, Canada
September 29 – October 3
<https://cigre.ca/2025>

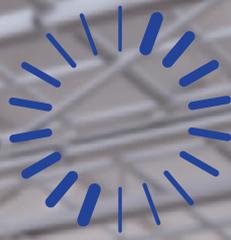
ESREF 2025
Bordeaux, France October 6 – 9
<https://esref2025.sciencesconf.org>

WiPDA 2025
Fayetteville, AR, USA November 10 -1
www.wipda.org

productronica 2025
Munich, Germany November 18 – 21
www.productronica.com

SEMICON Europa 2025
Munich, Germany November 18 – 21
www.semicon.europa.org

SPS 2025
Nuremberg, Germany November 25 – 27
<https://sps.mesago.com>



Need a low range current sensor that offers high resolution?



HMSR DA series

The new HMSR DA family of integrated current sensors designed by LEM is the first to include an ADC with a sigma-delta bitstream digital output.

High-resolution, ease-of-use and an output that follows the increase or decrease of the input with configurable delay, makes it easier to develop a wealth of control systems.

This makes the HMSR DA the first choice for standalone servo drives, robotics, high precision machines, automated guided vehicles (AGVs) and CNC machine tools.

www.lem.com

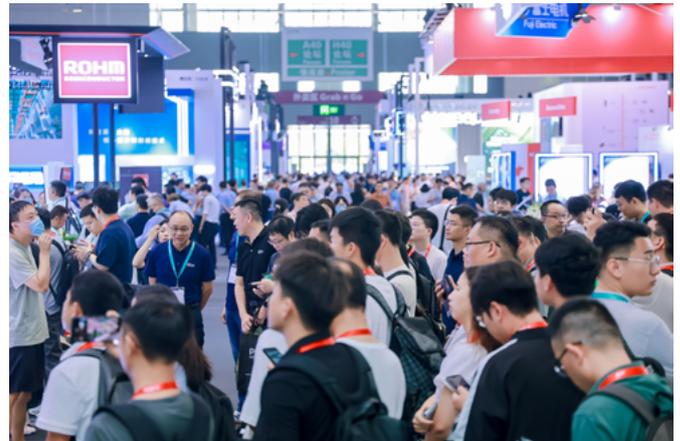
- Current range 6-30 A_{RMS} continuous at 125°C
- 75 A peak current
- Digital bitstream output with 10 MHz clock
- More cost-effective and compact than discrete alternatives

LEM

Life Energy Motion

PCIM Asia Shanghai Conference 2025 Programme to explore Power Electronics in AI and e-mobility

The PCIM Asia Shanghai Conference, Asia's foremost academic gathering for the power electronics industry, returns to Shanghai this September. The 2025 programme will unite industry leaders, technical experts and academics to explore advanced solutions and future trends, highlighting developments in cutting-edge technologies such as silicon carbide (SiC), gallium nitride (GaN), motor drives and motion control, and more. Debuting at the conference is the new "Dialogue with Speakers" zone, where dedicated booths will provide a setting for more direct and in-depth interactions between speakers and attendees. Held in conjunction with the PCIM Asia Shanghai exhibition, the PCIM Asia Shanghai Conference addresses key industry topics including motion control systems and power supply solutions. The exhibition, in turn, showcases the latest technologies in power electronics components, power conversion, intelligent motion and more. The combined programme brings together leading specialists from the power electronics sector, application fields, and research institutions worldwide to share their knowledge and discuss the future of the industry.

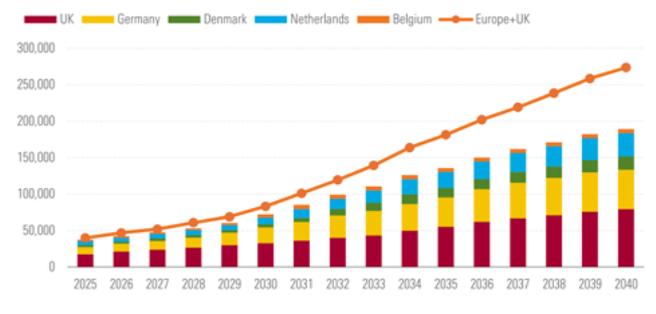


www.pcimasia-shanghai.com

Europe remains committed to growing Offshore Wind Energy

A study conducted by Morningstar DBRS makes it very clear: Europe remains an important market for offshore wind with rising relevance over the next few decades as it moves towards meeting its carbon emission reduction goals and increasing its energy independence. This contrasts sharply with the United States' path following President Trump's executive order on January 20, 2025, withdrawing all areas of the U.S. outer continental shelf from Offshore Wind Leasing. Europe has a long history of using offshore wind as part of its energy mix. The world's first offshore wind farm was completed in Denmark in 1991 by Orsted. The project consisted of 11 turbines with total generation capacity of 5 MW. The European offshore wind industry has grown significantly since then with Europe achieving 35 GW of installed generation by the end of the first half of 2024. Europe has a significant share of the offshore wind industry with 38% of the world's offshore wind capacity, with Germany and the U.K. as the main contributors. The European market is significantly larger than the U.S. offshore wind market with the U.S. Energy Information Administration reporting in December 2024 that there are only 130 MW of operating off-

Exhibit 2 European Offshore Installed Capacity (MW)—Forecast



Source: BNEF.

shore wind projects and 6.9 GW planned by projects by 2027. Offshore wind represents a key part of Europe's goal to transition to renewable electricity sources and to achieve energy independence. Bloomberg NEF (BNEF) forecasts European wind capacity will reach 40 GW in 2025, increasing to 80 GW by 2030 and 274 GW by 2040, with the U.K., Germany, and the Netherlands contributing the most to growth.

www.dbrs.morningstar.com

Research Center for Wide Bandgap Materials

onsemi announced plans to invest \$8 million dollars with Stony Brook University to establish a wide band gap research center that will advance innovation in power semiconductors and foster the next generation of skilled professionals in this field. The investment is part of a broader \$20 million strategic collaboration with Stony Brook University and Empire State Development aimed at positioning New York as a national hub for power semiconductor innovation.

The center aims to advance foundational research in silicon carbide and other wide band gap materials and device-enabling technologies - capabilities critical to improving energy efficiency in AI and electrifica-

tion. Expected to be fully operational in early 2027, the facility will feature specialized laboratories and advanced instrumentation for materials development, device integration, and performance characterization.



"Advanced power semiconductors are at the core of enabling the widespread adoption of AI and electrification. This new center will play a key role in accelerating innovation in one of the most critical fields for these global megatrends," said Dinesh Ramanathan, Senior Vice President of Corporate Strategy, onsemi. "Aligned with Governor Hochul's vision, and in strong partnership with Stony Brook and Empire State Development, we are building a pipeline of skilled talent who will drive the next wave of breakthroughs in power semiconductors and pave the way for our sustainable future."

www.onsemi.com



New High Power Density EcoSiC™ Modules

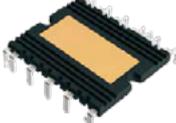
Compact high heat dissipation design sets a new standard for OBCs

ROHM has developed the new 4-in-1 and 6-in-1 SiC molded modules in the HSDIP20 package optimized for PFC and LLC converters in onboard chargers (OBC) for xEVs (electric vehicles). The lineup includes six models rated at 750V (BSTxxx1P4K01) and seven products rated at 1200V (BSTxxx2P4K01).

Lineup ideal for configuring high-power power supply circuit topologies such as PFC and LLC circuits

Adopting high thermal conductivity insulating materials ensures superior heat dissipation, facilitating insulation design

Delivers higher output compared to power modules of similar size

Part No.	Absolute Max. Ratings (T _J =25°C)			Topology	Module Package
	V _{DSS} [V]	R _{DS(on)} [mΩ]	I _D [A] ^{*1}		
BST91B1P4K01	750	13	90	4in1	 HSDIP20 [38.0mm x 31.3mm x 3.5mm]
BST47B1P4K01		26	47		
BST31B1P4K01		45	31		
BST91T1P4K01		13	90	6in1	
BST47T1P4K01		26	47		
BST31T1P4K01		45	31		
BST70B2P4K01	1,200	18	70	4in1	
BST38B2P4K01		36	38		
BST25B2P4K01		62	25		
BST70T2P4K01		18	70	6in1	
BST38T2P4K01		36	38		
BST25T2P4K01		62	25		
BST70M2P4K01 ^{*2}		18 ^{*3} / 36 ^{*4}	70 ^{*3} / 38 ^{*4}		

^{*1}: T_c=25°C VGS=18V ^{*2}: Combines chips with different ON resistances
^{*3}: Q1, Q4 pins ^{*4}: Q2, Q3, Q5, Q6 pins

EcoSiC™ is a trademark or registered trademark of ROHM Co., Ltd.

30 Years of Openair-Plasma Technology

Plasmatrete celebrated the 30th anniversary of the patent application for its Openair-Plasma technology with its Technology Days 2025 at the headquarters in Steinhausen, Germany. Due to its process stability, efficiency, environmental friendliness, and ease of integration into production environments, the Openair-Plasma technology has changed numerous industrial processes worldwide. More than 200 guests and 16 industry partners joined the Plasmatrete team for the celebration. This plasma technology is used to give materials special

properties for further processing including ultra-fine cleaning, activation, reduction, and coatings for a wide range of industrial applications. Plasmatrete technology is currently used in more than 100 automotive and battery production applications. E. g. PlasmaPlus PT-Bond technology serves as an environmentally friendly bonding agent that is often used to bond different materials in a stable, weather-resistant way. Eight interactive workshops complemented the event. For example, the workshop "REDOX effect: Reduction to High-Performance



Coatings" showed how oxidized and contaminated metal surfaces are cleaned in the semiconductor industry to meet the strictest standards for manufacturing electronic components. Plasma systems and reduction were also demonstrated live.

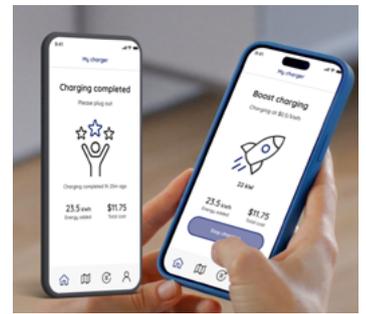
www.plasmatrete.com

Strategic Partnership for EV Charging Infrastructure

SolarEdge Technologies is proud to announce a strategic partnership with Schaeffler, to deploy electric vehicle (EV) charging infrastructure and software across Schaeffler sites. The partnership will support Schaeffler in commissioning around 2300 charging points in Europe. By integrating hardware and SolarEdge's EV charging software capabilities into Schaeffler's infrastructure, the collaboration will enable Schaeffler employees and fleet vehicle drivers to charge their EVs at company locations, starting with the newly electrified parking lot at Schaeffler's Technology Center (Technologiezentrum) at its global headquarters in Herzogenaurach, Germany.

Powered by SolarEdge's Wevo technology, now part of its advanced ONE for C&I energy optimization platform, the solution is designed to deliver a frictionless charging experience for employees including a custom app.

"We are excited to deepen our partnership with Schaeffler," said Naama Ohana, Chief Commercial & Industrial Division at SolarEdge. "Our solar technology has powered Schaeffler rooftops with safe, reliable energy for many years. Now, our Enterprise Service Group is proud to further support Schaeffler's energy transition by delivering EV charging software, services, and hardware. This is a great example of how our advanced software capabilities can add value to our customers' energy transition strategy."



www.solaredge.com

NORWE®

The grid contains the following elements:

- Top-left: Red plastic component with pins.
- Top-middle-left: RoHS 3 logo with a checkmark and the European Union flag.
- Top-middle-right: Clear plastic component.
- Top-right: Black plastic component with pins.
- Second row, left: Black plastic component with pins.
- Second row, middle-left: Yellow plastic component.
- Second row, middle-right: Black plastic component.
- Second row, right: Silver metal component.
- Third row, middle-right: United States Environmental Protection Agency logo.
- Third row, right: Red plastic box.
- Bottom-left: Red plastic component with pins.
- Bottom-middle-left: Yellow plastic component.
- Bottom-middle-right: REACH logo with a checkmark and the European Union flag.
- Bottom-right: Black plastic component with pins.
- Bottom-most-right: UN Global Compact logo with the text 'WE SUPPORT UN GLOBAL COMPACT'.



Megatrends for photovoltaic inverters

With energy prices on the rise and solar systems becoming more common, next-generation inverter technology is changing how we generate and use power. The most significant development in inverter design is related to the growth in Silicon Carbide (SiC) power devices: improving efficiency, power density, and system costs while meeting strict price-performance targets.

In our whitepaper, we will cover the following topics:

- Current megatrends in photovoltaic inverters for residential and commercial applications
- How you can improve the design of your PV inverter
- How you can support circuitry in complete designs
- Intelligent PV systems

Read our whitepaper and discover new breakthroughs that make solar systems smaller, smarter, and more affordable.

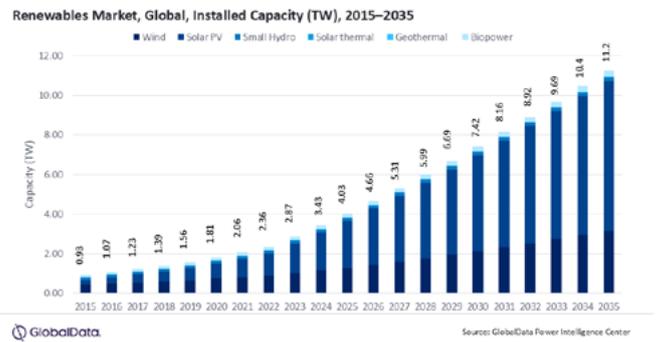


[Download whitepaper](#)



Global Renewable Power installed Capacity to surge to 11.2 TW by 2035

Renewable resources, particularly solar photovoltaic (PV) and wind energy, are gaining a larger share in the energy portfolio. Driven primarily by declining costs and strong policy support, particularly for solar PV and wind energy, the global renewable power installed capacity is estimated to surge from 3.42 TW in 2024 to 11.2 TW by 2035, according to GlobalData. The company's latest report, "Renewable Energy: Strategic Intelligence", reveals that the global renewables market expanded from a cumulative installed capacity of 0.93 TW in 2015 to 3.42 TW by the end of 2024, representing a compound annual growth rate (CAGR) of 16 %. The total cumulative installed capacity is projected to record a CAGR of 11 % during the period 2024-35. Solar PV and wind power were significant contributors to the renewable energy sector, accounting for 56 % and 33 % of the total installed capacity in 2024, respectively. The APAC region has emerged as the largest market for solar PV and wind installed capacity, boasting 1.18 TW and 0.67 TW in 2024, respectively. Artificial intelligence is transforming the renewable energy sector by enhancing generation optimization, advancing grid management, and increasing efficiency across multiple systems.



AI algorithms possess the capability to forecast renewable energy production, oversee grid operations in real-time, and refine energy storage strategies. These advancements contribute to heightened reliability and efficiency, thereby rendering renewable energy more effective and economical. Looking ahead, the onshore wind sector is forecasted to grow to \$186.9 billion (CAGR: 4 %) and the offshore wind sector to \$150.4 billion (CAGR: 14 %) by 2030.

www.globaldata.com

Partnership on Silicon Carbide Solutions for Power Management

Microchip Technology announced that under a new partnership agreement with Delta Electronics the companies will collaborate to use Microchip's mSiC™ products and technology in Delta's designs. The synergies between the companies aim to accelerate the development of innovative SiC solutions, energy-saving products and systems that enable a more sustainable future. Delta intends to leverage Microchip's experience and technology in SiC and digital control to accelerate time to market of its solutions for high-growth market segments such as AI, mobility, automation and infrastructure. This agreement prioritizes the companies' resources to validate Microchip's mSiC solutions to fast-track implementation in Delta's designs and programs. Other key advantages of the agreement are top-tier design support including technical training as well as insight into R&D activities and early access to product samples.



www.microchip.com

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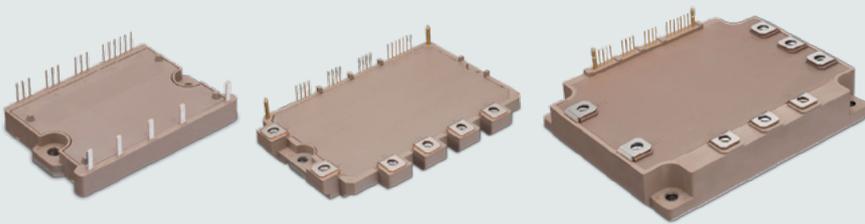


Scan for more information



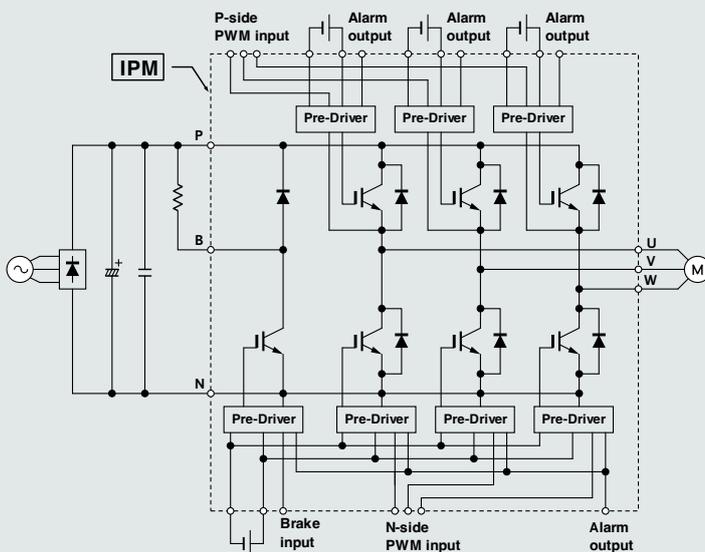
X series – Intelligent Power Modules (IPM)

ideal for Servo Systems, Elevators and Air Conditioners



MAIN FEATURES

- Reduction of losses and improvement of energy efficiency by optimizing 7th generation IGBT technology for IPM
- Embedded driver IC for optimum control and protection functions
- Single wire provides three alarm signals: over-current, over-heating, under-voltage
- 6in1 and 7in1 topology (inverter + brake)
- High temperature operating ($T_j=175^{\circ}\text{C}$)
- Reduced turn-on loss at high temperature operation by drive control
- Power range from 20A to 450A at 650V and 10A to 300A at 1200V





Company Location in South Africa added

Another Würth Elektronik branch opened in Brackenfell, Western Cape, South Africa. The location operates under the name Würth Electronics South Africa (Pty.) Ltd and will serve local customers, but will also be responsible for the markets of Botswana, Mauritius, Namibia, Tanzania and

Zambia. Ahmet Çakır, who also heads the branch in Turkey, will take over the management of the new location, under the leadership of Rob Sperring, Vice President for Southern Europe, Middle East and Africa. The Würth Electronics South Africa (Pty.) Ltd team currently consists of six employees. However, it will soon be expanded. The official opening ceremony for the new location will take place in early 2026. Four EMC seminars held by Würth Elektronik in South Africa's two largest cities, Cape Town and Johannesburg, have already been completed.

www.we-online.com

Survey reveals how Data is powering the Future for Solar Energy Innovation and Growth

A survey, conducted by Censuwide on behalf of Fluke, on key challenges for the solar



Data is the key to a bright future for solar, according to new research from Fluke

Businesses are increasingly interested in automating maintenance operations with strategies like condition monitoring and predictive maintenance. The real opportunity to overcome challenges in the solar industry lies in using smart tools to analyze data and identify potential issues before they cause failures.

Solar OEMs, technicians, and installers remain positive about solar's role in the future energy mix. Yet, the industry is being held back by a lack of understanding of data and smart technologies.

Two-thirds (63%) of all respondents predict that solar will become the dominant energy source in their country.



industry identifies improving panel efficiency, transitioning from reactive to predictive maintenance, and adopting smart technologies as top priorities. Crucially, data emerges as the driving force behind innovation and operational efficiency. The survey engaged over 400 solar OEMs, technicians, and installers across the UK, Germany, Spain and the USA to gain insights. The survey results also highlighted their attitudes toward emerging trends and their expectations for how the future of solar energy is likely to evolve in the coming years. The research revealed that nearly two-thirds of respondents (63%) believe solar will become the dominant energy source in their country. However, it also highlighted significant challenges that must be addressed to turn this optimistic vision into reality and pave the way for a solar-powered future. One of

the challenges that emerged in the survey's findings is the need to rapidly shift from reactive maintenance to a more proactive approach. With 91% of those surveyed reporting concerns about the efficiency of the current generation of solar modules and 39% of respondents identifying inverter failures as a common issue, it's clear an effective maintenance strategy is a necessity. Nearly a third of all respondents described their current maintenance strategy as reactive, while more than half indicated that implementing predictive maintenance was a key priority. 59% stressed the need to train technicians in advanced diagnostic tools to address evolving challenges, while 45% view AI integration in solar panel design, optimization, and maintenance as a key opportunity.

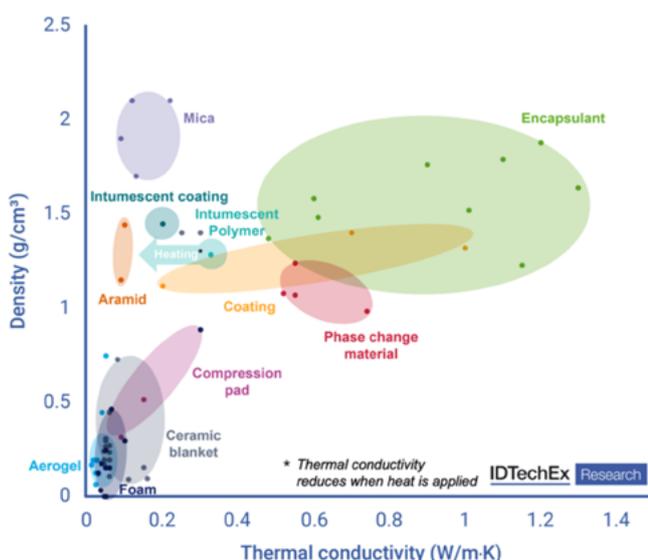
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Fire Protection Materials for EV Batteries 2025-2035: Markets, Trends, and Forecasts

Renewable resources, particularly solar photovoltaic (PV) and wind energy, are gaining a larger share in the energy portfolio. Driven primarily by declining costs and strong policy support, particularly

for solar PV and wind energy, the global renewable power installed capacity is estimated to surge from 3.42 TW in 2024 to 11.2 TW by 2035, according to GlobalData. The company's latest report, "Renewable Energy: Strategic Intelligence", reveals that the global renewables market expanded from a cumulative installed capacity of 0.93 TW in 2015 to 3.42 TW by the end of 2024, representing a compound annual growth rate (CAGR) of 16%. The total cumulative installed capacity is projected to record a CAGR of 11% during the period 2024-35. Solar PV and wind power were significant contributors to the renewable energy sector, accounting for 56% and 33% of the total installed capacity in 2024, respectively. The APAC region has emerged as the largest market for solar PV and wind installed capacity, boasting 1.18 TW and 0.67 TW in 2024, respectively. Artificial intelligence is transforming the renewable energy sector by enhancing generation optimization, advancing grid management, and increasing efficiency across multiple systems. AI algorithms possess the capability to forecast renewable energy production, oversee grid operations in real-time, and refine energy storage strategies. These advancements contribute to heightened reliability and efficiency, thereby rendering renewable energy more effective and economical. Looking ahead, the onshore wind sector is forecasted to grow to \$186.9 billion (CAGR: 4%) and the offshore wind sector to \$150.4 billion (CAGR: 14%) by 2030.

Fire Protection Materials for EV Batteries



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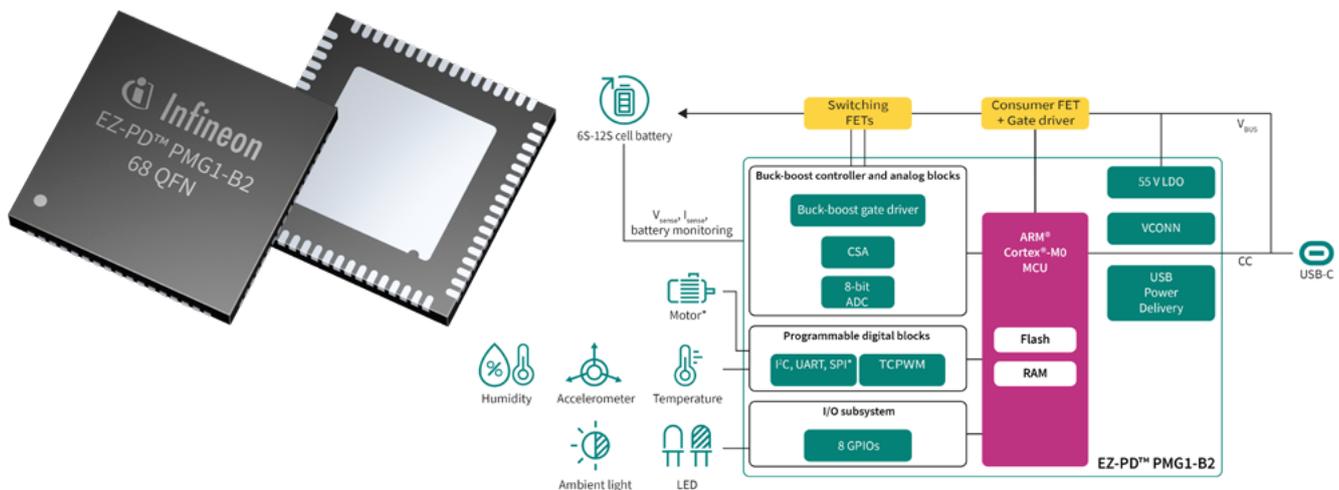
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A solution that is virtually ready-to-use for USB-C applications up to 240 W



Legacy and proprietary power connectors are slowly but surely giving way to the versatile and powerful USB-C, driven by a combination of government regulations, such as the European Commission's directive to establish a common charging standard, and consumer demand for more convenience and flexibility. With its reversible design, faster data transfer speeds, and higher power delivery capabilities of up to 240 W, USB-C is fast becoming the go-to interface for a wide range of applications, from low-power devices like smartphones and laptops to higher power devices like cordless vacuum cleaners and eBikes.

USB-C adoption, however, introduces new complexities, especially for devices with multiple USB-C ports. Traditional system architectures require in-depth USB knowledge, on-chip security, complex circuitry, and multiple components to manage power delivery and data transfer. To streamline this transition, Infineon has introduced EZ-PD™ PMG1, a portfolio of high-voltage MCUs with integrated USB Type-C PD that allow customers to turn their applications into USB-C-powered applications by simply replacing their main MCU with this single-chip solution.

Continuing the legacy, Infineon introduces EZ-PD PMG1-B2 Battery Charger with USB-C Power Delivery MCU, serving higher power embedded systems requiring USB Power Delivery's Extended Power range (EPR) up to 48 V, 5 A. EZ-PD PMG-B2 integrates a buck-boost battery charge controller that is capable of charging up to 12 cells, making it well suited for applications such as eBikes, eKick-scooters, power tools, cordless vacuum cleaners or kitchen appliances, as well as drones and robots.

EZ-PD PMG1-B2 supports a wide input voltage range (4.5 V to 55 V) and a programmable switching frequency from 200 kHz to 700 kHz. It is a programmable USB PD solution with on-chip 32-bit Arm® Cortex®-M0 processor, 128 KB flash, and 8 KB SRAM. It also includes various analog and digital peripherals such as ADC, PWMs,

serial communication blocks (UART/I2C/SPI) and timers. The MCU is available in a compact 68-QFN package (8 mm × 8 mm) with a pitch of 0.40 mm, enabling designs with reduced sizes. Being suited for an industrial temperature range of -40°C to 85°C with a maximum operating junction temperature of 125°C, EZ-PD PMG-B2 ensures a robust and reliable design.

Additionally, there are built-in integrations such as an I/O subsystem, analog blocks, and programmable digital blocks to simplify the design. The 10 GPIOs can be used for interactions with switches and LED lights, whereas the I2C, UART, SPI, and the TCPWM can be used to manage the control of humidity, temperature, accelerator, and communications with external battery monitoring systems (BMS). These integrations, along with the 8-bit ADC, reduce the BOM cost while also reducing the time-to-market for the end products.

Historically, Infineon has been the first to market for a number of USB products, such as the first USB PD controller, the first integrated USB PD hub, the first HV MCU with an integrated USB-C PD, and so on. Now with the EZ-PD PMG-B2, Infineon is again the first to the market for a 240 W Buck-Boost battery charger with a USB-C PD MCU for which the reference design is already available. The 240 W PMG1-B2 POC Battery Charger Demo board includes monitoring for battery voltage, current, temperature with two NTCs, as well as integrated protections for overvoltage, overcurrent, and undervoltage for the 48 V bus. This makes it highly suitable for drones and robots, as well as cordless power tool, garden tools and cordless home appliances.



To learn more about EZ-PD PMG-B2 and to order samples, visit <https://www.infineon.com/pmg1-b2>. Samples and solution boards are already available upon request, with mass production starting in Q1 of 2026.



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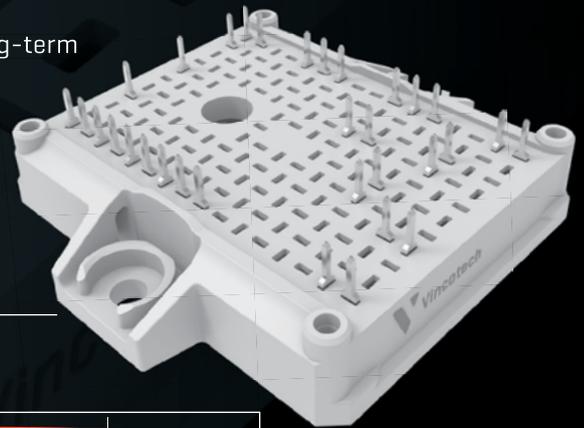
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The new 1200V flowPIM E2 featuring SiC MOSFETs, designed for power applications up to 12 kW

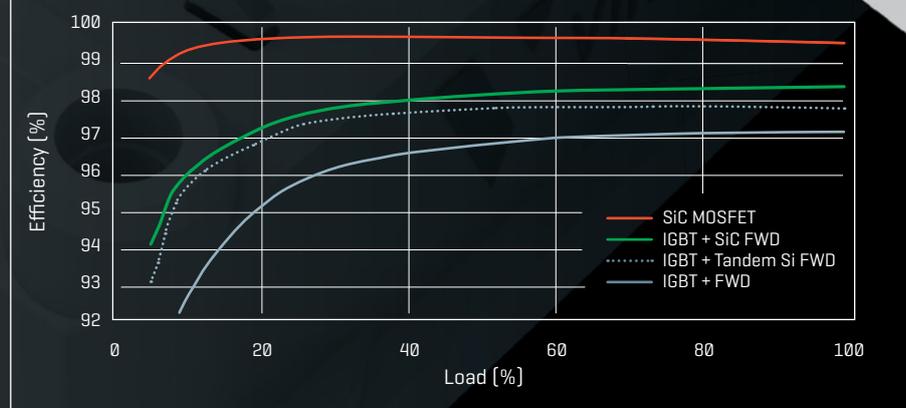
Unlock next-generation performance in HVAC systems with our cutting-edge integrated power module, combining both DC-DC converter and DC-AC inverter functionalities in a single Industry standard package. Powered by Silicon Carbide [SiC] MOSFET technology, this module delivers unmatched energy efficiency, thermal performance, and reliability—perfectly suited for modern air conditioning applications.

Main benefits

- / **High Efficiency:** SiC MOSFETs in the inverter stage drastically reduce switching losses
- / **Compact Integration:** Converter and inverter in one module simplifies system design, reduces footprint, and lowers BOM costs
- / **Superior Thermal Management:** Operates at higher junction temperatures with reduced cooling requirements
- / **Enhanced Reliability:** Robust design ensures long-term durability even in demanding HVAC environments
- / **Quiet Operation:** High-frequency switching minimizes acoustic noise, improving end-user comfort



Inverter Stage - Efficiency Comparison

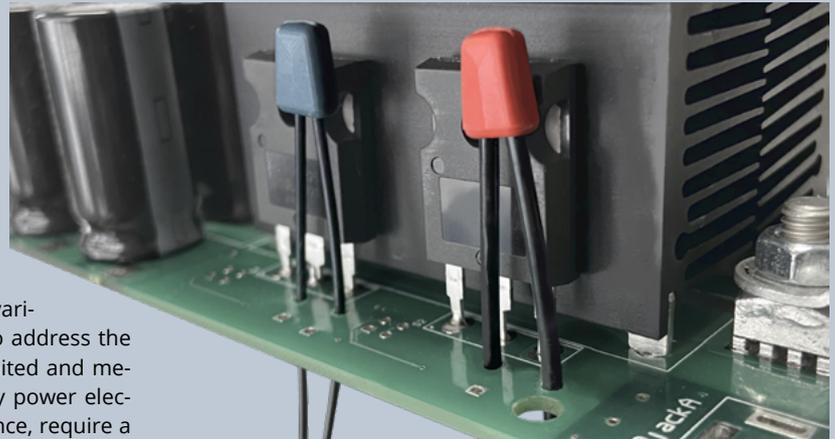


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Forked Rogowski Coil Enables True Through-PCB Current Measurement

Novel coil construction delivers 30 MHz bandwidth and 100 kA/ μ s di/dt capability for dense power electronics applications



Building on PEM's well-established CWTUM range of ultra-miniature Rogowski probes, the new "forked" variants – CWTUM-F and CWTUMHF-F – are designed to address the growing need for current measurement in space-limited and mechanically constrained environments, as high-density power electronics layouts and those with limited vertical clearance, require a different mechanical approach.

To address these issues, these novel "forked" geometry probes enable true through-PCB current measurement with industry-leading frequency response and noise immunity. This design facilitates non-intrusive probing of high-speed current waveforms, making it ideal for measurements in advanced converter topologies.

Design Innovation: Forked Coil Geometry

At the heart of this development is a unique forked Rogowski coil construction, engineered for threading around embedded or hard-to-reach PCB conductors. The lower profile of the coil also reduces the proximity to other nearby conductors, allowing measurement in very tight gaps, and away from sources of interference. Unlike traditional Rogowski probes the "forked" variants feature a slim-line clip-together mechanism, at just 7.5mm x 6mm it enables easy access through tight apertures that conventional probes cannot reach.

Model Comparison: CWTUM-F vs CWTUMHF-F

The new coil range includes two variants tailored to different performance requirements:

- CWTUM-F
- 1.3 mm coil thickness
- 15 MHz (-3 dB) bandwidth CWTUMHF-F
- 1.7 mm coil thickness
- 30 MHz (-3 dB) bandwidth

The marginal increase in coil thickness between the two variants is offset by significant performance gains in noise rejection and high-frequency signal fidelity.

High-Frequency Performance and Noise Immunity

The CWTUMHF-F variant incorporates PEM's patented electrostatic shielding that greatly reduces susceptibility to interference caused by parasitic capacitance and rapid voltage transitions. This is critical when measuring current in circuits with fast switching edges or significant ringing, such as those found in wide-bandgap-based motor drives and power converters.

High-Frequency Performance and Noise Immunity

The CWTUMHF-F variant incorporates PEM's patented electrostatic shielding that greatly reduces susceptibility to interference caused by parasitic capacitance and rapid voltage transitions. This is critical when measuring current in circuits with fast switching edges or significant ringing, such as those found in wide-bandgap-based motor drives and power converters.

Electrical Performance Highlights & Applications

Both variants share the following electrical capabilities:

- Peak di/dt capability: 100 kA/ μ s
- **Current range:** 60 A to 12 kA peak
- **Wide dynamic range**, suitable for both small-signal and large transient measurements

These characteristics make the probes well-suited to a variety of demanding applications, including:

- Current profiling in switch-mode power supplies
- Measuring capacitor ripple currents
- Diagnosing transient behaviour in inverters and power stages
- Monitoring motor drive performance under rapid switching conditions

The CWTUM-F offers a cost-effective solution for moderate switching environments, such as industrial drives, low-noise converters, and general-purpose test setups where spatial constraints are critical.

The CWTUMHF-F is targeted at high-performance converters, research labs, and wide-bandgap power systems requiring high-fidelity measurements in noisy conditions—delivering enhanced visibility into fast current waveforms and switching artefacts.



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Next-Gen SiC MOSFET & Si RC-IGBT: Bare-Dies and Transfer Mold Power Modules

High-Power-Density, High-Efficiency & Scalability for E-Mobility

With accumulated track record of over 34 million xEVs driven by its highly reliable power devices since 1997, Mitsubishi Electric is steadily moving forward in advancing its next generation of finely coordinated, in-house designed & developed efficient semiconductor bare-dies (SiC MOSFET & Si RC-IGBT) and compact high-reliability transfer mold packaging (T-PM) technologies meeting the ongoing trend towards high power-density, scalable, cost-effective reliable solutions for e-Mobility.

By K. Hussein, A. Saif; Mitsubishi Electric Europe B.V., Germany
M. Tarutani, K. Yoshida, T. Osaga; Mitsubishi Electric Corporation, Japan

Introduction

As the world faces the escalating crisis of climate change, the automotive industry is increasingly undergoing a transformative shift towards power train electrification. Electrified vehicles (xEVs), including hybrid and fully electric powertrains, are at the forefront of this transition, demanding innovative solutions that balance performance, reliability, cost, and efficiency.

To meet these evolving requirements, power electronic devices in xEVs must address several critical challenges: delivering high power and efficiency, withstanding harsh automotive environments, maintaining cost-effectiveness, and supporting intelligent integration. Power semiconductor devices are central to achieving these objectives. In particular, two technologies have emerged as key enablers: Silicon Carbide (SiC) MOSFETs and Reverse Conducting Si IGBTs (RC-IGBTs). Each offers distinct advantages tailored to specific application needs. SiC MOSFETs are ideal for high-power, high-frequency applications such as traction inverters, where efficiency, thermal performance, and power density are paramount. RC-IGBTs provide a cost-effective alternative by integrating both the IGBT and freewheeling diode in a one die design, making them suitable for applications where cost and moderate performance demands must be balanced.

General Outline of Automotive Products

Recognizing the diverse requirements of 400V and 800V xEV architectures, Mitsubishi Electric offers a robust portfolio of both bare die power devices and scalable power modules, including both SiC MOSFETs and Si RC-IGBTs technologies. These technologies represent the company's ongoing commitment to innovations that are linked to addressing the real-world challenges of next-generation electric vehicles.

Key factor in Mitsubishi Electric's automotive power devices success lies in the fine coordination of in-house designed and developed efficient semiconductor devices (SiC & Si) and compact high-reliability transfer mold packaging (T-PM) with Direct-Lead-Bonding (DLB) technology eliminating the wire-bonding limitation usually faced in conventional packages.

Overview of Mitsubishi Electric automotive bare-die products lineup is given in Figure1(a) for SiC MOSFET and RC-IGBT. Both technologies contain devices with blocking voltage ratings of 750V and 1200V/1300V. Gen 4 SiC and 3rd Gen. RC-IGBT bare dies are integrated inside the latest automotive power modules family: the J3-Series, shown in Figure1(b) [1].

The core-module, J3-T-PM, is a compact half-bridge that can be fitted with either SiC MOSFET or Si RC-IGBT, enabling solutions for both 800V and 400V battery classes within the same module footprint along with various built-in features. The J3-T-PM is solderable, in a modular way (J3-HEXA-S/L), to pinfin baseplate or directly to the cooling-structure of the inverter, covering a wide power range from 80kW to over 300kW~.

The following two parts of this article will explore the technical foundations and advantages of Mitsubishi Electric's SiC MOSFET and Si RC-IGBT device technologies, illustrating how they contribute to advancing xEV powertrain performance and supporting successful adoption.

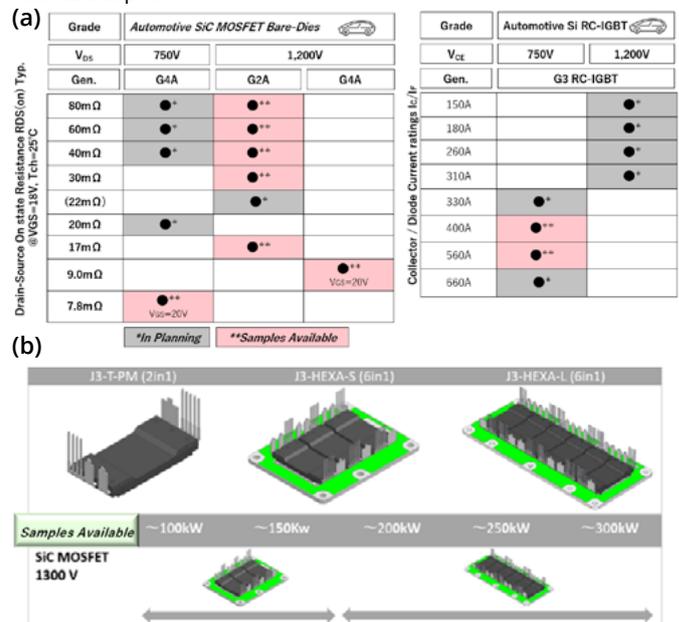


Figure 1: Lineup (a) SiC MOSFET and RC-IGBT bare dies (b) J3-series SiC/RC-IGBT power modules packages

Part-1

Evolution of Mitsubishi Electric's SiC MOSFET

Since the 1990s, Mitsubishi Electric has gained comprehensive experience in the design, development, and production of SiC devices for various high-efficiency demanding applications ranging from home air-conditioners to railway traction drives.



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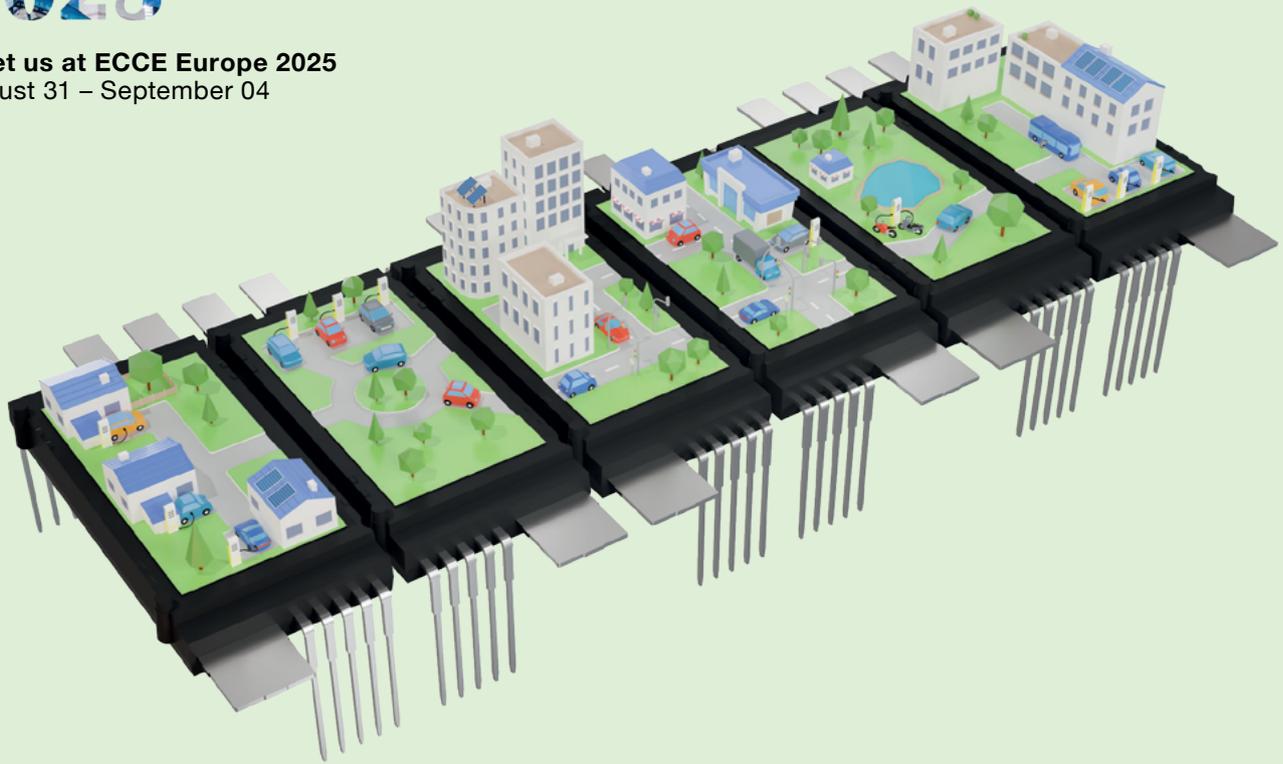
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SiC MOSFET & Si RC-IGBT for E-Mobility: Bare-Dies and Transfer Mold Power Modules

- // In-house developed, high-efficiency Si RC-IGBT and SiC MOSFET bare dies enable superior performance
- // Compact, high-reliability transfer mold packaging (T-PM) with optimized matching bare dies, ensuring enhanced thermal performance, scalability, and long-term durability
- // Half-bridge core module (J3-T-PM) compatible with 1300 V SiC MOSFETs and 750 V Si RC-IGBTs
- // Modular design approach (J3-HEXA-S/L) by soldering J3-T-PM to a pin-fin baseplate or directly to the inverter's cooling structure
- // Enabling scalable power level design concepts, from 80 kW to over 300 kW, to meet the growing demand for high power-density

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As shown in Figure 2, several generations have been introduced, featuring optimized cell sizes, improved carrier doping profiles and gate structures. Currently, Mitsubishi is steadily advancing forward developing next generations of innovative Planar SiC-MOSFETs as well as Gen.4~ Gen.5 with Trench structures. In parallel with the existing 6-inch facility, the full introduction of a new advanced 8-inch SiC wafer processing plant is scheduled for 2026 [2, 3]

Due to their various attractive features that meet e-Mobility requirements, Trench SiC MOSFET devices are of particular focus.

The following subsections will highlight some of the key innovative design concepts and technologies that have contributed to Mitsubishi Electric's success in optimizing the challenging trade-offs of trench-structures. Further, promising recent study results on the influence of proton implantation on SiC MOSFET electrical characteristics and bipolar degradation suppression will be discussed.

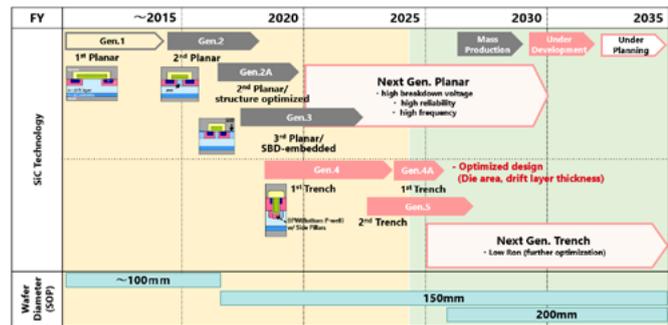


Figure 2: SiC MOSFET Roadmap

Optimizing Rdson vs Short-Circuit-Capability vs Switching-Loss Trade-off

One of the key advantages of Trench gate SiC MOSFET is that it realizes low on-resistance (low DC-losses/high-efficiency) because of its improved channel structure and high MOS channel density. However, high conductivity means it is extremely difficult to ensure short-circuit capability if a short-circuit occurs in the device. Hence, incorporating additional methods for controlling short-circuit capability in the device structure design is essential. Another important trade-off aspect to consider is the classical DC-loss vs Switching-loss where optimization is also essential. To address these important trade-offs, Mitsubishi Electric has developed proprietary trench-type SiC-MOSFETs with a unique structure that enables lower resistance, higher reliability and lower switching losses [4, 5]. The schematic of the developed trench SiC-MOSFET structure is shown in Figure 3 and its key features are realized by three unique implanted layers briefly summarized in the following:

- (1) P-type protective layer (BPW: Bottom P-Well) for relaxing the electric field applied to the bottom of the trench,
- (2) Sidewall P-type pillar (SP: Sidewall Pillar) for grounding the BPW, and
- (3) N-type Junction Field Effect Transistor (JFET) doping layer (JD: JFET Doping) for preventing narrowing of the current path.

Highlighting the unique feature of this structure, by adjusting the area density SP ratio (r_{SP}), defined as SP area/sidewall area, trade-off control between on-resistance and short-circuit capability could be realized as shown in Figure 4 (a-c). For example, designing r_{SP} as 2, a favorable performance of short circuit withstanding time (t_{SC}) of 2.2 μs with $R_{on,sp}$ as low as 2.2 $m\Omega cm^2$ @RT and 3.9 $m\Omega cm^2$ @150°C could be achieved.

Further, switching evaluation results confirmed that higher r_{SP} leads to lower loss at turn-off (E_{off}) and higher loss at turn-on (E_{on}). To compare with regards to the total DC and AC losses, calculations based on $R_{on,sp}$ @150°C; E_{on} and E_{off} @ $R_g=5 \Omega$ at the assumption of 20 kHz switching frequency with 49% duty cycle were performed. As shown in Figure 4(d), r_{SP} optimization brings improved t_{SC} without increase in AC loss but at the penalty of a slight increase

in DC loss. Hence, because of the developed structure, the trade-off relationships between DC/AC losses and t_{SC} can be adjusted by designing r_{SP} in accordance with the specific application requirements. This flexible performance controllability represents a clear improvement over conventional trench SiC-MOSFET structures.

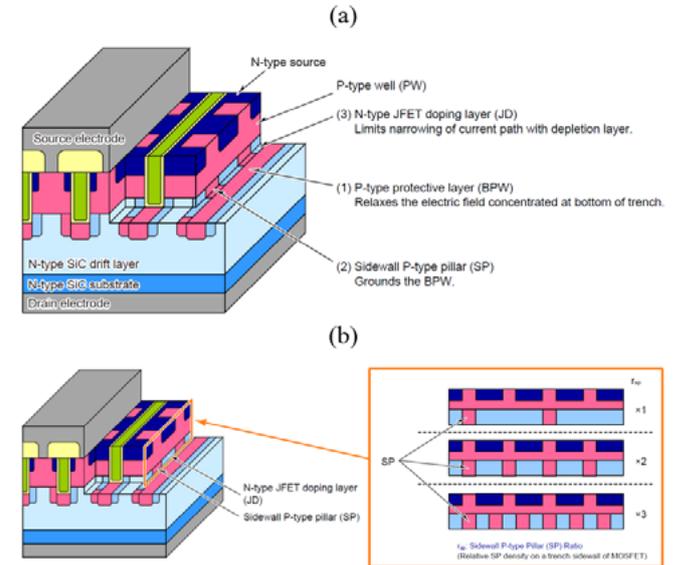


Figure 3: (a) Schematic of Mitsubishi proprietary trench SiC-MOSFET structure and (b) its controllable Sidewall P-type Pillar (SP) Ratio r_{SP}

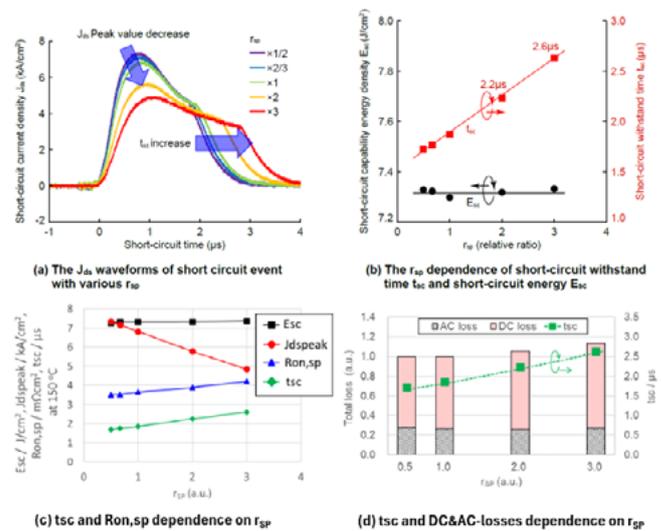


Figure 4: (a) waveforms of short circuit event with various r_{SP} (b) short-circuit withstand time t_{SC} and short-circuit energy E_{sc} dependence on r_{SP} , (c) t_{SC} and $R_{on,sp}$ dependence on r_{SP} , (d) t_{SC} and DC&AC-losses dependence on r_{SP}

Realizing proton implantation positive influence on SiC MOSFET electrical characteristics and bipolar degradation suppression
 Rather than adding an externally paralleled Schottky barrier diode (SBD), utilization of the body-diode of SiC MOSFET devices represents a very important aspect to realize compact and cost-effective power device solutions. However, bipolar degradation is a key issue that must be addressed when utilizing the bipolar operation in SiC power devices. Suppression of bipolar degradation with proton implantation technique has been reported as a possible approach. However, proton implantation is a complex process that can have both positive and negative effects on the electrical characteristics of 4H-SiC MOSFETs. Understanding these effects is crucial for designing and optimizing SiC power devices, particularly for automotive applications [6]. Following an optimized proton implantation approach, Mitsubishi Electric fabricated and evaluated, on experimental bases, very large numbers of proton implanted 4H-SiC

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MOSFETs (about 4,000 chips) to verify statistically its effectiveness in the suppression of the bipolar degradation as well as to consider its technological applicability to mass production process.

The cross-sectional schematics and flowchart of the evaluated SiC MOSFETs with and without proton implanted layer is shown in Figure 5 (a) and (b) respectively. The applied proton doses are $1 \times 10^{12}/\text{cm}^2$, $1 \times 10^{13}/\text{cm}^2$ and $1 \times 10^{14}/\text{cm}^2$.

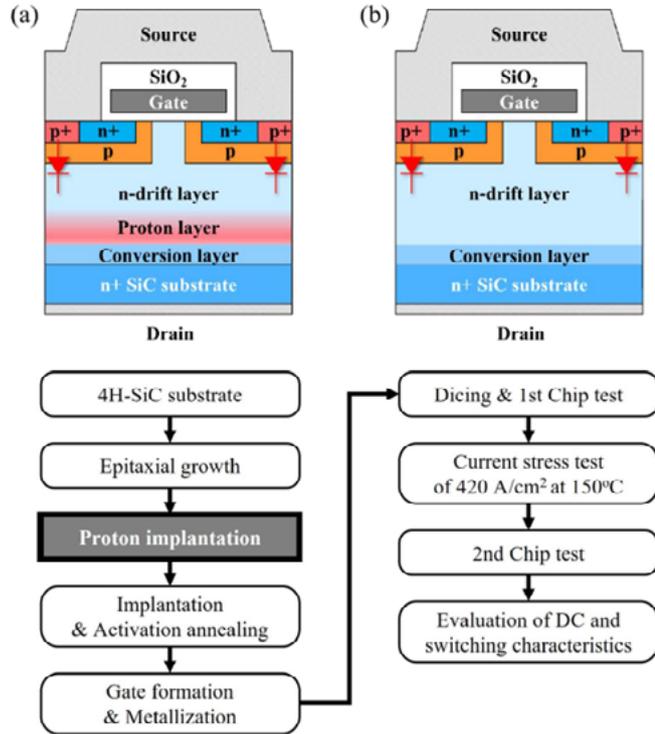


Figure 5: Schematics and flow chart of evaluated SiC MOSFETs (a) with proton implanted layer and (b) without proton implanted layer

After passing the initial 1st chip test, the fabricated devices were stressed by applying continuous current (typically, $V_{GS}=0$ V, $t=2$ min, $T=150^\circ\text{C}$ and $J_{SD}=420$ A/cm²) to the body diodes to evaluate the bipolar degradation suppression level. The reference for a “degraded” device was defined as an on-resistance increase of over 3% after the current stress. The numbers of the tested samples were 1270 (w/o), 880 ($1 \times 10^{12}/\text{cm}^2$), 844 ($1 \times 10^{13}/\text{cm}^2$) and 823 ($1 \times 10^{14}/\text{cm}^2$).

A summary of the DC-characteristics evaluation results after the current stress can be explained with the help of Figure 6 in the following:

- The positive impact of the proton implantation on the suppression of the SiC MOSFET bipolar degradation is clearly evident from these experimental results.
- With a proton dose of $1 \times 10^{14}/\text{cm}^2$, degraded MOSFET ratio significantly drops to about 3%, which is roughly 1/4th the value without proton implantation.
- The forward DC-characteristics were not influenced, and the only noticeable change was in the 3rd-quadrant (I_{SD} -vs- V_{SD} @body-diode mode) with an increase in the differential on-resistance (Figure 6(a) & (b)) and clear suppression of temperature dependence @ a proton dose of $1 \times 10^{14}/\text{cm}^2$ (Figure 6 (c)).
- With the body diode conducting only during the dead time under normal pulse width modulation (PWM), this 3rd-quadrant change is considered insignificant because it hardly affects the total loss.
- On the contrary, the suppression of temperature dependence in the 3rd-quadrant can be considered another positive impact of the proton implant because it helps eliminating current-imbalance among paralleled chips. In other words, this helps to evenly distribute dead-time current-stress among paralleled body-diodes instead of being focused on the hottest chip.

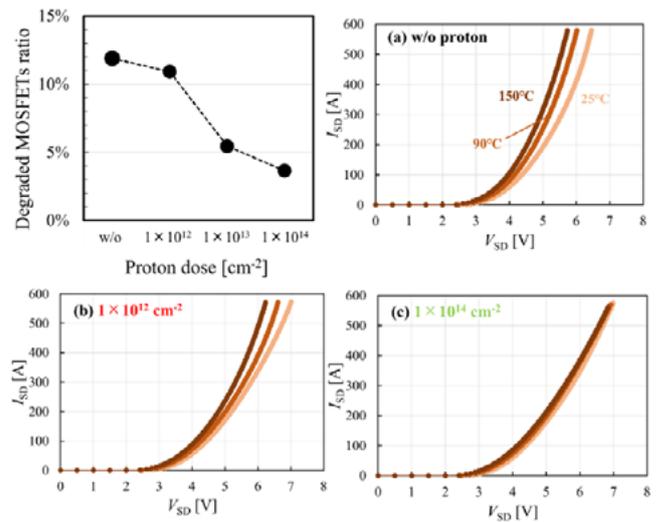


Figure 6: The ratio of the degraded MOSFETs after current stress in each proton dose condition and the influence on the body-diode 3rd-quadrant ($V_{GS}=-10$ V).

Finally, the impact of the proton implant on the switching characteristics of the body diode of current-stressed samples was evaluated under the conditions: Double pulse testing @ $V_{DS}=760$ V; $I_{DS}=380$ A; $V_{GS(lower)}=-5$ V; $V_{GS(upper)}=-5/+22$ V; 150°C .

A summary of the switching-characteristics evaluation results after the current-stress can be explained with the help of Figure 7 in the following:

- The positive impact of the proton implantation on the suppression of the SiC MOSFET reverse-recovery oscillations as well as surge-voltage is clearly evident from these experimental results.
- With a proton dose of $1 \times 10^{14}/\text{cm}^2$, SiC MOSFET body diode waveforms show favorable recovery characteristics enabling faster switching speeds for higher efficiency with less EMI noise concerns
- Significant Q_{rr} and ΔV reduction (58% and 96% respectively in this example) enabling higher efficiency and safe SiC MOSFET operation

Given the achieved promising results summarized above, establishing a suitable proton implantation condition will surely open the way for its introduction to the future mass production of bipolar-tolerant and reliable SiC MOSFETs. Further comprehensive optimization investigations are ongoing considering performance and other factors.

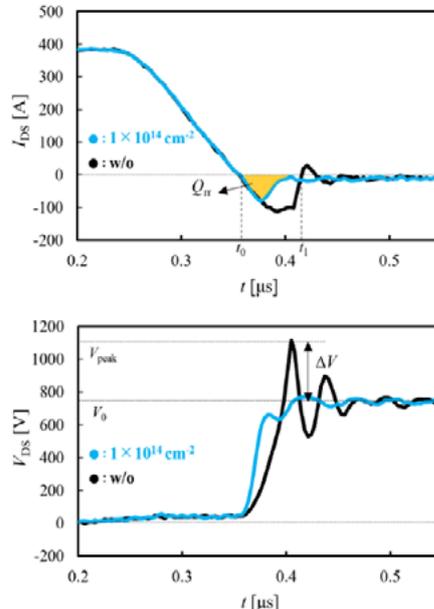


Figure 7: Reverse recovery waveforms of the body diode of current-stressed samples with&w/o proton implantation

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At the end of Part-1 of this article, a brief representative example of the performance capability of Mitsubishi Gen.4 Trench SiC-MOSFET chips when installed on the scalable J3-Series automotive modules is given in Figure 8. The example is based on inverter output RMS current vs switching frequency at an operating temperature of 175°C, with a main battery voltage of 800V, coolant temperature of 65°C, and coolant flow rate of 10 l/min.

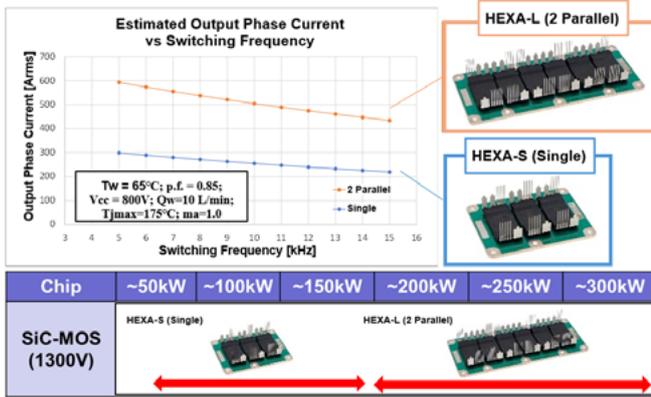


Figure 8: Representative example of the performance capability of Gen.4 Trench SiC-MOSFET chips on the scalable J3-Series automotive modules

Part-2

Evolution of Mitsubishi Electric’s RC-IGBT

The Reverse-Conducting Insulated Gate Bipolar Transistor (RC-IGBT) is an advanced power semiconductor device developed and continuously refined by Mitsubishi Electric. Designed to enhance efficiency, reduce system size, and lower overall costs, the RC-IGBT integrates both the IGBT and the freewheeling diode into a single chip which eliminates the need for an external diode, as required in traditional IGBT-based systems. This integration not only simplifies circuit design but also reduces component count and wiring between dies.

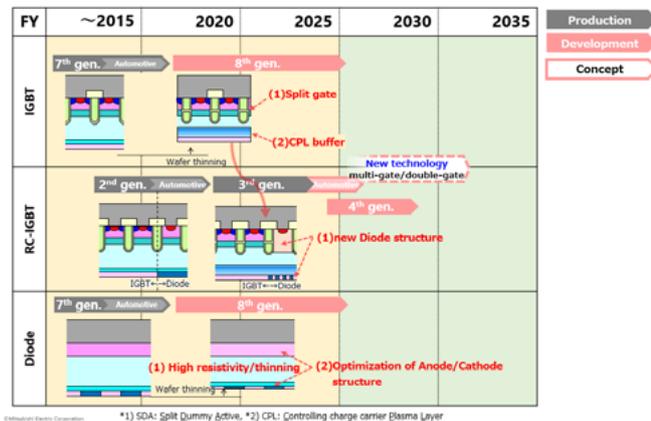


Figure 9: Transition of RC-IGBT Development

Figure 9 illustrates the evolution of RC-IGBT development at Mitsubishi Electric. In 2006, the company launched the world’s first-generation RC-IGBT, marking its initial application in motor control power modules for white goods [8, 10]. Building on this success, Mitsubishi Electric introduced the second-generation RC-IGBT in 2015 [9]. This version based on latest development of Carrier-Stored-Trench-Gate-Bipolar-Transistor (CSTBT™) at that time (7th Gen IGBT) structure optimized through microfabrication and thin-wafer technology, significantly reduced conduction and switching losses. Initially used in industrial applications, it was later adopted for automotive applications due to its superior performance. Currently, Mitsubishi Electric is developing the third-generation RC-IGBT based on 8th generation of CSTBT™ and diode. The advanced technologies and design improvements that is implemented in this generation will be highlighted in the following sections.

Advantages of Single-Chip RC-IGBT

This single-chip solution integrating both IGBT and free-wheeling diode offers several advantages over conventional discrete-component designs in terms of thermal performance, electrical efficiency, and mechanical integration.

1. Optimized Chip Utilization and Module Miniaturization

The shared structures such as the guard ring can be utilized. This not only reduces the total chip area required but also eliminates redundant or unused spaces between separate components. As a result, module size can be significantly reduced, contributing to more compact system designs.

2. Improved Heat Dissipation Through Chip Integration

In motor control applications, the diode can generate a large amount of heat in a short time, especially under fault conditions such as a motor lock. This instantaneous heat generation poses a challenge for thermal design and can restrict the allowable current through the system.

RC-IGBT addresses this condition by physically integrating the IGBT and diode into the same silicon die. This integration leads to:

- Expansion of the heat dissipation path: Thermal energy can spread more evenly across the larger, unified chip area, refer to Figure 10 (a).
- Reduction of thermal resistance: A single heat flow path reduces the temperature rise during high-load operation.

Due to staggered heat generation between the IGBT and the diode, they do not produce peak heat simultaneously. This temporal separation reduces thermal stress, improving the overall reliability and current-carrying capability of the device.

Electrical Performance Gains Through Simplified Internal Wiring

In traditional module layouts with separate chips, longer internal wiring is required for interconnection. The resulting high parasitic inductance can degrade switching performance and increase EMI. By integrating the components into a single chip, internal wiring can be significantly shortened (refer to Figure 10 (b)), reducing inductance and associated voltage spikes during switching which leads to:

- Greater design flexibility: Internal layouts can be optimized to suit various thermal or electrical requirements.
- Better use of space: The saved space can be used to incorporate larger chips for increased current capacity, or to shrink the module further, supporting miniaturization of the final product.

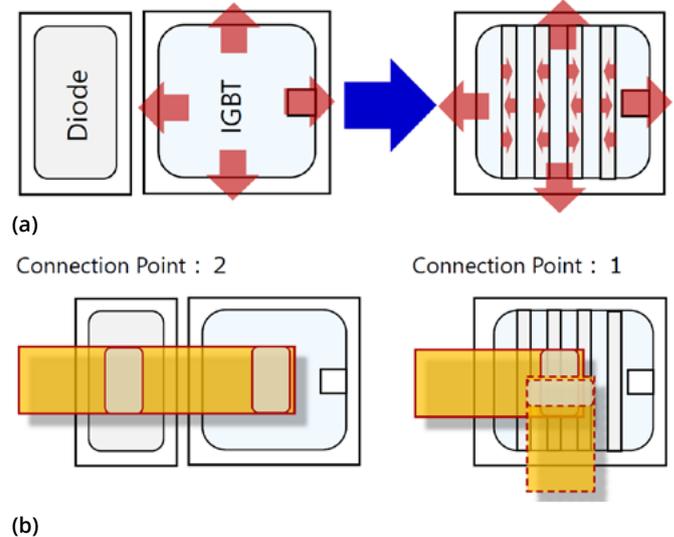


Figure 10: Benefits of integrating IGBT and FWD into one Chip (a) improved heat dissipation (b) simplifying internal wiring

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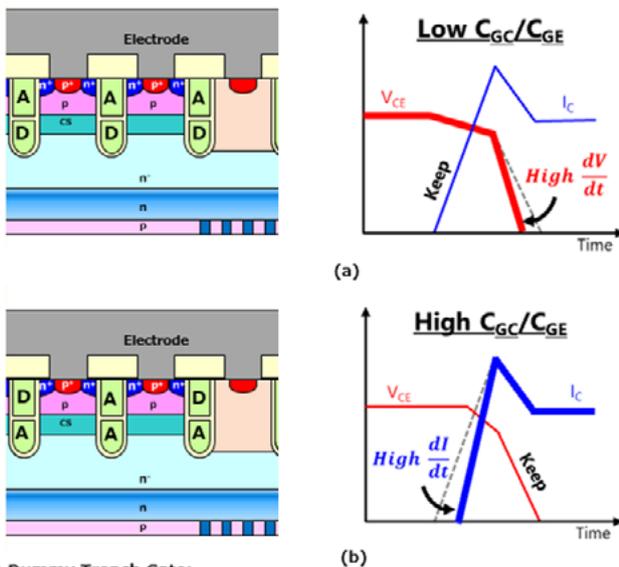
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3rd Generation Reverse Conducting IGBT

The design of RC-IGBT requires not only the technology to reduce power loss by optimizing the structure inside the IGBT and thinning the wafer, which are common issues with single IGBTs, but also the technology to improve heat dissipation through the free-diode structure design and layout design inside the chip, which are unique to RC-IGBTs. The following four technologies are considered in the design optimization or 3rd Gen RC-IGBT to meet both reliability, power losses and thermal design requirements [10].

a) Optimization Technology for Gate Capacitance of MOS Structure

To reduce switching loss, recent advancements focus on optimizing gate capacitance. Conventional gate control adjusts the gate resistance (R_g), but this simultaneously affects both di/dt and dV/dt , limiting optimization. To overcome this, the 3rd Gen RC-IGBT introduces a two-stage trench gate structure as shown in Figure 10, enabling independent control of CGE and CGC. This expands the tunable range of the CGC/CGE ratio, allowing targeted improvement of either di/dt or dV/dt without compromise. For example, with Split gate technology (Figure 11 (a)) lowering CGC/CGE increases dV/dt , reducing turn-on loss (E_{on}) by 20%, while increasing CGC/CGE using SDA technology (Figure 11 (b)) boosts di/dt , cutting E_{on} by 38%. These capacitance optimization techniques are applicable to both single IGBT and RC-IGBT structures.



D: Dummy Trench Gate; A: Active Trench Gate

Figure 11: Schematic cross-sectional views of (a) Split gate (b) Split Dummy Active (right)

b) Thin Wafer Technology Using New Buffer layer

The most effective way to reduce conduction loss in IGBTs and free-wheeling diodes is to reduce the thickness of the wafer, however, this has the trade-off that the IGBT's SCSOA capability deteriorates. One way of adjusting the SCSOA is by lowering the concentration of the CS layer. Another indirect improvement effect on the SCSOA trade-off can be realized by a new buffer technology for Controlling charge-carrier Plasma Layer (CPL) developed mainly to suppress switching surges. CPL is a layer formed in the backside buffer region by a high-energy implantation of light elements and a low-temperature annealing process. By applying CPL, it is possible to suppress the increase in the electric field strength on the emitter side during SC operation particularly at room-temperature. By applying it to a CSTBT rated at 1200V/230A for instance, wafer thickness was reduced by approximately 10% while maintaining the SC capability, hence improving the conduction loss. In addition, the implementation of CPL solved the issue of the snap-off behavior during turn-off as it allows holes to remain in the backside prevent-

ing a rapid depletion of the carriers during surge voltage. Suppressing this phenomenon also enables reducing of wafer thickness.

c) RC-IGBT Chip Diode Placement Technology

In RC-IGBT, the IGBT and diode interfere with each other, so the boundary can cause an increase in on-state voltage, but since they also function as heat dissipation, the thermal resistance can be reduced and the power density can be increased compared to conventional methods. Since the IGBT's area is larger, the diodes are placed in within the area of the IGBT. The layout can be classified into stripe layout and island layout.

From a heat dissipation perspective, the island layout with a longer boundary length is advantageous. Accordingly, for the 3rd Generation RC-IGBT, a high-density island arrangement was developed to meet the stringent thermal management requirements of automotive applications. By increasing the diode density, heat dissipation efficiency was improved (T_j was reduced by 18%) and resulted in enhanced thermal distribution, effectively dispersing localized heat. The chip diode technology implemented in the 3rd Generation RC-IGBT also addresses snapback behavior in the I-V characteristics, ensuring a stable performance.

As shown in the experimental results in Figure 12, the device effectively mitigates excessive transient heat generated during IGBT short circuit testing. Furthermore, by finely arranging the Diode layout, the short-circuit withstand time is improved by 34% compared to the conventional stripe layout, demonstrating the superior thermal and electrical robustness of the technology.

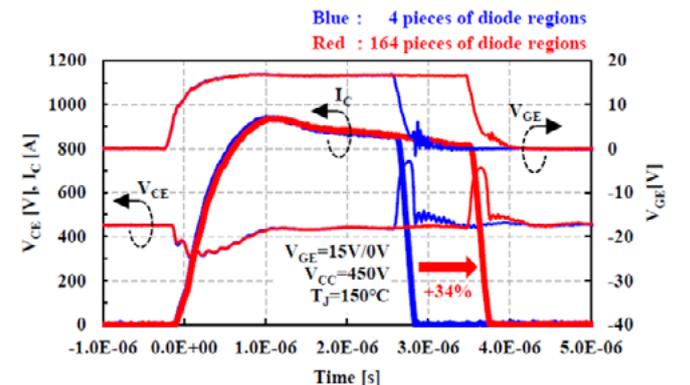


Figure 12: SCSOA of 3rd Gen. RC-IGBT with low and high density diode regions

d) Carrier Injection Diode Structure for RC-IGBT

To enhance RC-IGBT performance, a low-carrier injection diode structure was developed as demonstrated in Figure 13 to reduce recovery losses while maintaining ohmic contact. Key improvements include:

- Low-Concentration Anode Layer: The conventional anode layer is replaced with a lower-doped one, using a partial contact p+ layer to maintain good ohmic contact and suppress hole injection.
- Partial Cathode Layer: A selectively formed cathode layer (via precise photolithography process) limits carrier injection from the cathode while ensuring ohmic contact with the Al-based electrode. Optimizing the anode-cathode structure enables characteristic adjustment without lifetime control, achieving higher T_j by suppressing leakage current.
- Additionally, Local Lifetime Control: Proton implantation is applied to reduce carrier lifetime, further cutting tail current and switching losses in both the diode and IGBT regions.

These optimizations balance injection control and conductivity, enhancing efficiency and reducing losses in 3rd Gen. RC-IGBT.

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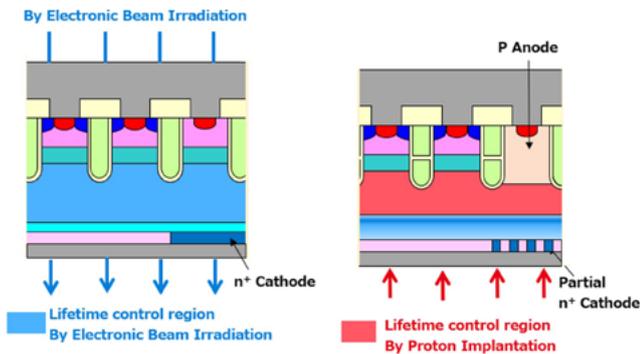


Figure 13: Schematic cross-sectional views of 2nd Gen. RC-IGBT (left) and 3rd Gen. RC-IGBT (right)

T_{vj} Simulation performance of RC-IGBT with J3 package

Despite the 3rd Generation RC-IGBT having a 22% smaller active area compared to the 7th Generation chipset, it achieves a 20% reduction in thermal resistance.

The current handling capability of the 3rd Gen. RC-IGBT was evaluated through simulations based on device characterization data and the resulted thermal resistance (see Figure 14). The simulation parameters were as follows: main battery voltage = 400 V, PWM switching frequency (f_{sw} = 6, 8, and 10 kHz, coolant temperature (T_w) = 65°C, and coolant flow rate = 10 L/min. Under 8 kHz switching, the inverter output current exceeds 250 Arms, while maintaining a maximum junction temperature below 175°C. Compared to the 7th Generation IGBT chipset, the 3rd Gen. RC-IGBT demonstrates improved performance.

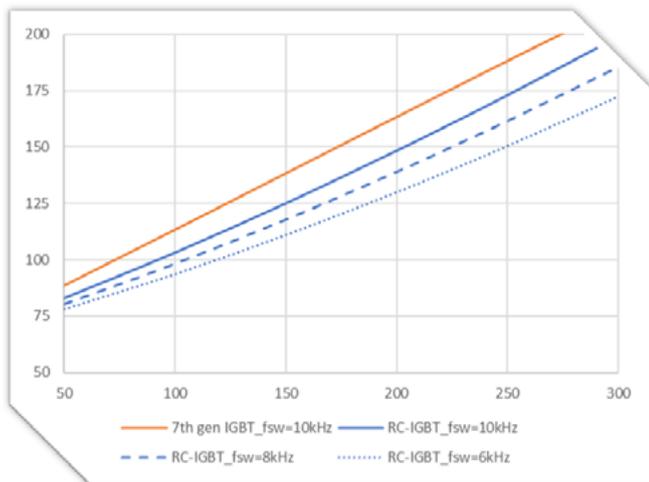


Figure 14: T_{vj} simulation of J3 based RC-IGBT

Closing Remarks

Mitsubishi Electric is steadily moving forward in advancing its next generation of innovative efficient semiconductor bare-dies (SiC MOSFET & SiC-IGBT) and compact high-reliability transfer mold packaging (T-PM) towards scalable, cost-effective, and reliable e-Mobility solutions.

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Increasing Power Density using Low Voltage eGaN FETs in High-Voltage Server Power Supplies – Part 3: ISOP LLC Converter

By Alejandro Pozo, Michael de Rooij, and Marco Palma, all Efficient Power Conversion

Introduction

In part one of this series, we presented some of the benefits of multilevel topologies for the AC/DC and Isolation DC/DC stages in a server power supply. A brief introduction to popular examples of both were presented.

Part two of the series focused on the AC/DC stage and showed the key features of a four-level totem-pole PFC converter. Details of the hardware and control algorithm were shown, as well as its performance when operating from a 240 V_{AC} input and delivering up to 5 kW into a 400 V_{DC} bus.

In this third and last part of the series we delve into the Isolated DC-DC converter that follows the PFC. Figure 1 shows the block diagram of a fixed-ratio converter, with four LLC modules arranged in an input-series, output-parallel (ISOP) configuration. The converter can process up to 5.5 kW between the 400 V_{DC} input bus and a 50 V_{DC} output bus, while offering galvanic isolation between them.

Converter Overview and Benefits

The converter shown in Figure 1 utilizes four isolated LLC converters in an ISOP configuration. It has an overall input-to-output voltage ratio of 8:1, so each LLC converter only experiences a quarter of the input voltage and processes a quarter of the total output power. As a result, low voltage devices with better figures of merit than high-voltage components [1, 2] can be used. Moreover, the design of each LLC converter is greatly simplified due to the lower power rating needed as well as the lower conversion ratio required of 2:1. In this example, when the input voltage is 400 V_{DC} with a total output power of 5.5 kW, each LLC module only has 100 V at its input and delivers 1375 W into the common 50 V output.

The topology selected for each LLC module is based on a primary half-bridge with split capacitors, and a center-tap full-wave rectifier. The same 150 V-rated and 2.2 m Ω -typical GaN transistors, EPC2305 [3], are used in the primary and rectifier sockets of the LLC. This is possible because in this implementation all FETs experience the same voltage stress and similar RMS current. Consequently, a minimum FET count is realized for each module, unlike Ma et al [4], and the design of the transformer is greatly simplified, enabling a planar solution with the windings built into a printed circuit board (PCB) with as low as 8-layers.

A key property of ISOP LLC converters is its ability to self-balance the input voltages for each module without a dedicated circuit or control algorithm [4]. This is achieved by design using a high magnetizing inductance (L_m) to resonant inductance (L_r) ratio, yielding a wide frequency range around the operating point in which the gain is largely independent of component tolerances.

In addition, the configuration discussed in this article renders additional benefits compared to a single module solution. First, is the possibility to phase shift the operation of each LLC module to reduce the output current ripple and minimize the total output capacitance. Second, the lower voltage stress on all the components within each LLC module allows smaller size and lower component height. And third, the distributed nature of the power losses over a larger area simplifies the thermal solution.

Hardware

Figure 2 shows the hardware implementation of the experimental 400 V to 50 V, 5.5 kW ISOP LLC converter. It was designed to meet the physical dimensions specified by the Open Compute Project (OCP) ORv3 48 V PSU Specification [5]. The unit consists of a motherboard and four identical LLC-module boards, two plugged into the top side and two on the bottom side of the motherboard.

The motherboard also hosts the controller, a dsPIC33CK from Microchip, input and output bus ceramic capacitors, and signal and power connections to each LLC module. The LLC modules are implemented on four identical boards, each with all the necessary components to be operated as a standalone 100 V to 50 V, 1375 W isolated converter.

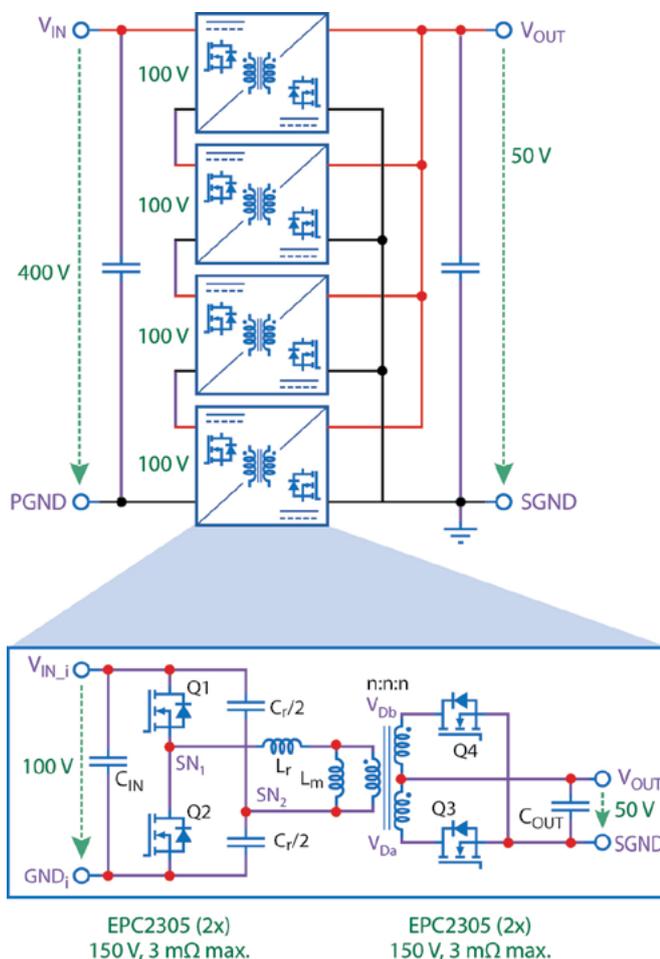
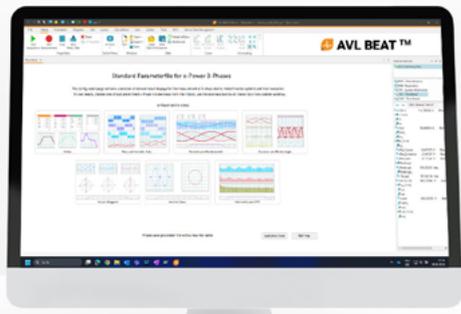


Figure 1: Block diagram of the ISOP LLC converter and simplified schematic of the LLC modules.



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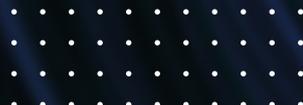
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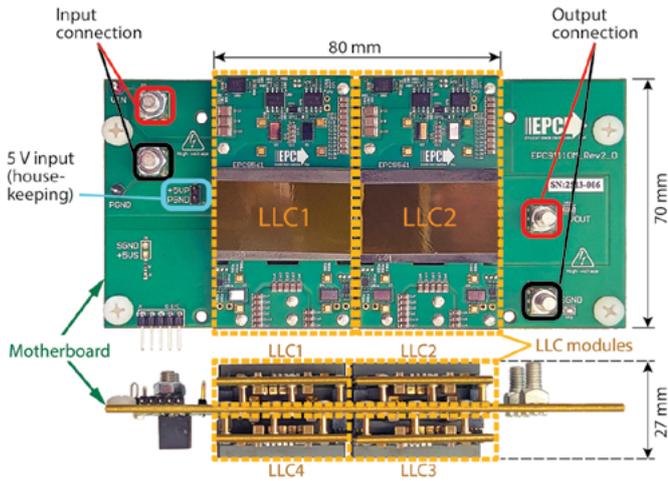


Figure 2: Top and front photos of the EPC91110KIT ISOP LLC converter [6].

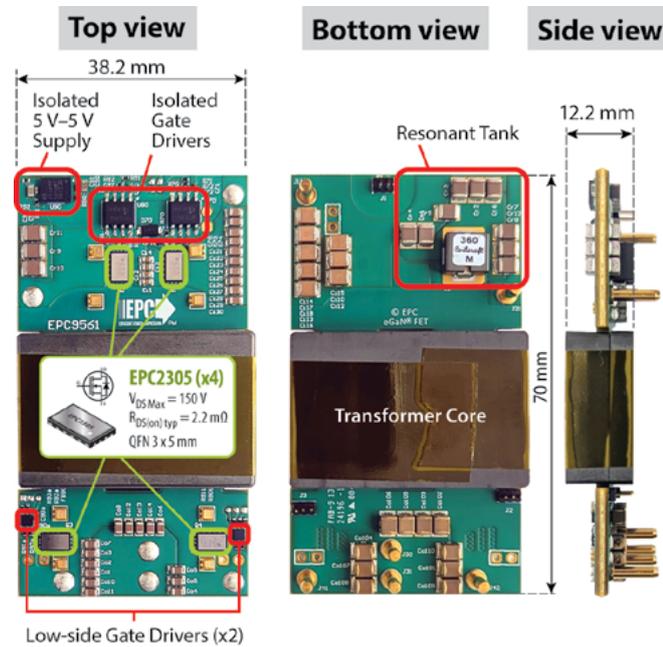


Figure 3: Photos of the LLC-module board with various components highlighted.

Figure 3 shows photos of one LLC module with the main components highlighted.

The GaN transistors in the primary side of the LLC are controlled with two isolated gate drivers. In all the modules, the input side of the gate drivers is referenced to the secondary-side ground (SGND in Figure 1), common with the controller. The output side of the gate drivers is different for each module (GND_i in Figure 1), depending on their relative position within the ISOP configuration. A small isolated 5 V – 5 V power supply [7], combined with a conventional bootstrap circuit, is used to power the output side of the isolated gate drivers within each module.

The transformer core is based on a standard E + I geometry using Proterial's ML95S material, although other materials were also tested with some differences in performance. The windings of the transformer are built into 6 of the 8 layers of the PCB, with a copper thickness of 2 oz. The airgap of the core was adjusted to realize ZVS turn-on in the primary FETs. The resonant tank, mostly located on the bottom side of the PCB, comprises several COG ceramic capacitors and an external 36 nH ferrite-based inductor to establish a resonant frequency of approximately 1 MHz. The switching frequency of the GaN FETs is set to match the resonant frequency to minimize losses.

Experimental Results

The experimental unit shown in Figure 2 was operated between a 410 V_{DC} input and a 51 V_{DC} output while delivering up to 5.5 kW. Two transformer variants were evaluated using the same converter schematic and components, transformer core geometry, PCB stack-up, and turns ratio. With the only difference between variants being the number of turns for each winding. Efficiency and power losses for both designs are provided in Figure 4. One variant uses a 2:2:2 turn transformer, having one PCB layer for each turn, while the other variant uses a 1:1:1 turn design, where each winding comprises two turns in parallel. The former achieves a peak efficiency of 98.5% and full-load efficiency of 97.5%, while the latter reaches 98.2% peak efficiency and approximately 98% at full load. These numbers are the result of a trade-off between core losses, which dominate the low-load losses for the 1:1:1 design, and winding losses which are the main loss mechanism in the 2:2:2 variant.

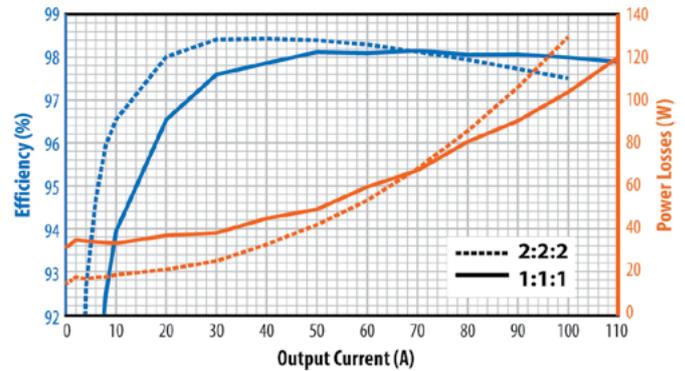


Figure 4: Efficiency and Power Losses with Vin = 410 VDC, Vout = 51 VDC, operation for two transformer variants.

Concurrently, the input voltages for each LLC module within the converter were recorded for both transformer variants at various output powers. The results are presented in Figure 5, demonstrating excellent voltage sharing among the modules to within 2% of the 100 V.

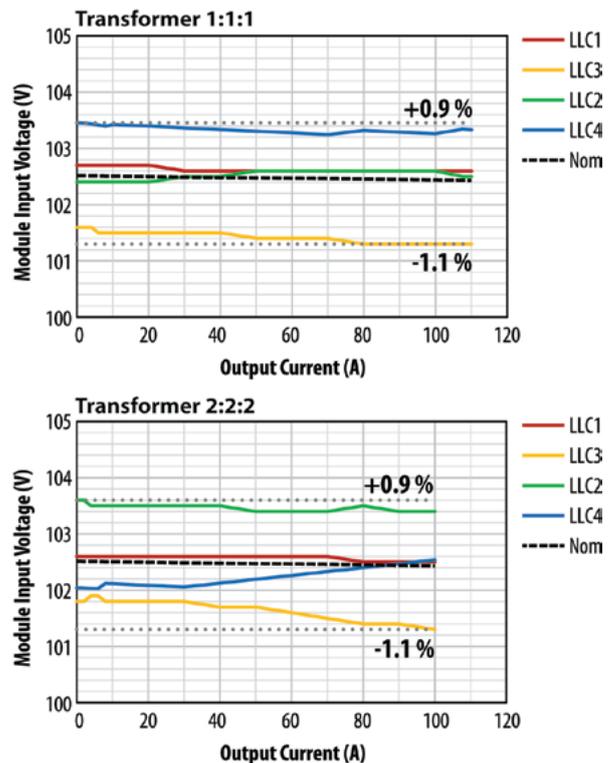


Figure 5: Differential input voltages of all LLC modules for both transformer variants operating from a 410 V input bus and delivering up to 5.5 kW into a 51 V bus.

Scalability to high voltage and higher power

The growth in Artificial Intelligence (AI) caused the data center electricity usage to more than double between 2017 and 2023, and the trend is expected to accelerate even more in the next few years [8]. This increasing demand for power is driving changes in the architecture of the power distribution in server racks, shifting from a 50 V_{DC} distribution bus to an 800 V_{DC} or ±400 V_{DC} bus [9]. Fortunately, the ISOP converter presented in this article can be easily repurposed as an 11 kW, 800 V to 50 V or a ±400 to 50 V, without significant changes to the LLC module and overall converter, by simply adding additional modules to the ISOP configuration.

With the goal to increase the processing power per rack (i.e. more GPUs per rack), changes in the server rack are expected to extend beyond the power supply, as we have seen recently in prototypes from some of the key players in the industry [10]. In this new architecture the isolation stage is integrated into the IT motherboard. Liquid cooling and a more demanding height restrictions increase the need for higher power density, while requiring even larger conversion ratios such as 16:1 (800 V_{DC} – 50 V_{DC}) or 64:1 (800 V_{DC} – 12.5 V_{DC}). Therefore, the benefits of a modular approach like the ISOP LLC converter discussed in the previous sections could become the enabling technology.

Conclusions

This article presented a fixed-ratio, 5.5 kW, 400 V_{DC} to 50 V_{DC} isolated converter using only 150 V-rated GaN transistors in a simple ISOP configuration. The experimental results demonstrate peak efficiencies well above 98% and full load efficiency of 98% while achieving a power density of 596 W/in³ (36.4 W/cm³). Self-balancing of the cascaded LLC inputs is realized by design, avoiding dedicated components or control schemes. Moreover, the combination of ISOP LLCs with low-voltage GaN devices offers an ideal solution for the increasing demand for power in servers.

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LTO Batteries for Peak Shaving in Mobile and Stationary Applications

Batteries for peak shaving must withstand a very high number of charge and discharge cycles. With peak shaving, smaller generators or grid connections with lower output can be used, and costly infrastructure investments can be reduced. This article explains the battery requirements involved and highlights the unique characteristics of Lithium Titanium Oxide (LTO) batteries compared to other battery chemistries.

By Sacha Rupp, Senior Manager Battery Division, Toshiba

Peak shaving refers to the targeted reduction of peak loads on the consumer side through the use of supportive battery systems to efficiently cover short-term energy demands. This does not involve increasing energy generation, but rather using stored energy to offset temporary peaks.

Many companies have highly fluctuating energy demands, for example, in generator and crane applications, which can involve the simultaneous operation of several machines, the startup of production systems, or the heating of boilers. Without buffering these peak loads, grid connections or generators would have to be dimensioned for the maximum peak load, resulting in high costs and inefficient use.

Why peak shaving?

The main goal of stationary battery storage systems is to store energy. In photovoltaic (PV) systems, for instance, energy generated when the sun is shining is stored and used at a different time when needed. This creates requirements for maximum capacity at minimum cost. The key metric is the cost in euros per kilowatt-hour (kWh) of installed capacity. However, this capacity is used relatively infrequently. In PV systems, the battery is charged and discharged at most once per day, usually only a fraction of a full cycle, and at a slow rate over several hours. The situation is entirely different in peak shaving. Here, the battery is not used to store energy but rather to deliver the power needed to balance load peaks. The primary demands on the battery are reversed: instead of maximizing capacity, the aim is to deliver as much power as possible with minimal capacity. The more frequently the battery can help avoid peaks, the greater its value. The main objective of a peak shaving battery is therefore not to store a lot of energy, but to use the stored energy as efficiently as possible. The decisive cost factor is euros per GWh of energy used over its lifetime. This results in the following requirements:

Battery requirements for peak shaving

Batteries for peak shaving must withstand a very high number of charge and discharge cycles. While a PV system might complete an average of 0.5 cycles per day, adding up to 1,800 full equivalent cycles over ten years, a peak shaving battery used 10 times a day must withstand 36,500 cycles over the same ten-year period. These cycles generally contribute to the ageing of lithium-ion batteries. The number of possible cycles strongly depends on the specific energy density of the battery cells. The higher the energy density, the faster the cells age due to cycling. Lithium nickel manganese cobalt oxide (NMC) cells with the highest energy densities of over 250 Wh/kg last only a few hundred cycles before reaching end-of-life at 80% of their original state-of-health (SoH) capacity. Lithium iron phosphate (LFP) cells with a slightly lower energy density of around 150 Wh/kg usually last a few thousand cycles. LTO (Lithium Titanium

Oxide) cells store the least energy (~100 Wh/kg) but can withstand tens of thousands of cycles even under demanding load profiles. Another challenge is the significantly higher charge rate (C-rate) in peak shaving. The C-rate indicates how fast a cell can be charged or discharged relative to its capacity. For example, a 10 Ah cell charged at 10 A is at 1 C and would fully charge in one hour. If large load peaks are to be covered with a small battery, the cells must withstand high C-rates during discharge and recharge. C-rates also affect battery ageing. Rapid charging above 1 C accelerates ageing in NMC and LFP cells. The graphite anode cannot absorb lithium ions quickly enough, leading to lithium plating (discussed below), especially at low temperatures and high state-of-charge (SOC). This issue does not occur with LTO cells. LTO offers high power density and can be charged and discharged at high C-rates within minutes. Even under continuous 5C/5C usage, an LTO cell survives tens of thousands of cycles. Using conventional Li-ion batteries (NMC or LFP) for peak shaving, therefore, requires significant oversizing. This reduces C-rates to acceptable levels but increases footprint, weight, and cost. Despite this, ageing remains a limiting factor, and regular battery replacement is needed. LTO technology can prevent premature replacement, and its compact design reduces both size and cost. The next section illustrates this with a hybrid generator example.

Advantages of LTO batteries: an example

Hybrid generators, commonly found in mining, construction, outdoor events, and telecommunications, often operate under harsh environmental conditions and extreme temperatures, and comprise conventional diesel or gas internal combustion engines with battery storage systems to manage load peaks efficiently.



Figure 1: The use of LTO batteries in mobile hybrid generators enables the use of generators with lower output.

By integrating a battery, short-term peak loads are absorbed so that the generator does not need to be designed for extreme peak loads. This allows the generator to operate continuously in its optimal power range, increasing reliability and enabling a smaller and thus more cost-efficient generator. In the economic evaluation of battery systems for hybrid generators, the total cost of



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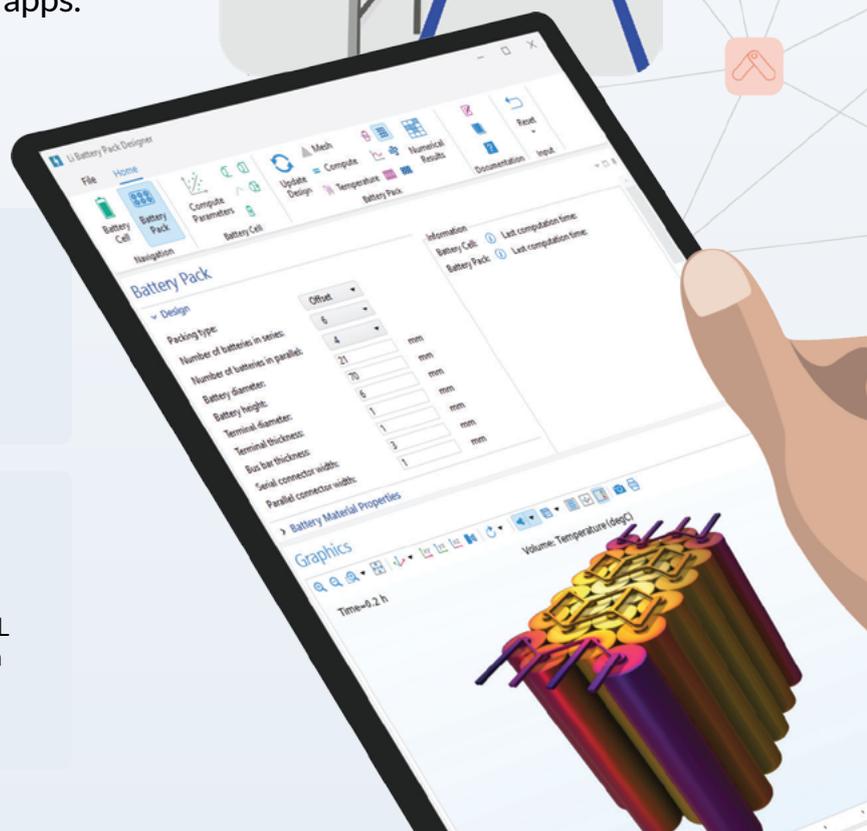
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ownership (TCO) is a crucial factor. The following sample calculation illustrates why LTO batteries, despite higher costs per kWh, can represent a more economical solution than LFP batteries. A key advantage of LTO batteries is their ability to handle high charge and discharge currents, allowing them to be dimensioned much smaller for the same application. In this example, the LTO battery has a capacity of only 15 kWh, whereas a comparable LFP solution requires 60 kWh — four times as much. Although the relative price per kWh for LTO is assumed to be three times higher than for LFP, the acquisition cost of the battery remains lower (45 vs. 60). However, the LTO battery must perform four times more cycles per day with the same energy throughput. Despite the more intensive usage, the service life of the LTO battery is about twice as long as that of the LFP battery. Thus, the TCO over 10 years clearly favors LTO:

	LTO	LFP
Capacity [kWh]	15	60
Relative price/kWh	3	1
Total relative cost	45	60
Equivalent full cycles per day	8	2
Lifetime [y]	10	5
Relative TCO for 10 years	45	120

Figure 2: Toshiba LTO batteries achieve lower TCO compared to LFP cells.

Although LTO initially appears more expensive, the higher cycle stability and smaller system size significantly reduce long-term costs. The LFP battery would need to be replaced within 10 years, thereby increasing the TCO.

Application example: container crane systems

Modern container cranes face the challenge of handling high peak loads while simultaneously reducing operating costs and environmental impact. Hybrid crane solutions with high-performance battery storage systems enable significant efficiency gains through peak load management, energy recovery, and reduced dependence on diesel generators.



Figure 3: In hybrid hoisting or gantry cranes, LTO cells can reduce the consumption of fossil fuels from diesel generators (bottom right).

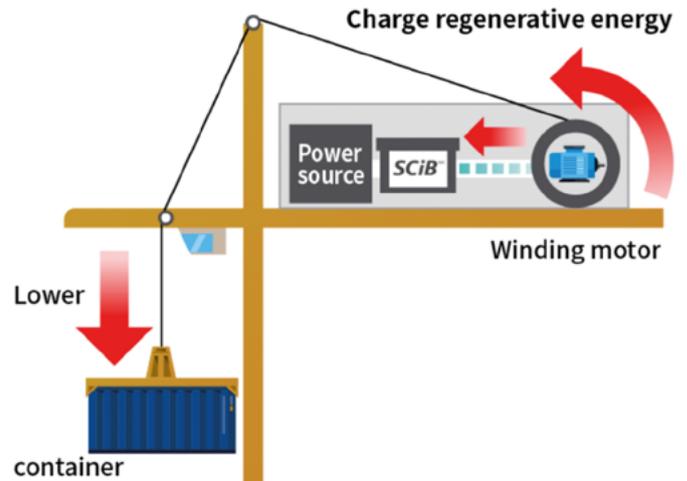


Figure 4: The motion or gravitational kinetic energy generated when lowering loads is fed back into the battery.

The hybrid energy system for container cranes in the example combines a 63kWh LTO battery (SCIB™ high-power modules, 19s3p) with a 30kW diesel generator. This means that the battery with an energy of 63 kWh consists of a configuration of 19 modules in series and 3 in parallel. A total of 57 modules are therefore installed in this battery. Each module in turn consists of a configuration of cells connected in series and parallel. Normally it is then a 2p12s module. Depending on the application, Toshiba's standard, or high-power cells (HP suffix) are used.

While crane operation temporarily demands power levels of 250 to 300 kW, the battery can absorb these load peaks and relieve the generator. As a result, a significantly smaller diesel generator unit is needed, reducing fuel consumption and emissions. Additionally, more than 10% of the energy is recovered through recuperation, further improving overall energy efficiency.

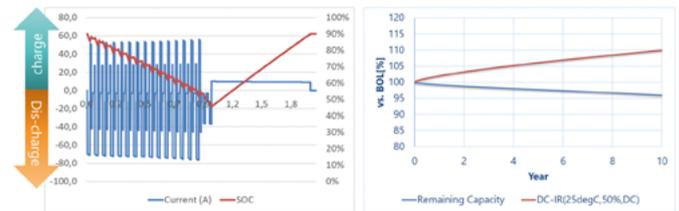


Figure 5: Example load profile of a hybrid crane application.

Figure 5 shows the load profile of this application at the cell level. The battery cells must withstand very high charge and discharge currents of 3–4 C to reliably manage the dynamic load fluctuations. With 14 hours of operation per day (7 load cycles), this results in a daily energy throughput of 471 kWh. This means the battery undergoes 27,375 equivalent full cycles over 10 years. Despite this demanding load profile and extreme cycle stress, the LTO cells retain a remaining capacity of 96 % after 10 years. The combination of a high-performance LTO battery and a reduced diesel generator represents a future-proof solution for the hybrid operation of container cranes. In addition to significant fuel and emissions savings, operators benefit from lower maintenance requirements, stable operating costs, and an extremely long battery lifespan. Thanks to the high performance and recuperation capability, this system offers a sustainable and economical alternative to conventional drive systems in port operations.

LTO battery cell compared to LFP and NMC cells

Why LTO cells can withstand very high charging currents, enable a long service life, and are simultaneously extremely safe lies in the technical design of the Li-ion cell. Each cell is essentially based on four functional components: anode, cathode, separator, and

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electrolyte. While the cathode side is implemented with different materials depending on the desired cell characteristics, such as LFP or NMC, conventional cells almost exclusively use graphite as the anode material. A key exception is the LTO cell, whose electrochemical behaviour fundamentally differs from classical cells due to the use of Lithium Titanium Oxide as the anode material. The anode material used has a decisive influence on a number of electrochemical and physical properties of the cell. In particular, it affects the electrochemical potential of the anode relative to lithium, which in the case of graphite is around 0.1–0.2 V, only slightly above that of metallic lithium. This proximity enables a high cell voltage and thus high gravimetric and volumetric energy density. However, graphite is thermodynamically unstable in this potential range when in contact with the liquid electrolyte. This leads to the electrochemical decomposition of the electrolyte and the formation of what is known as the solid electrolyte interphase (SEI). The SEI acts as a necessary passivation layer that prevents further reactions with the electrolyte. However, it is also an electrochemically inactive component, whose growth over time causes a gradual reduction in cell capacity and an increase in direct current internal resistance (DCIR). Repeated cycles or prolonged storage at elevated SOC levels can cause continuous growth of this layer, which is considered one of the main causes of calendar ageing. In contrast, the LTO anode exhibits a significantly higher electrochemical potential of about 1.55V vs. Li/Li^+ . This voltage is sufficiently distant from the reduction potential of the electrolyte, meaning no SEI formation is necessary. The material displays electrochemically nearly inert behaviour toward the electrolyte. This property has several significant advantages: there is no electrochemical decomposition, ageing behaviour is minimal, and the cell maintains stable performance over very long periods with consistently low DCIR.

Disadvantages and advantages of LTO cells

One disadvantage of this high anode potential, however, is the reduced cell voltage, which for LTO cells typically lies around 2.4 V, compared to 3.2–3.7 V for LFP or NMC cells with graphite anodes. Consequently, the specific energy density of LTO cells is significantly lower than that of their conventional counterparts.

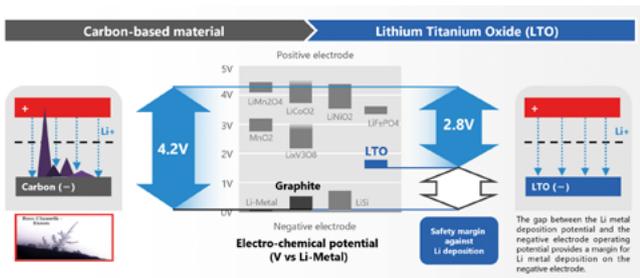


Figure 6: Differences in electrochemical potential ensure maximum safety.

In addition to electrochemical stability, LTO also offers critical advantages in terms of the mechanical integrity of the cell. While graphite experiences a volume change of up to 10% during the insertion and extraction of lithium ions, which can lead to structural damage and cracking of the SEI, LTO, due to its spinel structure, displays what is known as “zero strain” behaviour. The volume change during (de-)lithiation is less than 0.5 %, thereby avoiding mechanically induced degradation processes. This results in exceptionally high cycle stability. Properly designed cells can achieve over 20,000 full cycles while retaining more than 90 % of their original capacity. Such capacity retention under extreme conditions, including charge/discharge rates of 5 C (50 A), an ambient temperature of 35 °C, and a full state-of-charge range (0–100 % SOC), is not achievable in conventional Li-ion cells. The corresponding test results are documented in Figure 7.

Capacity recovery over 90% after 20,000 cycles

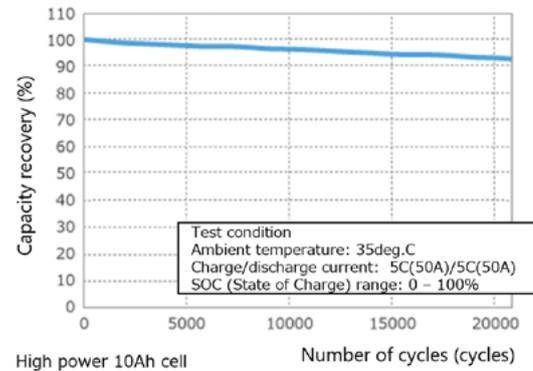


Figure 7: Long-term measurement of capacity retention after 20,000 cycles of an SCiB 10 Ah cell.

Another major advantage of LTO anodes relates to charging behaviour. When using graphite, there is a risk of so-called lithium plating at high charge rates, low temperatures, or high SOC. In this case, lithium ions are no longer intercalated but deposited as metallic lithium. This effect can not only lead to further SEI growth and thus accelerated ageing, but in some cases also lead to the formation of needle-like dendritic structures that can penetrate the separator and cause internal short circuits. LTO, by contrast, is capable, due to its spinel structure, of intercalating lithium ions extremely quickly and uniformly without plating. This allows high charging speeds across a broad range of temperatures and SOC levels and makes LTO cells one of the few cell technologies capable of true fast charging with full depth of discharge (DoD). Finally, the absence of SEI and resistance to plating results in significantly greater operational safety. On one hand, the LTO anode prevents the formation of dendrites, which could otherwise lead to safety-critical short circuits. On the other hand, in the event of a short circuit — for example, due to mechanical damage — a fully discharged LTO cell discharges only slowly due to its high resistance, significantly reducing the risk of thermal runaway (see Figure 8). Moreover, the classic trigger for thermal chain reactions — the thermal decomposition of the SEI — is absent in LTO cells, which gives them greater thermal stability compared to conventional Li-ion cells.

LTO phase transition prevents thermal runaway

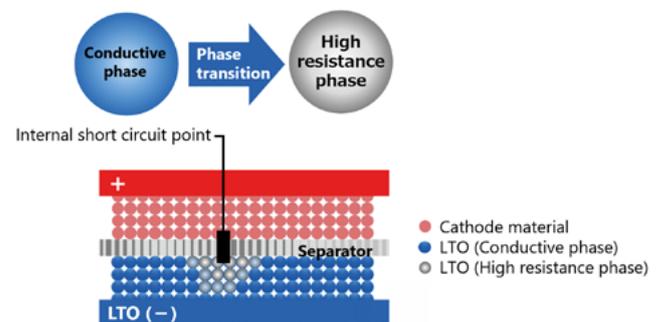


Figure 8: LTO phase transition prevents thermal runaway.

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Part 2: Achieving Galvanic Isolation and Protection in High-Performance Systems with Solid-State Isolators

An optimal isolation strategy can determine design success and accelerate time to market — especially in high-voltage industrial systems. Infineon's SSI family offers a compact, efficient solution that integrates protection and control functions while simplifying thermal and circuit design. This article explores practical solid-state relays (SSR) implementations using Infineon SSI and CoolMOS™ devices and compares them to conventional SSR designs based on silicon-controlled rectifiers (SCRs) or TRIACs.

By Davide Giacomini, Director of Marketing, Power IC Group,
and Sameh Snene, Product Applications Engineer, both Infineon Technologies

The Limitations of Conventional Solid-State Relays

Large industrial control cabinets typically house critical power distribution components such as circuit breakers, power meters, fuses, and SSRs. As shown in Figure 1, these SSRs are commonly used to control lighting systems, ventilation groups, air conditioners, refrigeration lines, and other infrastructure loads.

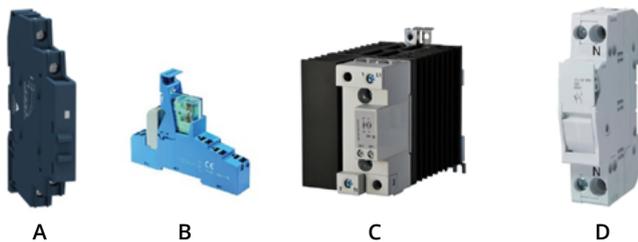


Figure 1: DIN rail mount SSR (A, B and C) and a DIN rail Fuse socket (D)

Compared to electromechanical relays (EMRs), SSRs deliver longer operating life and enable remote capabilities. However, SSRs based on TRIACs or SCRs are often challenged by high power dissipation, large heat sink and board space requirements, and a lack of integrated fault protection. Additional challenges include limited DC operation due to forced commutation techniques and an absence of real-time fault monitoring.

The limitations of conventional SSRs in real-world products are highlighted by evaluating a typical DIN rail-mounted SSR. This 6 A, single-phase relay uses a random-voltage switching SCR output. It accepts 4–32 V DC input and supports 24–280 V AC output at up to 6 A. At full load, the voltage drop is <1.3 V, resulting in ~7.8 W power dissipation.

The SSR lacks integrated protections. Off-state leakage is 0.1 mA, while turn-on and turn-off times are 0.1 ms and 0.5 cycles, respectively. dv/dt immunity is 500 V/ μ s and fusing thresholds are 410 A²·s (50 Hz) and 375 A²·s (60 Hz). Load current ranges from 150 mA to 6 A.

Without built-in protection, a large portion of the housing is dedicated to heat sinking. In space-constrained DIN-rail cabinets with poor airflow, heat buildup can shorten service life.

The Advantages of SSI-Based SSRs

SSI devices provide compelling benefits in power distribution environments, particularly in applications where SSRs based on TRIACs or SCRs are used. Importantly, an optimal isolation strategy directly determines design success and time-to-market. Solutions with integrated features that support high-voltage circuitry across a broad range of industrial and commercial applications offer definitive advantages, particularly when addressing diverse system requirements.

Here, we compare the DIN rail SSR with a solution built around Infineon's SSI technology. Because this is an AC application, two CoolMOS™ devices are required. Our goal is to reduce on-state power dissipation by a factor of three at full output current. To meet this target, the required total $R_{ds(on)}$ can be estimated using:

$$R_{ds(on)} = \frac{P_{diss}}{3 * 2 * I_{max}^2} = \frac{7.8}{3 * 2 * 6^2} = 36m\Omega$$

Where P_{diss} is the reference SSR's power dissipation (7.8 W), and I_{max} is the maximum output current (6 A). This implies that each MOSFET should have an $R_{ds(on)}$ below 36 m Ω .

Based on the CoolMOS™ options available, the IPT60T022S7 in a TO-LEADLESS (TOOL) package meets this requirement, with an $R_{ds(on)}$ of 22 m Ω at 25°C. While $R_{ds(on)}$ will approximately double at 150°C, the device still stays within target limits.

For better thermal protection and real-time temperature monitoring, a T-series CoolMOS™ device with an integrated temperature sensor is recommended. This enables accurate die temperature tracking and minimizes the risk of SSR failure due to thermal overload. For this reason, the selected gate driver for this example is the iSSI30R12H, which features independent thermal and current sense input pins.

Next, we calculate the minimum buffer capacitance (C_{buf_min}) required at the BUF terminal using the following equation:

$$C_{buf_min} = 1.2 * \frac{Q_{m1} + Q_{m2}}{V_{buf_th_min} - V_{g_min}}$$

Where:

- Q_{m1} and Q_{m2} are the gate charges of the MOSFETs at the desired turn-on gate voltage (V_{g_min})
- $V_{buf_th(min)}$ is the minimum fast turn-on comparator threshold voltage from the iSSI30R12H datasheet



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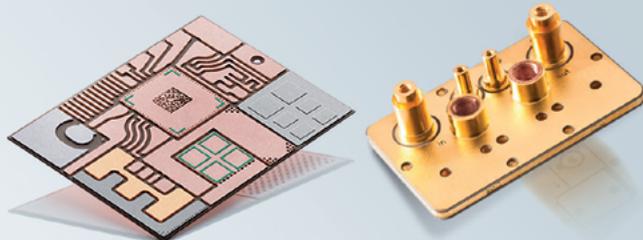
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- V_{g_min} is the minimum gate-source voltage required to fully turn on the MOSFETs
- The 1.2 factor adds margin for gate charge tolerance

In AC operation, the MOSFETs alternate between conducting and blocking. When one device is in conduction via its body diode, it functions like a synchronous rectifier. In this condition, the gate charge during turn-on bypasses the Miller plateau, resulting in a lower effective Q_m . As such, Q_{m1} and Q_{m2} are different and must be derived from the gate charge curves in the datasheet.

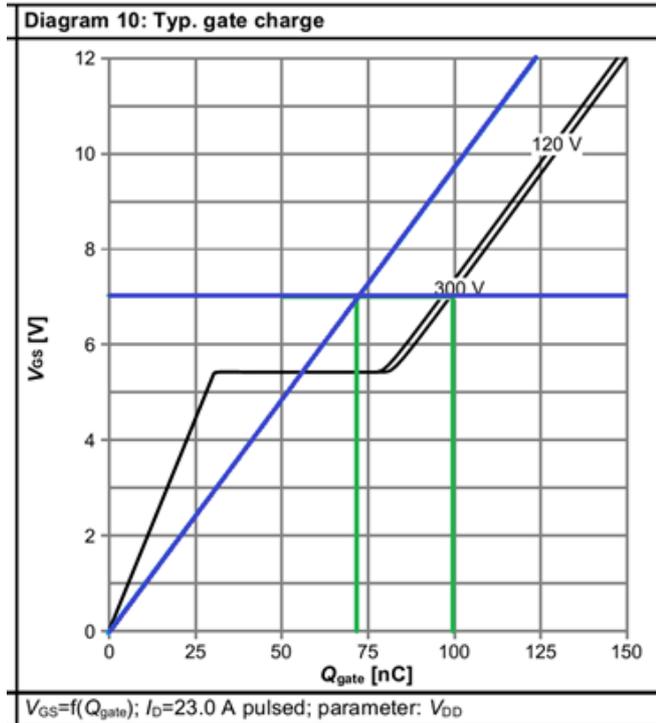


Figure 2: Extrapolation of Q_{m1} and Q_{m2} from the gate charge characteristic

For the example design using the iSSI30R12H driver and IPT60T022S7 MOSFETs:

- $Q_{m1} = 100 \text{ nC}$ (CoolMOS™ off/open)
- $Q_{m2} = 70 \text{ nC}$ (CoolMOS™ conducting via body diode)
- $V_{buf_th(min)} = 10 \text{ V}$ (datasheet)
- $V_{g_min} = 7 \text{ V}$ (MOSFET gate threshold for reliable turn-on)

Substituting the formula:

$$C_{buf} = 1.2 \cdot \frac{100 \text{ nC} + 70 \text{ nC}}{10 \text{ V} - 7 \text{ V}} = 68 \text{ nF}$$

Leakage Current in Off-State

When the SSR is off, leakage current flows through the MOSFETs due to the absence of an air gap. This leakage stems from two primary sources: Zero gate voltage drain current (I_{DSS}) and output capacitance energy-related ($C_o(er)$).

For the IPT60T022S7, the datasheet values are:

- $I_{DSS} = 50 \mu\text{A}$ (typ) @ $V_{DS} = 600 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_j = 150^\circ\text{C}$
- $C_o(er) = 303 \text{ pF}$ @ $V_{DS} = 0\text{--}300 \text{ V}$

When off, one MOSFET conducts through its body diode during each AC half-cycle, while the other sees the full 0–320 V swing. The resulting current through $C_o(er)$ for a 50 Hz AC line is:

$$I_{C_o(er)} = 320 / [1 / (2\pi \times 50 \times 303 \text{ pF})] \approx 30.5 \mu\text{A}$$

Adding both effects gives the worst-case leakage current at 150°C of:

$$I_{leak} \approx 50 \mu\text{A} + 30.5 \mu\text{A} = 80.5 \mu\text{A}$$

Protections: Short Circuit

Using MOSFETs instead of SCRs enables fast short-circuit protection. Traditional SSRs require fuses—slow to react, bulky, and single-use. A short on one load can also trip the breaker and shut down multiple lines.

In contrast, Infineon’s SSI with CoolMOS™ enables precise, real-time intervention. The CS pin on the iSSI30R12H has a 200 mV threshold. To trigger protection at $\sim 10\times$ the rated current (6 A), the shunt resistor is calculated as:

$$R_{shunt} = 200 \text{ mV} / (10 \times \sqrt{2} \times 6 \text{ A}) \approx 2.4 \text{ m}\Omega$$

The total SSR resistance at 150°C , including two IPT60T022S7 devices and the shunt, is:

$$R_{total} \approx 2 \times 2 \times 22 \text{ m}\Omega + 2.4 \text{ m}\Omega \approx 90.4 \text{ m}\Omega$$

$$V_{drop} = 90.4 \text{ m}\Omega \times 6 \text{ A} \approx 542 \text{ mV}$$

This is $\sim 58\%$ lower than the 1.3 V drop of the SCR-based SSR, enabling smaller heat sinks.

To avoid noise-triggered faults, a low-pass filter is added at the CS input resulting in:

$$R_f = 100 \Omega, C_f = 1 \text{ nF}$$

$$f_p = 1 / (2\pi RC) \approx 1.59 \text{ MHz}$$

The protection response time is:

$$T_{OC} = t_{CS(off)} + Q_g / I_{off} \approx 1 \mu\text{s} + 150 \text{ nC} / 488 \text{ mA} \approx 1.48 \mu\text{s}$$

Overtemperature Protection

The iSSI30R12H integrates thermal protection by sourcing a 50 μA bias current to monitor the CoolMOS™ die temperature. Shutdown is triggered when the sensor voltage drops below 1.095 V, corresponding to a junction temperature of $\sim 155^\circ\text{C}$.

The device includes a built-in comparator with noise filtering. To further stabilize readings, an external RC filter matching the overcurrent filter frequency is recommended:

$$R_f = 100 \Omega, C_f = 1 \text{ nF} \rightarrow f_p \approx 1.59 \text{ MHz}$$

This configuration ensures fast, reliable thermal shutdown and helps protect the MOSFETs under high-load conditions.

Transient Voltage Suppression and Miller Clamping Protection

To protect the MOSFETs from voltage spikes during fault conditions or inductive load switching, a TVS or MOV (shown as D1 in Figure 3) should be mounted close to the MOSFET drains. The clamp’s breakdown voltage must exceed the SSR’s peak line voltage but remain below the CoolMOS™ breakdown threshold.

For 280 V AC operation:

$$V_{peak} = 280 \text{ V}_{AC} \times \sqrt{2} \approx 396 \text{ V}$$

An ideal TVS option is SMCJ400CA, with a 400 V standoff and 1,500 W peak power rating.

Surge transients can also induce high dv/dt across switches, which may couple through parasitic capacitances and cause unwanted turn-on. The iSSI30R12H includes a Miller clamp to prevent this.

Datasheet values:

- $V_{MC \text{ max}} = 3.6 \text{ V}$, $R_{MC} = 600 \Omega$
- Assume $dv/dt = 10 \text{ V/ns}$

$$I_{MC} = 3.6 \text{ V} / 600 \Omega = 6 \text{ mA}$$

$$C_{MC(min)} = 6 \text{ mA} / (10 \text{ V/ns}) = 0.6 \text{ pF} \rightarrow \text{use } 1 \text{ pF}$$

Optionally, a 3.3 V Zener can be added between each MC pin and GND2. However, this is often unnecessary since the device tolerates up to 100 mA for sub-1 μs pulses.

Input Stage

The iSSI30R12H supports separate Vcc1 and IN pins, allowing multiple devices to be driven in parallel from a 3.3 V microcontroller. For single wide-range input, Vcc1 and IN can be tied together, requiring only one input resistor—that must be sized for the clamped Vcc1 max of 3.5 V.

For 12–24 V industrial inputs:

$$R_{in} = (12\text{ V} - 3.5\text{ V}) / 16\text{ mA} \approx 536\ \Omega \text{ (E48)}$$

Input power at 24 V:

$$P_{in} = (24\text{ V} - 3.5\text{ V}) / 536\ \Omega \times 3.5\text{ V} \approx 134\text{ mW}$$

Resistor power dissipation:

$$P_R = (24\text{ V} - 3.5\text{ V})^2 / 536\ \Omega \approx 784\text{ mW}$$

Use a 1–1.5 W resistor, or a 3.3 V DC/DC converter for better efficiency. The bypass capacitor can be sized from datasheet specs:

$$C_{in} = 3.3\text{ nF (max 4.7 nF)}$$

Component Summary: DIN Rail SSR

With all key components selected, the SSR output stage is defined as shown in the schematic. Using iSSI30R12H and 2× IPT60T022S7, we compare the new design against the commercial reference. Table 2 summarizes performance across metrics such as Rds(on), power dissipation, protection response, and thermal behavior. This comparison highlights improvements in efficiency, protection, and footprint enabled by Infineon’s SSI-based SSR architecture.

Schematic reference	Calculation reference	Value	Comments
U1	U1	iSSI30R12H	Infineon SSI
T1, T2	PT60T022S7	IPT60T022S7	Infineon CoolMOS™ T-series
Rsh	Rsh	2.4m	Shunt resistor
D1	TVS	SMCJ400CA	1500W in SMC package
D2, D3	DZ	3.3V	Diode zener 500mW
R3, R4	Rf _{oc} , Rf _{ot}	100Ω	smd resistor
R5, R6	none	0 Ω	Not used
C3, C4	C _{MC}	1pF	2kV smd capacitor
C5	C _{buf}	68nF	50V smd capacitor
C6, C7	Cf _{oc} , Cf _{ot}	1nF	50V smd capacitor
R1	R _{in}	536Ω	1W resistor
C1	C _{in}	3.3nF	25V smd capacitor

Table 1: Component summary for a 600V – 6A SSR

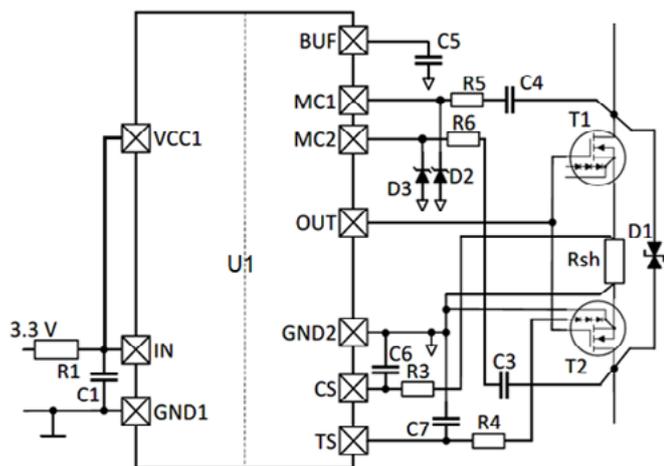


Figure 3: SSR application schematic

Specification	Single phase SSR, 6A, DIN rail	Single phase SSR, 6A, DIN rail (iSSI30R12H + 2x IPT60T022S7)
Type	Random voltage switching SCR Output	Random voltage switching MOSFETS Output
Operating Voltage / Current	4 - 32 VDC Input 24 - 280Vac Output, 6 A	12-24 VDC Input 24 - 280Vac Output, 6 A
Maximum Voltage Drop	< 1.3V (on – state) Pdiss _{max} = 1.3*6A = 7.8 W	< 542 mV (on – state) Pdiss _{max} = 0.542*6 A = 3.25 W
Maximum T for Fusing	410 A ² .s for 10 ms at 50 Hz * 375 A ² .s for 8.33 ms at 60 Hz * * No protections	Over Current protection set at 60 Arms (≈ 85A peak) Over Temperature Protection set at Mosfets’ Tj = 155°C
Maximum Leakage Current	0.1 mA (off state)	< 36 uA @ Tj=25°C
Load current	0.15 – 6 A	0 – 6 A (no minimum holding)
dV/dt	500 V/μs off-state at maximum voltage	> 10 V/ns, with protection
Response Time	0.5 cycle (turn-off) 0.1 ms (turn-on)	~2.5 ms (turn – on) < 1.5 μs (turn-off in OCP & OTP)

Table 2: DIN rail SSR solution comparison

Specification	Pre Assembled ‘Hockey Puck’
Type	Single Phase Panel Mount SCR Output / Zero Voltage Switching
Operating Voltage / Current	3-32 VDC input 24 - 280Vac Output, 25 A
Maximum Voltage Drop (Power Dissipation)	< 1.35V on-state =1.35*25 = 33.75 W
Maximum T for Fusing	370 for 8.33 ms @ 60 Hz* 380 for 10 ms @ 50 Hz* *No protections
Maximum Leakage Current	0.1 mA Off state
Load current	0.05 – 25 A
dV/dt	500 V/us off -state
Response Time	0.5 cycle (turn-off) 0.5 cycle (turn-on)

Table 3: commercial panel mount SSR characteristics



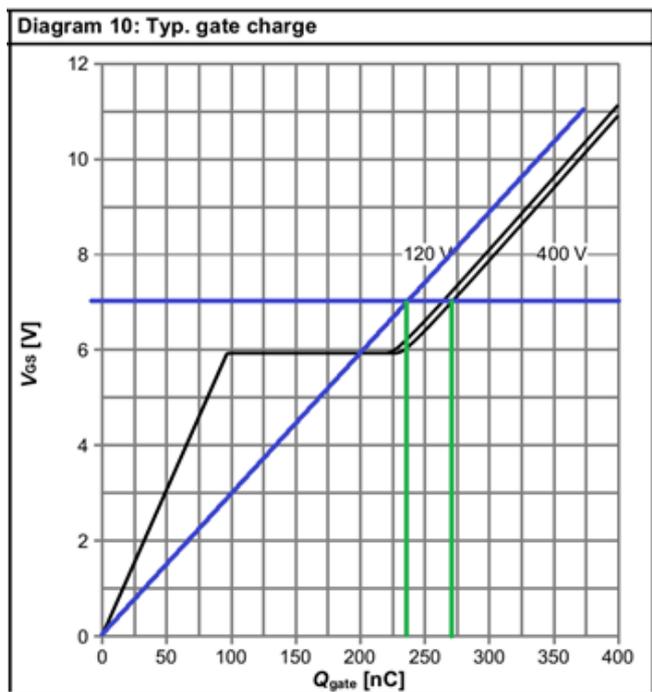
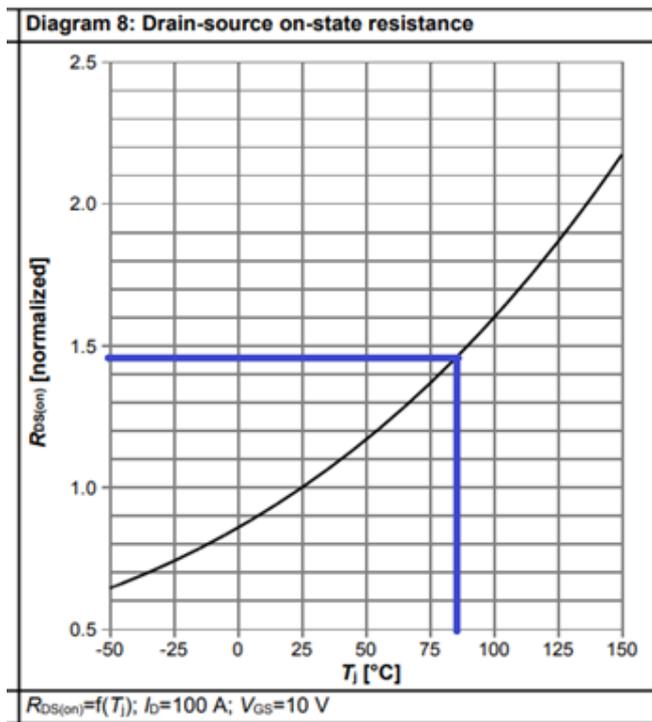


Figure 4: R_{ds(on)} and Q_g values for IPDQ 60R007CM8

Panel-Mount SSR Overview

The panel-mount SSR example follows the same design approach, targeting a 25 A output. Based on thermal and R_{ds(on)} targets, IPDQ60R007CM8 is selected for its low 7 mΩ resistance at 25°C. At an average operating temperature of 85°C, its R_{ds(on)} rises to ~10.15 mΩ, which remains acceptable without paralleling devices. For optimal thermal performance, two IPDQ60T010S7 devices can be used in parallel, though at a slightly higher cost.

Since the selected CoolMOS™ doesn't feature integrated temperature sensing, the design uses the iSSI30R11H paired with an external PTC—B59721A0100A062—for thermal protection. Based on its 200 mV threshold and internal 50 μA bias current, shutdown occurs around 92–100°C at the heat sink.

Thermal Optimization and Temperature Protection

In this example, the B59721A0100A062 PTC is used, with its resistance-temperature curve shown in Figure 5. The iSSI30R11H triggers thermal protection when its V_{TS} input goes above 200 mV. With a typical internal current source of 50 μA, this corresponds to:

$$R_{OTP(typ)} = 200 \text{ mV} / 50 \text{ } \mu\text{A} = 4 \text{ k}\Omega$$

This equates to a heatsink temperature between 92°C and 100°C. For accurate operation, tolerances in the internal current source and comparator threshold must be factored into the design.

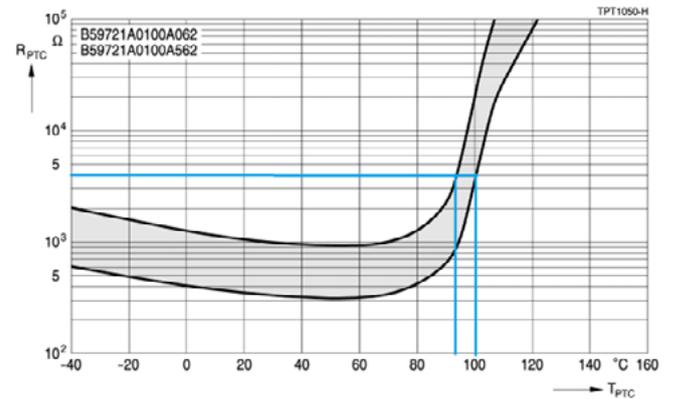


Figure 5: B59721A0080A062 PTC characteristic

Component Summary: Panel-Mount SSR

With all components selected, calculated as for the previous paragraph we can complete the DIN rail SSR design as shown in the schematic below.

Schematic reference	Calculation reference	Value	Comments
U1	U1	iSSI30R11H	Infineon SSI
T1, T2	IPDQ60R-007CM8	IPDQ60R-007CM8	Infineon CoolMOS™ 8 R-series
Rsh	Rsh	590 m	Shunt resistor
D1	TVS	SMCJ400CA	1500W in SMC package
D2, D3	DZ	3.3V	Diode zener 500mW
R3, R4	R _{f_{oc}} , R _{f_{ot}}	100Ω	smd resistor
R5, R6	none	0 Ω	Not used
C3, C4	C _{MC}	1pF	2kV smd capacitor
C5	C _{buf}	220nF	50V smd capacitor
C6, C7	C _{f_{oc}} , C _{f_{ot}}	1nF	50V smd capacitor
R1	R _{in}	536Ω	1W resistor
C1	C _{in}	3.3nF	25V smd capacitor
PTC	R _{OTPTyp}	B59721A-0100A062	Temperature sensor

Table 4: Component summary for a 600V - 25A SSR

Using the kit parts—iSSI30R11H and 2× IPDQ60R007CM8 — we compare performance against the original commercial SSR. The comparison includes key metrics such as on-state voltage drop, thermal behavior, switching response, and protection features. Results are summarized in the following table.

Specification	Pre Assembled 'Hockey Puck'	Single phase SSR, 25A, DIN rail (iSSI30R11H + 2x IPDQ60R007CM8)
Type	Single Phase Panel Mount SCR Output / Zero Voltage Switching	Single Phase Panel Mount Random voltage switching MOSFETs Output
Operating Voltage / Current	3-32 VDC input 24 - 280Vac Output, 25 A	12-24 VDC Input 24 - 280Vac Output, 25 A
Maximum Voltage Drop	< 1.35V on-state $P_{diss_{max}} = 1.35 \cdot 25 = 33.75 \text{ W}$	< 522mV (on - state @ $T_j=85^\circ\text{C}$) $P_{diss_{max}} = 0.522 \cdot 25 \text{ A} = 13.05 \text{ W}$
Maximum T for Fusing	370 for 8.33 ms @ 60 Hz* 380 for 10 ms @ 50 Hz* *No protections	Over Current protection set at 250 Arms ($\approx 350 \text{ A peak}$) Over Temperature Protection set at $T_c = 92^\circ\text{C}$ to 100°C
Maximum Leakage Current	0.1mA Off state	< 66 μA @ $T_j=25^\circ\text{C}$
Load current	0.05 - 25A	0 - 25 A (no minimum holding)
dV/dt	500 V/ μs off-state at maximum voltage	> 10 V/ns, with protection
Response Time	0.5 cycle (turn-off) 0.1 ms (turn-on)	< 2.0 μs (turn-off in OCP & OTP) ~8 ms (turn - on)

Table 5: Panel mount SSR solution comparison

Conclusion

Infineon's new family of SSIs simplifies SSR development for industrial and commercial applications. Optimized for use with CoolMOS™ devices, these isolators establish a new performance benchmark in SSR design.

Together, the SSI and CoolMOS solution deliver key advantages over traditional TRIAC- or SCR-based SSRs—including up to 50% lower power dissipation, smaller heat sinks, reduced board space, and lower system weight. Integrated overcurrent and overtemperature protection eliminate the need for external fuses. The MOSFET-based output stage enables fast switching, DC operation, and removes minimum load constraints. Leakage current is reduced, and dv/dt immunity exceeds 1,000× that of conventional designs.

These improvements enable short-circuit-protected SSRs that reduce thermal stress, save space, and improve reliability in power distribution systems. By streamlining protection, control, and thermal design, Infineon's SSIs help reduce development cycles, ensure design success, and accelerate time to market.

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Mersen specifically improves the eco-balance of its products

As a manufacturer of passive components, Mersen is committed to further reduce their ecological footprint. The company has therefore analysed the environmental impact of its components. The result: depending on the type of component, a reduction in weight can increase energy efficiency, but can also have negative ecological effects. The experts also found some starting points for design optimisation.

By Simon Landrивon, Marketing Communications Manager Europe, Mersen

Against the backdrop of climate change, the industry must reduce its ecological impact and take environmental criteria into account as early as the product design phase. Life cycle analyses are an important tool for improving the environmental compatibility of electronic products. The eco-design and sustainability of power electronic components are therefore the focus of several new research projects. However, the environmental impact of power electronics as a whole is being analysed, but not that of individual passive components.

As a manufacturer of these products, Mersen believes it has a responsibility to further reduce their ecological footprint. In an eco-design study, the company has therefore analysed the environmental impact of its components.

Life cycle assessment is an important measuring tool

The preferred method for assessing the environmental impact of passive components is the life cycle assessment. It enables a better understanding of the critical points and shows the corrective measures that need to be taken to reduce the overall environmental impact. The life cycle assessment of products takes into account their weight, energy consumption, the composition of the materials and the waste generated during production. Co-operation with the users of the products is also important: They can provide important information on distribution channels and how the components are used in practice. Mersen used the EIME software to create the life cycle assessments. With its help, environmental impacts can be analysed either on the basis of life cycle phases or by individual components.

Life cycle analysis of a laminated bus bar

One of the product groups analysed in the ecodesign study was laminated bus bar. Consisting in an arrangement of conductive and insulating layers, bus bars distribute the current between different points. As the current density is different at the individual points of the circuit, hot spots occur – the losses due to the Joule effect can be considerable here.

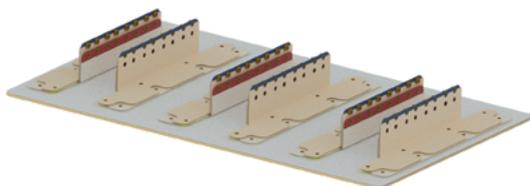


Figure 1: Laminated bar bus for a power conversion application in wind energy

Image: Mersen

For the eco-design study, a representative bus bar was analyzed: a piece dedicated to wind turbine, with dimensions of approx. 500 mm x 1000 mm and a total weight of 42.9 kg. 94 percent of the bus bar consists of copper conductors with a thickness of 1.5 mm. The result of the bus bar analysis: 5,235 kg of CO₂ equivalent are emitted over the entire service life. By converting electrical energy into thermal energy, a maximum temperature rise of 14 °C is achieved, as the experts found out using a thermoelectric simulation with the COMSOL Multiphysics software. This corresponds to 14.2 MWh of losses during the product's service life. What was also determined: the use phase of products has by far the greatest environmental impact in terms of most of the indicators analysed, such as global warming.

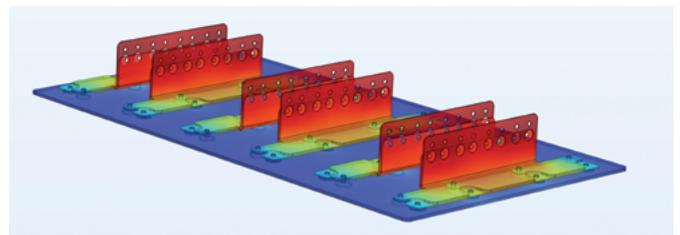


Figure 2: Thermoelectric simulation of the heating of a laminated bar bus (1.5 mm thick) during a nominal current flow. Image: Mersen

The end-of-life phase, on the other hand, has the greatest impact on the indicator for freshwater eutrophication (PEF-Epf) and metal depletion (PEF-ADPe). This is due to the copper recycling phase.

The study also identified a number of potential improvements, including optimising energy efficiency. Mersen has already investigated changes to the design of the bus bar: by increasing the conductor thickness, the power loss (Joule effect) has been reduced and a significant reduction in climate impact has been achieved.



Figure 3: Laminated busbars from Mersen ensure the transmission of generated energy in IGBTs and capacitors in wind turbines, among other things. Image: Marketplace2/Adobe Stock/made with AI

22 per cent less CO₂ emissions

Passive components are subject to high stress during the utilisation phase, as they have a high power loss and a long service life. However, this applies less to the belay devices, which dissipate less energy. Reducing the weight of these products therefore becomes a real challenge, which has a significant impact on the overall CO₂ footprint.

Mersen investigated the carbon footprint of its belay devices and then optimised their design. While the weight of the original product was 63 g, the eco-designed version weighed only 46 g thanks to optimised plastic and metal components. This corresponds to a weight reduction of 26 per cent and a reduction in CO₂ equivalents of 22 per cent compared to the material extraction phase. With 4 million of these products manufactured by Mersen every year, this means a total reduction in environmental impact of 356 tonnes of CO₂ equivalents.



Figure 4: An engineer works on the generator of a wind turbine, which converts mechanical energy into electricity.

Image: Marketplace2/Adobe Stock/made with AI

Higher output despite weight reduction

When optimising the design of a fuse, however, the reduction in weight did not result in any savings in CO₂ equivalents. The opposite was the case: although the weight was reduced from 920 g to 810 g, the power emitted by the fuse increased from 3300 MJ to 3600 MJ over its 20-year service life. In the overall balance of the fuse, the increase in performance led to an increase in CO₂ equivalents of 8 per cent.

The example of the fuses shows that material savings do not lead to a reduction in CO₂ emissions for every passive component. However, the weight reduction did have one advantage: the environmental impact of raw material extraction was reduced by 50 per cent.

Replace copper with aluminium

In the case of bus bars, the ecodesign study revealed significant savings in CO₂ equivalents by increasing the conductor thickness. However, if the bus bars are made of copper, a greater thickness means a considerable increase in costs. One alternative here is to replace copper with aluminium. If the temperature rise is equivalent to that of copper, the use of aluminium makes it possible to significantly reduce the weight of the bus bar. At the same time, using a 2.5 mm thick aluminium conductor instead of a copper version reduces the impact on global warming from 5.3 t CO₂ equivalents to 4.7 t CO₂ equivalents – that is a reduction of 10 per cent. However, the study did not take product costs into account. It is true that aluminium is a more economical metal than copper. However, the effort required to provide aluminium with corrosion protection is high.



Figure 5: Laminated busbars from Mersen are also used in many photovoltaic systems. Image: Mike Mareen/Adobe Stock 312486036

Ecodesign reduces environmental impact

Life cycle analysis is an important tool for assessing the environmental impact of products. The results of Mersen's latest ecodesign study clearly show that there are many options for reducing the ecological footprint of passive components. However, a comprehensive consideration of the electrical system is necessary. In the case of the bus bar, this is the prerequisite to compensate for an increase in weight due to thicker conductors, e.g. through a lighter cooling system or energy savings during the service life of the product. Not to forget, the impact transfer is also a key parameter during ecodesign activities.

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Field Failures in Power Modules – Potential Root Causes and Approaches how to avoid them

System suppliers are faced with the challenge of selecting the needed power module considering the price and reliability as well. This article describes key factors for the harsh environment reliability set up of modules and systems. Which potential risks are there, and which field conditions are expected? Which ventilation and design are suited on the system side?

By Markus R. Meier, Group Leader Reliability & Surfaces, Zestron Europe

A variety of stressors act on the power module and the system, which need to be considered when selecting the modules and the respective materials. System manufacturers who integrate power modules in a final product (e.g. integrated power supply solutions) can actively influence the robustness of their systems here by selecting the power module suitable for their mission profile (performance versus costs) as well as through system design. Regarding system design, system manufacturers need to ensure that stress factors are minimized and not, in the worst case, amplified. For this, process deficiencies (e.g. during power module system integration), material and component selection, housing, and ventilation situation need to be discussed.

In addition to discussing the possible approaches to system design for improving system reliability, Zestron has gained experience over the past years with the application of rapid HAST (highly accelerated stress test) quality testing regarding module selection. These tests allow for an initial pre-selection of suitable modules before conducting the required but time-consuming qualification tests. Thus, they can reduce optimization and selection cycles, thereby shortening the time-to-market and reducing costs. Hereby, an evaluation of the stressed modules via impedance spectroscopy can also help to uncover hidden or emerging deficiencies, which may become effective over the years in the field and lead to failures. The risk for failures in the field thus can be minimized and costs for repair and warranty can be reduced.

Intrinsic and/or extrinsic stressors

A power electronics module is subjected to a variety of stressors in the field. In addition to external stress (extrinsic stressors), there are also numerous intrinsic stressors primarily determined by the design and layout of the module (Figure 1). The latter are often dependent on the type of chip used (Si, SiC, GaN), as this largely influences the switching frequency, voltage transitions (dv/dt), and consequently, the operating temperature. The thermomechanical and high-voltage stresses resulting from these factors primarily affect materials of the semiconductor itself or the materials in its direct vicinity, such as chip metallization and passivation, solder or sinter joints, and the insulating materials used. Selecting materials that are compatible with this intrinsic stress is therefore crucial for the reliability of the power module.

Extrinsic stressors typically encompass three major load scenarios: (thermo-)mechanical stress (including stressors such as temperature fluctuations and shocks, vibrations, impact loads, etc.), harmful gases and humidity. Particularly in the areas of harmful gas and humidity stress, the boundary between extrinsic and intrinsic stressors can be fluid. For example, exposure to harmful gases can also result from the outgassing of volatile components from materials used during module or system manufacturing (such as sulfur outgassing from vulcanized rubber seals or phosphorus from poly-

amide housings), which constitutes an intrinsic, design- or material-induced cause underlying failures. Nevertheless, an unfavorable enclosure or ventilation situation can lead to the accumulation or buildup of moisture within the system or module in certain areas.

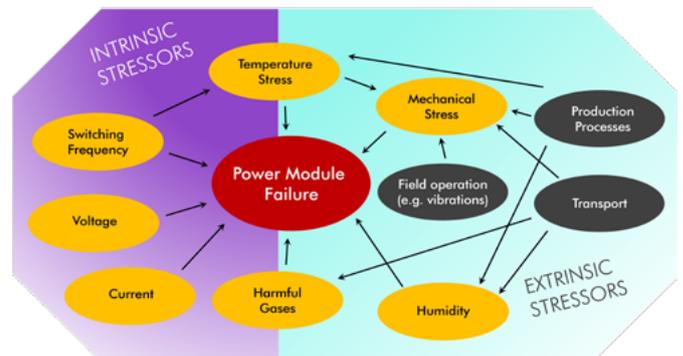


Figure 1: Common stressors affecting power electronics reliability.

Dendritic structures after field stress or qualification tests

Particularly when moisture interacts with the module, typical failure mechanisms are triggered, which can lead to the formation of dendritic structures. These structures develop between the applied potential difference and can grow on the surface within a moisture film formed by condensation, or also within a polymer material that is exposed to moisture and has absorbed a sufficient amount of water into the bulk material. On the one hand, as previously described, this can occur due to moisture stress in the field; on the other hand, a corresponding H³TRB (High-Temperature High-Humidity High-Reverse-Bias) test during product validation and qualification (see AQG324) can also trigger this stress and provide an indication of the module's moisture robustness under humid environmental conditions in the field.

Especially in high-voltage applications, dendritic structures are usually found within a polymer material or along the interface between, for example, the insulation material and the substrate or chip surface. These structures are very easy to detect in the insulation trenches of silicone-encapsulated power modules, as they offer excellent optical accessibility. Nevertheless, although more difficult to observe, dendritic structures after moisture and high-voltage stress can also be found in other insulation systems such as epoxy mold compounds, coatings, or in the case of embedded components [1, 2], in areas of the corresponding FR4 circuit board structure, such as the epoxy base material or the solder resist (Figure 2).

The dendrites may initially represent a purely optical anomaly and not lead to any electrical irregularities or changes in the module's functionality. This is especially the case when the insulation distance between the dendritic structure and the opposite potential

is still sufficiently large, or when minimal leakage currents or low resistances have no significant impact on the electrical functionality of the entire module. Typically, these leakage currents manifest as slight drifts in the corresponding H³TRB curves over the 1000 h testing time.

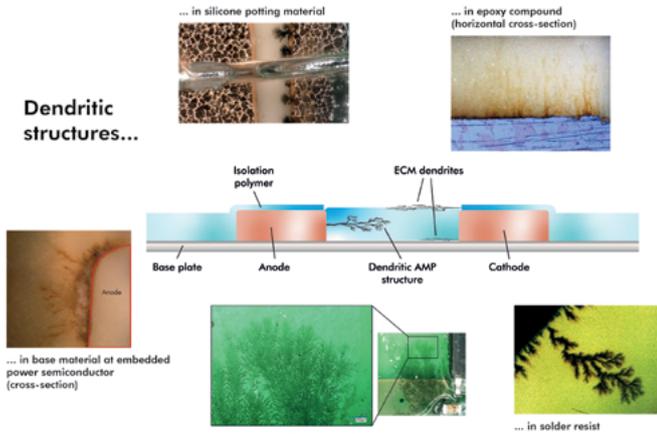


Figure 2: Dendritic structures in various polymer systems after humidity stress in the field or during qualification testing. [1,3-6]

However, if there is no significant or sudden decrease in resistance – particularly below the specified limit – these effects are often given only minor attention, and the test is considered passed. The occurrence of dendrites between insulation trenches in the field often remains unnoticed until a sufficient reduction of the insulation distance occurs, leading to electrical irregularities or malfunctions that necessitate further investigation and disassembly of the module. The failure characteristics in such cases are very diverse. They can range from purely leakage current behavior to thermal events

(thermal runaway), or to a voltage breakdown in the area of the bridging dendritic structure in the isolation trenches at sufficiently high voltages (Figure 3).

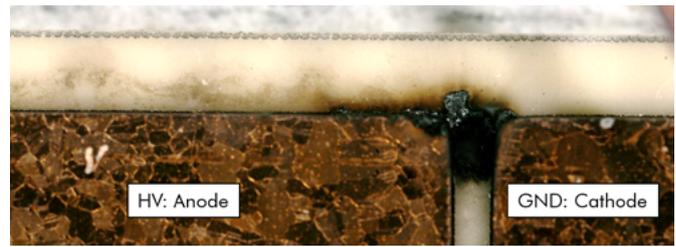


Figure 3: Voltage breakdown after partial bridging of the isolation trench by migration products. [3]

Failure mechanisms behind the phenomenology

Dendritic structures formed through corresponding moisture exposure under the respective potential difference (DC or AC with a corresponding DC component) on surfaces or within polymer materials are visually very similar. However, upon closer examination and with the background of the knowledge about the electrical wiring of the system it is noticeable that dendrites growing on the surface are usually of a cathodic-anodic nature. In contrast, most dendritic structures within a material tend to originate from the anode side. Additionally, the times until failure – i.e., the formation of a conductive path or filament – are significantly shorter for cathodic-anodic grown dendrites (minutes to hours along surfaces) than for anodic-cathodic structures (weeks to years typically within polymer bulk material).

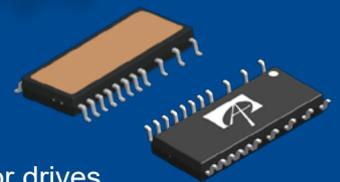
When examining the underlying mechanisms of these phenomena, it becomes clear that electrochemically, the same processes occur; however, external influences are decisive for the actual manifesta-

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tion of the phenomena. Particularly the material properties of the insulation system, the potential difference, and its magnitude are typical external influences.

The “standard” dendrite growth from cathode to anode on surfaces, characterized by the formation of a metallic dendrite, is referred to as electrochemical migration (ECM). ECM requires a water film with an applied electrical potential (> 1.5 V). For this mechanism to happen, only a few monolayers of water molecules are sufficient. When the water film connects the electrical potentials (DC), the anode material dissolves. The produced metal ions migrate to the cathode, where the reaction back to the metal occurs. The produced dendrite grows from the cathode back to the anode, creating a conductive connection [3, 4].

Anodic Migration Phenomenon

In contrast, the occurrence of dendritic structures within the bulk material of polymer substances – primarily exhibiting an anodic-cathodic growth direction – is referred to as an Anodic Migration Phenomenon (AMP) [3, 4, 7]. In case of AMP, the chemical reactions and migration processes described for ECM occur in channels within polymer materials (insulation materials, mold compounds, conformal coatings, underfill, etc.) that connect the anode and cathode.

However, these channels may be formed by aging or degradation of the respective polymer material, caused by stressors such as high voltage, high temperature or temperature changes and humidity often combined with quality tolerances in the polymer material [5]. At high humidity, these channels between anode and cathode are filled with water. Metal cations released from the anode then begin to migrate within the channels toward the cathode. Since there is a gradient from the acidic to the alkaline pH (caused by electrolysis reaction of water in presence of an electric potential), the ions

precipitate at the pH boundary (acidic/alkaline) within the channels, forming a metal hydroxide deposit from the solution. The visual appearance of these channels filled with deposits resembles dendrites that begin to grow from the anode [3, 4].

AMP predominantly occurs in areas with high electric field strength (edges, tips, roughness, etc.), as these are most susceptible to partial discharges. Consequently, polymer degradation begins there. Additionally, the aforementioned quality variations in polymer materials mostly caused by process tolerances, such as porosity, low degree of cross-linking, weak adhesion or delaminations increase susceptibility to partial discharges, and this leads to accelerated aging and degradation of the polymer matrix [3, 5].

How to avoid module failures or deal with them

The susceptibility to AMP failures and thus the reliability of the power module or the entire system is primarily determined by the type of insulation material used. Although the material is selected during the design phase based on the expected mission profile and the corresponding stressors (both extrinsic and intrinsic), the selection is mainly made based on existing datasheets, material properties, and previous experience. Within the field of failure analyses that Zestron performed over the past years the company found out that these failures are rarely due to incorrect material selection of the insulation materials. Instead, failure analysis indicates that most AMP failures are caused by defects in the polymer material (coatings, potting, moldings, base material, solder mask, etc.), which were triggered by the application process itself or previous manufacturing steps.

For module suppliers, it is important to note that the parameters provided by the manufacturers are obtained under standard conditions and for specific process parameters (curing, layer thicknesses,

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mixing ratios, etc.) for each material. However, the mass production material properties (such as dielectric strength, mechanical stability, CTE, etc.) often change significantly when deviating from the ideal or specified process conditions. Thus, there can be a substantial difference in material quality when transitioning from prototype production to series manufacturing. Developments in the field of e-mobility and the increasing efforts to integrate components and semiconductors into FR4-based PCBs (embedded components) also demonstrate that transferring these to higher stress conditions – particularly higher voltages – is not a straightforward 1:1 process even though manufacturers have years of experience with corresponding materials and processes.

Process stability at module supplier enables reliability

Ensuring the reliability of a power module, especially under challenging operating conditions, the application and curing of the used polymer material is important. To gain the maximized performance of the material according to datasheet specification the adoption of the datasheet parameters to the individual – especially geometric – conditions are key (according to datasheet specifications). The most critical parameters here are primarily the degree of crosslinking and the adhesion of the polymers to the respective substrate. From a process perspective, besides the application process itself (considering the specific component geometries), the curing process and the surface to be coated, potted, molded, or laminated are decisive (Figure 4). The latter is significantly influenced by the preceding manufacturing steps (such as soldering, sintering, etc.). Also, subsequent process steps like large area sintering or soldering e.g. on a cooling base plate may cause or enhance delamination effects caused by additional thermo-mechanical stress.

In addition to the interplay of these factors, especially during series ramp-up and ongoing production, it is essential to ensure that the optimal process conditions are maintained throughout the entire process chain. The final key to achieving moisture robustness of the power module is therefore continuous process monitoring by control of the insulation material quality.

Module selection and system design

In addition to the quality of the materials used and their interaction within the power module itself, it is often worthwhile to also consider the overall system. Besides the intrinsic moisture robustness of the module (discussing material selection and their combination), the system also plays a role in determining the extent to which moisture can access the module. A key factor here can be the enclosure design, which is crucial in preventing moist ambient air from reaching the module. This begins with the question of whether moisture-permeable membranes are used in the enclosure, allowing any ingress moisture to escape rather than accumulate, up to considerations of ventilation and air flow management.

Are there areas where laminar flow is absent, and moist ambient air is preferentially directed toward the module? Or could turbulence

in the airflow actually reduce overall humidity within the system? Additionally, it is important to identify the heat-carrying masses within the system as well as components that preferentially absorb or adsorb moisture (considering the material itself and possibly enhanced by hygroscopic contaminants from soldering or sintering

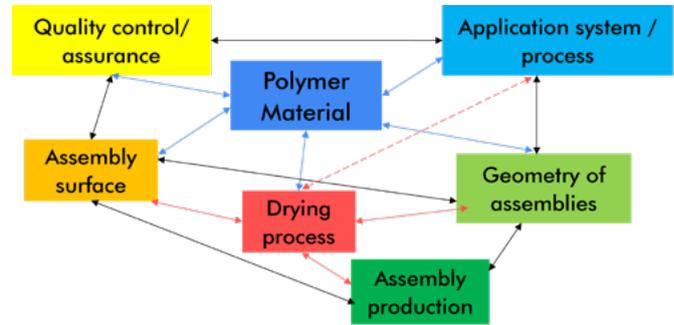


Figure 4: Influences on the polymer quality. [5]

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processes). In some cases, simply changing the direction of airflow during ventilation can be sufficient, since forcing air through an enclosure often causes more turbulence than sucking air through it.

The measures and considerations mentioned above to achieve a reliable system can be discussed and implemented by the system supplier. From supplier perspective, there is no direct influence on the power module itself or its quality and reliability. Therefore, it is in their responsibility to select a suitable module based on operational requirements in the field and the aforementioned mission profile. Always having in mind that not all eventualities during operation can be covered the system manufacturer needs to ensure compliance with the operating conditions and limitations specified by the module manufacturer for each module. Potential restrictions and maximum conditions in the field on system level should be clearly communicated, here. Nonetheless, due to the previously mentioned process variations, there are quality differences among various modules. To assist in module selection, appropriate qualitative tests can be applied, which provide indications of potential vulnerabilities in the field under stress conditions (moisture, harmful gases, thermal, mechanical, voltage, etc.).

Quality check – Fast pretesting

A crucial aspect is to question the extent, location, and timing of moisture or harmful gas ingress into the critical structures of the module (such as metallizations, chips, bond wires, etc.). The factors to examine include the degree of crosslinking and the homogeneity of the polymer network, as well as defect-free bonding and adhesion to the respective substrate surfaces. Susceptibility to AMP and partial discharges can be triggered by delaminations, porosity, or insufficient integration of fillers into the polymer matrix.

To support the selection of modules based on the preliminary pre-selection made by the system manufacturer, rapid quality tests such as the high-voltage “Coating Reliability Test” (CoRe test) according to IEC PAS 61191-10 can be helpful. Zestron currently applies this test up to 800 V. In this test, the module is subjected to water, representing a worst-case scenario to uncover potential weaknesses without claiming to predict the module’s lifespan. By monitoring possible leakage currents of different modules over a test duration ranging from several hours to a few days, significant quality differences can be effectively identified.

For comparative testing of power modules regarding delaminations, network inhomogeneities, and penetration paths for moisture and harmful gases, a quality test based on iodine vapor can be used [4, 6]. This is a multimodal highly accelerated stress test (HAST) that simultaneously applies stressors such as moisture, harmful gas, and temperature. Due to this combined stress environment, the test duration can be significantly shortened. An initial pre-selection of modules for subsequent qualification testing (e.g., according to AQG324 via H³TRB) can be completed within a few hours. Besides saving time and reducing the duration of optimization cycles, this approach can also substantially lower development costs.

Stress influence effects on functionality

Does the applied stress influence the functionality of the module or the electrical circuit? This fundamental question remains, when analyzing and interpreting the results after quality testing, as well as exposure to any stress (H³TRB testing, vibration, mechanical shock, etc.). It brings the initially and currently in the community debated issue back into focus, whether an optically visible dendritic structure in the insulation trench after H³TRB testing or field stress constitutes a problem, even if no obvious electrical anomalies are observed in the circuit characteristics or electrical functionality.

One way to judge these optical or covered electrical irregularities more sensitively is through impedance spectroscopy (EIS) for module evaluation. Zestron has gained experience with this approach,



Figure 5: Procedure of test evaluation supported by impedance spectroscopy (EIS).

performing impedance spectroscopy not as an absolute measurement but in a comparative manner – measuring before and after stress exposure (Figure 5).

This method allows even minor changes in the impedance profile to indicate early signs of creeping currents or low-impedance pathways in the system, thus revealing potential module deficiencies under continued stress. Depending on which contacts are measured, it can also provide indications as to whether the weaknesses are more likely located on the chip side, at the interface between the chip and the insulation material, or within the insulation material itself. In many cases, the impedance profile can also predict which weaknesses are to be expected. For example, delamination effects and water ingress in polymer systems influence the impedance curve differently.

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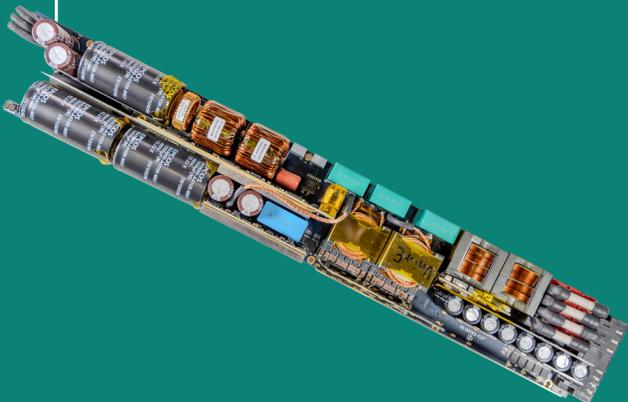
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95 W/in³



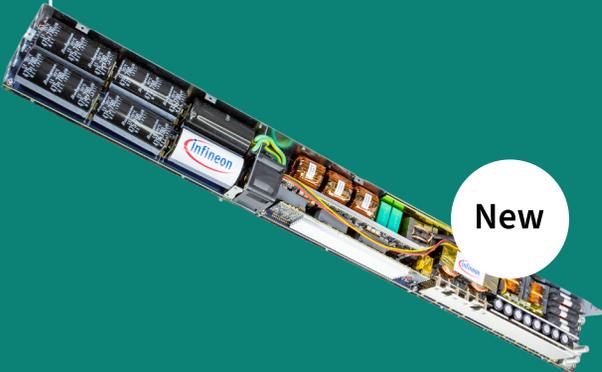
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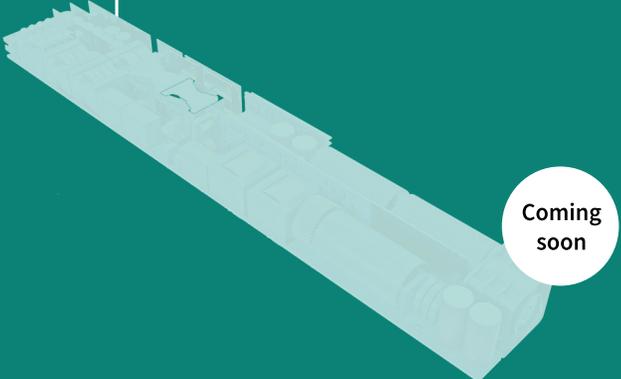
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How to choose a Charger for your Li-ion Batteries: Maximising Battery Life and Charger Efficiency

“Choosing the correct method of charging your batteries is important in ensuring they perform optimally and last longer. Selecting the right charger is as vital a decision as the choice of battery.

By Dag Pedersen, Marketing Manager, Mascot



Figure 1: Which Li-ion charger fits best?

As with most other charger types, Li-ion chargers use the typical three main charging phases (figure 2):

Step 1: Constant current charge

When a Mascot charger is connected to mains and a battery, it starts in ‘constant current’ (CC) mode, and charges at maximum current with a yellow LED indicator until the battery reaches 80 % – 95 % capacity. If the battery voltage is below 3 V per cell, a low current start-up will be applied. If normal voltage isn’t reached, charging stops, and the LED light flashes red four times.

Step 2: Constant voltage (timer) charge

While in ‘constant voltage’ (CV) mode, the charge current decreases, and the LED flashes yellow. The charger remains in this mode until the current has decreased to the end of charge level or the CV timer runs out.

Step 3: Charge complete

When fully charged, the LED turns green, and the charger can remain connected, starting a new cycle if the battery voltage decreases with 0.1 V per cell. Li-ion chargers, when compared to lead-acid chargers, have a number of benefits including higher voltage per cell, tighter tolerances, and no trickle or float charge. Li-ion cell manufacturers are very strict on the correct setting because Li-ion cannot accept an overcharge.

What is the best charging current?

The battery’s mAh or Ah capacity determines the appropriate charging current; most Li-ion cells should not exceed a 1 C charge rate, with 0.5 C being ideal for longer battery life. Charging at a lower current, especially below 0.5 C, helps improve performance and longevity. If the application requires a faster charging, then the

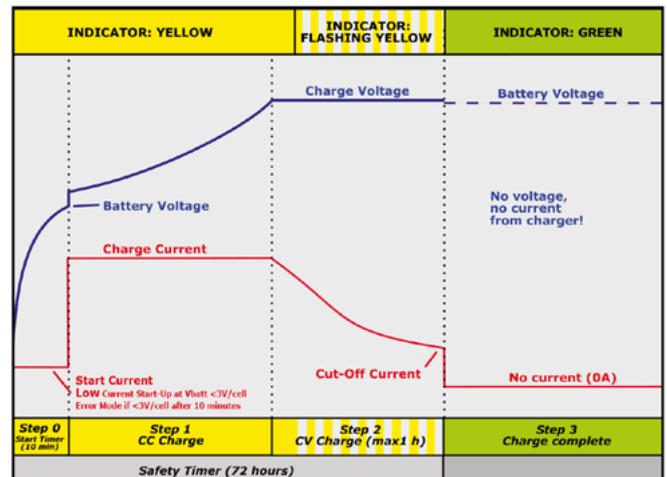


Figure 2: Charging voltage profile of a typical Li-ion charger circuit.

charging current will generally be increased. As a general rule of thumb, batteries shouldn’t be charged when in use, but the best way to do so would be to use a charger that delivers at least 25 % of the total Ah of a battery.

Selecting a charger

When selecting a charger, there are several factors to consider. These include where it will be used, the battery’s capacity, available charging time, and required power output. If the charger will be used abroad, look for one with universal input (90 V to 264 V). For outdoor use, use an output with a waterproof (IP67) rating. If ambient temperatures are extreme, opt for a charger with a sensor during charging. It is also important to verify the charger’s certifications and approvals, as these are good indicators of quality and compliance with standards. Efficiency figures should also be compared to identify the most energy-efficient option. Ideally, a high-quality charger should offer optimised charging modes (pre-charge, CC, CV) and include protective features such as overvoltage, undervoltage, short circuiting, reverse polarity, and temperature protections, as well as meeting safety and EMC regulations.

It’s also important to use chargers from reputable brands with professional R&D and manufacturing capabilities, which can offer safer products and custom designs. Low-cost chargers should be avoided as they may shorten battery life, especially those without end-of-charge control or those with trickle charging that may lack current control. Avoid chargers that cause ripple power fluctuations above 5 %, as these can damage the battery; some brands may not adhere to this standard. Always check the specifications before making a purchase.

Optimizing charger performance

To optimise charger performance and protect your batteries avoid using unregulated chargers and never exceed the specified charging voltage to prevent damage. Store batteries in a cool, well-ventilated area and avoid charging in extreme temperatures. Calculate charge time by dividing the battery's amp-hour rating by the charger's amp rating, adding time for top-off charging. Turn off devices or disconnect loads during charging, as parallel loads can interfere. For longevity charge batteries to 40 - 50 % before storage. Note: Some chargers may not fully charge the battery to 100%, so monitor accordingly.



Figure 3: A typical high-quality charger for Li-ion batteries.

There are so many different types of chargers on the market that it's vital to spend time considering the options available and making the right choice. The most important thing to check is that the voltage matches your battery, and that the quality is sufficient for your needs. Cheaper chargers can be fine if the decision to purchase one is informed, and the charger is used safely. However, if budget permits, investing in higher quality products will ensure a longer life for both your chargers and your batteries - decreasing cost in the long run.

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Studies have shown that charging to a slightly lower voltage can dramatically increase the number of cycles that you can get out of the battery. Charging to 4.1 V instead of 4.2 V (which is the equivalent of charging to around 90 %) has been shown to add 50 % or more cycles to a battery over its entire lifespan. To do this, a higher-specification charger is required.

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Reports of Silicon's Death Have Been Greatly Exaggerated

Silicon remains the backbone of the power semiconductor industry due to its mature manufacturing base, cost structure, and reliability. However, in recent years the industry has only seen incremental improvements in silicon power technology. The last significant breakthrough took place in 1998 with the commercialization of Superjunction devices, more than 25 years ago.

By Ryan Manack, Vice President of Marketing, iDEAL Semiconductor

SuperQ™ is a new MOSFET architecture that extends the performance of silicon power devices within this established framework. It uses a novel, patented asymmetrical reduced surface field (RESURF) structure that significantly increases the n-conduction region of the device – up to 95% of the conduction area versus 50% or less in traditional Superjunction and other RESURF technologies.

This structural shift enables notable reductions in on-resistance ($R_{DS(on)}$) and switching losses while maintaining the proven advantages of silicon: low cost, high-volume manufacturability, and robust reliability.

Commercialization of devices based on this technology began in July 2025, with iDEAL Semiconductor launching an initial product lineup including both 150 V and 200V MOSFETs, which are in full production. Higher-voltage offerings, from 250 V to 400 V, are in development as part of the near-term roadmap.

SuperQ is positioned for applications where silicon's cost and availability are critical but where performance headroom is still required – such as motor drives, AI data-center power delivery, telecom, and other high-efficiency power conversion systems. In this article we'll examine how the technology enables these advances in Cost x Performance versus legacy silicon devices.

SuperQ Technology: Architectural Benefits

To better understand SuperQ, it's essential to trace the evolution of power semiconductor architectures, starting with 1979's "HEXFET" MOSFET. This structure utilized 100% of the silicon area for conduction but suffered from quadratic resistance increases at higher voltages, which significantly impacted efficiency (see Figure 1).

In 1998, RESURF architectures, more commonly referred to as "Superjunction," were commercialized. This technology introduced 2-dimensional charge balancing which allowed for higher voltage blocking (BV) and resistances that scaled almost linearly with BV. However, these architectures dedicate only about 50% of the die to conduction, with the remaining P-regions only

supporting voltage blocking (see Figure 1). Performance in these devices is plateauing as the architectures reaches manufacturing limits with correspondingly higher costs.

As a result, the industry steered research dollars towards alternative, wide-bandgap (WBG) materials like silicon carbide (SiC) and gallium nitride (GaN). These semiconductor technologies gave further gains but came with significantly higher costs as well as manufacturing complexities, long term reliability risks, and implementation challenges.

Unlike Superjunction architectures, SuperQ uses an asymmetrical RESURF structure (see Figure 1). Further gains in performance are achieved by widening the silicon's N-conduction regions. SuperQ replaces Superjunction's P-pillar with a proprietary, patented high aspect ratio deep trench with sidewall charge. The technology achieves voltage blocking at 19–20 V/ μm and enables thinner epitaxial layers with higher doping profiles.

This results in a dramatically lower specific on-resistance (R_{sp}), which is 2.6x better than traditional silicon at 200 V, without departing from silicon's mature ecosystem (see Figure 2).

The design also leverages a simple, CMOS-compatible manufacturing flow on high-volume 200 mm or 300 mm wafers, ensuring high yields and compatibility with existing fabs.

Unlike Superjunction's complex epi+implant process, SuperQ is optimized for performance and cost. The platform is scalable across diodes, MOSFETs, IGBTs, power ICs,

and can be used for voltages from 60 V to 1,200 V, with potential extensions to future alternative semiconductor materials when they are commercially viable.

Performance Metrics and Benefits

SuperQ offers improved performance through measurable gains in silicon MOSFET figures of merit (FOM). Its architecture optimizes the conduction area, resulting in a significant reduction in on-resistance. For instance, the 150 V technology scales as low as 2.5 m Ω in a TOLL package, which is equivalent to the industry leader and 1.6x lower than the next best competitor.

At 200 V, iDEAL is capable today of 3.7 m Ω in a TOLL – almost half of the industry leader and 2.6x lower than the next best competitor. At 400 V, capabilities in a TOLL package extend not just below silicon but industry's lowest silicon carbide device at 400 V.

Beyond conduction, switching metrics stand out. Switching charge (Q_{SW}) is reduced by up to 2.1x compared to leading competitors (see Figure 3). This parameter, proportional to switching time, minimizes losses as shown by the formula for half-cycle switching loss

$$P_{SW} = \frac{1}{2} * V * I * \frac{Q_{SW}}{I_G} * F_{SW} \quad (1)$$

As a result, SuperQ devices can switch up to 2.1x faster or save the equivalent power losses, supporting higher frequencies in demanding topologies. The device also stores less energy in the device's Output Capacitance (C_{OSS}). Compared to silicon competitors it is up to 4.4x lower. Even compared to industry leading GaN devices, capacitive

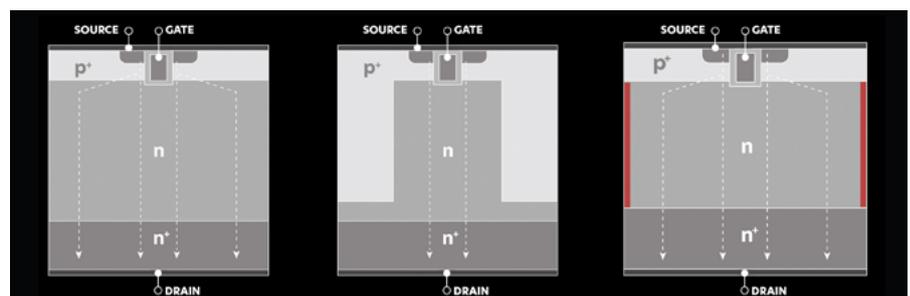


Figure 1: Evolutionary diagrams of MOSFET structures, showing SuperQ's asymmetrical design (right) versus conventional HEXFET (left) and Superjunction (middle)

stored energy (E_{OSS}) is cut in half (see Figure 3).

$$P_{EOSS} = E_{OSS} * F_{SW} \tag{2}$$

Applications and Reliability

SuperQ’s versatility extends to a wide array of high-demand applications, addressing the growing need for efficient power management in an electrifying world. Target sectors include AI data centers, switch-mode power supplies (SMPS), telecom infrastructure,

Voltage	iDEAL Semi	Comp A	Next Best Comp	Improvement
150V	2.5 mΩ	2.5 mΩ	3.9 mΩ	Up to 1.6x
200V	3.7 mΩ	6.7 mΩ	9.5 mΩ	Up to 2.6x
250V	7.3 mΩ	20.0 mΩ	16.0 mΩ	Up to 2.7x
300V	8.7 mΩ	N/A	19.0 mΩ	Up to 2.2x
400V	11.5 mΩ	14.4 mΩ (SiC)	65.0 mΩ	Up to 5.7x

Figure 2: Lowest $R_{DS(on)}$ in TOLL package for iDEAL’s SuperQ devices versus two industry-leading competitors

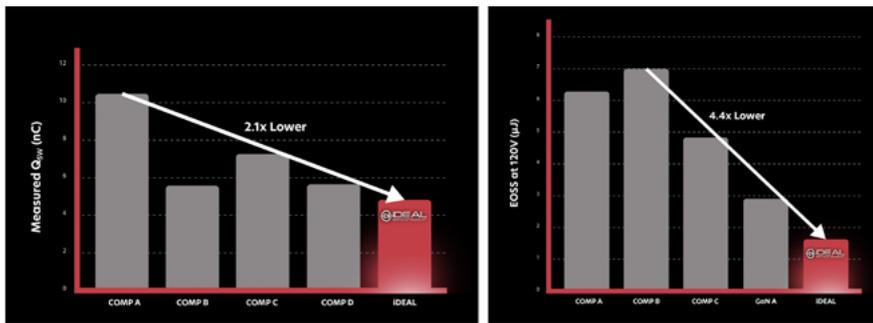


Figure 3: SuperQ vs. competition in measured Q_{SW} (left) and E_{OSS} parameters (right)

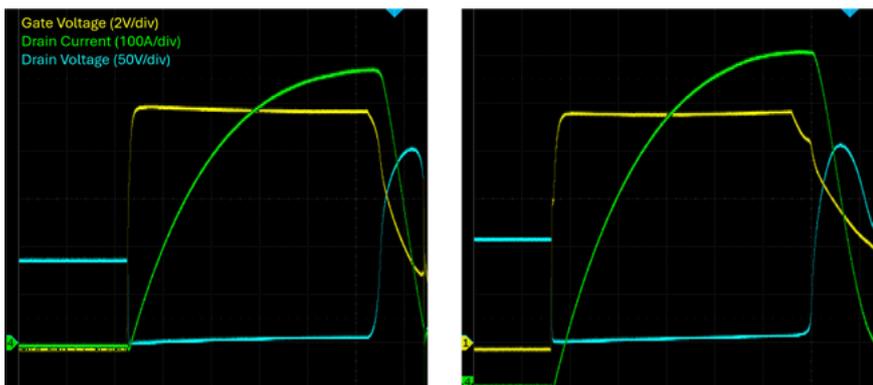


Figure 4: Peak short circuit current to failure for Competitor A (left, 570A) and SuperQ (right, 692A) for similar $R_{DS(on)}$ and silicon area. Green = Drain Current, Blue = Drain-to-Source Voltage, Yellow = Gate-to-Source Voltage

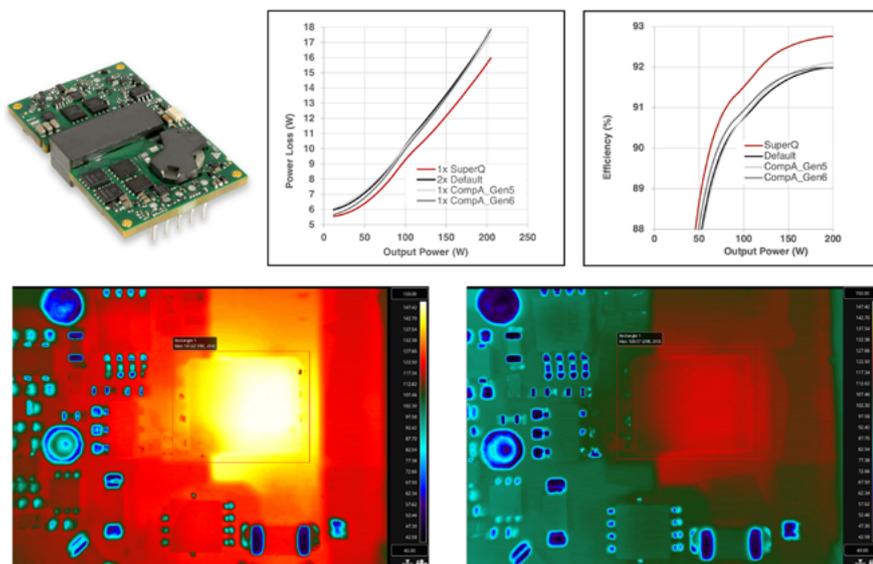


Figure 5: SuperQ performance in an isolated DC/DC converter. Competition 152°C (left), SuperQ 121°C (right). 48Vin, 12Vout, 17A, 5min soak, no forced air cooling

USB-C fast charging, solar inverters, medical devices, and battery backups, where low $R_{DS(on)}$ and switching losses minimize heat and size. SuperQ MOSFETs are used in a variety of ways – as synchronous rectification for 54 V AI servers, protection-type linear switching in battery applications and control MOSFETs in Telecom and other isolated DC/DC bricks.

In brushless direct current (BLDC) motor drives, SuperQ is used for both three-phase inverter switching as well as battery protection. When operated as a battery disconnect switch, it combines industry leading on-resistance and robustness including short-circuit current handling up to 700A (see Figure 4).

Another specific example in Telecom/Networking: SuperQ is used as the primary side control MOSFET in a commercially available isolated DC/DC converter operating at 270 kHz in an Active Clamp Forward topology. iDEAL’s SuperQ devices reduce power loss by up to 2 Watts and run as much as 31°C cooler than leading competitors. This translates to improved thermal management and longer system lifespan—benefits made possible by SuperQ’s low resistance and ultra-low Q_{SW} and E_{OSS} .

On reliability, the SuperQ architecture is engineered to exceed industry standards, with all devices 100% production-screened for unclamped inductive switching (UIS) and delivering energy ratings that surpass application needs.

The safe operating area (SOA) offers wide current/voltage margins and thermal stability, preventing runaway in pulsed operations. Qualified to 175°C junction temperatures, SuperQ endures rigorous JEDEC tests – including HTRB, HTGB, thermal cycling, BHAST, IOL, HTSL, and UHAST – stressed at least twice the standard levels. This level of screening and qualification ensures long-term reliability in even the most demanding industrial, automotive, and data center environments.

Future Implications

The introduction of SuperQ technology represents a significant step forward in extending the performance limits of silicon power devices. By implementing an asymmetrical RESURF structure, SuperQ achieves notable reductions in $R_{DS(on)}$, Q_{SW} , and E_{OSS} , while maintaining the advantages of established silicon processes.

SuperQ provides a practical path for system designers seeking higher efficiency and power density without moving away from the mature silicon manufacturing ecosystem. Covering a voltage range from 150 V to 400 V, the platform offers competitive conduction and switching performance for applications such as AI data centers, motor drives, industrial automation, and telecom power systems.

As power conversion requirements continue to grow in complexity and scale, SuperQ demonstrates that silicon still has room for meaningful innovation and performance enhancement.

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How to Model Coupled Inductors in a SEPIC Converter

This article discusses how to best model coupled inductors in a single-ended primary inductance converter (SEPIC) topology. Methods to build a proper model are introduced and the equations are included. If the coupled inductor is not modeled correctly, the simulated result can be quite different from the bench result.

By Wei Gu, Director, Product Applications, Analog Devices

A single-ended primary inductance converter (SEPIC) topology allows for the input to be higher, equal, or lower than the desired output voltage (Figure 1). The conversion ratio as a function of duty cycle is shown in continuous conduction mode (CCM) in Equation 1.

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1-D} \tag{1}$$

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown. Compared to the flyback converter, the SEPIC converter has the advantage that both the power MOSFET and the output diode voltages are clamped by the capacitors (C1 and COUT), therefore there is less voltage ringing across the power MOSFET and the output diodes. The SEPIC converter requires much smaller input capacitors than those of the flyback converter. This is because, in the SEPIC converter, inductor L1 is in series with the input, and the ripple current flowing through the input is continuous.

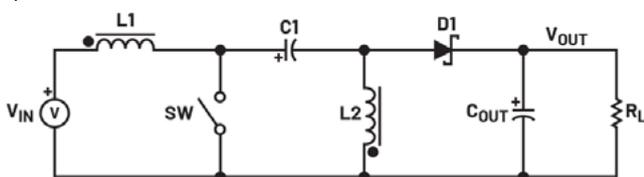


Figure 1: A SEPIC converter.

Given an operating input voltage range and having chosen the operating frequency and ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using Equation 2.

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \times \Delta I_{SW} \times f} \times D_{MAX} \tag{2}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1 μH to 100 μH. By making L1 = L2, and winding them on the same core, the value of the inductance in the Equation 2 is replaced by 2L, due to the mutual inductance shown in Equation 3.

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \times f} \times D_{MAX} \tag{3}$$

Coupled Inductors

Using a coupled inductor can simplify the design of the SEPIC converter by reducing the number of discrete components required and minimizing the complexity of the control circuitry. This can lead to cost savings, a smaller footprint, and a significant reduction of the complexity of the small signal model, enabling higher bandwidth by eliminating the SEPIC resonances calculated in Equation 4.

$$f_{SEPIC_RESONANCE} = \frac{1}{2\pi\sqrt{(L1 + L2) C1}} \tag{4}$$

While the coupled inductor is superior in performance, the simulated inductor current waveforms in LTspice don't always match the bench result. This is mainly due to the inaccuracy of the coupled inductor model. When a coupled inductor is simulated in LTspice, careful attention must be made to its model. For example, do not set K to 1 in a simulation without adding associated leakage inductors. Otherwise the simulated inductor currents become discontinuous, as shown in Figure 2.

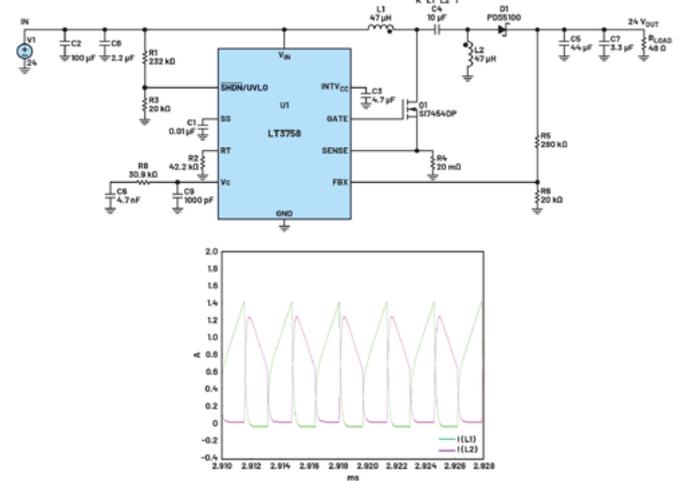


Figure 2: An LT3758 SEPIC with K = 1 and its simulated current waveforms.

Modeling a Coupled Inductor

To properly model the coupled inductor, explicitly adding a leakage inductor is a must if K is set to be 1. Also, due to various winding structures, it's possible that the two magnetizing inductances are different. One of the coupled inductor models is shown in Figure 3 and a bench test is necessary to obtain the values since inductor vendors typically do not provide the needed values.

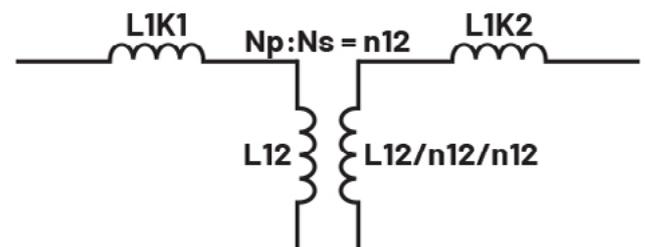


Figure 3: A coupled inductor model.

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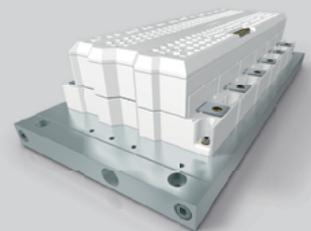
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Calculating these parameters based on the measured data is shown in Equation 5.

$$\begin{aligned}
 L11 &= L1k1 + L12 \\
 L22 &= L1k2 + \frac{1}{n12^2} \times L12 \\
 L1k11 &= L1k1 + n12^2 \times L1k2 \\
 L1k22 &= L1k2 + \frac{1}{n12^2} \times L1k1
 \end{aligned}
 \tag{5}$$

While L11 is the measured primary self-inductance with secondary open, L22 is the measured secondary self-inductance with primary open, L1K11 is the measured primary inductance with secondary shorted, and L1K22 is the measured secondary inductance with primary shorted. In this example, the measured L11 is 46.66 μH, L22 is 45.78 μH, L1K11 is 0.725 μH, and L1K22 is 0.709 μH. Therefore, the calculated n12 is 1.011, L12 is 46.374 μH, L1K1 is 0.286 μH, and L1K2 is 0.429 μH. The completed coupled inductor model is shown in Figure 4.

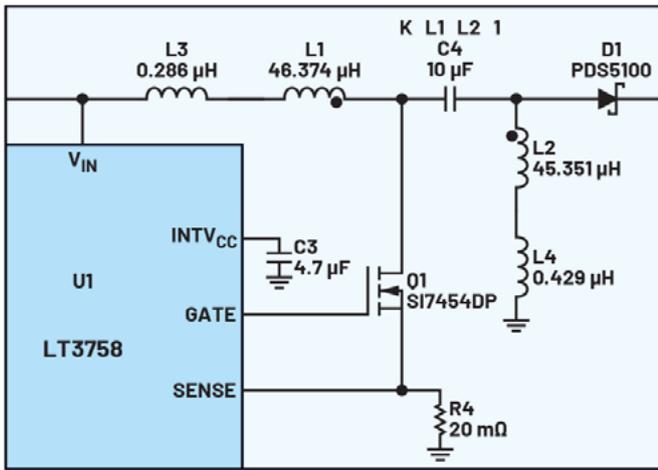


Figure 4: A completed coupled inductor model.

The simulated results match the bench result well (figure 5). In this example, the measured L11 is 46.66 μH, L22 is 45.78 μH, and L1K11 is 0.725 μH. The calculated Lm is 45.857 μH. The calculated K is 0.992.

$$k = \frac{Lm}{\sqrt{L11 \times L22}}
 \tag{6}$$

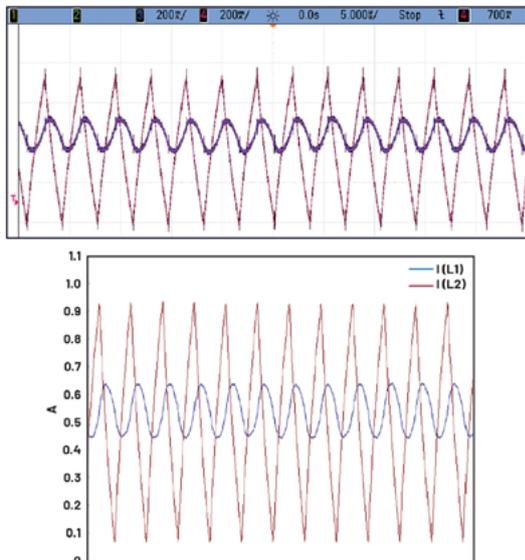


Figure 5: Bench result vs. simulation results.

The simulated result based on the model in Figure 8 matches the bench result well with this inductor model, too.

Another way to model the coupled inductor is to use the non-unit coupling factor. In this case, the leakage inductors do not need to be explicitly specified as shown in Figure 6.

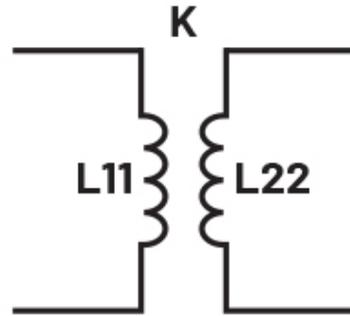


Figure 6: A coupled inductor model with non-unit K.

The same bench test on the coupled inductor is performed to collect the information for calculating the K. Equations with two-port parameters are shown in Figure 7.

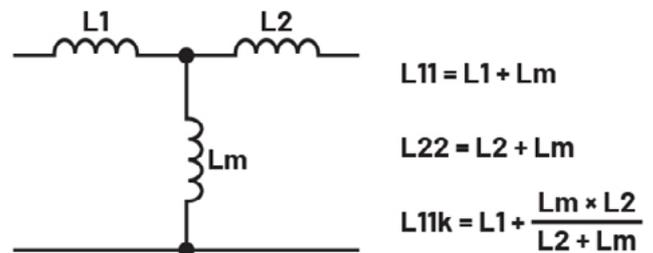


Figure 7: Equivalent circuit and its equations.

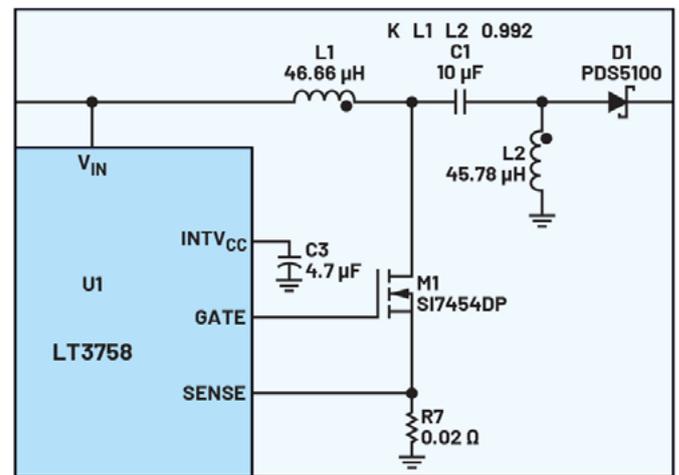


Figure 8: A complete coupled inductor model with a non-unit K.

Conclusion

Power supply designers are sometimes confused by the nonideal inductor current waveforms obtained from LTspice simulation or bench test. With the proper coupled inductor model, the simulated inductor current waveforms match well with the bench result.

Reference

Erickson, Robert W. and Dragan Maksimović. Fundamentals of Power Electronics, 2nd edition. Kluwer, January 2001.

HITACHI



Thyristors - Real power for heavy industries

Hitachi Energy's new range of 8500 V high-power thyristors with 100 mm pole piece offers lowest on-state losses and highest blocking stability. The safe operation temperature up to $T_{jmax} = 125\text{ }^{\circ}\text{C}$ assures reliable operation in demanding industrial applications.



hitachienergy.com/semiconductors

Low Profile AC-DC Power Supply Rated up to 900 W

Acopian Power Supplies launched their higher power LP2 switching power supplies rated up to 900 Watts. Models are available in both single and wide-adjustment DC output voltages ranging from 5VDC to 125VDC and 0-5VDC to 0-125VDC and up to 900 watts.



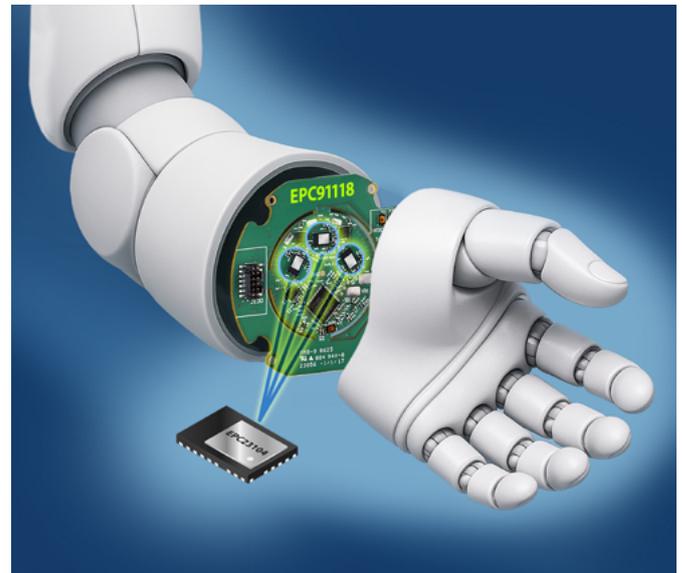
All models are voltage and current programmable. In addition, these units are constant current controllable and can also be controlled from 0 volts and 0 amps to their rated output. All models have been tested to run off GFCI circuits. These switching power supplies are highly configurable. Standard features include, but are not limited to universal input (90-265VAC) or they can operate off DC input (110-350VDC); PFC, output enable, constant voltage and current modes, voltage and current monitor terminals and programming capabilities, short circuit and overload protection, touch-safe pluggable connectors, remote sensing, 'V ok' signal monitoring and 'Soft start' operation. Optional features include N+1 redundancy/paralleling up to 4 like models, alarm with relay contacts and moisture/fungus proofing. Models can be convection cooled (600 watts) or fan cooled (900 watts). These power supplies are ideal for use in test equipment, analog systems, power, military, aerospace, manufacturing, controls, medical, aviation, r&d applications and more.

www.acopian.com

GaN-Based Motor Drive Reference Design for Humanoid Robots

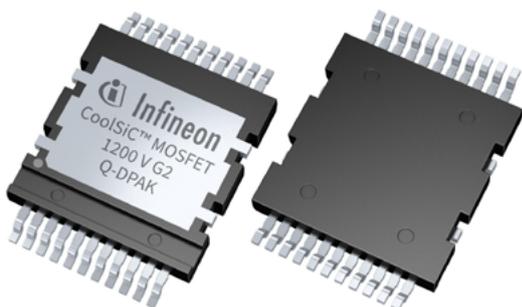
Efficient Power Conversion Corporation (EPC) introduces the EPC91118, which is claimed to be "the first commercially available reference design to integrate gallium nitride (GaN) IC technology for humanoid robot motor joints". Optimized for space-constrained and weight-sensitive applications such as humanoid limbs and compact drone propulsion, the EPC91118 delivers up to 15 A_{RMS} per phase from a 15 V to 55 V DC input in a compact circular form factor. At the heart of the EPC91118 is the EPC23104 ePower™ Stage IC, a monolithic GaN IC that enables higher switching frequencies and reduced losses. The GaN-based power stage is combined with current sensing, a rotor shaft magnetic encoder, a microcontroller, RS485 communications, and 5 V and 3.3 V power supplies - all on a single board that fits entirely within a 32 mm diameter footprint. Each of the phases of a 3-phase BLDC motor can be driven with 15 A_{RMS} at a PWM frequency of 100 kHz with 50 ns dead time. The fully integrated board includes a controller, sensor and power conversion and uses MLCC-only DC link capacitors to reduce size and to increase liability. While the inverter has a diameter of 32 mm, the external frame's diameter is 55 mm.

www.epc-co.com



1200 V MOSFETs in a Q-DPAK Package

Infineon Technologies has launched the CoolSiC™ MOSFETs 1200 V G2 in a top-side-cooled (TSC) Q-DPAK package. These devices deliver enhanced thermal performance, system efficiency, and power density. They were specifically designed for demanding industrial applications that require high performance and reliability, such



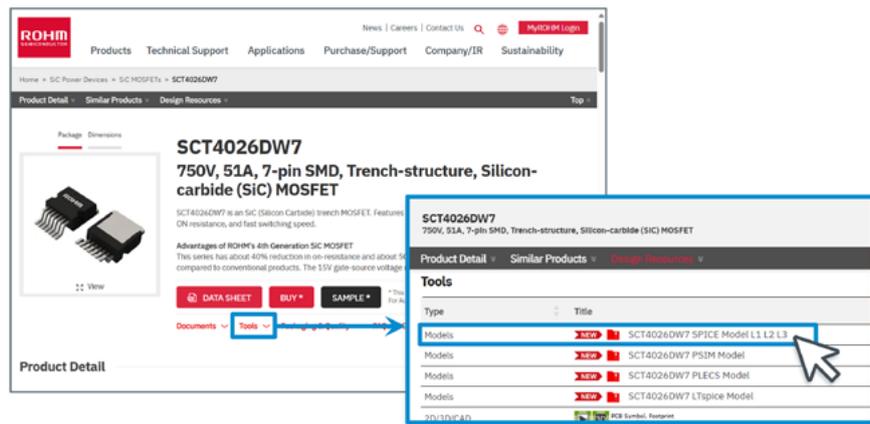
as electric vehicle chargers, solar inverters, uninterruptible power supplies, motor drives, and solid-state circuit breakers. The CoolSiC 1200 V G2 technology enables up to 25 percent lower switching losses for equivalent $R_{DS(on)}$ devices, thereby increasing system efficiency by up to 0.1 %. Utilizing Infineon's .XT die attach interconnection technology, the G2 devices achieve more than 15 % lower thermal resistance and an 11 % reduction in MOSFET temperature compared to G1 family products. The $R_{DS(on)}$ values, range from 4 m Ω to 78 m Ω , while the technology supports overload operation up to a junction temperature (T_{vj}) of 200 °C. The CoolSiC MOSFETs 1200 V G2 are available in two Q-DPAK configurations: a single switch and a dual half-bridge. Both variants are part of Infineon's broader X-DPAK top-side cooling platform. The standardized package height across all TSC variants - including Q-DPAK and TOLT - is 2.3 mm.

www.infineon.com

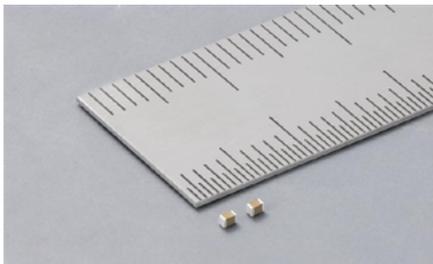
Level 3 SPICE Models featuring enhanced Simulation Speed

ROHM has announced the release of new Level 3 (L3) SPICE models that deliver significantly improved convergence and faster simulation performance. ROHM's earlier Level 1 SPICE models for SiC MOSFETs were precisely replicating key device characteristics. However, challenges such as simulation convergence issues and prolonged computation times revealed the need for further refinement. The L3 models utilize a simplified approach that maintains both computational stability and accurate switching waveforms while reducing simulation time by approximately 50% compared to the L1 models. This allows for high-accuracy transient analysis of the entire circuits at significantly faster speed, streamlining device evaluation and loss assessment in the application design phase. By the end of April 2025, ROHM has released 37 L3 models for its 4th Generation SiC MOSFETs, available for download directly from the Models & Tools section of each product page. The L1 models will continue to be offered alongside the new versions. A comprehensive white paper is also provided that facilitates model adoption.

www.rohm.com



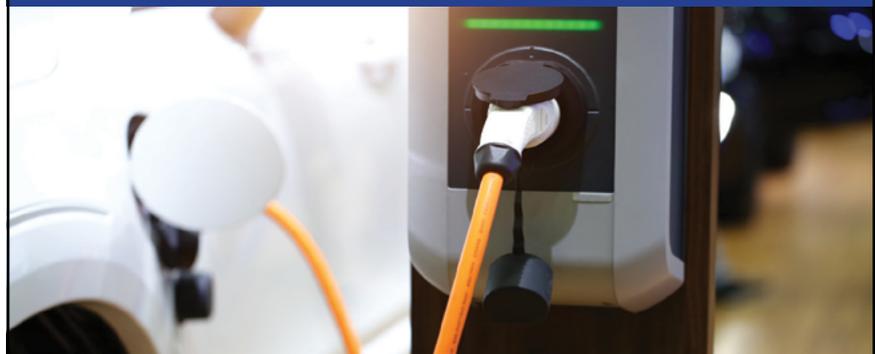
47 μF Multilayer Ceramic Capacitor in 0402-inch Size



Murata has begun "the world's first mass production of the 0402-inch size (1.0 × 0.5 mm²) multilayer ceramic capacitors (MLCC) with a capacitance of 47 μF. The devices are available in two variants with different temperature characteristics. Compared to Murata's conventional 0603-inch size product with the same capacitance, this new capacitor reduces mounting area by approximately 60 %. Additionally, it delivers about 2.1 times the capacitance of Murata's previous 22 μF product in the same 0402-inch size. The MLCC is available in two variants - the X5R (EIA) GRM158R60E476ME01 with an operating temperature range of -55 to +85 °C, and the X6S (EIA) GRM158C80E476ME01 with an operating temperature range of -55 to +105 °C. Both devices feature a ±20% tolerance and rated voltage of 2.5Vdc.

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- Maximize performance characteristics

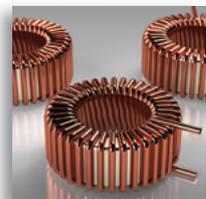
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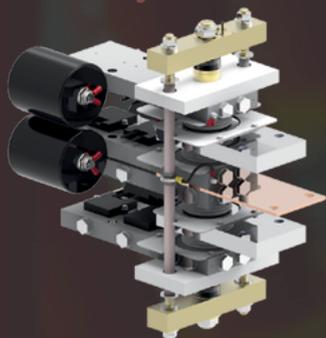
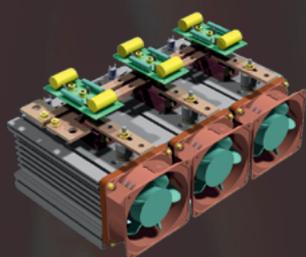
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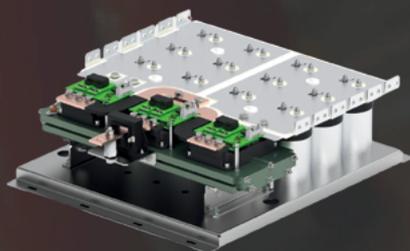
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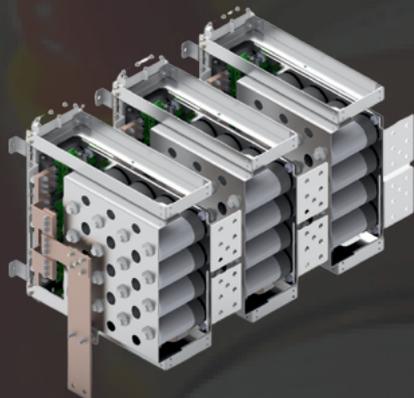
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DC/DC



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Our North-American division:

TVS Diodes cut Clamping Voltage

Littelfuse launched the 5.0SMDJ-FB TVS Diode Series, a 5000 W surface-mount solution in a DO-214AB package engineered to protect sensitive DC power lines from overvoltage transients. This series incorporates foldback technology, which delivers up to 15% lower clamping voltage (V_C) compared to traditional solutions, while maintaining Breakdown Voltage (V_{BR}) above the Reverse Stand-off Voltage (V_R). It is a drop-in replacement to legacy 5.0SMDJ series with the same DO-214AB (SMC) footprint. These devices protect DC power lines across a variety of demanding applications, including Power over Ethernet (PoE) systems, AI and data center servers, ICT equipment power supplies and industrial DC power distribution.



www.littelfuse.com

Simplifying Reverse Battery Polarity and Overvoltage Protection in Automotive Architectures

Diodes Incorporated introduced the AP74502Q and AP74502HQ automotive-compliant 80 V ideal diode controllers, providing protection against reverse connections and voltage transients. Typical applications include ADAS, body control modules, infotainment systems, exterior lighting, and USB charging ports. They also include a load disconnect function in case of overvoltage and undervoltage events, while they are suitable for all 12 V, 24 V and 48 V systems. The AP74502Q and AP74502HQ controllers also support input voltages as low as 3.2 V for operation even during severe cold crank conditions. Both devices share a peak gate turn-off sink current of 2.3 A, enabling rapid turn-off of the external N-channel MOSFETs when required, for example, during overvoltage or undervoltage events. When the charge

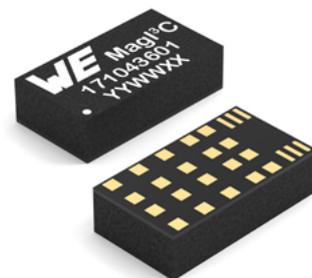


pump is enabled, the operating quiescent current is 62 μ A, and 1 μ A in disabled mode. The AP74502Q features a peak gate source current, typically 60 μ A, which provides a smooth start-up with inherent inrush current control. Both, AP74502Q and AP74502HQ are available in the industry-standard SOT28 package with an operating temperature range from -40 °C to +125 °C.

www.diodes.com

Power Modules for higher Currents

Würth Elektronik has expanded its Mag1³C-V DLM power module series with two new models. With output currents of 4 A and 5 A respectively, they further enhance the performance of the existing portfolio of compact DC/DC power supply modules. The modules are designed for input voltages from 4 to 36 V and come in a space-saving LGA-26 package (11 × 6 × 3 mm³). They provide an output voltage from 1 to 6 V and, like all power modules in the Mag1³C-V DLM series, integrate the essential components for a DC/DC power supply in its package: switching regulator with integrated MOSFETs, controller, compensation circuitry, and a shielded inductor. The power modules are claimed to “maintain high efficiency across the entire output current range by automatically switching between operating modes based on load requirements”. So, they contribute to a minimal output ripple, which is needed for precise and interference-sensitive applications. Typical applications include point-of-load DC/DC converters, industrial, medical, test and measurement equipment, or for supplying power to DSPs, FPGAs, MCUs, MPUs, and interfaces. The Mag1³C-V DLM modules achieve peak efficiencies of up to 96 percent and impress with their EMC performance in accordance with EN55032 Class B / CISPR-32. Additional features include selectable switching frequencies, automatic PFM/PWM transition, and a sync function for synchronizing to individual clock frequencies.

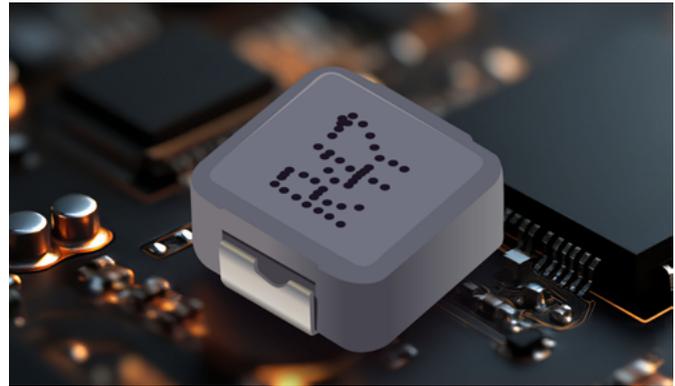


www.we-online.de

Shielded Power Inductor Series

Bourns announced its SRP4020T series shielded power inductors. This series features a carbonyl powder core with “excellent thermal stability and magnetic performance”, making it suitable for demanding environments. Its shielded construction suppresses magnetic interference and enhances Electromagnetic Compatibility (EMC). Offered in a (4.45 x 4.0 mm²), low-profile (1.8 mm) package, the SRP4020T Series supports operating temperatures up to +150 °C. The inductance range for this series is from 0.47 to 10 µH.

www.bourns.com



Board-mount EMI Filters

TDK Corporation introduced the TDK-Lambda RGF board-mount EMI filters. Suitable for power supplies with high input current requirements, these 20 and 40 A filters are designed to provide differential mode filtering. The RGF filters are encapsulated for protection in harsh environments, measure 52.8 x 35.2 x 12.7 mm³ in size, and feature a 5-sided metal case. The design includes two threaded and two non-threaded mounting holes, suited for cooling in both conduction and convection-cooled systems. Applications include harsh industrial, commercial-off-the-shelf (COTS), test and measurement, communications, broadcast, and robotics. The input voltage ranges from 0 to 80 V and withstands input transients of up to 100 V for 100 ms durations. The operating case temperature is between -40 to +120 °C, with a qualified Thermal Cycling Test (TCT)



of 700 cycles, or -40 to +125 °C with a 60 °C/minute ramp, and a 30 minute dwell time. The RGF filters are compliant to MIL-STD-810G 516.6 Procedure I & IV for shock and MIL-STD-810G 514.6 Procedure I, Cat 10 for vibration.

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Ultra-Fast Current Shunt Series

PMK announces the launch of its Ultra-Fast Current Shunts (UFCS), an innovation that aims to set a new industry standard for current measurement in high-performance power electronics. Designed to meet the demands of next-generation systems, UFCS shunts combine >1 GHz bandwidth with

ultra-low insertion inductance (<200 pH), enabling unparalleled signal fidelity in the analysis of ultra-fast transient currents. The UFCS shunts are ideally suited for applications involving GaN and SiC power semiconductors, where accurate switching loss measurements and pulse current analysis are critical. Their non-inductive frequency response ensures clean and reliable data acquisition, even in the most demanding wide-bandgap (WBG) environments.

With a compact, solder-in form factor and high current carrying capability, UFCS shunts deliver consistent and robust performance while minimizing parasitic effects. Whether you're validating high-speed switching behaviour or characterizing fast current pulses, the UFCS models provide the precision and reliability required in

today's advanced power electronics designs. For measurements requiring high common-mode rejection, the UFCS can be paired with PMK's FireFly® optically isolated voltage probes. Alternatively, they can be connected directly to any 50 Ω input measuring device for general-purpose use.

The first models available in the UFCS series include 11 mΩ, 24 mΩ, and 52 mΩ versions, covering a wide range of applications. 1 mΩ and 5 mΩ versions will follow shortly, expanding the portfolio for even higher current measurements without compromising signal fidelity. With UFCS, PMK redefines what's possible in current measurement, empowering engineers to push the boundaries of innovation in power electronics.

www.pmk.de



Gate driver photocouplers enhance MOSFETs and IGBTs switching efficiency

Toshiba Electronics Europe introduced gate driver photocouplers to control 1 A and 6 A class gate drive currents for small- to medium-capacity MOSFET and IGBT gate drives. The TLP579xH series is suitable for driving SiC MOSFETs and IGBTs in green energy and

factory automation applications, including industrial photovoltaic (PV) inverters, uninterruptible power supplies (UPSs), and electric vehicle (EV) charging stations, which operate in harsh thermal environments. All three devices in the TLP579xH series are designed to drive small to medium capacity power devices as well as IGBTs. The TLP5791H has a performance of -1.0/+1.0 A for peak high-level/low-level output current (I_{OLH}/I_{OHL}), with an under voltage lock out (U_{VLO}) threshold voltage (V_{UVLO+}) of 9.5 V (max.), a U_{VLO} threshold voltage (V_{UVLO-}) of 7.5 V (min.), and a U_{VLO} hysteresis voltage ($V_{UVLOHYS}$) of 0.5 V (typ.). With the TLP5794H, the peak output current spans from -6.0/+4.0 A for I_{OLH}/I_{OHL} , with a V_{UVLO+} of 13.5 V (max.), a V_{UVLO-} of 9.5 V (min.), and $V_{UVLOHYS}$ of 1.5 V (typ.). The TLP5795H is capable of -4.5/+5.3 A for peak high-level/low-level output current (I_{OLH}/I_{OHL}), with V_{UVLO+} of 13.5 V (max.), a V_{UVLO-} of 11.1 V (min.), and $V_{UVLOHYS}$ of 1.0 V (typ.). The TLP579xH series is a rail-to-rail output device that enables switching characteristics with less voltage drop from the power supply voltage. It operates within a temperature range of -40 °C to +125 °C and is housed in a SO6L package, featuring a minimum creepage distance of 8.0 mm and an isolation voltage of 5000 V_{RMS} .

www.toshiba.semicon-storage.com



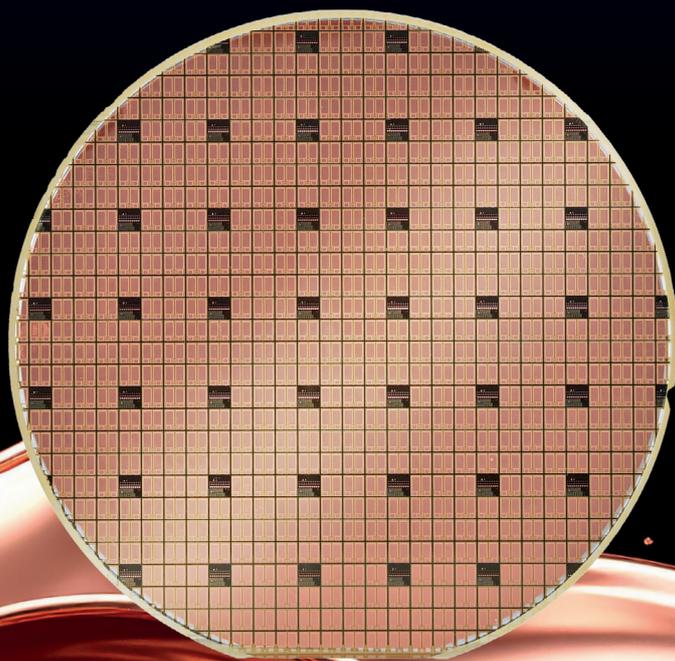
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