

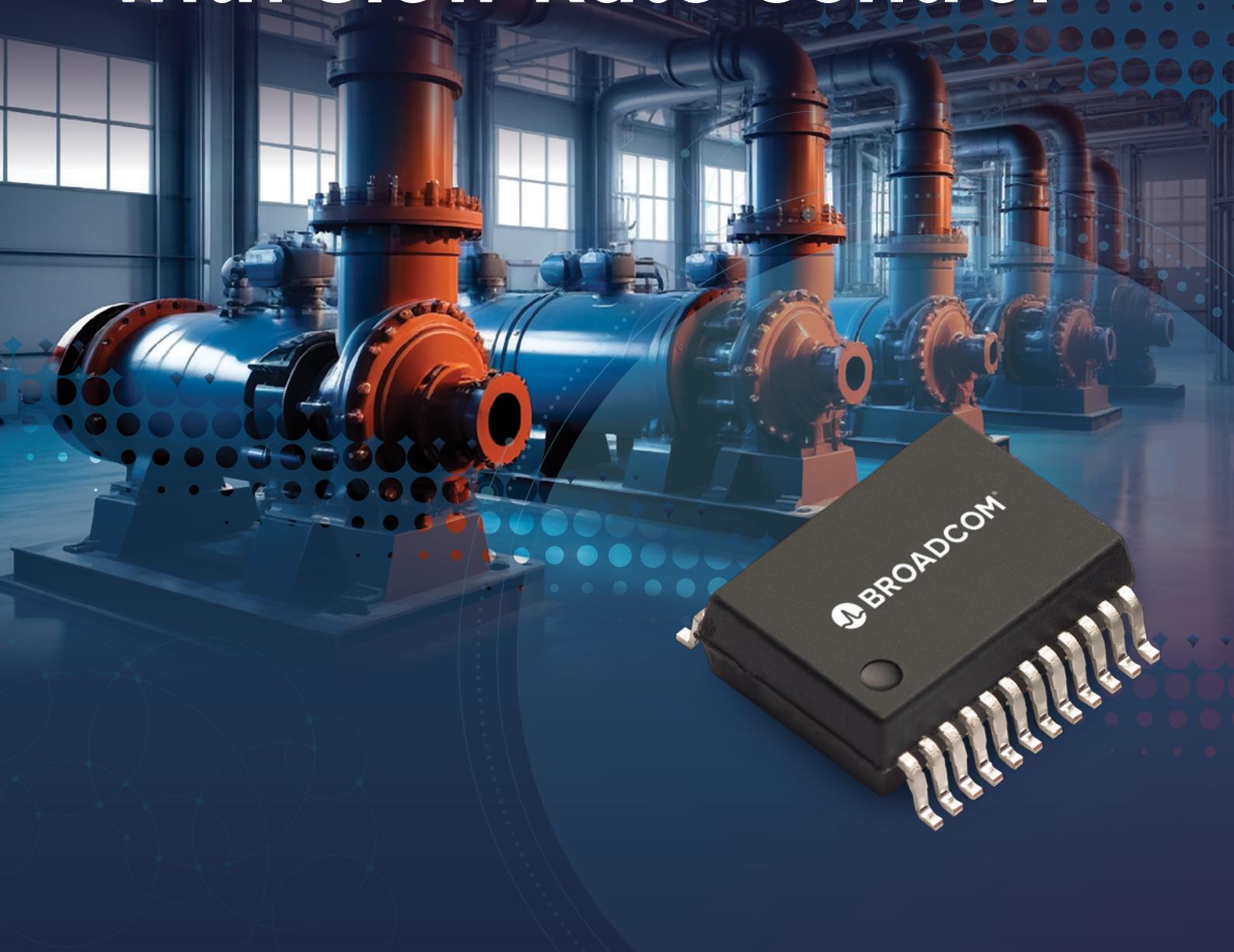
Bodo's Power Systems®

Electronics in Motion and Conversion

January 2026

GATE DRIVE OPTOCOUPLED

Improve Motor Lifetime and Efficiency with Slew Rate Control





POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the

- Differential inductance $L_{\text{diff}}(i)$ and $L_{\text{diff}}(jUdt)$
- Amplitude inductance $L_{\text{amp}}(i)$ and $L_{\text{amp}}(jUdt)$
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Also suitable for 3-phase inductors

WIDE RANGE OF MODELS

7 models available with maximum test current from 100A to 10000A and maximum pulse energy from 1350J to 15000J

KEY BENEFITS

- Very **easy and fast** measurement
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APPLICATIONS

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- **Routine tests** of small batch series and mass production



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www.ed-k.de

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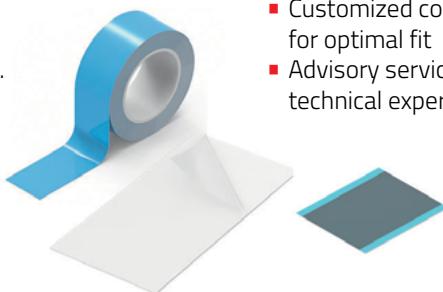


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Hall 2 - 110

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Highlights

- Gap filling, heat spreading and hybrid solutions
- Customized components for optimal fit
- Advisory services from technical experts

A Media

Katzbek 17a
24235 Laboe, Germany
Phone: +49 4343 42 17 90
Fax: +49 4343 42 17 89
info@bodospower.com
www.bodospower.com

Founder

Bodo Arlt, Dipl.-Ing.
bodo@bodospower.com

Editor in Chief

Alfred Vollmer, Dipl.-Ing.
alfred@bodospower.com

Correspondent Editor Bavaria

Roland R. Ackermann, Dipl.-Ing.
roland@bodospower.com

Editor China

Min Xu - xumin@i2imedia.net

US Support

Rusty Dodge
rusty@eetech.com

Creative Direction & Production

Bianka Gehlert
b.gehlert@t-online.de

Publisher

Holger Moscheik
holger@bodospower.com

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Dare to participate in the 2026 Challenge!



When I wrote this viewpoint, I had just returned from Bodo's Wide Band Gap Event in Munich, where we heard a lot about GaN and SiC, and more often than in previous years the experts talked about provisioning power for data centers. Using artificial intelligence normally requires at least 10 times the amount of energy than a typical web search, often even more. And the expected AI tsunami hasn't really gained its full momentum so far. This means we will need a lot of energy to power the data centers, and energy efficiency is and will be key.

Last year, Onsemi calculated, that a 1 % improvement of the data center efficiency can save 10 TWh of energy per year; that's a 1 with 13 zeroes. They calculated that 10 TWh is enough energy to power 926,000 US homes for a year or to produce 16 pumpkin spice lattes for every person on earth or to produce the heat for more than 1,800 homes for a year, however, they did not specify whether these homes are located in Alaska or in Hawaii or at whatever location.

With both GaN and SiC semiconductors we have the potential to work on intelligent power designs which can make a big difference. May be some engineers will dare to meet the 2026 challenge: Improve the efficiency of an already really efficient system by another (at least) 2.6 % within the year '26. Tell us about it; the best efficiency gain will receive a speaker slot at Bodo's WBG Event 2026.

The entire team of Bodo's Power Systems wishes you a great 2026 full of health, success and happiness.

By the way: To make children happy, we have once again donated 1,000 € to UNICEF instead of sending Christmas cards. In 2026, let us all contribute to make power designs better and – of course – more efficient!

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive, of every issue of the magazine, is available for free at our website bodospower.com.

My Green Tip of the month is a life hack that I learned from my parents: Never tilt the windows, never leave the windows open only a few centimeters – especially in summer and wintertime. When you ventilate, then open the windows entirely on one side of your house or apartment and on the opposite side as well. This way the cold air can rush through the rooms and replace the warm room air with fresh cold air with a positive side effect: The pushed-out warm air carries out a lot of moisture (from cooking, exhaling, plants etc.), while the incoming cold air is very dry. In Germany we call this "Stoßlüften", which literally translates into push/bump air exchange or burst/shock ventilation. If you keep Stoßlüften to less than two minutes you will exchange the air, but you will not significantly cool down the walls, floors, furniture etc. as their heat capacity is much higher than the heat capacity of air. Only a few minutes after finishing the Stoßlüften it'll be cozy and warm again – without significant additional heating. That's the efficiency of everyday life!

Events

embedded world 2026

Nuremberg, Germany March 10 – 12
www.embedded-world.de

CIPS 2026

Dresden, Germany March 10 – 12
www.cips.eu

AMPER 2026

Brno, Czech Republic March 17 – 19
www.bvv.cz/en/amper

APEC 2026

San Antonio, TX, USA March 22 – 26
www.apec-conf.org

emv 2026

Cologne, Germany March 24 – 26
[https://emv.mesago.com](http://www.emv.mesago.com)

SEMICON China 2026

Shanghai, China March 25 – 27
www.semiconchina.org

The Magnetics Show Europe 2026
Amsterdam, NL February 24 – 26
<https://themagneticsshow.materialsweekeurope.com>

DesignCon 2026
Santa Clara, CA, USA February 24 – 26
www.designcon.com

PLECS Conference 2026
Zurich, Switzerland March 3 – 4
www.plexim.com

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www.apec-conf.org

As The Premier Event in Applied Power Electronics™, APEC focuses on the practical and applied aspects of the power electronics business. This is not just a designer's conference.

APEC has something of interest for anyone involved in power electronics!



Power Partnership for in-orbit AI Processing

Vicor has partnered with Spacechips, developer of space-electronics solutions for satellites and spacecraft, to design power-dense, reliable transponders for in-orbit AI processing. Spacechips' AI1 transponder is radiation-tolerant, rugged and compact featuring Vicor's FPA power modules (Factorized Power Architecture). The demand for smaller satellites with sophisticated computational capabilities and reliable and robust onboard processor systems to support the 5 to 10 year duration of a mission, is pushing the limits of the latest ultra deep submicron FPGAs and ASICs and their power delivery networks. These high-performance processors have demanding, low-voltage, high-current power requirements and their system design is further compounded by the complexities of managing thermal and radiation conditions in space. In response, Spacechips has introduced its AI1 transponder, a small, on-board processor card containing an ACAP (Adaptive Compute Acceleration Platform) AI accelerator. The smart, re-configurable receiver and transmitter delivers up to 133 tera operations per second (TOPS) of performance that enables new Earth-observation, in-space servicing, assembly and manufacturing (ISAM), signals intelligence (SIGINT), and intelligence, surveillance and reconnaissance (ISR) and telecommunication applications to support real-time, autonomous computing while ensuring the reliability and longevity to complete longer missions. FPA is a power delivery system design



that separates the functions of DC/DC conversion into independent modules. In Vicor's radiation tolerant modules, the bus converter module (BCM) provides the isolation and step down to 28 V, while the pre-regulator module (PRM) provides regulation to a voltage transformation module (VTM) or current multiplier that performs the 28 V DC transformation to 0.8 V.

www.vicorpower.com

Strategic Partnership to accelerate GaN Adoption in India

Navitas Semiconductor and Cyient Semiconductors, a provider of ASIC, ASSP and power solutions, have announced a strategic long-term partnership intended to advance the adoption of GaN technology in India and establish a complete, end-to-end GaN ecosystem. Through this partnership, Navitas Semiconductor and Cyient

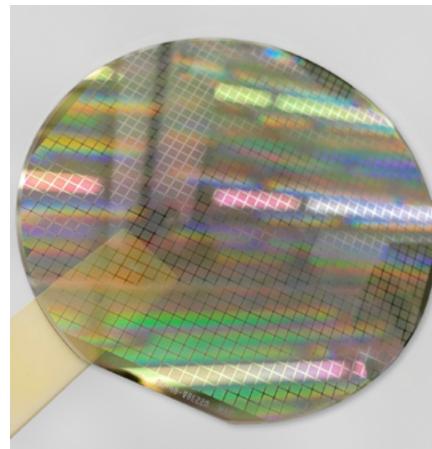


Semiconductors intend to co-develop GaN products, digital and mixed signal ICs, GaN based system modules and design enablement platforms targeting India's high voltage, high power market segments such as AI data centers, electric mobility, performance computing, energy grid infrastructure and industrial electrification. The partnership seeks to build a robust local supply chain and manufacturing ecosystem in support of the Indian Government's "Make in India" initiative. In addition, through this partnership Navitas and Cyient Semiconductor aim to deploy IC technology in accelerating solution development for high voltage and high-power markets. This is expected to include products based on Navitas' existing GaN technologies, along with new products tailored for India's unique market needs. This initiative is intended to empower Indian design houses and OEMs with locally sourced GaN components and manufacturing support, enabling faster development cycles and reducing barriers to GaN adoption in India.

www.navitassemi.com

Foundry Service for SiC MOSFETs

Through its XbloX platform, the analog/mixed-signal and specialty foundry X-FAB is offering direct access to a standardized yet flexible set of SiC process technologies that accelerate the development of advanced power devices. From rapid prototyping to full production, the modular and fully scalable XbloX platform helps SiC device developers to expedite engineering assessments and technology release, with production starts that are claimed to be up to nine months faster than traditional methods. The standardized module configuration of the XbloX WBG discrete foundry model imparts two major benefits for those designing or refining advanced SiC devices.



Firstly, X-FAB takes on process development activities with the introduction of a Process Installation Kit (PIK), where design and implant recipes provide the key differentiators. Secondly, the use of XbloX takes care that wafer manufacturing at X-FAB becomes a highly scalable activity in line with application requirements, differing considerably from the less scalable production provided by a traditional foundry model for customer-specific SiC technologies. The planning phase, for example, is claimed to be up to six times shorter than that required by conventional approaches.

www.xfab.com

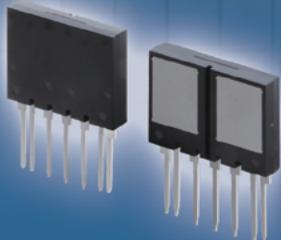
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SiC Power Modules

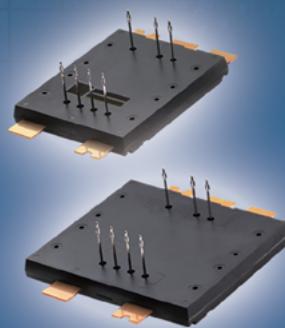
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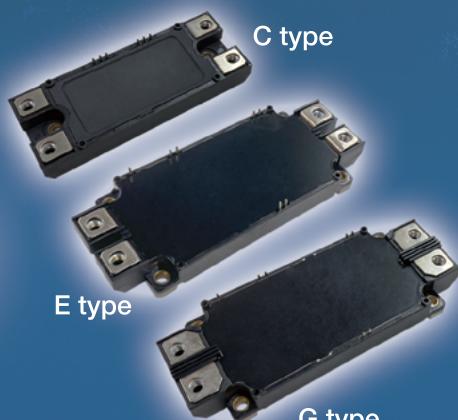
DOT-247



TRCDRIVE pack™



Case type



- Compact 4-in-1/6-in-1
- Circuit-oriented element layout (4-in-1, 2-in-1, etc.)
- Improved heat dissipation characteristics

- 2-in-1 TO-247-4L
- Improved heat dissipation performance
- Half-bridge/source common

- Parallel multi-chip configuration provides high current capability
- Low Ls improves switching performance
- Reduced size through improved heat dissipation performance

- Parallel multi-chip configuration provides high current capability
- Gel encapsulation in case



TRCDRIVE pack™ and EcoSiC™ are trademarks or registered trademarks of ROHM Co., Ltd.

Technology and Foundry Partnership for GaN

GlobalFoundries (GF) and Navitas Semiconductor announced a long-term strategic partnership to strengthen and accelerate U.S.-based gallium nitride technology, design and manufacturing.



Together, the companies will collaborate, develop and deliver solutions for critical applications in high power markets that demand the highest efficiency and power density, including AI datacenters, performance computing, energy and grid infrastructure and industrial electrification. Through this long-term partnership, GF and Navitas Semiconductor will manufacture next-generation GaN technology at GF's Burlington, Vermont (USA) facility, leveraging the site's expertise in high-voltage GaN-on-Silicon technology and Navitas Semiconductor's GaN technology and device expertise. Development is set for early 2026 with production expected to begin later in the year. By combining GF's manufacturing capabilities and Navitas' GaN capabilities, this strategic partnership is expected to "provide customers with the most advanced, secure and scalable GaN solutions".

www.gf.com

"Innovation Award" & "Young Engineer Award"

The Semikron Danfoss Innovation Award and the Semikron Danfoss Young Engineer Award are given for outstanding innovations in projects, prototypes, services or novel concepts in the field of power electronics in Europe, combined with notable societal benefits in form of supporting environmental protection and sustainability by improving energy efficiency and conservation of resources. Both prizes have been initiated by the SEMIKRON Foundation in 2012. The prizes are awarded in cooperation with the European ECPE Network. The deadline for submission ends on 17 January 2026! Please send your proposal resp. your application with the reference 'Semikron Danfoss Innovation Award' by email to Thomas Harder, General Manager of ECPE e.V., thomas.harder@ecpe.org.



The receipt of your proposal will be confirmed by email in due time.

www.ecpe.org



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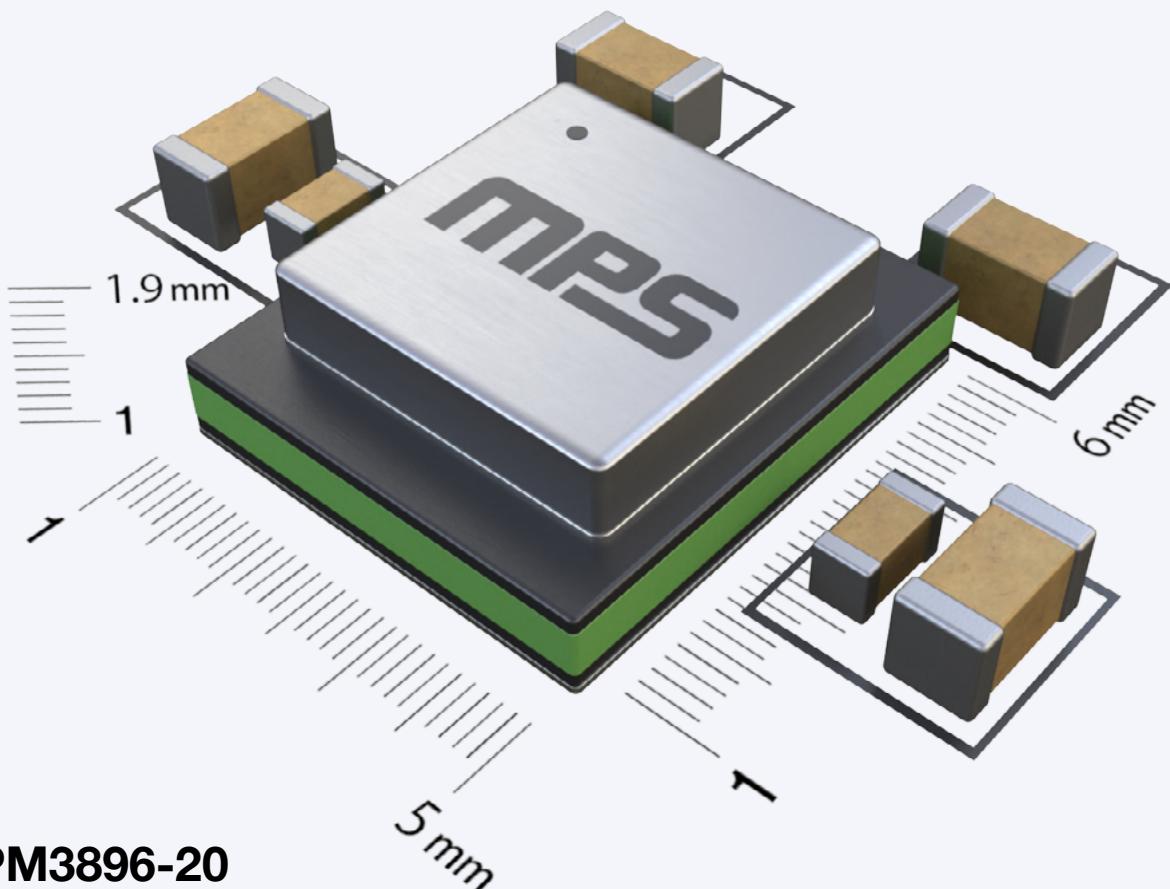
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Shorten your design cycle.



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5V, 20A, 5mm x 6mm x 1.9mm

Key Benefits:

- Small-Sized, Fully Integrated Solution
- Reduced Overall Solution Size
- High Efficiency for Various Applications
- Ease of Use: Simple & Flexible → Designer-Oriented
- EMI Class-B Certification and Fast Time-to-Market
- Anytime Support from MPS
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 - Voltages from <7V Up to >50V
 - Currents from <1A Up to >100A

Suitable Applications:

- Industrial & Test Equipment
- FPGAs
- Drones & Robotics
- Optical Communications
- Datacenters & AI

[Learn More](#)



mPS

Advanced SMPS Solutions for AI Server Power Supplies in Korea

Wise Integration, Powernet and KEC announced the signing of a strategic memorandum of understanding to co-develop next-generation switched-mode power supply solutions designed specifically for AI server applications in South Korea.



The partnership aligns with the country's push to expand AI infrastructure and build out the next generation of high-density data centers.

Under the agreement, Wise Integration will supply its GaN power devices, digital-control expertise and technical support. Powernet Technologies Corporation will lead development of new SMPS designs using Wise's WiseGan® and WiseWare® technologies. KEC Corporation will manage backend manufacturing, including module integration and system-in-package production tailored to the thermal and reliability demands of AI-server racks.

In addition to accelerating the design and development of competitive AI-server power supply solutions and creating business opportunities in Korea's AI server market, the project aims to shorten the solutions' time-to-market using WiseGan and WiseWare technologies. The collaboration builds on an earlier partnership between Wise Integration and Powernet, launched to serve OEMs that require compact, digitally controlled power-supply systems for faster, smaller and more energy-efficient electronic equipment.

www.wise-integration.com

Registration is now open for pre-APEC 2026 Workshops

PSMA has opened registration for both the PSMA Capacitor Workshop and the Power Magnetics @ High Frequency Workshop to be

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The multinational power electronics association

PSMA / Technical Forums / Magnetics / Workshop / Magnetics Forum

Magnetics Forum

Magnetics Info & Resources for the Power Electronics Industry.

held on Saturday, March 21 in San Antonio, TX prior to the start of APEC 2026. The PSMA Capacitor Workshop returns to APEC after a four year hiatus. The PSMA Capacitor Committee has put together an agenda and is looking to relaunch this workshop series. The PSMA Power Magnetics @ High Frequency Workshop returns for the 11th consecutive year and is looking forward to starting a second decade of delivering valuable information to the community. Both workshops will share a demo/exhibitor area that will also be home for the workshop lunches and networking hour. Space for both workshops is limited. Early bird registration for both workshops runs until January 30th, 2026.

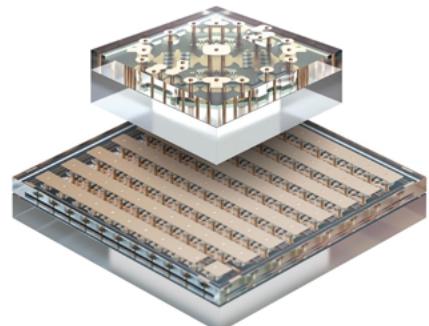
www.psma.com

One-Millionth Ideal Switch shipped

Menlo Microsystems has announced the shipment of its one-millionth Ideal Switch®. Unlike traditional switching technologies, the Ideal Switch delivers high performance without compromising between size, weight, efficiency, and reliability. This capability allows OEMs to design smaller, lighter, faster, and more energy-efficient systems that can be readily scaled, offering new solutions to tackling the limitations of switching technologies. The key

high-growth markets adopting Ideal Switch technology include Test & Measurement (Menlo already supports 14 of the top 20 semiconductor manufacturers), Aerospace & Defense and Power Switching. The adoption of the Ideal Switch across these markets reflects its growing role in addressing system-level bottlenecks caused by the limitations of traditional mechanical and semiconductor-based switches.

www.menlomicro.com



Silicon Valley Headquarters and Munich R&D Office opened



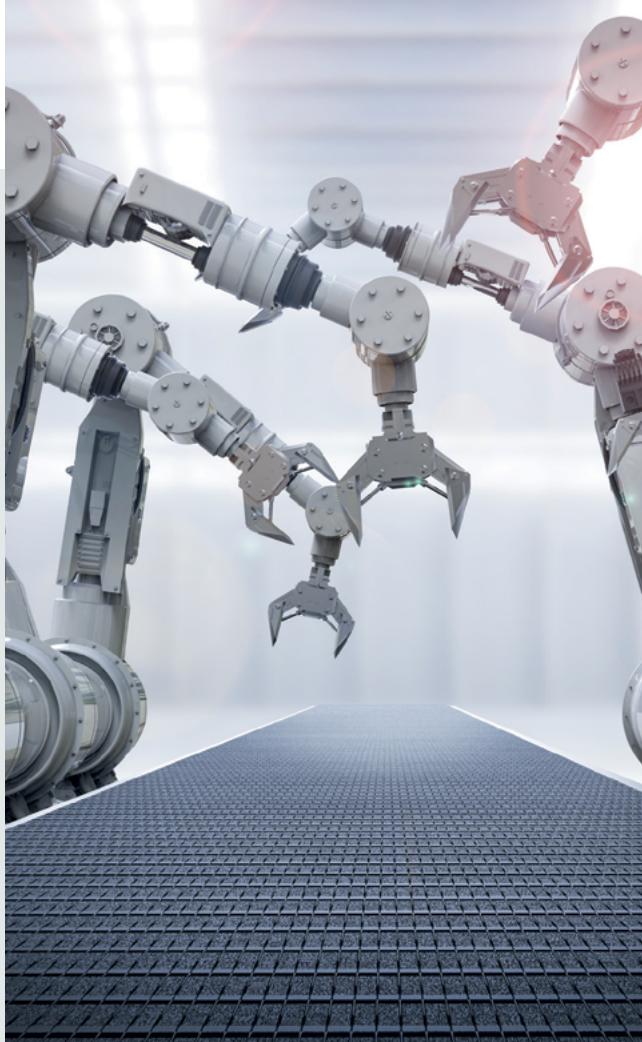
Empower Semiconductor announced an expansion of its global operations with the opening of its headquarters in Milpitas, California, and the establishment of a dedicated research and development (R&D) center in Munich, Germany. These strategic investments follow the company's series D financing round. The expanded Milpitas space is purpose-built to support rapid development of Empower's next-generation vertical power-delivery platforms and derivatives. The Munich site serves as a regional innovation hub.

www.empowersemi.com



The 7th Generation Modules

Dual XT, Premium Dual XT &
Dual XT RC-IGBT



MAIN FEATURES

- DualXT - Main Features
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- Premium Dual XT – Additional features
 - Advanced bond wire design
 - High thermal conductive ceramic substrate
 - Package material with CTI > 600
 - $V_{iso} = 4 \text{ kV}$
 - High power density
- Dual XT Reverse Conducting IGBT
 - RC-IGBT integrates IGBT and FWD functions into a single chip
 - This technology leads to further miniaturization
 - Increase of power density
 - Extended chip area leads to a chip temperature reduction by lower $R_{th(j-c)}$
 - Benefits in thermal behavior of the chip and module



Communications Manager appointed

As of January 1, 2026 Maurizio Di Paolo Emilio will become Director of Global Marketing Communications of EPC – Efficient Power Conversions. Maurizio holds a Ph.D in physics and is a content editor & technical writer, who has put specific focus on power electronics, wide bandgap semiconductors, renewable energy as well as space electronics. He decided to take this career step in order to be "at the forefront of the transition from silicon to the GaN era". He thinks that the rise of GaN is not just a simple technological upgrade but a fundamental change with profound impact on the world of AI (Artificial Intelligence) including scalability, sustainability, and ethics. Maurizio aims "to craft a communication strategy that blends technical storytelling with technological innovation, helping designers and product teams navigate complex technologies".

www.epc-co.com



Successful Premiere of the PCIM Asia New Delhi Conference

Under the theme "Agent of Change", the PCIM held its first conference in India this year. The Dr. Ambedkar International Conference and Exhibition Centre in New Delhi was the place to be on 9 – 10 December, with an impressive audience of industry experts taking in presentations by renowned companies in power electronics along with a targeted overview of future-oriented investment and expansion opportunities. The PCIM Asia New Delhi Conference presented itself as a force driving technological progress in the region,



aiming to create a forward-thinking platform that will foster strategic partnerships and promote collaboration among major players in industry, research, and politics.

With over 520 participants, more than 120 speakers, and over 75 presentations, the Indian edition of the PCIM Conference also featured professional exchange at the highest level. Current research results and technical innovations in the field of power electronics were explained in detail, providing valuable impetus for the industry's further development. In addition, illustrative poster presentations offered insights into pioneering projects and the results they have already achieved.

At the center of the event, however, was naturally the conference, with the accompanying expo featuring a total of 50 exhibitors showing off their latest products and applications. Companies such as Mitsubishi Electric, Infineon, and Rohm were on hand in New Delhi to experience the dynamic Indian market for power electronics first-hand.

The successful premiere of the PCIM Asia New Delhi Conference has now set the stage for further inspiring events focused on future-oriented technologies and strategic exchange, which are sure to continue driving the development of India's power electronics industry.

www.pcim.in

Joining Forces for Data Center Power Solutions

Delta and Siemens Smart Infrastructure have formalized a global partnership to deliver prefabricated, modular power solutions designed to accelerate the deployment of data center infrastructure,



while significantly reducing CAPEX. The partnership is expected to "ensure hyperscale and colocation operators enjoy a strategic advantage in the competitive AI and cloud computing data center market, with the highest performance in power management and reliability". The core of the agreement centers on the delivery of prefabricated, integrated containerized power solutions (SKIDs, eHouses). By prefabricating and pre-testing these modular power systems off-site with an optimized layout, the solution provides a standardized, plug-and-play approach that is said to reduce time-to-market by up to 50 %, to lower construction risk, and to maximize valuable data center square footage. The efficient design can provide up to 20 % CAPEX reduction and up to 27 % lower carbon emissions by using less concrete in the space-optimized layout.

www.deltaww.com

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- Max. 15 MHz sampling rate
- Up to 5 kV / 4 MHz

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Productronica 2025 Drives Positive Industry Trend

Internationality among exhibitors reached record level

By Roland R. Ackermann, correspondent Editor, Bodo's Power Systems

Productronica 2025, held from November 18 to 21 in Munich, impressively demonstrated its significance as the world's leading trade fair for electronics development and production, while celebrating its 50th anniversary. The event saw an increase in exhibitor and visitor numbers compared to the previous edition, with over 1,600 exhibitors from 52 countries presenting their innovations. The trade fair covered the entire value chain of electronics production, from technologies and components to software and services.

In total, more than 47,000 visitors from 98 countries came to Munich for Productronica 2025, covering 10 halls, which was more international than ever before. The share of exhibiting companies from abroad was around 58 percent (2023: 54 percent). In a ten-year comparison, the internationality of exhibitors even rose by more than ten percentage points (2015: 46 percent).



Key topics at Productronica 2025 included Advanced Packaging, Power Electronics, and Trustworthy Microelectronics, reflecting the industry's rapid development and the increasing global demand for electronic components. The co-location with SEMICON Europa – occupying three halls and also celebrating its 50th anniversary – created a vibrant environment for innovation and international collaboration.

Exhibitors and visitors expressed high satisfaction, with 98% of visitors rating the event as excellent to good and 95% stating that it met their expectations regarding innovations.

The sharp rise worldwide in demand for electronic components has thrust the topic of trusted microelectronics further into the industry spotlight. Productronica 2025 picked up on this trend and showed how new technologies, testing solutions, and manufacturing approaches are helping improve transparency and security along the entire value chain. The trade fair thus sent a clear signal for the future viability of the industry.

Messe München CEO Dr. Reinhard Pfeiffer underscores the event's significance: "Productronica 2025 has impressively demonstrated how important it is for global electronics manufacturing. Record internationality and the strong partnership with SEMICON Europa create a vibrant environment for innovation. The outstanding feedback from our exhibitors and visitors affirms its status as the industry's most important meeting place."

Exhibitor and visitor satisfaction at the highest level

In the overall rating, both exhibitors and visitors were once again very satisfied with Productronica. According to a survey carried out by the market research institute Gelszus, 98 percent of the visitors rated the event as excellent to good. In addition, 95 percent of the visitors surveyed said that Productronica had lived up to their expectations regarding innovations. The exhibition also received top

marks from exhibitors. For 91 percent of companies, the trade fair was excellent to good. 90 percent of the exhibitors praised the high quality of the visitors.

Frank Berthaux, Sales Director Germany Keysight stated: "Productronica brings together the people shaping the future of electronics. Keysight is proud to be here supporting our customers with the tools and insights they need to design, test, and deliver with confidence." Keysight was e.g. introducing new high-performance ATE power supplies ranging from 1.5 kW to 12 kW, including both unidirectional and bidirectional power supplies as well as regenerative electronic loads. By combining superior density with robust automation software, the portfolio enables developers to validate complex devices with multiple kilowatts of power with increased precision and repeatability while reducing space and energy requirements.

Advantest, global leader in semiconductor test systems, presented innovative test solutions for semiconductors: solutions for AI, high-performance computing, 6G, industry and automotive, including the new scalable MTe test platform for power semiconductors such as SiC and GaN. Other highlights included enhancements to the V93000 system for silicon photonics, AI tools and the SiConic solution for SoC validation.

Battery Manufacturing Equipment

Battery and energy storage production was a prominent area at Productronica 2025, highlighting the industry's crucial role in enabling electric mobility and sustainable energy systems. On show were innovations and solutions for the entire battery value chain, emphasizing the need for efficiency and scalability in manufacturing processes, especially with the rise of gigafactories. Productronica 2025 successfully served as a platform for experts to exchange ideas and collaborate on the future of battery manufacturing, particularly in the context of Europe's need for a resilient and sustainable supply chain.

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Improve Motor Lifetime & Efficiency with Slew Rate Control Gate Drive Optocoupler

Variable Speed Drives (VSD) uses Pulse Width Modulation (PWM) technique in modern electrical drives in industries where precise control of motor speed and efficiency are paramount. PWM technique controls the amount of power delivered to electrical devices by modulating the width of pulses in a square wave signal. While PWM offers precise control and efficient power management, its implementation can significantly affect the rate of change of voltage over time (dv/dt) in electrical drives. The primary mechanism through which PWM affects dv/dt is by introducing rapid voltage transition, leading to higher peak voltage level.

By Chun Keong Tee, Product Manager of Isolation Products Division, Broadcom

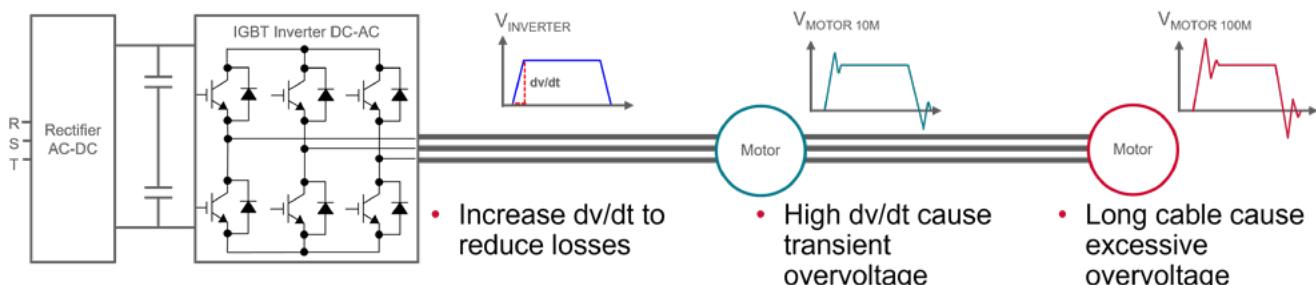


Figure 1: High dv/dt Causes Excessive Overvoltage

As the cable length increases, the impedance of the cable also increases due to its inductance and capacitance. The increase in impedance results in higher voltage spikes and dv/dt at the motor terminals. The elevated dv/dt level induced by long cable lengths can stress the insulation of motor windings and cause electromagnetic interference (EMI). High dv/dt causes partial discharge, insulation aging, and insulation failures, compromising the reliability and safety of the motor system. To mitigate these effects, various measures such as using shielded cables and passive filters are often implemented.

Effect of Cable Length on Motor Lifetime

The length of the cable between the VSD and the motor plays a significant role in the performance and reliability of the motor system. Figure 2 estimates the overvoltage spike with reference to the bus voltage with increasing cable length. Using 1200 V/600 A IGBT module as an example, the typical bus voltage is 600 V with allowable overvoltage not exceeding the absolute maximum ratings of 1200 V. The 600 A IGBT module switches around 100 ns. Based on this switching time and from Figure 2, the maximum allowable length is approximately 70 ft before the overvoltage exceeds 2 times the bus voltage at 1200 V.

Figure 3 shows an estimation of the motor wire insulation life with reference to cable length. Using the same example of 1200 V/600 A IGBT module with 100 ns switching time. The cable length can vary from 10 ft to 70 ft before the overvoltage exceeds 2 times the bus voltage. This translates to 60,000 hours or 6.8 years of motor wire insulation lifetime.

The long cable can affect the overvoltage spikes and reduce the lifetime of motor wire insulation. However, it is unavoidable to have long cable connection between the VSD and motor in a factory environment. Therefore, it is critical to mitigate these effects by controlling the PWM dv/dt to an acceptable level.

Standards for VSD Admissible Voltage and EMI

The IEC and NEMA standards provide guidelines for admissible voltages for various motor types in Figure 4. For US NEMA standards, if we used the fastest rise time of 200 ns, the permissible dv/dt ranges from 6 to 9 kV/ μ s. For international IEC standards widely adopted in Europe, the fastest rise time of 100 ns will derive a permissible dv/dt ranges from 10 to 20 kV/ μ s. Adding margin, The VSD will need to control the PWM dv/dt at a range of 4 to 15 kV/ μ s to prevent the overvoltage from exceeding the limits of the standards.

Electromagnetic interference (EMI) is also an increasing problem for VSD operates at higher frequency and IGBT switches faster. The higher dv/dt will generate more EMI signal errors to other nearby industrial equipment. CISPR 11 is the international product stan-

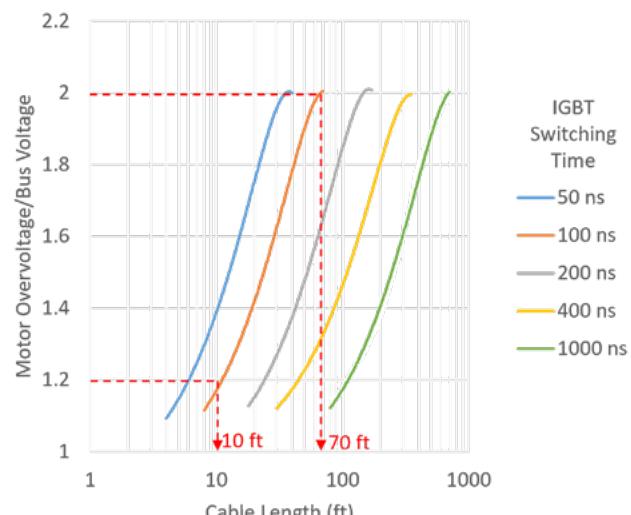


Figure 2: VSD to Motor Cable Length and Overvoltage [1]

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dard for EMI disturbances for industrial, scientific and medical, ISM equipment. VSD is classified under Class A, Group 1 of the CISPR 11 for industrial equipment. Figure 5 shows the conducted EMI emission limits for industrial motor drives. Therefore, it is also crucial to control the dv/dt to keep the EMI within the limits of the standard.

Limiting High dv/dt

A commonly used technique to mitigate dv/dt is installing a passive dv/dt filter between the VSD and the cable. The dv/dt filter consists of passive components inductor, capacitor and resistor. The drawbacks of passive filter are power loss, large filter size and costs.

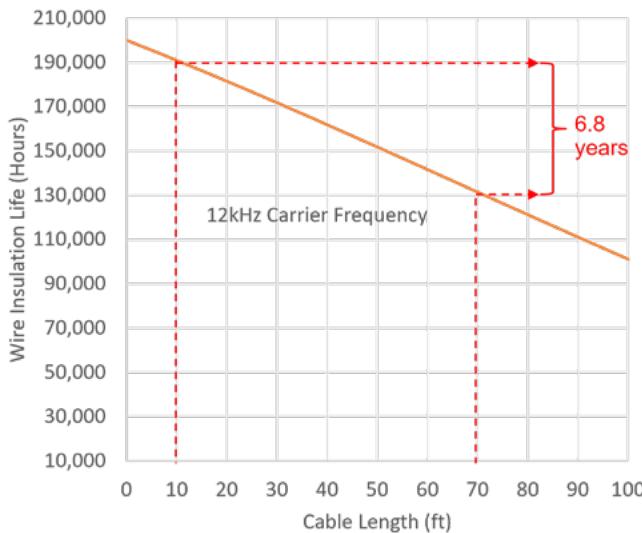


Figure 3: Motor Wire Insulation Life vs Cable Length [2]

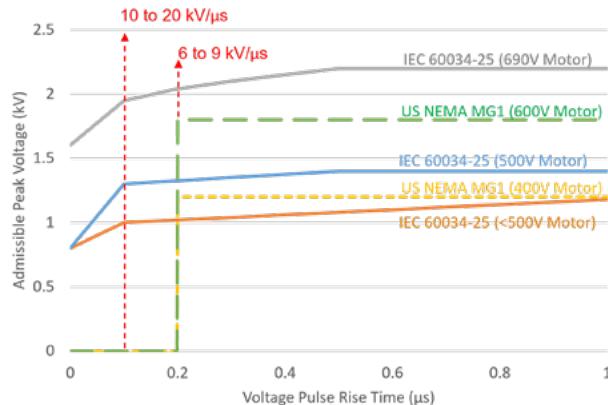


Figure 4: IEC & NEMA Standards of Admissible Withstand Overvoltage [3]

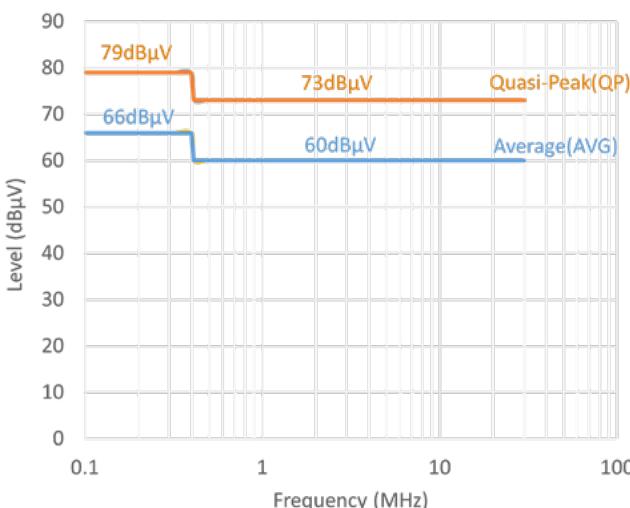


Figure 5: CISPR/EN 55011 Class A Conducted Emission Limits [4]

On the other hand, the slew rate control gate driver offers a simple, small and cost-effective alternative to dv/dt filter. Based on IGBT current feedback loop, the gate driver will control its current dynamically through the gate resistors. By varying the gate resistors, the dv/dt of the VSD can be controlled and not exceed the withstand voltage or EMI limits discussed earlier. This paper will discuss how the new Broadcom® gate drive optocoupler, ACFJ-3405 is used to control the dv/dt.

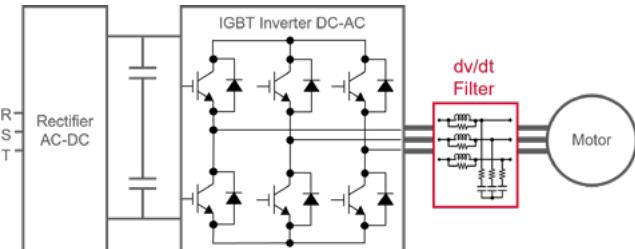


Figure 6: Passive dv/dt Filter Consists of Inductor, Capacitor and Resistor

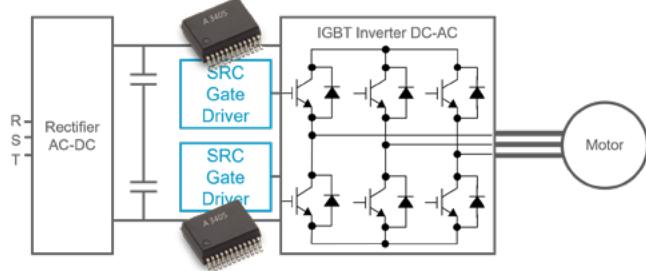


Figure 7: Slew Rate Control Gate Drive Optocoupler

Slew Rate Control Gate Drive Optocoupler

The ACFJ-3405[5] is a 12 A gate drive optocoupler with two selectable modes of output drive to optimize the slew rate of IGBT switching. It also features IGBT DESAT fault, IGBT gate fault, and system power supply fault monitoring, shutdown, and feedback to help meet VSD motor drive functional safety standards.

The ACFJ-3405 is packaged in a compact, surface-mountable 400 V CTI SO-24 package. This full-featured and easy-to-implement smart gate driver is certified to provide reinforced galvanic isolation meeting safety regulatory of the IEC/EN/DIN and UL/cUL.

Figure 8 shows typical application diagram of the slew rate control (SRC) gate driver. The SRC gate drive optocoupler receives the PWM and SRC signals from the microcontroller. The PWM signals are then transmitted across the isolation barrier of the gate driver. The SRC signal will then select the outputs, V_{OP1} or both V_{OP1} and V_{OP2} , in which the PWM signal will be sent to the gate of the IGBT. The microcontroller decides which mode of SRC levels based on the feedback of the IGBT or load current.

Figure 9 maps the IGBT current, I_C to the required gate current, to keep the dv/dt below the permissible dv/dt of 5 kV/us. At low IGBT current, for example 40 A, the gate driver will deliver a low output current, I_{OP1} to keep the IGBT slew rate at 2.5 kV/us. On the other hand, in a design without slew rate control, a high gate current might cause the dv/dt to exceed the permissible limits at 6 kV/us at 40 A.

When the IGBT is switching at a higher current, for example 120 A. The gate driver will deliver a higher gate current, $I_{OP1} + I_{OP2}$, to switch the IGBT at a higher slew rate but still within the permissible target. However, doing so, the dv/dt will be higher but optimized (see green dotted line), to reduce the switching losses.

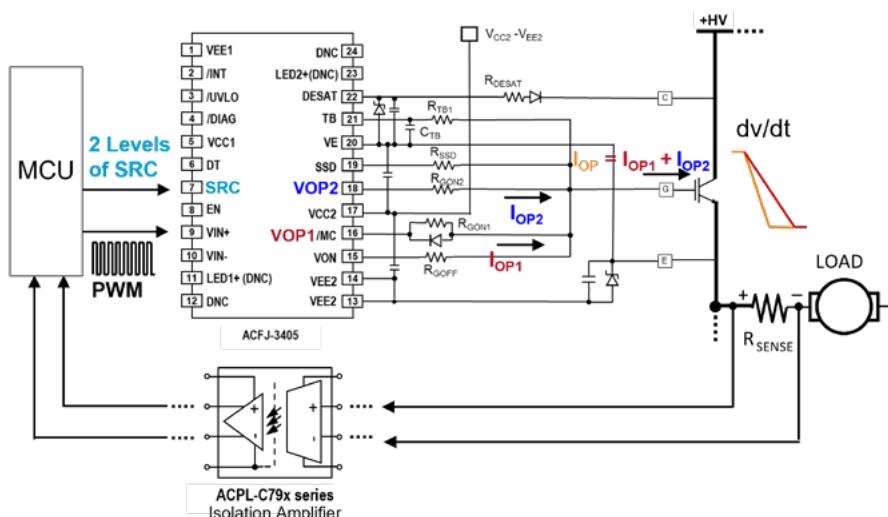


Figure 8: The Operation of Slew Rate Control Gate Driver

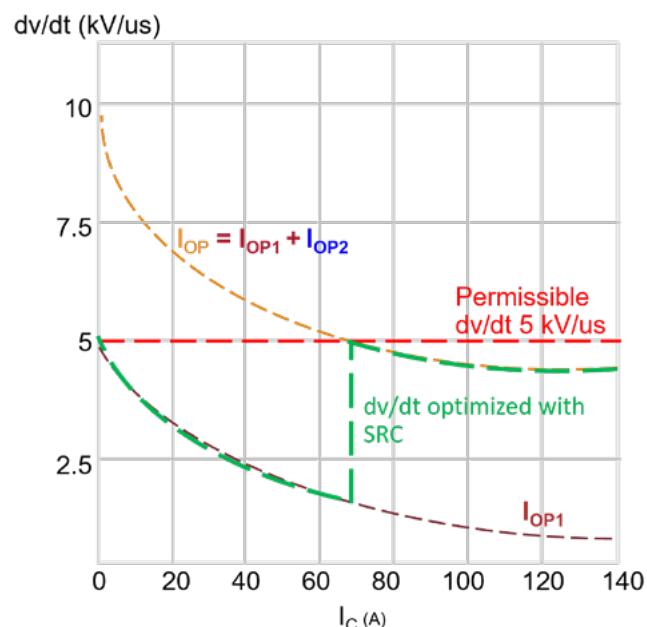
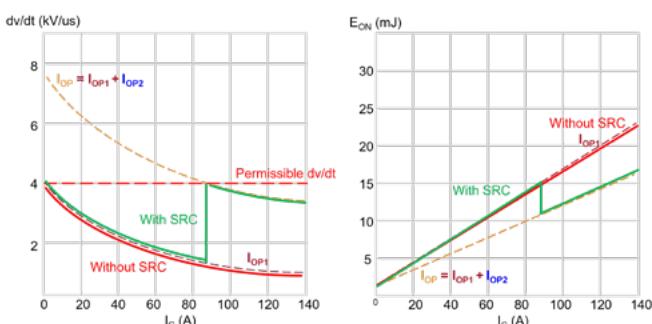
Figure 9: The Relationship of dv/dt, IGBT Current (I_C) and Gate Driver Current

Figure 10: The dv/dt & EON of the 60 kW VSD with and without SRC

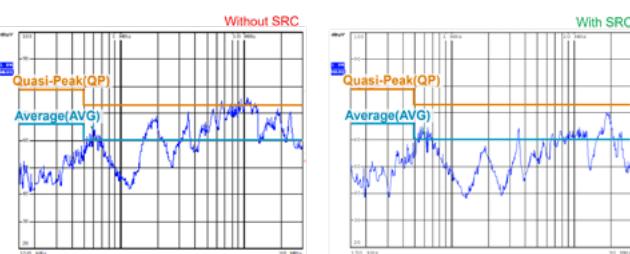


Figure 11: The EMI of the 60 kW VSD with and without SRC

Effectiveness of the SRC Gate Driver

The effectiveness of the SRC gate driver is verified on a 60 kW VSD, using 1200 V/200 A IGBT module with a cable length of 100 m. The permissible dv/dt is set at 4 kV/ μ s. The gate driver is set to switch from a lower gate current, I_{OP1} to a higher gate current $I_{OP1} + I_{OP2}$, when the IGBT current increases to 90 A. The results in Figure 10, denoted by the green line, show the dv/dt profile from 0 to 140 A with SRC. The red line denotes dv/dt profile without SRC.

Although the green and red dv/dt lines are within the permissible dv/dt , the one with SRC will have a lower switching loss as shown in the second plot of Figure 10. At 90 A, the SRC will switch the IGBT at a higher dv/dt and help to reduce the E_{ON} energy. Comparing the E_{ON} lines, the green E_{ON} line with SRC is 5 mJ lesser, which translates to lower overall power loss and higher efficiency.

Using the same 60 kW inverter with 100 m cable setup, the conducted emission is measured with, and without SRC, and according to CISPR 11 standard. The first plot in Figure 11 shows the EMI exceeding the standard of the conducted emission, quasi peak when the IGBT is switching at high dv/dt without SRC control. The second plot shows the optimized EMI without exceeding the quasi peak with SRC control.

Summary and Conclusion

This article explains the benefits of PWM technique and its side effects due to dv/dt . The long cable between the VSD and motor amplifier amplifies the dv/dt , causing EMI and overvoltage that reduce the motor lifetime. The article uses the standard for VSD admissible voltage to estimate the level of dv/dt that is permitted in different VSD operations. With the permissible dv/dt defined, the article compares how the SRC gate drive is more beneficial than the conventional solution of passive dv/dt filter. These benefits were demonstrated by using ACFJ-3405, an SRC driver in a 60 kW VSD with a cable length of 100 m. Measurement results show that the dv/dt was kept below a permissible of 4 kV/ μ s with lower switching loss and EMI better controlled to CISPR 11 standard.

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Improving Voltage Regulation in a Buck Converter with Isolated Output

One or more isolated outputs can be easily added to a buck converter, representing a cost-effective alternative to push-pull or flyback topologies for power levels below 15 W. However, the added isolated outputs are not directly regulated, and the final output voltage obtained is influenced by several component and operating parameters. Which are these parameters? And which design considerations are necessary to ensure the isolated output voltage(s) remain close to their target levels over the full load range? The answers are provided in this article.

By Eleazar Falco, Senior Application Engineer, Würth Elektronik

The buck converter is arguably the most ubiquitous switching power supply topology found in low power systems, providing an output voltage which is lower than the input voltage. Although in its standard form the input and output stages are not galvanically isolated, the topology lends itself well to the addition of one or more galvanically-isolated voltage rails, as required in applications like isolated communication interfaces and gate driver systems. Here, the buck solution represents a simple and cost-effective alternative to other topologies like flyback or push-pull converters, especially for low power levels below 15 W. However, unlike its primary non-isolated output, the added 'secondary' voltage rails are not directly regulated. Therefore, appropriate design measures are required to prevent them from deviating substantially from their target levels over the full range of operating conditions. Starting with an analysis of the topology and its operation, this article identifies the factors affecting the isolated/secondary output voltage and provides design guidance to minimize its variation, all supported by real measurements.

Adding isolated outputs to a buck converter

The power stage of a synchronous buck converter is shown in Figure 1, highlighted in grey. Considering 'ideal' components, the duty-cycle (D) of the PWM signal driving the control transistor (Q₁) sets the converter output voltage (V_{OP}), as follows:

$$V_{OP} = D \cdot V_{IN} \quad (E.1)$$

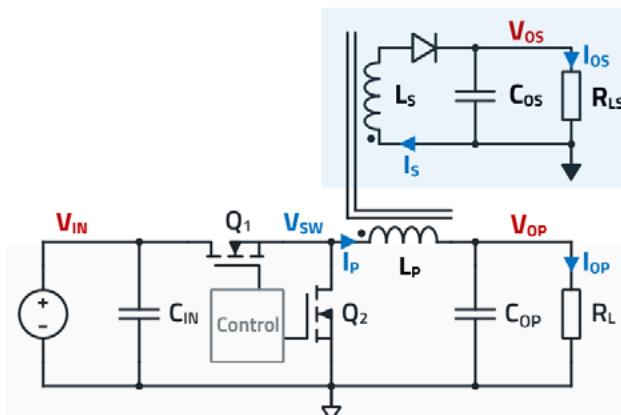


Figure 1: Schematic of a buck converter with additional isolated output.

Regarding the inductor (L₁), the voltage appearing across its terminals during the time Q₁ conducts (Δt_{ON}) corresponds to the difference between input and output voltages:

$$V_{L1_ON} = V_{IN} - V_{OP} \quad (E.2)$$

In most applications, the input voltage is not fixed, but varies within a set range, and so will the voltage across the inductor during the on-time. During Q₁ off-time (Δt_{OFF}), the voltage across the inductor changes polarity and equals the output voltage in absolute value (ignoring parasitic voltage drops):

$$V_{L1_OFF} = -V_{OP} \quad (E.3)$$

Unlike the input voltage, the output voltage is kept fixed in steady-state operation by a closed feedback control loop, and based on E.3, so is the inductor voltage during Δt_{OFF} . Thus, if an additional winding (L₂) is added, magnetically coupled to L₁ and with the same number of turns, then by transformer action, V_{OP} will also appear

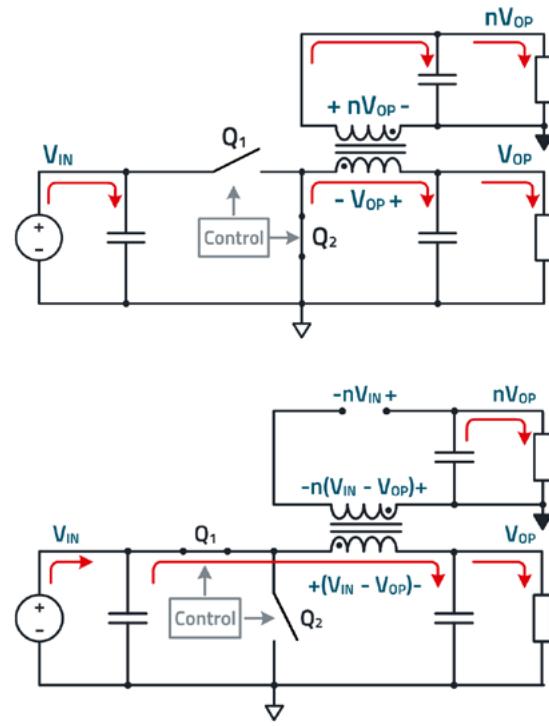


Figure 2: Equivalent circuit during Q₁ on-time (bottom) and Q₁ off-time (top)

across L_2 during the off-time. By adding a peak rectifier circuit (diode and capacitor) to the second winding (secondary) as highlighted in blue in Figure 1, the diode will be forward-biased only during Δt_{OFF} and V_{OS} will also appear across the secondary load (R_{LS}) (ignoring D_1 voltage drop).

During the on-time, D_1 will be reverse-biased and the winding current will be zero. The load will be supplied by C_{OS} in this time interval. As L_2 is now disconnected from the load, V_{OS} will not be affected by variations in the input voltage and will keep the same value as during the off-time as long as C_{OS} is correctly sized to supply the isolated load without causing excessive droop in the isolated output voltage. The equivalent circuits during the on- and off-times are shown at the top and bottom of Figure 2, respectively, illustrating this functionality.

The secondary/isolated output voltage is set as:

$$V_{OS} = n \cdot V_{OP} \quad (E.4)$$

Where 'n' is the turns ratio between secondary and primary windings:

$$n = \frac{N_{OS}}{N_{OP}} = \frac{\text{Turns secondary winding}}{\text{Turns primary winding}} \quad (E.5)$$

Note how V_{OS} can be set higher or lower than V_{OP} by simply adjusting the turns-ratio of the coupled windings.

Figure 3 shows measured waveforms of the primary winding current (I_p - violet), secondary winding current (I_s - gold) and switch-node (V_{SW} - blue) for the following specification: $V_{OP} = 5$ V, $D = 0.5$, $I_{OP} = 0.1$ A, $I_{OS} = 0.3$ A, $F_{SW} = 350$ kHz and using a 22 μ H coupled inductor with $n=1$. During Δt_{ON} , I_s is zero and the primary winding current rises with a mostly 1st order slope as in a standard buck converter. Net energy is stored in the magnetic core airgap and in C_{OP} , while on the secondary side, C_{OS} supplies R_{LS} .

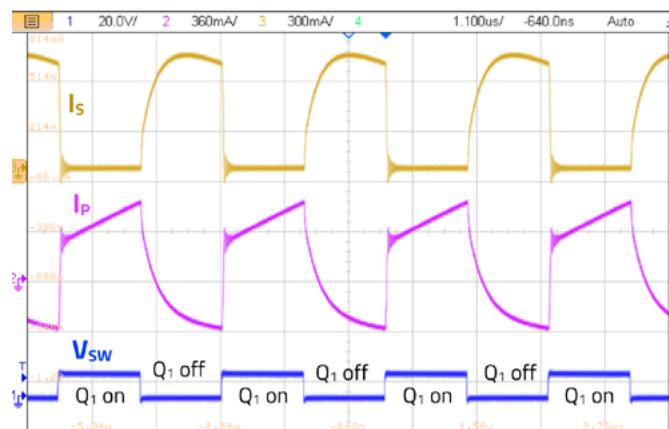


Figure 3: Measured waveforms of a buck converter with additional isolated output.

During Δt_{OFF} , D_1 conducts and energy (previously stored during the on-time) is transferred now from the primary to the secondary side. Part of it comes from the magnetic field of the coupled inductor, while the rest was stored in the electric field of the primary output capacitor (C_{OP}). As 'transformer action' takes place, there is current 'reflection' on the primary and secondary windings. The waveshape of the windings' currents during the off-time depends on converter operating conditions (especially the duration of the off-time window) as well as component parasitics, so it can differ from those of Figure 3 for a different specification and component selection from those considered in this example. An analysis on this goes beyond the scope of this article, but Ref[1] can be consulted for more details.

Analysis of isolated output voltage variation

Unlike V_{OP} , which is tightly regulated by the buck converter control system, V_{OS} is only 'indirectly' regulated. In the case of ideal components without parasitic elements, V_{OS} would be a perfectly scaled version of V_{OP} . But in reality, the voltage drops across components' parasitic elements, as well as operating conditions like primary and secondary load currents, will all determine the final output voltage appearing across the secondary load.

When analyzing V_{OS} regulation, the off-time interval, where energy is transferred from primary to secondary, must be considered. Figure 4 (top) shows the equivalent circuit during Δt_{OFF} with $n=1$ and the main components' parasitic elements. These are the on-resistance of the low-side MOSFET (R_{DS}), the primary winding resistance (R_p), the secondary winding resistance (R_s) and the transformer leakage inductance (L_k), referred to the secondary side. In addition, the non-linear forward voltage drop across the diode (V_f) is also included, as it has a big influence on V_{OS} .

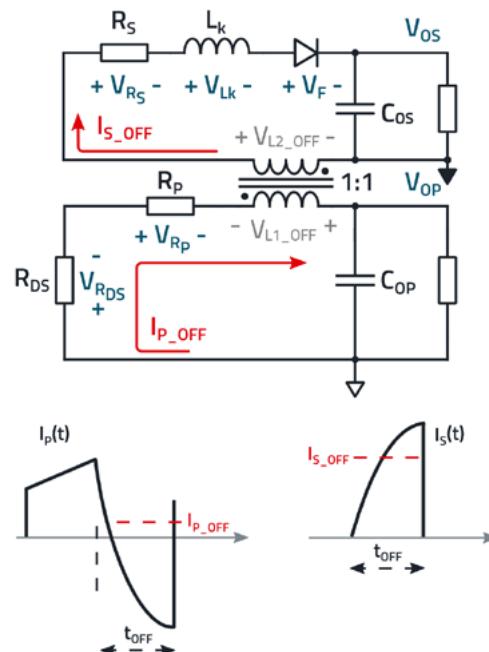


Figure 4: Equivalent circuit and current waveforms during off-time.

The average voltage drops during Δt_{OFF} across these elements will determine the resulting voltage on the isolated output, as follows:

$$V_{OS} = V_{OP} + V_{R_{DS}} + V_{R_p} - V_f - V_{Lk_off} - V_{R_s} \quad (E.6)$$

For the calculation, the average current levels during the off-time on the primary (I_{p_OFF}) and secondary (I_{s_OFF}) windings are considered (Figure 4 (bottom)), calculated as:

$$I_{p_OFF} = I_{OP} - \frac{D}{(1 - D)} \cdot n \cdot I_{OS} \quad (E.7)$$

$$I_{s_OFF} = \frac{I_{OS}}{(1 - D)} \quad (E.8)$$

The individual voltage drops across the parasitic resistive elements are then:

$$V_{R_{DS}} = I_{p_OFF} \cdot R_{DS} \quad (E.9)$$

$$V_{R_p} = I_{p_OFF} \cdot R_p \quad (E.10)$$

$$V_{R_s} = I_{s_OFF} \cdot R_s \quad (E.11)$$

Note from E.8 how I_{S_OFF} is always positive, so the voltage drops on the secondary side will always cause a reduction of V_{OS} from the reflected voltage across the secondary winding during the off-time (V_{L2_OFF}). In contrast to this, for a set duty-cycle, I_{P_OFF} may be positive or negative depending on how the primary and secondary load currents compare (E.7). If I_{P_OFF} is positive, the resistive voltage drops on the primary side will make the voltage across the primary winding (V_{L1_OFF}) (which is reflected to the secondary winding scaled by 'n') to be higher than V_{OP} . This may help to offset the effect of the voltage drops on the secondary side, reducing V_{OS} deviation from its target level.

Regarding the output diode, its average forward voltage during the off-time can be directly obtained from the I-V curve given in its datasheet, as follows:

$$V_f = V_D (@ I_{S_OFF}) \quad (E.12)$$

Of all the parasitic voltage drops happening during Δt_{OFF} , the most complex to calculate accurately is the one related to the leakage inductance. However, an approximation can be made and an expression obtained which helps to gain a qualitative understanding into its dependence upon other parameters.

The instantaneous voltage across the leakage inductance is:

$$V_{Lk}(t) = L_k \cdot \frac{dI_{S_OFF}(t)}{dt} \quad (E.13)$$

Its average voltage drop during the off-time is approximated as follows:

$$V_{Lk_OFF} \approx L_k \cdot \frac{\Delta I_{OFF}}{\Delta t_{OFF}} \quad (E.14)$$

In E.14, ΔI_{OFF} is the difference of the secondary winding current between start and end of the off-time window.

Considering a secondary winding current waveform increasing with a mostly 1st order slope during the off-time (valid for cases with very short Δt_{OFF} , high L_k and/or high I_{OS}), the following approximation can be made:

$$V_{Lk_OFF} \approx L_k \cdot \frac{2 \cdot I_{OS} \cdot F_{SW}}{(1 - D)^2} \quad (E.15)$$

The result in E.15 shows that the net voltage drop across the leakage inductance during the off-time increases with the isolated load current, the duty cycle, the switching frequency and the leakage inductance value itself. Observe how this is the only voltage drop affected by the switching frequency.

Design guidelines

Based on this analysis, the following design guidelines should be considered to minimize deviations of the isolated output voltage from its target level:

- Low switching frequency
- Low duty-cycle
- Low conduction resistance of Q_1
- Low winding resistances of coupled inductor
- Low leakage inductance (i.e. high coupling factor) of coupled inductor
- Low forward voltage of output diode (i.e. Schottky type)

From the above considerations, a low switching frequency and proper diode and coupled inductor selection are the ones that the designer can control more easily. If the non-isolated output is not used and the input voltage range is not very wide, then the duty-cycle can also be freely set to a low value. In contrast, the options for R_{DS} are more limited, as in this topology with such low output power levels, a small range of converter ICs with integrated transistors are typically used to keep the solution size and cost low.

Experimental Results

To confirm the above design guidelines, measurements on a real converter prototype are performed.

In Figure 5, experimental results show the negative effect of a higher switching frequency on the isolated output voltage for the following specification: $V_{OP} = 5$ V, $I_{OP} = 0.4$ A, $D = 0.5$ and $L = 22 \mu\text{H}$ (DPC-HV 7448841220). Here, measurements for switching frequencies of 200 kHz and 800 kHz are compared and as expected, V_{OS} remains closer to the target level when operating at a lower switching frequency, as the voltage drop across the leakage inductance is lower.

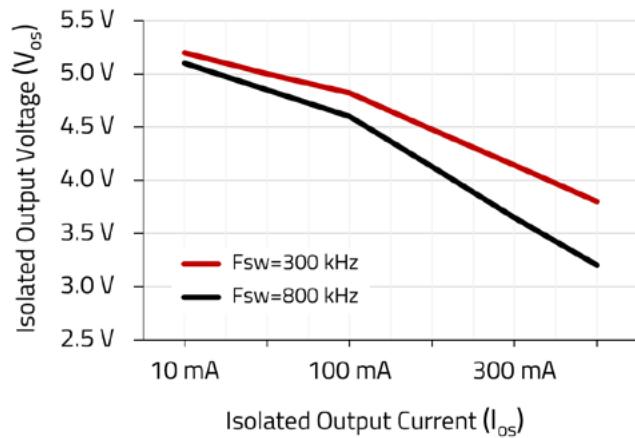


Figure 5: V_{OS} vs. I_{OS} at switching frequency (F_{SW}).

In Figure 6, the measured variation of V_{OS} with isolated load current at low and high duty-cycles of 20% and 80% is shown for the basic specification with $V_{OP} = 5$ V, $I_{OP} = 0.4$ A, $F_{SW} = 300$ kHz and $L = 22 \mu\text{H}$ (TDC-HV 76889440220). As anticipated, a lower duty-cycle results in a lower deviation of the isolated output voltage.

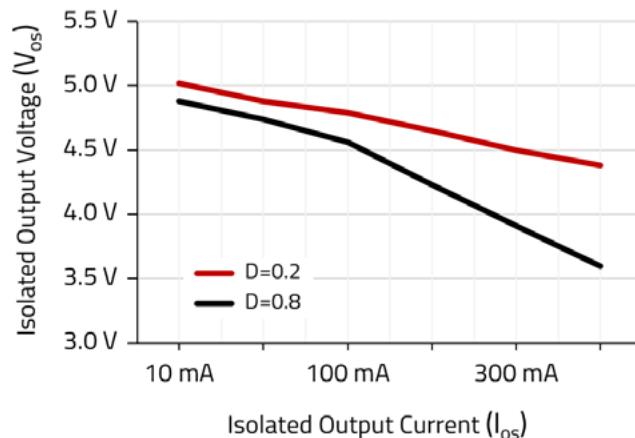


Figure 6: V_{OS} vs. I_{OS} at duty-cycle (D).

Regarding the influence of circuit components, the forward voltage of the output diode does not vary much with load current, as opposed to the voltage drop caused by the leakage inductance of the coupled inductor. The WE-MCRI 1090 coupled inductor series from Würth Elektronik feature variants with high and low leakage inductances, targeting different applications. For each magnetizing inductance offered, all parameters other than the leakage inductance are kept equal in both variants, allowing for a direct comparison of the impact of the coupling factor in the circuit. Considering the following specification: $V_{OP} = 5$ V, $I_{OP} = 0.1$ A, $D = 0.42$, $F_{SW} = 300$ kHz, results using WE-MCRI with $L = 22 \mu\text{H}$ and coupling factor variants of 0.98 and 0.76, equivalent to leakage inductances of 0.45 μH and 5.6 μH , are compared in Figure 7. Observe how the 'high-leakage' coupled inductor is unusable in this topology: with only 150 mA of load current, the output voltage has already dropped more than 2.5 V, compared to only 0.2 V for the 'low-leakage' part.

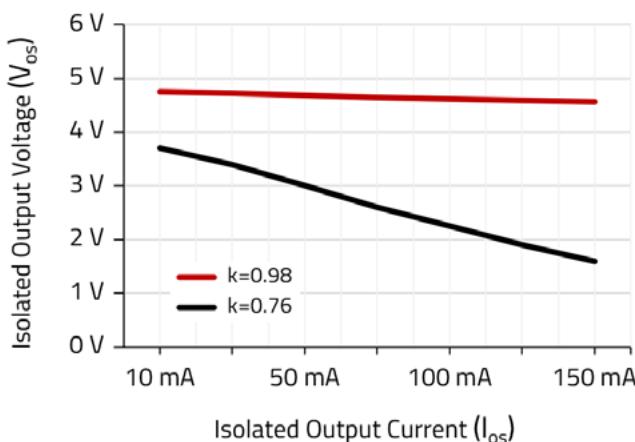


Figure 7: V_{os} vs. I_{os} at coupling factor (k).

While a high leakage inductance can be of advantage in some converters, like the SEPIC (Ref[2]), in the case of the buck with isolated output, a low leakage inductance is essential for correct operation.

Conclusion

Understanding the elements affecting the secondary output voltage(s) and designing accordingly to minimize their influence is key when designing a buck converter with isolated output(s). Parameters like the switching frequency and duty-cycle as well as the optimal selection of the output diode and coupled inductor all play a key role in this, as it has been shown in this article. As a further read, Würth Elektronik's ANP017 application note (Ref[1]) provides a detailed analysis of the topology, a step-by-step design example as well as alternative solutions to improve the regulation of the isolated output voltage, helping to gain a deeper insight into the operation and important design considerations of this topology.

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- [1] Application Note ANP017 – Designing buck converters with isolated outputs, Würth Elektronik: <http://www.we-online.com/ANP017>
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About the Author

Eleazar Falco holds a BSEE equivalent from the University of Elche (Spain). After graduation, he worked in the electronics hardware development of various home appliances and electronic products in the United Kingdom, focusing on analog circuits, power supply design and motor control. Since 2018, Eleazar is an Application Engineer at Würth Elektronik in Germany, where he supports different product areas with a focus on power electronics applications.

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Enabling flexible, high efficiency designs

A new family of Gate Driver ICs for Automotive Traction Inverters

The growing adoption of e-mobility is driving significant demand for power electronics, particularly inverters. Since these systems depend on high-performance power modules to achieve their efficiency targets, manufacturers are intensifying their efforts to enhance this crucial component.

By Lan Fang (Corresponding author), Christopher Wille, Thoralf Rosahl, Andreas Menzel,
all Robert Bosch GmbH

To improve overall performance, many are replacing traditional Si-IGBTs with SiC-MOSFETs and adopting more advanced packaging technologies and innovative design processes.

However, this represents only one of the numerous optimization strategies. A different path focuses on the control of switching behavior. By upgrading to advanced gate driver ICs, manufacturers can influence and optimize the switching performance, losses, and robustness without the need for a complete redesign of the set-up and architecture. This minimally invasive alternative raises a key question: How do different gate-driving topologies influence system efficiency, and what improvements can be achieved simply by changing the way power devices are driven?

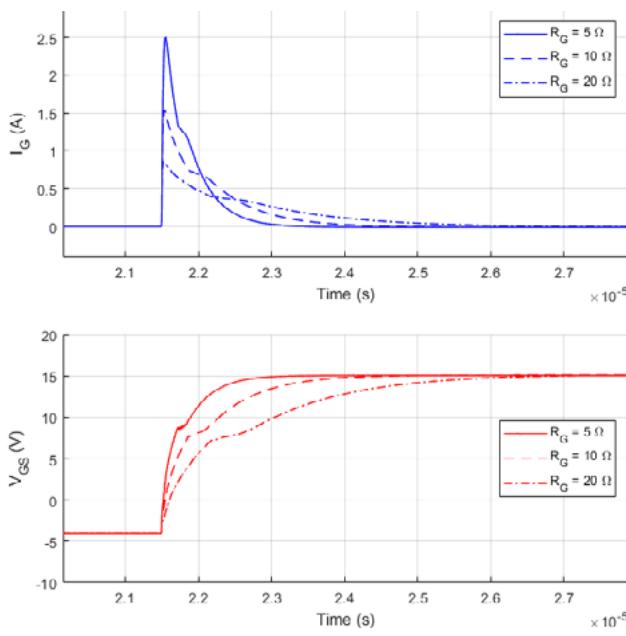
Beyond VSGD: exploring current-source and gate-shaping approaches

Most designs today rely on voltage-source gate driver (VSGD) ICs, which regulate the turn-on and turn-off of power devices by applying high and low gate-source voltages. To better understand how alternative driving concepts influence overall system performance, Bosch initiated a research into different gate-driver topologies, focusing on current-source gate drivers (CSGDs) and adaptive gate-shaping gate drivers (GSGDs).

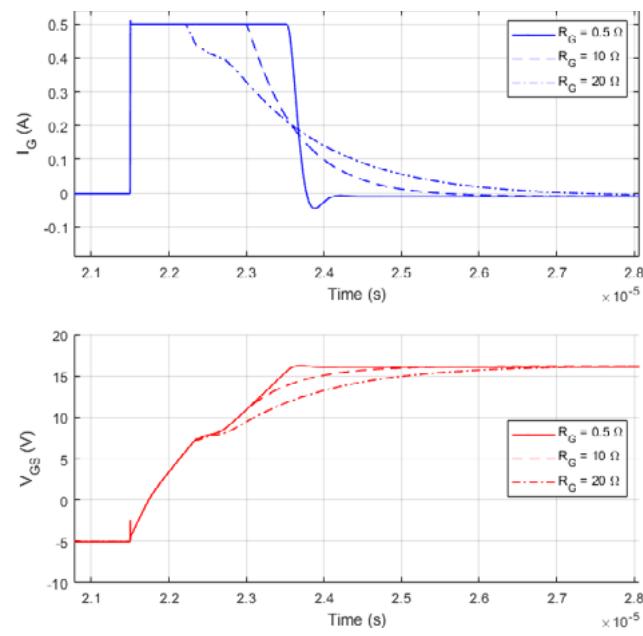
CSGDs drive the power transistor with a controlled gate current (I_G), enabling precise management of the gate charge (Q_G) and fine-tuning of dv/dt and di/dt . The imposed I_G still causes a voltage drop across the gate resistance ($R_{G,int}$) inside the power transistor or power module. However, there is no $R_{G,ext}$ between the driver output and the power transistor anymore, which typically defines the switching behavior in VSGD implementations.

Figures 1(a) and 1(b) illustrate typical V_{GS} and I_G waveforms for VSGD and CSGD under different external R_G values. Notably, the gate current remains constant in CSGD operation. In a VSGD, the peak I_G scales approximately with $1/R_G$, and the Miller plateau makes dv/dt highly dependent on R_G , forcing a tradeoff between switching losses and electromagnetic interference (EMI). In addition to these effects, another critical parameter is the voltage overshoot generated during switching, caused by parasitic inductances in the circuit layout.

In contrast, a CSGD regulates I_G directly, producing an almost R_G -independent V_{GS} ramp and predictable dv/dt through the Miller plateau. This reduces overshoot, ringing, and switching losses. In practice, a small R_G is retained for damping and segmented gate-current profiles can be programmed to balance switching speed and EMC requirements, improving repeatability, efficiency, and overall system reliability.



a) Voltage source gate driver



b) Current source gate driver

Figure 1: Typical gate voltage and current waveforms of voltage source gate driver (a.) and current source gate driver (b.) with different gate resistances



Vincotech

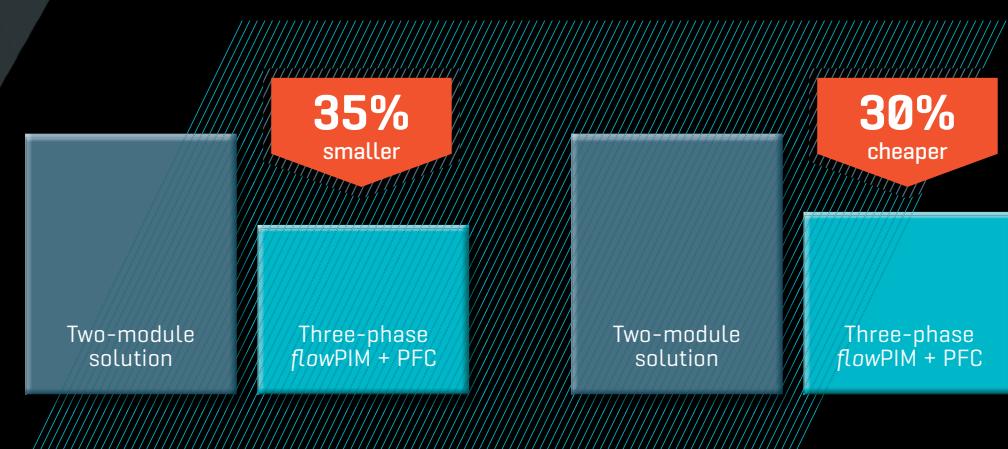
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EMPOWERING YOUR IDEAS

Unlike conventional VSGDs or CSGDs, the GSGD considered here can continuously vary the gate current (I_G) throughout the switching transition. This technique is specifically known as gate-current shaping (G_S). The resulting gate-current profile is a time-ordered sequence of I_G setpoints, where each segment is defined by a programmed current amplitude and its corresponding time interval. The Bosch gate driver makes it possible to select the optimum waveform for the system.

Figures 2(a) and 2(b) illustrate the power device's switching waveforms under a GSGD that continuously shapes I_G during turn-on and turn-off, respectively. During a turn-on event, staged current segments ($I_{G_{on1}}-I_{G_{on4}}$) pre-charge the gate, control di/dt and dv/dt through the Miller plateau, and balance a fast V_{DS} falling slope against reduced reverse-recovery and switching losses. During a turn-off event, a pre-discharge followed by controlled discharge segments ($I_{G_{off1}}-I_{G_{off4}}$) shapes dv/dt and di/dt across the Miller plateau to minimize V_{DS} overshoot and EMI while shortening the transition.

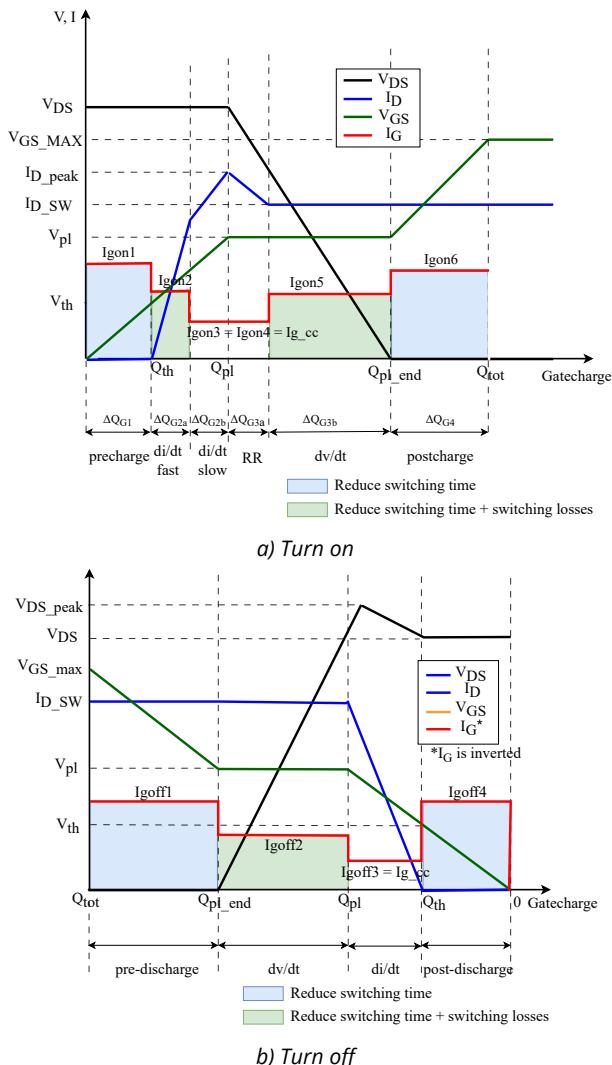


Figure 2: Current control gate driver turn-on (a.) and turn-off (b.) modelling with gate shaping

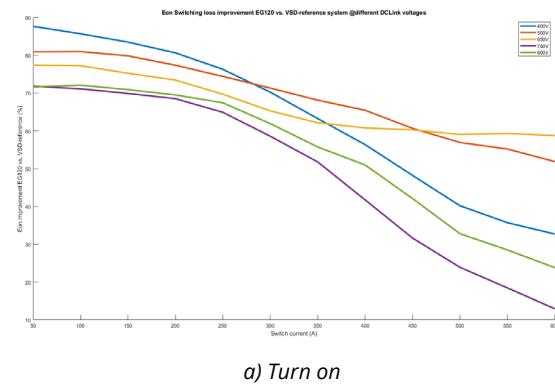
Advancing switching performance with the EG120's programmable gate-current profiles

Bosch's EG120, a CSGD IC featuring programmable gate-current shaping, served as the GSGD in this study and underpins the reported double-pulse and inverter-level comparisons. Different I_G profiles are applied in the turn-on and turn-off phases. The device supports up to six segments for turn-on and five for turn-off, with up to 133 profiles that can be stored in the on-chip memory and

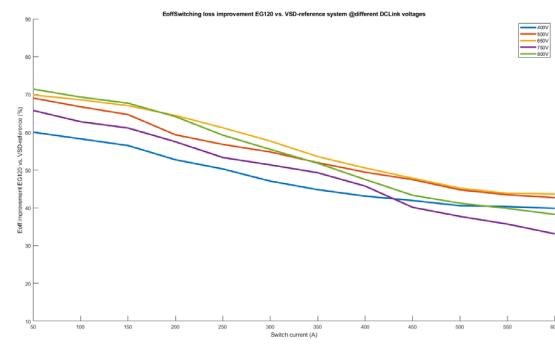
selected in real time based on changing operating conditions such as DC-link voltage (V_{DC}), switching current (I_{SW}), and temperature (T), allowing the driver to optimize overshoot, EMI, and switching losses.

To evaluate the impact of the gate driver topology on overall system performance, a benchmarking experiment was conducted using two identical architectures. One system incorporated VSGD ICs, while the other utilized the GSGD EG120 ICs. All other conditions, including the power modules, the DC-link capacitor and the cooling system, were strictly kept the same to ensure that the driver-chip type was the sole independent variable for accurate performance assessment.

Compared to a VSGD baseline, the turn-on event shows up to a 90% reduction in turn-on energy at bus voltages from 400 V to 800 V. During the turn-off event, the EG120 likewise achieves coordinated loss reduction: optimized I_G shaping combined with an active Miller clamp suppresses overshoot and ringing, thereby lowering thermal stress and enhancing device reliability. The results for switching efficiency improvements and I_G profiles across different V_{DC} levels during turn-on and turn-off events are presented in Figure 3.



a) Turn on



b) Turn off

Figure 3: EG120 double pulse test – turn-on efficiency curve (a.) and turn-off efficiency curve (b.)

System-level testing on motor bench

Across the full operating load, V_{DS} overshoot was limited to a maximum of $V_{DC_link} + 300$ V. The power module used in the double-pulse tests is rated 1200 V. Based on these results, the selected I_G shaping profile was deployed and evaluated on a motor test bench to assess its impact on switching losses and drive efficiency.

The motor test bench was configured with a 650 V DC bus supply and a 380 V AC-rated motor, operating at a 10 kHz carrier frequency and an ambient temperature of 25 °C. At a rated torque of 230 Nm and a speed of 6855 rpm, the system delivered 165 kW of mechanical output power. Figure 4 illustrates the inverter efficiency map comparing VSGD and EG120 gate drivers. The X-axis represents motor speed (0-10,000 rpm), while the Y-axis represents motor torque (0-400 Nm). Efficiency isolines highlight performance differences across the operation range.

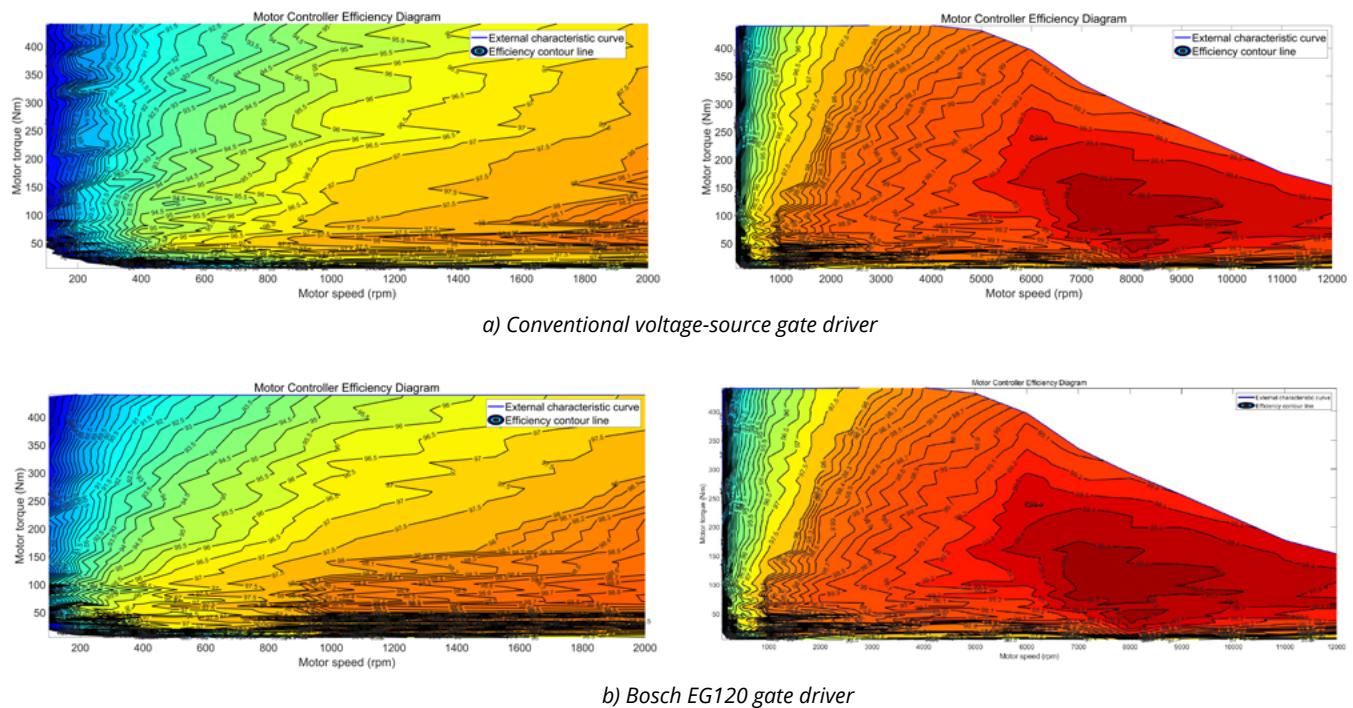


Figure 4: Torque-speed characteristics comparing conventional voltage-source gate driver (a.) with a Bosch EG120 (b.) at different operating conditions.

Under identical test conditions, the EG120-based inverter achieved a peak conversion efficiency of 99.6% and maintained $\geq 99.4\%$ at the rated operation conditions (230 Nm, 6,855 rpm, 165 kW). At partial loads of 25% (57.5 Nm), 50% (115 Nm) and 75% (172.5 Nm), the measured efficiencies were 99.49%, 99.57%, and 99.49%, indicating stable high efficiency across the operating range. The VSGD baseline measured 99.43%, 99.40%, and 99.34% at the corresponding load points, i.e., gains of approximately 0.06-0.17 percentage points with EG120.

Efficiency analysis shows that using a gate-shaping SiC-MOSFET driver shifts the whole efficiency map upwards to higher efficiency values, the high-efficiency "red zone" expands, and new efficiency peaks emerge. For urban speeds of 20-30 km/h, the motor typically operates at 1300-2400 rpm, where efficiency improvements range from 0.2 to 0.6 percentage points.

Compared to the VSGD baseline, the EG120 sustains high efficiency across a broader operating envelope, with more uniform distribution and fewer low-efficiency regions. The 3D plot (Figure 5) confirms lower system losses, and a reduced peak-to-valley spread.

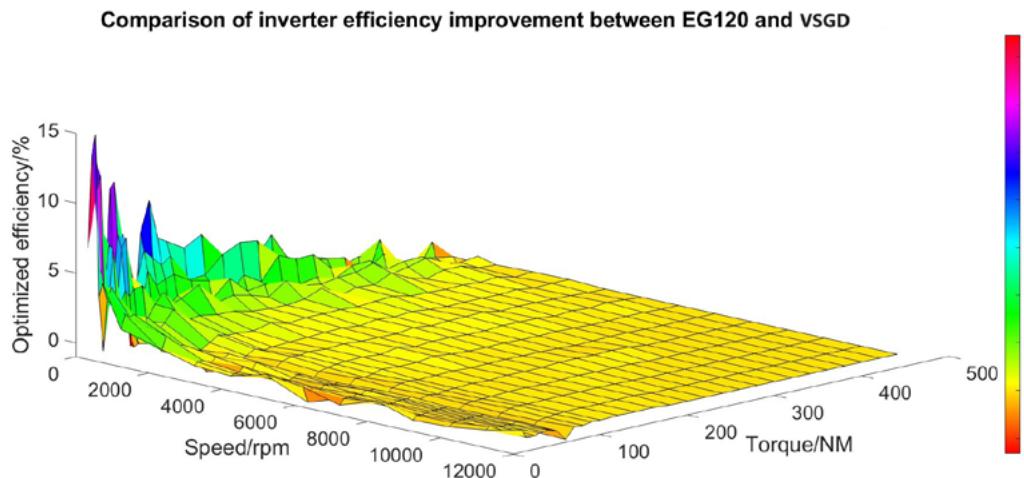


Figure 5: 3D efficiency and loss map for EG120 vs. baseline

Conclusion

The results show that meaningful efficiency gains in e-mobility inverters do not require a redesign of the power stage. By upgrading only the gate driver, Bosch's EG120 delivers lower switching losses, reduced overshoot, and a consistently higher efficiency map across the full operating range. These improvements translate directly from double-pulse measurements to real motor bench performance, with gains of up to 0.6 percentage points in typical driving conditions.

In a nutshell, programmable gate-current shaping offers a practical, minimally invasive way to enhance inverter efficiency while keeping existing hardware architectures mostly unchanged. Future work will focus on extending these results through adaptive, AI-driven optimization strategies that dynamically adjust gate-current profiles across an even wider range of operating conditions.

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Solving DC/DC Power Challenges in Military Avionics Through Modularity (Part 3)

Following our exploration of military standards and practical transient suppression, we now turn to a common challenge in switch-mode power supply (SMPS) design: containing conducted noise. In this article we will explore conducted noise paths and filtering techniques. Traditionally, managing bus interruptions has relied on large bulk capacitors to maintain energy on the primary side. In this third part of the series, we examine how GAIA-converter's approach—embedding a boost converter within a board-mounted module—reduces the required capacitor value for a given hold-up time.

By Christian Jonglas, Technical Support Manager, GAIA Converter

DC/DC converters, as switch-mode power supplies, generate conducted noise on their input and output leads. This noise appears as an alternating current waveform superimposed on the DC current, comprising multiple frequency harmonics. These harmonics originate from switching components (e.g., MOSFETs and rectifying diodes) that, when combined with parasitic capacitance or inductance, form high-frequency resonant circuits during transient operation. Two distinct propagation modes exist, each requiring specific mitigation techniques for DM noise and CM noise:

Differential Mode (DM) Noise: Current flows between the positive lead and its return path (negative lead). This noise is relatively straightforward to suppress, typically requiring only a basic LC filter with ~40 dB/decade attenuation to meet compliance limits.

Common Mode (CM) Noise is more challenging to eliminate, CM noise flows simultaneously through both positive and negative leads, returning via earth ground. It propagates through parasitic capacitances (e.g., across isolation barriers or chassis connections), inducing AC voltages along its path. CM noise arises from high dV/dt switching transitions and typically occupies higher frequencies.

For DO-160 and MIL-STD-461, limits are specified in $\text{dB}\mu\text{A}$, where:

$$I_{(\mu\text{A})} = 10^{(I_{(\text{dB}\mu\text{A})}/20)}$$

Figure 1: To convert a current in $\text{dB}\mu\text{A}$ to its value in μA the reverse logarithmic needs to be used.

$$0 \text{ dB}\mu\text{A} \equiv 34 \text{ dB}\mu\text{V} \text{ thus:}$$

$$\text{dB}\mu\text{V} = \text{dB}\mu\text{A} + 34 \text{ dB}\mu\text{V}$$

Figure 2: By adding 34 to a value in $\text{dB}\mu\text{A}$ we convert it in $\text{dB}\mu\text{V}$ in a 50Ω system

Or with the Equivalent limits in $\text{dB}\mu\text{V}$ (for 50Ω systems):

Measurements use a Line Impedance Stabilization Network (LISN) inserted between the D.U.T (device under test) input and lab power supply. The LISN isolates the test circuit from lab power supply interference and provides a standardized 50Ω test port for spectrum analyzer connection.

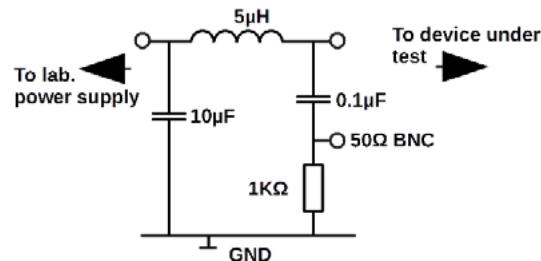


Figure 3: The LISN defined into the DO-160 standard allows to isolate the lab power supply and offers a normalized source impedance for testing.

Designing filters with discrete components or using COTS

The first method to reduce common-mode noise in isolated DC/DC converters consists of placing capacitors across the isolation barrier. If the capacitors placed between the input and output pins have a value significantly higher than the few picofarads of the isolation barrier itself, they will drastically reduce the impedance of the barrier for high-frequency noise currents, thereby lowering the developed voltage.

If a chassis ground is available, it can be even more efficient to place four capacitors between the hot points and the chassis, as shown in Figure 4. To reach the lowest impedance, the best choice is to connect the common-mode capacitors as close as possible to the converter pins and the ground plane, minimizing any access inductance that could create uncontrolled resonances.

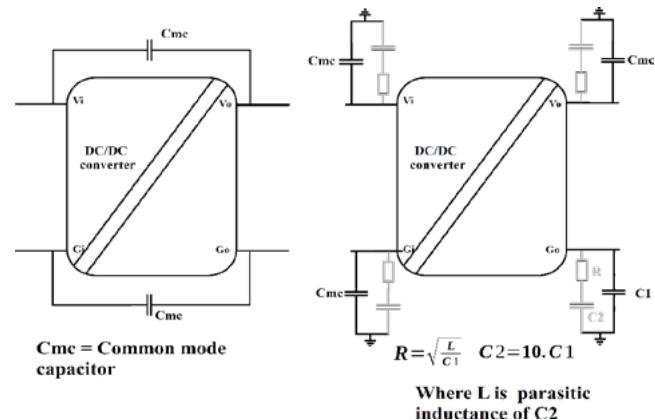


Figure 4: Common mode capacitors can be placed across primary/secondary isolation, or across input and output pins and chassis.

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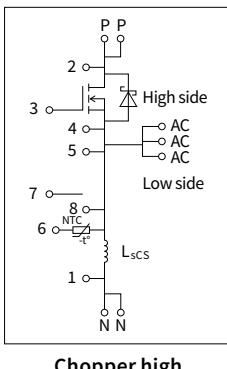
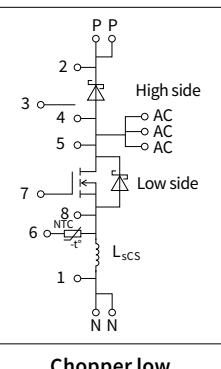
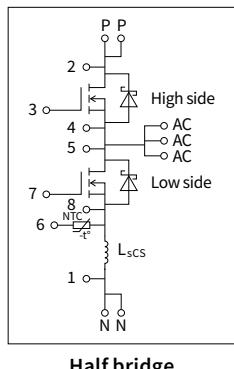
Package Highlights

- High mounting compatibility with Si IGBT module
- Lower loss characteristics than Si IGBT module
- High channel temperature ($T_{ch,max} = 150^\circ\text{C}$)
- Low stray inductance
- Low thermal resistance

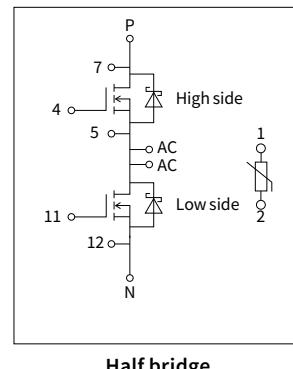
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Internal circuit options



Internal circuit option



In some cases, a snubbing circuit may be placed in parallel with the common-mode capacitor to further reduce total impedance at the capacitor's self-resonance frequency (also shown in Figure 4). Fortunately, most SMD chip capacitors have self-resonance frequencies high enough to avoid overlapping with the predominant harmonics of common-mode noise from typical SMPS designs, meaning this snubbing circuit can often be omitted.

When it comes to discrete filters, design might seem straightforward as they often consist of only passive components. Typically, the design starts with choosing an LC filter, where the component selection depends on the DC/DC converter's switching frequency. However, the engineer must carefully consider several parameters:

- What should be the quality factor (Q) of the filter?
- How can potential over-voltages from surges be damped?
- How can the inrush current, due to internal capacitors, be limited?

In most cases, the filter will also include one or more common-mode inductors to further reduce the common-mode noise. While selecting a standard market-available inductor is the simplest option, it often results in an oversized component. This happens because choosing an inductor with the needed inductance often restricts the available options to parts rated for much higher maximum currents than needed, resulting in unnecessarily large form factors. An optimized solution is to build a custom common-mode inductor. A common-mode inductor essentially consists of a ferrite core with two windings in the same direction. For differential-mode currents (currents flowing in opposite directions), the magnetic fluxes cancel each other out, and the core presents minimal impedance. For common-mode currents (currents flowing in the same direction), the magnetic fluxes add up, maximizing impedance.

The main advantage of building a custom common-mode inductor is the ability to select a core with a saturation level much lower than that needed for DC current — because differential-mode fluxes cancel each other. However, designing a custom inductor requires skillful calculation, thorough qualification, and significant time investment. GAIA has undertaken this task, developing over the past 25 years a complete range of passive filters directly matched to their DC/DC converters, ensuring full EMI compliance. These filters are optimized for form factor, inrush current limitation, and have been qualified for military and aerospace applications. The GAIA filters series ranges from 2 A, 50 V (FGDS2A50V) to 35 A, 100 V (FGDS35A100V), enabling the design of power supplies from 50 W to 500 W. The entire range operates from -55 °C to 105 °C and offers a high MTBF of 8 to 27 million hours.

Hold-up Function: Maintaining Power Integrity During Bus Interruptions

When it comes to power source transfers, the DO160G standard is clear: equipment must continue to operate despite short interruptions—up to 200 ms for category A, 50 ms for category B, and up to 1 s for categories D and Z. Similarly, ABD100 outlines comparable requirements. On the military side, MIL-STD-704 accepts a bus voltage drop to 0 V for up to 7 s, but only demands that equipment survives without damage, not necessarily without interruption. To meet these stringent requirements, one of the simplest and most effective solutions is to use a tank capacitor placed ahead of the DC/DC converter. Aluminum capacitors—or equivalent tantalum capacitors [3.1]—are typically used. These capacitors act as a reservoir during a bus dropout. However, some precautions must

be taken. Without a limiting resistor, the capacitor would cause a massive inrush current at power-up. To counter this, a resistor is added in series to limit the current. But during energy restitution, the resistor must be bypassed to avoid losses, what can be fixed with a diode connected in parallel. In the basic configuration shown in Figure 5, the required capacitor value to maintain 100 W at the converter's input (able to operate down to 9 V) over a 50 ms hold-up time can be calculated simply (figure 6):

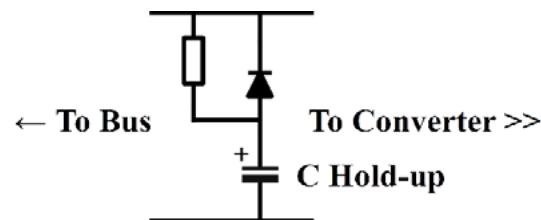


Figure 5: The simplest way to achieve the hold-up function requires a large capacitor, and a power resistor bypassed by a power diode.

To address these challenges more efficiently, GAIA has developed, a tiny hold-up module that boosts the 28 V bus voltage up to 80 V during normal operation. This solution significantly reduces the required capacitance—by nearly a factor of 10 in our example, bringing it down to around 1580 μ F.

$$C = \frac{2 \times \text{Power} \times \text{Time}}{\text{MaxVoltage}^2 - \text{MinVoltage}^2} = \frac{2 \times 100 \times 0.05}{28^2 - 9^2} = 14220 \mu\text{F}$$

Figure 6: The hold-up capacitor value remains large if it is charged only at 28 V_{DC}.

Beyond energy storage, these hold-up modules offer a range of critical functions like adjustable power-fail detection to precisely match the converter's minimum input voltage, adjustable capacitor voltage to optimize the energy storage, reverse polarity protection, and many more features. Over time, GAIA has built a range of hold-up solutions, making life easier for designers while reducing the PCB space once occupied by bulky capacitor banks.

Configuraron:	With No Module	With HUGD50	With LHUG150	With HUGD300	With FLHG60/ PSDG48
Needed capacitor value	14224 μ F 50V	7330 μ F/50V	2450 μ F/80V	1580 μ F/100V	31330 μ F/25V
Capacitor voltage	28Vdc	38Vdc	65Vdc	80Vdc	20Vdc**
Capacitor volume(in3)*	3.34	1.5	1.2	1.16	2

* Based on typical aluminium capacitor available

** These two models do not boost capacitor voltage but leverage the lowest volume that 25V aluminium capacitors offer.

Table 1: Capacitance reductions achieved for a 50 W power supply requiring a 100 ms hold-up time. This reduction is made possible thanks to the hold-up modules.



Figure 7: Only two small aluminum capacitors enable this DO-160 compliant 120 W power supply architecture (GRD-12) to continue operating during a 50 ms input bus interruption. This is made possible by the internal hold-up module.

Once the principles of conducted noise propagation are fully understood, effective filtering becomes a straightforward exercise. This is particularly true with GAIA's integrated filters. Furthermore, meeting challenging bus interruption requirements like those in DO-160 or MIL-STD-704 is easily achieved using the company's hold-up modules. Their ability to reduce the hold-up capacity value for any interruption duration takes care of compliance without the need for large, board-space-consuming capacitors. The functional diagram in Figure 8 illustrates the concept of a compliant modular power supply architecture, in which each front-end component meets one or more specific requirements of the standards.

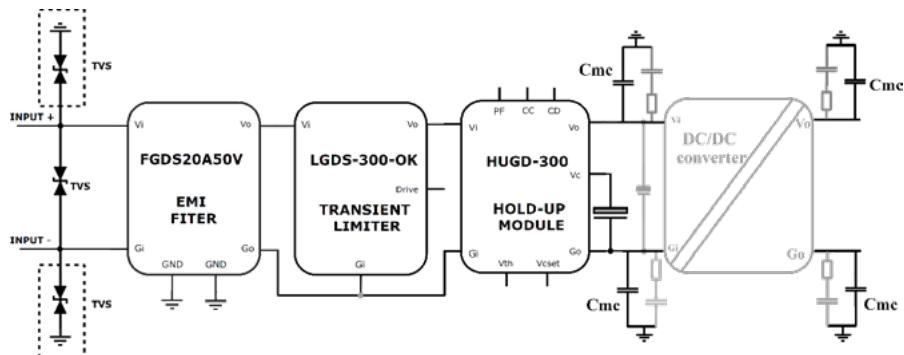


Figure 8: The front-end stage of a GAIA's mil-aero compliant power architecture contains the TVS, the EMI filters, the transient limiter and the hold-up module alongside the 2 hold-up capacitors.



Figure 9: Example of a 250 W power architecture that can be built using evaluation boards, which are fully documented within the "evaluation board service manual" [3.2].

As the front end section of our compliant power architecture has now been defined, the 4th and last part of this article series will delve into the core of energy conversion. By leveraging the functions described, this part 4 will demonstrate how to construct a complete, standards-compliant power supply.

[3.1] <https://www.vishay.com/docs/42115/ep2.pdf>

[3.2] https://www.GAIA-converter.com/wp-content/uploads/application_notes/EVGTJ2040.pdf

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Reliability Features of Power Electronics as an SOA Component for Sustainable Automotive Development

The article outlines how digital twins, predictive control, neural networks and Power-HIL turn power electronics into active SOA components, adding reliability and lifetime benefits to sustainable automotive systems.

By Oleksandr Solomakha, Chris Hermann, Diego Kuderna Melgar, Valentyna Afanasenko, Dominik Koch, Ingmar Kallfass, Institute of Robust Power Semiconductor Systems, University of Stuttgart, Germany

The shift towards electromobility and service-oriented architectures (SOA) in the automotive industry is leading to a redefinition of the role of power electronics (PE). Modern trends demand that PE components offer not only high performance, but also the ability to adapt, interact with other subsystems, and provide information about their own condition.

If in the past the drivetrain inverter was perceived as a “black box” with fixed logic and a limited lifetime, it now has to become a “digital participant” of the vehicle’s service-oriented architecture. Such a component must be able to evaluate its current state, predict degradation, adapt its behavior, and integrate into broader systems, including predictive maintenance, route planning, and centralized traffic management (Figure 1).

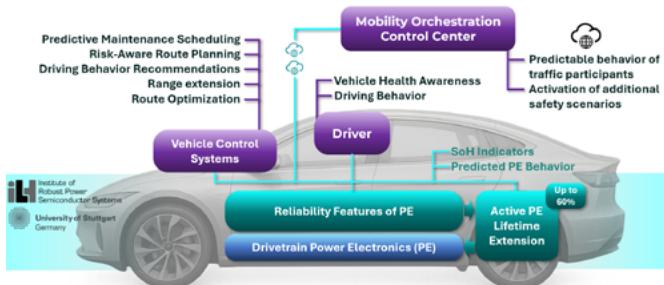


Figure 1: Contribution of Power Electronics Reliability Features to SOA-Based Vehicle Systems.

The Institute of Robust Power Semiconductor Systems (ILH), University of Stuttgart, developed and validated a concept for integrating the drive train inverter power electronics into the SOA structure of a vehicle by applying predictive control, digital twins, neural networks, and Power-Hardware-in-the-Loop (Power-HIL). This concept enables a transition from reactive maintenance to proactive resource management of power modules and provides a foundation for the sustainable and safe operation of electric vehicles (Figure 2).

Multi-level SOA Architecture with Power Electronics Integration

The integration of power electronics into the service-oriented vehicle architecture is implemented through a multi-level structure of digital services, where each level performs a specific role and interacts with the others according to SOA principles.

1. Drivetrain Power Electronics

At the foundation of the system are the drivetrain inverters based on modern SiC MOSFETs. These are physical devices that act as efficient power switches to provide switched-mode energy conversion, motor control, and are directly exposed to thermal and electrical stress.

2. Conventional Control of Power Electronics

The traditional inverter control system is responsible for delivering the target currents, voltages, and frequencies required for motor operation in response to the driver or system commands. It functions independently of reliability and degradation forecasting tasks.

3. State-of-Health Estimation of Power Electronics Based on a Multi-level Digital Twin and Deep Neural Network

At this level, the behavior of the power electronics is predicted using a digital model of the inverter combined with a neural network estimation of the remaining useful life. The digital twin reconstructs parameters of the inverter that are not directly measurable and includes a built-in aging model. The data comprise electrical, thermal, and control parameters, power losses, as well as degradation- and temperature-sensitive electrical characteristics (DTSEPs). The output of this layer is the estimation of State-of-Health (SoH) and Remaining Useful Life (RUL), provided as a digital service.

4. Predictive Control for Extending Power Electronics Lifetime and Efficient Route Planning

Using the predictive digital twin, the behavior of the power electronics is calculated within a given predictive horizon. Based on this vector of predictive values, an optimal control trajectory is generated to extend the lifetime of the power electronics.

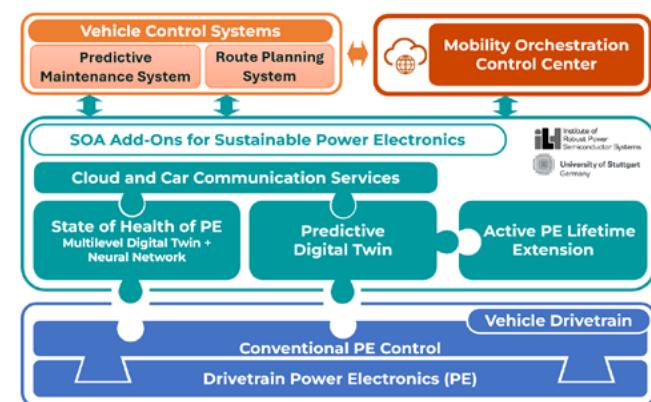


Figure 2: SOA add-on for drive train inverter of the EV.

HITACHI



Škoda Group

HV LinPak

After establishing itself as the new standard in the railway application with the Low Voltage (Viso=6kV) variant, the LinPak is now offering a High Voltage variant (Viso=10.2kV). While delivering the higher isolation voltage, it keeps the key features that made the LV variant a big success: phase leg configuration with very low stray inductance, high current density, separation of DC and AC terminals for ideal busbar and gate drive design. With these technical features, it accommodates Si IGBT as well as SiC MOSFET dies with blocking voltage 3.3kV, 4.5kV and 6.5kV.



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In both cases, a degradation factor is calculated to indicate the effectiveness of the approach. An important feature of active lifetime extension is that the processes are implemented at the driver level of the power semiconductor devices and do not interfere with the main motor control, which fully complies with the SOA concept.

5. Vehicle Control Systems

The obtained state estimations and predictions of the power electronics can support enhancements and enable optimization of vehicle-level functions such as:

- Predictive Maintenance
- Range extension
- Risk-Aware Route Planning
- Driver Behavior Recommendations

6. Traffic Orchestration Layer

At the top level, a global orchestrator coordinates the behavior of the vehicles, exchanges data via V2X, and takes into account the predicted condition of components in each vehicle. This enables route planning with reliability awareness, activation of adaptive safety scenarios, and improved predictability of traffic participants.

Each layer implements its own logic and interacts with others through standardized digital interfaces. Such a modular architecture allows power electronics to be integrated as an active SOA component, providing not only energy conversion functions but also a digital service for state estimation, lifetime prediction, and reliability management.

State-of-Health Estimation of Drivetrain Power Electronics

A key factor for the reliable and safe operation of drivetrain power electronics is the ability to objectively assess its current condition. In the proposed architecture, this is achieved through the SoH module, which provides a digital service for evaluating the remaining lifetime and degradation risk of the power module.

The SoH module assessment mechanism is based on two complementary technological components:

- **Multi-level digital twin of the power electronics**, covering:
 - System level for electrical, thermal, and control processes,
 - Semiconductor module level for thermal and loss models of the power module,
 - Semiconductor chip level for temperature-sensitive electrical parameters and an aging model.

This digital twin enables real-time evaluation of the dynamic behavior of the power electronics, including parameters not directly measurable in practice.

- **Deep neural network**, trained on data collected in a Power-Hardware-in-the-Loop (Power-HIL) setup, where real drivetrain inverter operating conditions were reproduced. The neural network uses TSEPs to evaluate both SoH and RUL.

The SoH module estimation becomes a digital service, delivering additional value at different levels:

- **For the driver** — providing information about the overall condition of the power electronics and recommendations on driving behavior (Vehicle Health Awareness).
- **For vehicle control systems** — SoH module data may be integrated into:
 - Predictive Maintenance Scheduling,
 - Route selection considering expected component degradation (Risk-Aware Route Planning),
 - Adaptation of drivetrain control strategies under limited resource (Driving Behavior Optimization).

- **For the centralized traffic orchestrator** — SoH module information enables:
 - Predictable behavior of traffic participants,
 - Activation of additional safety scenarios.

In this way, the SoH module transforms power electronics from a passive element into an intelligent participant of the vehicle's digital ecosystem, providing real-time data to enhance the reliability and resilience of the entire system.

Behavior Prediction of Drivetrain Power Electronics

Based on the predictive driving horizon (speed, traction force, route profile, etc.), which is already available in advanced vehicle control systems, the digital twin calculates the electrical parameters of the power electronics: current, voltage, frequency and derives losses and the junction temperature of the semiconductors from them.

The junction temperature is a key parameter for the reliability of semiconductor components. Using its predicted trajectory, a dedicated algorithm evaluates how quickly the power electronics will degrade under a given predictive scenario.

This information can be used for:

- actively extending the lifetime of semiconductors and power modules,
- integration into vehicle control systems for route optimization, as an additional cost function in route planning. This approach was tested with the ZF EcoControl system, and the results of this evaluation are shown in Figure 3.

Forecasting junction temperature and degradation requires modeling of a complex multi-parameter system with cross-coupled feedback between electrical, thermal, and control variables. The digital twin provides the necessary modeling depth and adaptability, enabling this functional block to be realized as part of predictive control strategy. Such a digital twin can be implemented on an embedded system with a processor clock of 200+ MHz and at least 2 MB of memory.

Application Example: Active Lifetime Extension System for Semiconductors

One of the main factors of power electronics degradation is thermos-mechanic stress accumulation caused by sharp fluctuations of the semiconductor junction temperature. Using data from the predictive digital twin and the realtime route planning, the thermal trajectory can be forecast in advance and a control algorithm applied to minimize the amplitude of temperature peaks.

This strategy is implemented at the driver level and adapts the MOSFET gate control parameters without interfering with the main inverter control system. This makes it possible to integrate it as an independent service within the SOA framework.

Such control can extend the lifetime of power electronics by up to 60% compared to conventional operation modes, with only a moderate increase in additional electrical losses.

Experimental Implementation using Power-HIL

To validate the concept, a Power-Hardware-in-the-Loop setup was built using two 50 kW inverters (SiC and IGBT) connected in a back-to-back configuration. The tests were carried out by reproducing driving cycles FTP75, FTP72 for normal driving, US06 for aggressive driving, HWFET for highway driving, and WLTP 3b for a mixed mode drive profile.

This setup made it possible to:

- simulate real driving profiles,
- validate the digital twins by comparing estimated and experimental trajectories,
- obtain realistic data for training the neural network SoH model and testing its performance (Figure 4).

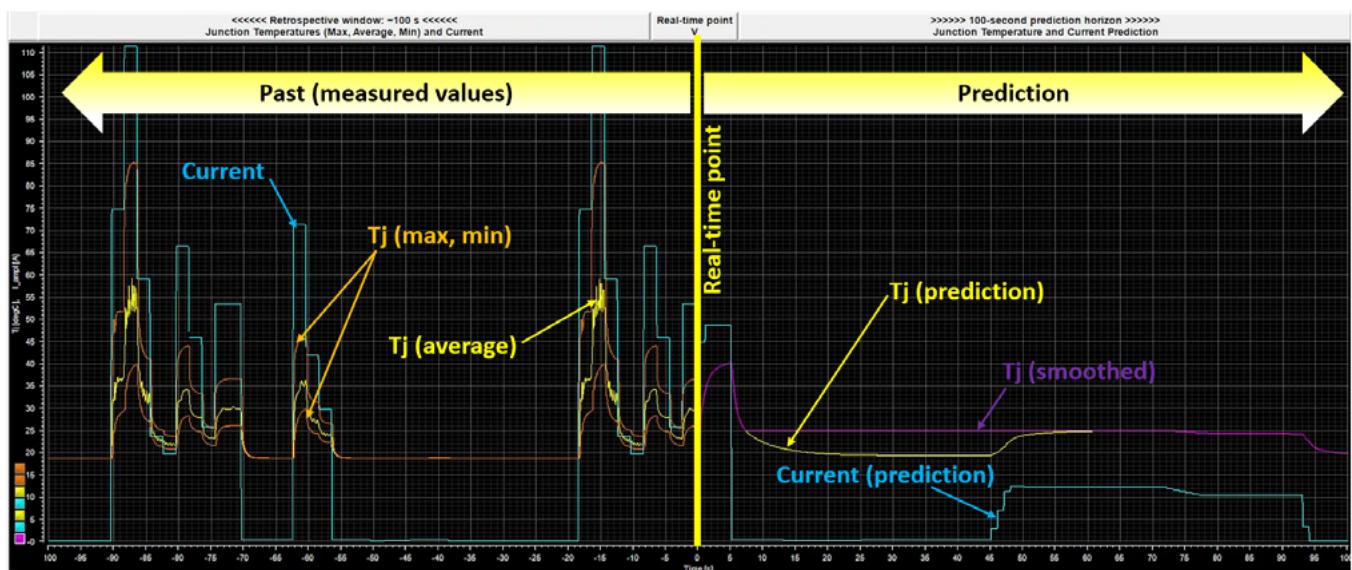


Figure 3: Testing with ZF EcoControl route planning system via cloud

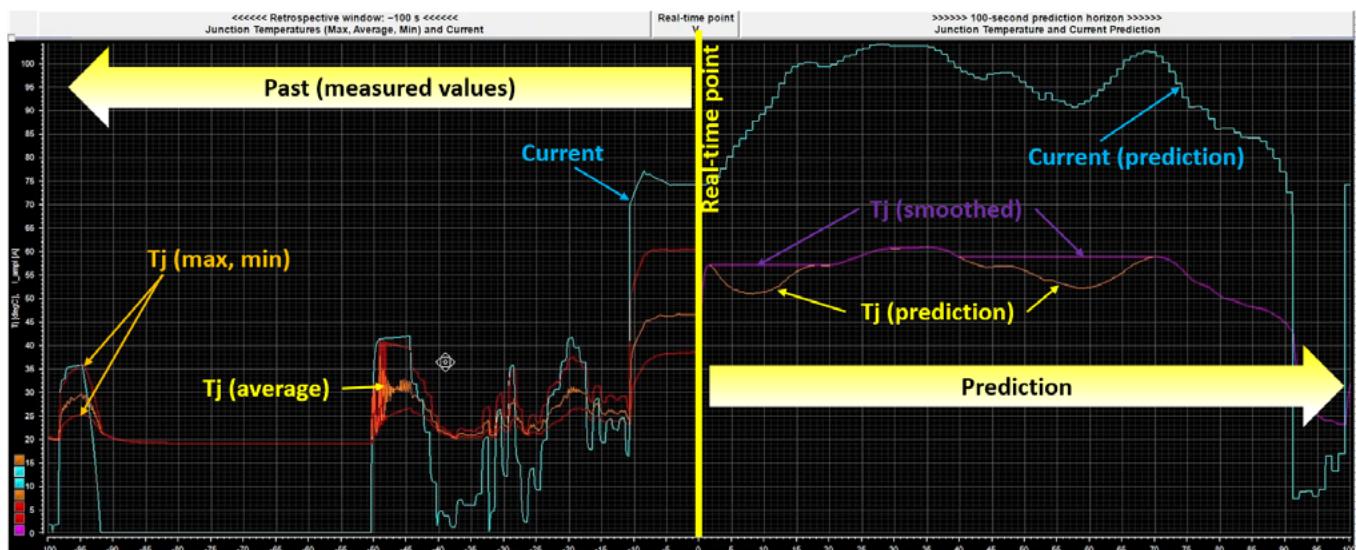


Figure 4: Testing with FTP75 drive cycle data

Conclusion

The integration of the Reliability Features of the drivetrain power electronics into the vehicle's digital ecosystem is not just an improvement of individual components, but a transition to a new level of PE integration into the digital domain for sustainable electromobility:

- Power electronics become a “speaking” component, providing a digital service.
- Interaction with routing and service systems increases the adaptability of the vehicle.
- Centralized vehicles management gains access to real-time reliability data of components and initiates safety-oriented driving scenarios.

Such a structure meets the challenges of sustainable development: not only reducing energy consumption, but also extending component lifetime, reducing waste, improving maintainability, and minimizing the risk of failures in operation.

Acknowledgement

The authors acknowledge the financial support of the research within the “AUTotech.agil - Architecture and Technologies for Orchestrating Automotive Agility” project (FKZ 01IS22088A) by the Federal Ministry of Education and Research of Germany (BMBF).

The implementation and testing were carried out by the team of Institute of Robust Power Semiconductor Systems of University of Stuttgart. Special thanks to our colleagues from ZF Friedrichshafen AG and to all partners involved in the AUTotech.agil project for their support and collaboration.

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DC-Link Management for Regenerative Servo Drives: Brake Choppers, Sizing, and EMI Pitfalls

DC-link management is the discipline that keeps energy on the DC bus of a regenerative servo drive safe, stable, and useful. Braking events can push bus voltage up in milliseconds, and poor design can turn that energy into trips, heat, or electromagnetic noise instead of productivity.

The hook is simple. Every deceleration either pays you back or punishes you.

By Rene Ymzon, Marketing Manager, Advanced Motion Controls, AMC

The importance is high because modern machines pack more inertia and faster cycles into smaller cabinets where margins are thin. In this guide you will learn what the DC link is, why regeneration stresses it, how brake choppers actually behave, how to size choppers and resistors correctly, and how to avoid the most common EMI pitfalls. You will also see when an active front end is the smarter option and when a humble resistor is all you need.

We will keep the tone practical so you can apply the ideas the same day on a real machine. By the end you will have a concise playbook for safer decels, quieter cabinets, and fewer nuisance faults.

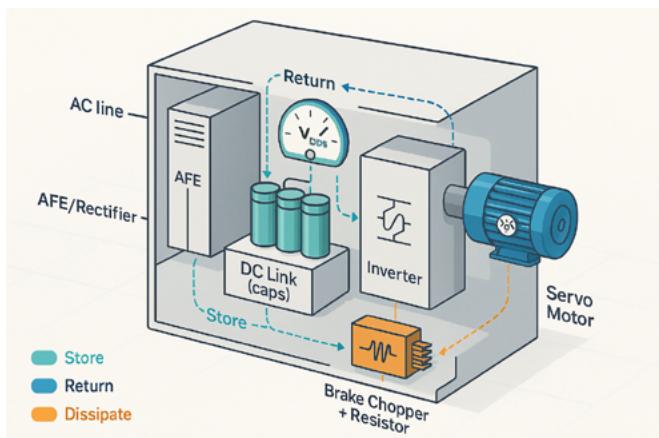


Figure 1: How servo drives manage energy flow: storing, returning, or dissipating regenerated power inside a motion-control system

What is the DC link in a servo drive?

The DC link is the intermediate energy store that connects the rectifier or active front end to the inverter stage that feeds the motor. The DC link smooths pulsating input power, provides a local reservoir of energy, and sets the reference voltage the inverter switches against. A stable DC link reduces current ripple, improves control loop headroom, and limits overvoltage trips during braking. The block view is simple. AC line flows to a rectifier or AFE, then to bus capacitors and film decoupling, then to an inverter that produces three phase PWM to the motor. During motoring the DC link delivers energy to the motor. During regeneration the motor returns energy that raises bus voltage.

Typical servo buses run from roughly 300 to 800 VDC depending on mains and topology. Capacitance spans hundreds to thousands of microfarads and ripple targets sit in the low single digit percent under rated load before regen events occur. For background on motion power stages and DC bus behavior, a useful primer on modern

servo drives helps connect control concepts to practical hardware decisions.

1. Typical bus voltages: 325 VDC for 230 VAC class, 565 VDC for 400 to 480 VAC class, higher for specialty systems
2. Typical capacitance: 470 μ F to several mF depending on power and sharing
3. Typical ripple targets: 2 to 5 percent under steady load, briefly higher during transients

DC bus capacitors

DC bus capacitors are energy storage components that reduce ripple and absorb short transients on the DC link within a servo drive. In this context the capacitors define how stiff the bus feels to sudden load changes and how much short-term regen energy can be buffered before other actions are needed. Electrolytic capacitors offer high capacitance density with higher ESR and limited lifetime. Film capacitors offer low ESR and excellent high-frequency performance with lower capacitance per volume. Thermal performance, ripple current rating, and lifetime at hot-spot temperature dominate selection. Higher ESR increases losses and temperature rise which shortens life. Lower ESL and strategic placement near switching nodes tame ringing and radiated noise.

1. Selection factors: voltage margin of at least 20 percent, ripple current rating at worst-case temperature, ESR and ESL at PWM frequencies, lifetime at hot-spot per manufacturer curves, mounting and creepage for the cabinet environment

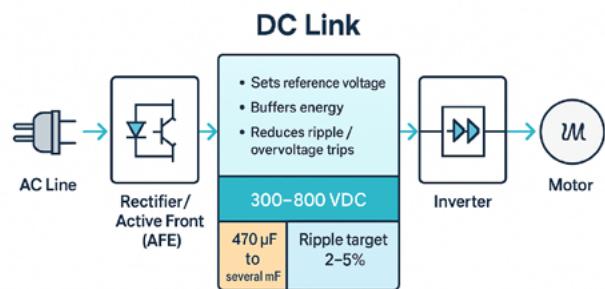


Figure 2: The DC link acts as the energy buffer and voltage stabilizer between the rectifier and inverter, ensuring smooth, reliable power delivery to the motor.

Precharge circuit

Precharge is the process that limits inrush current to DC bus capacitors when a servo system powers up so components are not stressed and breakers do not trip. In this article precharge matters because big capacitor banks look like a short at t0. A resistor, NTC, or active precharge path fills the capacitors gradually before

the main contactor closes. The main applications include multi-axis buses, drives with large electrolytic banks, and systems with line-side contactors. The working principle is straightforward. Insert resistance or a controlled switch to limit current, sense bus voltage to a threshold, then bypass with a contactor.

1. Common topologies: fixed resistor and contactor bypass for simplicity, NTC thermistor for cost-sensitive builds, active MOSFET precharge for tight control and reduced heat, sequence options for multi-supply cabinets

Why do regenerative servo drives need DC-link management?

Regenerative servo drives need DC-link management because braking events push energy back into the DC bus which raises the bus voltage toward overvoltage trip limits. The subject is not optional. Unmanaged regeneration stresses capacitors, triggers faults, and can compromise safety. The general picture is energy that was kinetic becomes electrical and has to go somewhere quickly. The details include how motion profiles concentrate energy, how vertical axes inject constant regen when lowering, and how multiple axes couple through a shared bus. The outcome is predictable. Either you return it to the grid, buffer it briefly, or burn it as heat in a resistor. Good management keeps the DC link inside safe limits while maintaining machine throughput.

1. Fast bus rise scenarios: high inertia rapid decel, emergency stops from top speed, gravity loads on Z axes, multiple axes braking at once on a shared supply

Where does the energy go during braking?

Braking energy goes to one of three places by design. The drive can push it back to the grid through an active front end, the capacitors can store it for a short interval, or a brake chopper can dump it as heat in a resistor. Returning to the grid is most efficient but requires cost and commissioning. Storing in capacitors is temporary and sized by ripple and trip limits. Dumping to a resistor is simple and robust for short bursts.

1. Returned to grid: highest efficiency and improved power factor, best for sustained regen and energy savings, requires AFE hardware and setup
2. Stored in DC caps: zero wiring complexity and instant response, limited by voltage rise and ripple current, best for small or very brief events
3. Dissipated in resistor: low cost and simple logic, thermal design required, best for intermittent or bursty regen profiles

Brake Chopper Hysteresis

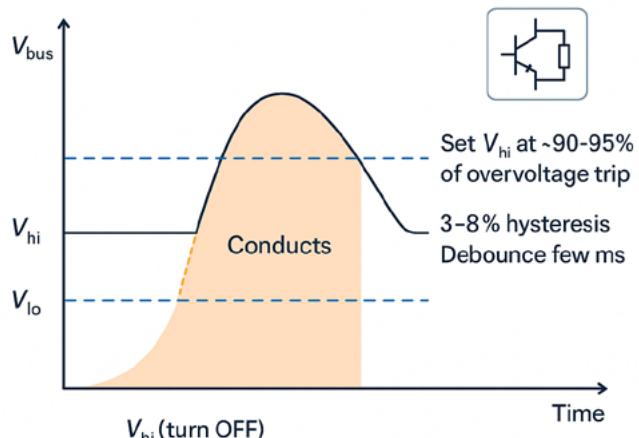


Figure 3: Brake chopper hysteresis controls when excess DC-bus energy is dissipated, preventing overvoltage trips during regeneration.

How does a brake chopper work?

A brake chopper is a protection and energy management technology that senses DC bus voltage and switches a transistor to divert current into a braking resistor when the bus exceeds a set threshold. In this context a chopper turns dangerous peaks into controlled heat so the drive continues operating. The main applications are machines with intermittent decel energy, gravity axes that need a sink, and shared buses that see combined braking. The working principle is threshold control with hysteresis. When V_{bus} rises above V_{hi} the chopper turns on and current flows into the resistor. When V_{bus} drops below V_{lo} the chopper turns off. Device choice can be IGBT or MOSFET depending on bus voltage and current. Thermal limits, duty cycle, and coordination with drive overvoltage settings define safe operation.

1. Key parameters: V_{hi} and V_{lo} thresholds, peak current, switching duty, average power, resistor value and rating, thermal class and cooling approach

What operating thresholds and hysteresis should you set?

The operating thresholds should be set below the drive's overvoltage trip and above normal ripple so the chopper acts early without chatter. Start by identifying the drive's DC bus overvoltage limit and select V_{hi} at a safe margin below it. Choose V_{lo} to create a reasonable hysteresis band that prevents rapid toggling while preserving headroom for new regen events. On shared buses coordinate settings so one device is the primary sink.

1. Typical settings: V_{hi} at 90 to 95 percent of the drive's overvoltage trip, hysteresis band of 3 to 8 percent of nominal bus, debounce or on-time minimums of a few milliseconds for stability
2. Multi-axis caveats: designate a primary chopper on the common bus and stagger thresholds to avoid beating between sinks

What protection features and fail-safes matter?

Essential protection features include over-temperature shutdown of the resistor and switch, detection of open or shorted resistor, and diagnostics for a stuck-on transistor condition. Coordination with fuses and a crowbar element can protect against catastrophic faults. A discharge or bleeder resistor helps bring the bus down safely when power is removed. Data logging turns surprises into trends you can act on.

1. Recommended logs and interlocks: temperature of resistor and switch, duty cycle history, peak power time stamps, interlock with STO or main fault relay, alarm if duty exceeds design envelope

How to size the brake chopper and resistor?

The sizing workflow follows the machine's physics then converts that energy picture into electrical and thermal limits you can trust. The overview is gather motion and inertia data, compute energy and peak power, pick thresholds, choose a resistor that satisfies current and voltage, then check average and transient thermal limits. This how-to has 6 steps that move from mechanics to heat so you do not over or undersize the hardware. Finish by validating wiring gauge, clearances, and cooling so lab math survives the cabinet. Common mistakes include using motor inertia only, ignoring vertical axes, and forgetting the resistor's thermal time constant. A practical cross check is to simulate the worst real move and compare calculated duty to measured bus traces on a scope.

Step-by-step sizing method (worked logic)

This section gives an overview of the full method then applies it as a checklist you can use on any axis. You start with the motion profile and end with thermal headroom because heat is what enforces reliability in production. There are 6 steps and they are purposely simple so you can run them from a spreadsheet or a quick script without waiting for a full digital twin. Tie each step to real data you can pull

from the machine or commissioning logs and keep a margin for parts aging and seasonal temperatures.

1. Collect the motion profile and total reflected inertia including load and gear train
2. Compute kinetic energy and peak regen power during the worst deceleration interval
3. Pick V_{hi} and V_{lo} relative to the drive's overvoltage trip and define the allowable current window
4. Choose resistor value R so current from V_{bus} into R stays below the chopper device limit while still absorbing power effectively
5. Check average power E divided by decel time against the resistor's continuous and short term ratings and thermal time constant
6. Validate enclosure cooling, wiring, and spacing then repeat for multi-axis buses with a diversity factor so peak events do not stack unrealistically

Cost ranges for DC-link options

Budgets matter so it helps to frame options early. Typical costs depend on power class and duty profile and they vary by enclosure and certification needs. Entry integrated chopper modules for small to mid-size drives are modest, resistor banks scale with wattage and IP rating, and AFEs command higher upfront cost with potential energy payback in continuous regen plants. There are 6 main cost factors and understanding them avoids surprises at purchase order time.

1. Average ranges: integrated chopper adders can be a few hundred to low thousands USD or EUR, standalone resistor banks span from low hundreds to several thousands depending on kW and IP rating, compact AFEs begin in the low thousands and scale significantly with power and filtering

Sizing Workflow for Brake Chopper and Resistor

1. Gather motion profile and total inertia
2. Compute kinetic energy and peak regen power
3. Set V_{hi} and V_{lo} thresholds
4. Choose R respecting device current and bus voltage
5. Thermal check average and transient / duty cycle
6. Enclosure cooling and wiring validation, multi-axis

Common mistakes

- Ignoring vertical axes or overhauling loads
- Undersizing resistor continuous power
- Choosing too high R causing insufficient clamping
- Forgetting duty and pulse energy rating
- EMI oversight



Creating a compatible future

See how compatibility is shaping the future.

Figure 4: A step-by-step workflow for correctly sizing a brake chopper and resistor, along with common mistakes to avoid in regenerative motion systems.

2. The 6 cost drivers: power level of axis or bus, duty cycle and thermal class required, enclosure and IP rating for the environment, certification and safety documentation, cabling and installation complexity, commissioning effort including EMC testing and tuning

What are the most common EMI pitfalls on the DC link?

The most common EMI pitfalls increase radiated and conducted noise, raise fault rates, and risk noncompliance. Problems usually start with geometry and end with measurement shortcuts that hide root causes. Long parallel conductors form antennas, high ESL placement creates ringing, and shield terminations done as an afterthought let common mode currents roam through everything else. Team skills vary and cabinet constraints are real. A short checklist of mistakes can prevent weeks of trial and error.

For deeper design examples and test-based discussions of these topics, industry coverage from Bodo's Power Systems provides context on switching devices, layouts, and EMI troubleshooting that pairs well with the practices below.

1. Do not route long untwisted DC bus leads that create large loop area which radiates strongly
2. Do not ignore common mode currents that couple through stray capacitances to chassis
3. Do not allow ringing from high ESL layouts that amplify switch node transitions
4. Do not let fast edges exceed EMC limits without adding snubbers or filters
5. Do not break shields or float panels which undermines a low impedance ground bond
6. Do not share long DC buses between axes without dv dt control or local film caps
7. Do not mount the resistor so far away that hot loops and magnetic fields grow uncontrolled

How to mitigate EMI on regenerative systems?

Mitigation is a process that begins with geometry then adds selective components and ends with proof on test instruments. This how-to has 8 steps that move from placement to measurement so you can catch issues before compliance day. Start small with loop area and bond quality. End precise with probes and pre-scan data so you know what frequency bands matter.

1. Minimize loop area by keeping positive and negative bus conductors close and short
2. Add film capacitors near switching devices to provide a low ESL local energy path
3. Select snubbers or RC damping sized from measured ringing frequency and impedance
4. Apply common mode chokes or dv dt filters on motor outputs when cable lengths are long
5. Terminate shields 360 degrees to chassis at a defined point or per vendor guidance
6. Bond all grounds with low impedance straps or copper so returns are not forced through signal paths

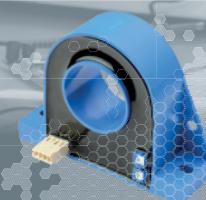
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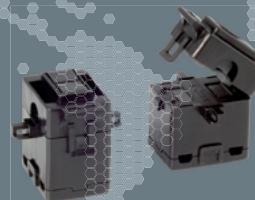
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7. Separate power conductors from control wiring and cross at right angles when required
8. Validate with a scope and a simple pre-compliance scan so fixes are based on data, not guesswork
9. Probe points to prioritize: DC bus ripple at the caps, inverter switch node, braking resistor leads during chopper events, chassis bond near the filter entry

Conclusion

DC-link management is the quiet heart of a reliable regenerative servo system. The DC link shapes how energy moves, how fast you can stop, and how often you trip on overvoltage. Brake choppers provide a rugged sink for bursts. Active front ends provide efficiency and power quality for sustained events. Good sizing turns physics into numbers you can buy. Good EMI practice turns numbers into cabinets that pass tests and run clean. If you put these ideas into your next design review you will harvest the energy you already paid to spin up and you will ship a machine that stops hard, stays up, and sounds civilized.

www.a-m-c.com

Factor	Brake chopper	Active front end
Efficiency	Low during braking because energy is dissipated as heat	High because energy is fed back to the grid
Capex	Low initial cost for module and resistor	High initial cost including filters and protection
Wiring and commissioning	Simple wiring and straightforward setup	Complex wiring and commissioning expertise required
EMC impact	Local hot loops need careful layout and snubbing	Line-side emissions require filters but motor-side can be calmer
Best use cases	Intermittent or bursty regen and emergency stops	Continuous regen, gravity loads, and energy saving mandates
Failure modes	Resistor overtemp, transistor failure, open resistor	Tuning errors, grid disturbances, filter aging
Space and thermal	Small footprint but needs airflow for resistor	Larger footprint with line reactors and cooling needs

Brake chopper vs active front end regeneration

Designing for Speed: What OEMs need to know when integrating high-speed Drives

Our accelerating world calls for ever faster motors. From wastewater treatment to data centers, industries all over the world are scaling up to meet bold challenges and increasing demand. Original equipment manufacturers (OEMs) are responding with upgraded technology, to provide their industrial clients with the efficient performance they need so they can scale. As a result, we're seeing the rise of a new generation of high-speed industrial applications – defined by high-speed motor frequencies of 120 Hertz (Hz) and over. This article explains why specialized variable speed drives (VSDs) are needed to work with these applications.

By Juha Saukko, OEM Sales Manager - Segment Compressors, ABB

High-speed motors open up new possibilities. Efficient cooling for bigger buildings and more advanced data centers. Faster, more thorough aeration and cleaning of wastewater. All while using significantly less energy than it would take to do the same job with traditional motors.

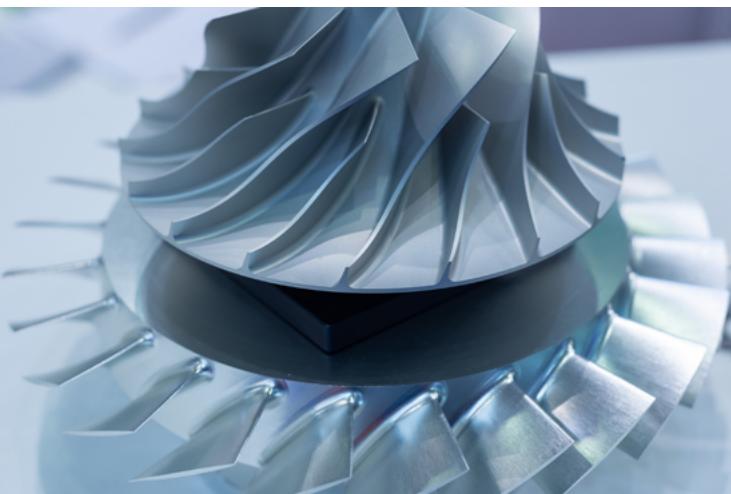
But like any emerging technology, high-speed applications also bring new challenges. Higher speeds also mean greater stress on the motors, components and surrounding equipment. And in the large-scale facilities and processes these applications support, the impact of downtime for maintenance or repairs, planned or unplanned, can be drastic. In large-scale food and drink refrigeration, downtime could mean huge amounts of food spoiling and going to waste. In data center cooling systems, downtime could reduce computation speeds or lead to lost data. In offices and residential buildings, the occupants won't stay quiet for long when the air conditioning system goes down.

One challenge is that the standardization familiar from more traditional industrial motors has not yet arrived for high-speed applications. This makes an OEM's choice of drive crucial to the success of the application. A good high-speed drive must be versatile enough to control any number of unique high-speed motor designs, while consistently supplying enough current for these powerful machines. And that's not the only consideration for OEMs joining the high-speed revolution.

Advanced technology brings new complexities

ABB's own definition of a high-speed application is when the motor frequency is over 120Hz. And beyond this limit, a high-speed drive needs a higher than usual switching frequency. VSDs control the motor by sending out pulses of voltage. The switching frequency (SwF) determines the length of the pulses.

Each pulse nudges the output frequency to match the desired pattern; so while the output voltage follows a digital sawtooth pattern, the output frequency resembles the smooth analogue sine wave created by more traditional fixed-speed drives.



SwF for motor control is like resolution for picture quality. The higher the SwF, the more closely and accurately the drive can control the output frequency, nudging it moment by moment towards the desired smooth sine wave.

The latest high-speed drives can achieve a SwF of 18 kilohertz (KHz) – or even higher, though most still need a separate sine filter to further smooth the output frequency.

But a higher SwF also presents some challenges. This is because a high SwF can cause high Total Harmonic Distortion (THD). This can exacerbate overheating, which necessitates output current derating. Overheating is an issue in many high-speed applications before we even consider the way the drive delivers power. Industrial heat pumps and cooling compressors naturally operate at high temperatures, and anywhere components are moving at high speed, they will generate a certain amount of heat.

THD quantifies the amount of harmonic distortion present in a signal. Harmonic distortion refers to the presence of frequencies that are multiples of the fundamental frequency of a signal, and THD is expressed as a percentage of the fundamental frequency's power. In simple terms, THD indicates how much a signal deviates from a perfect sine wave due to the presence of unwanted harmonic frequencies. A lower THD value generally indicates a cleaner, less distorted signal, while a higher THD value suggests more distortion

To decrease the heat generated, most high-speed applications also use air bearings or magnetic bearings to reduce friction. But it is important to note that in magnetic bearings, magnetization starts to decrease above 80°C and the rotor can become demagnetized if the temperature reaches 160°C or higher, causing motor failure, and leading to costly downtime.

Therefore, to prevent damage, most high-speed applications specify a temperature range within which the drive must reduce its output to cool the motor down. But during any time this output current derating is in effect, the application is not operating at peak efficiency.

Then there's the issue of electromagnetic compatibility (EMC): essential for regulatory compliance in the European Union, but often neglected in other regions, where it's treated as less of a priority by governments and regulators.

Many industrial applications need an EMC filter to reduce the transfer of electromagnetic noise between the drive and the mains power supply. Without an EMC filter, electromagnetic interference can disrupt other local businesses in the form of flickering lights and can even disrupt local radio broadcasts.

High-speed applications, with their higher SwF and motor frequencies, need different kinds of external filter to protect the local grid. Filters like a motor sine filter and line EMC filter are usually additional pieces of equipment, separate from the drive, which need space and expertise to install and maintain, and can add new points of failure to the overall system.

Since this technology began emerging, some OEMs may have decided not to pursue high-speed applications because of these considerations. But advances in high-speed drive technology, including the ACS880 high-speed drive from ABB, combined with new demands and new challenges facing industry, make now the perfect time to reassess the potential of high-speed applications.

Turbo-boosting efficiency in key industries

Traditional industrial blowers and compressors use oil-free screws to accelerate the air flow. Oil-free screws are mechanically complex, so they need regular maintenance, and their bearings (which, despite the name, are oil-lubricated) can require additional cooling.

Thanks to advancements in high-speed motors and drives, many of the applications that have traditionally used oil-free screws can now upgrade to superior impeller-based designs. Impellers can be mounted directly on the motor axle and have far fewer moving parts, so they need relatively little maintenance, can operate for much longer lifetimes, and cut out the need for oil-based lubrication. Aerodynamic impellers also move air with more efficiency than a traditional screw. High-speed motors and impellers are at the heart of a new generation of turbo blowers and turbo compressors that are already helping a range of industries to advance.

Turbo blowers are mainly used to aerate water. This process is the most energy-intensive part of wastewater treatment, accounting for 50% of a plant's total energy consumption. Switching to high-speed applications has unlocked energy savings of up to 45% in wastewater treatment plants - compared to lobe or screw compressors. One of the United Nations' Sustainable Development Goals calls for water and sanitation for all. To achieve this without also massively increasing energy consumption, high-speed applications are a must for the water and wastewater industry.

Aeration using turbo blowers can also increase fuel efficiency for large seagoing vessels by injecting a layer of air bubbles between the water and the ship's hull. This reduces drag, letting container ships and similarly sized vessels slice through the water, using less fuel to maintain the same speed.

Turbo compressors, meanwhile, are solving scaling and efficiency challenges in heating, ventilation, air conditioning and refrigeration (HVACR). Bigger buildings, more advanced data centers, global food and drink supply chains: in a heating climate, all these applications call for large-scale, efficient cooling and refrigeration, and centrifugal chillers powered by turbo compressors are meeting this need.

And at the other end of the temperature scale, turbo compressors also allow heat pump technology to work at an industrial scale, so district heating, industrial ovens and chemical process plants can all switch away from using gas for heating - reducing their emissions and their exposure to volatile commodity prices.

Next-generation high-speed drives accelerating industry
But what about all those challenges holding back some OEMs from embracing high-speed applications?

As industries and governments balance reducing energy and emissions with meeting increasing global demand - for water, for food, for physical goods, for data and computation - anyone still cautious about offering high-speed applications, whether alongside or instead of traditional applications, is liable to be left behind. But cautious OEMs may be reassured to know that high-speed drive technology is advancing alongside high-speed motors and their applications.

The incoming generation of specialized high-speed drives, led by the ACS880 high-speed drive from ABB, offers significantly improved efficiency, ease of installation and longevity. Perhaps the most attractive feature of the ACS880 drive is that it significantly reduces the need for current output derating, giving OEMs and their clients access to more optimized solutions with the space and cost savings of high-speed applications.

The ACS880 offers 2-phase modulation with a maximum SwF up to 18KHz (the upper limit of what most equipment can stand) or 3-phase modulation with a SwF up to 12KHz. Combined with real-time monitoring and sophisticated remote motor control, these systems allow the drive to be calibrated to run most high-speed applications at the lowest possible temperatures, preventing the heat buildup that triggers derating.

The flexibility and control these combined systems afford also mean that OEMs installing the ACS880 can, in some cases, do away with separately installed sine filters. And the ACS880 has a built-in EMC filter. So instead of three separate pieces of equipment all needing expert installation and maintenance - a drive, sine filter, and EMC filter, each representing a separate potential cause of downtime - OEMs can plan for a single, compact, easily installed high-speed drive. ABB high-speed drives only need maintenance once every nine years on average, so clients can count on high levels of uptime over the long term.

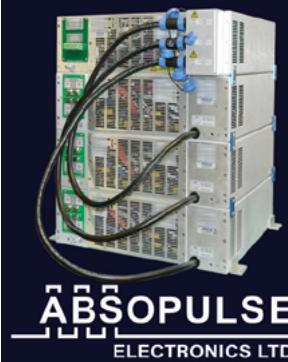
Even outside the European Union, where the issue is hardly regulated, EMC will become a more and more important consideration as more high-speed applications are connected to the grid.

Thorough testing is key to success

With standardization still some way off for high-speed applications, the design of the drive motor control algorithm is all-important for good equipment performance. OEMs considering switching drive suppliers can't assume the same settings will carry over. The SwF that worked for one combination of drive and motor will not necessarily be the SwF a new drive needs to get the best out of the equipment. At this stage in the technology's evolution, it's still best to test high-speed applications and drives together thoroughly, before putting them to work and joining the high-speed revolution.

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Addressing Power Supply Systematic Failures – Part 1: Using Output Discharge

By improving the robustness and systematic capability of power supply blocks, related systematic failures are eliminated. The first part of this series discusses three power supply solutions for a common systematic failure, which is related to output discharge when using LDOs.

By Bryan Angelo Borres, Senior Product Applications Engineer, and Ino Lorenz Ardiente, Senior Systems Design Engineer, Analog Devices

Power supply blocks provide one of the most critical functionalities in electronics systems, as their behavior affects how the system will behave during the different modes of operation—power-up, power-down, steady-state operation, and in the event of failures—which is critical in achieving the safe state in functional safety applications. Note that one of the three key requirements in complying with the basic functional safety standard is systematic capability. This requirement focuses on preventing and controlling systematic failures, which arise from design flaws, errors in specification, and poor management processes. With such requirements comes the need to address systematic failures of a power supply.^{1,2}

Eliminating systematic failures due to a power supply involves using the correct specification, providing the necessary sequencing, and ensuring that their loads are always operating within their margins. Image sensors in sensor subsystems and microcontrollers in logic subsystems are one of the most sensitive components in a safety-related system, as shown in Figure 1. If system reset involves automatically restarting the power supply to such subsystems, it may incur damage to the components.

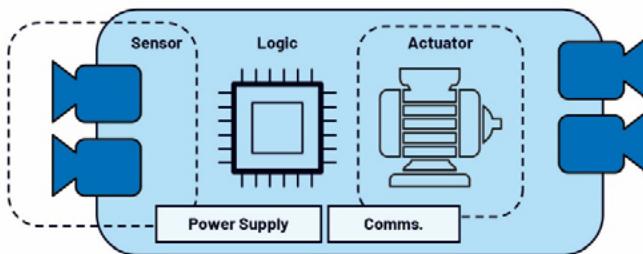
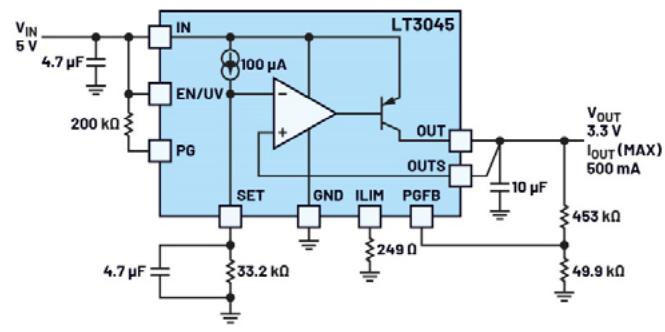


Figure 1: Example autonomous mobile robot (AMR) subsystems.¹

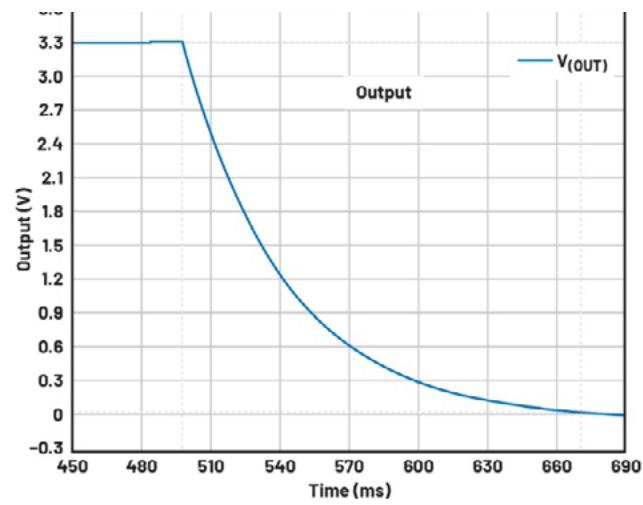
For an image sensor, having an incomplete power-up or power-down cycle stresses its circuitries.³ When the system is turned off, power to the image sensor should also be turned off as quickly as possible so the imager can be promptly restarted under ideal conditions, namely with no voltages lingering in the circuit. If the sensor is powered from a typical linear regulator, even though power to the regulator may turn off, the regulator's output is often held up by the output capacitor, allowing the image sensor to remain powered up and potentially disrupting the desired turn-off and turn-on performance of the system. Figure 2 shows an example of a power supply with 3.3 V on a 10 μ F output capacitor. This example has a 160 ms discharge time into a 10 k Ω load simulated using LTspice®.

Using Output Discharge Functions

One way to ensure that output voltages are fully discharged upon turn off is by using output discharge functions. These functions are necessary in applications requiring exact power sequencing and faster turn-off times, as they address floating outputs of power rails upon system power down to alleviate issues during power cycling.



(a)



(b)

Figure 2: Power supply example (a) using an LDO and (b) its output voltage discharge time.

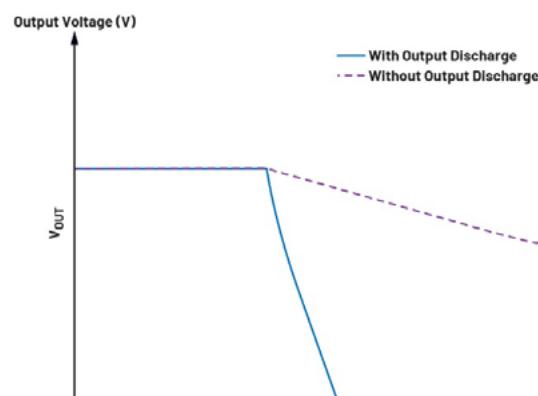
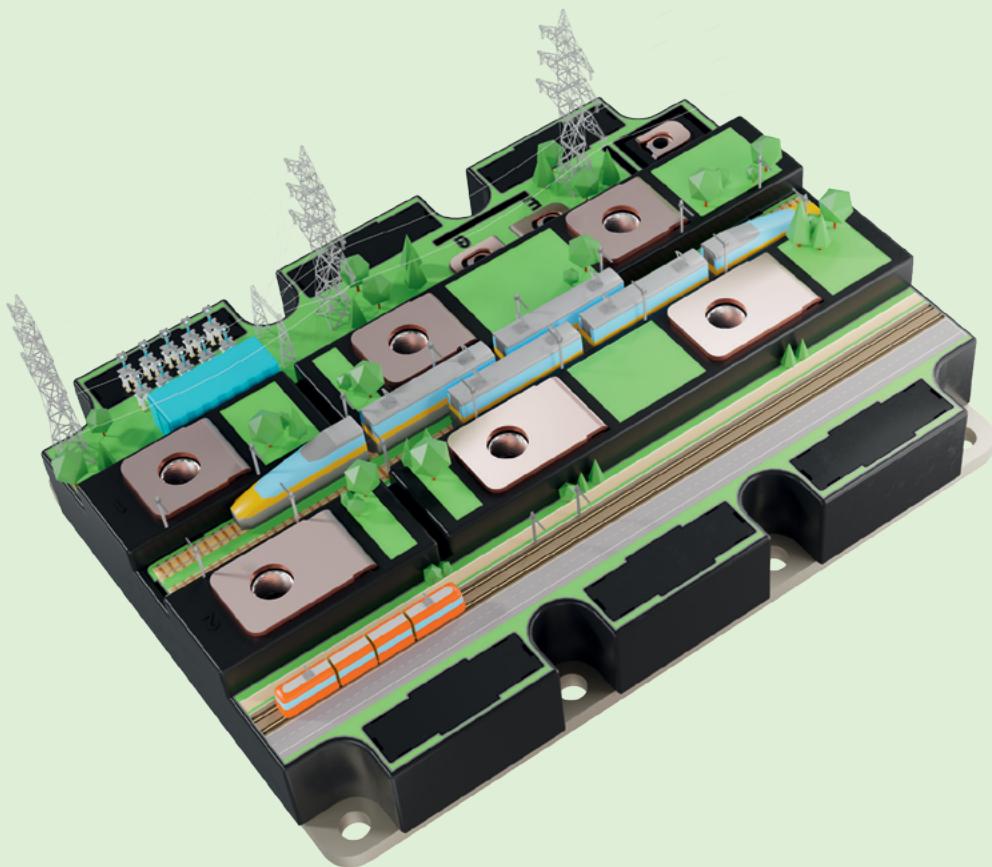


Figure 3: Output discharge operation.



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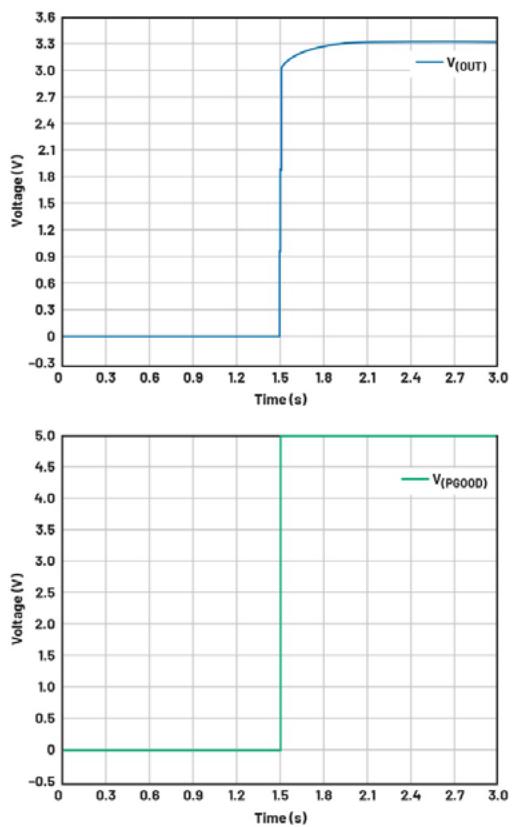


Figure 4: PGOOD signal demonstration (a) upon assertion and (b) deassertion.

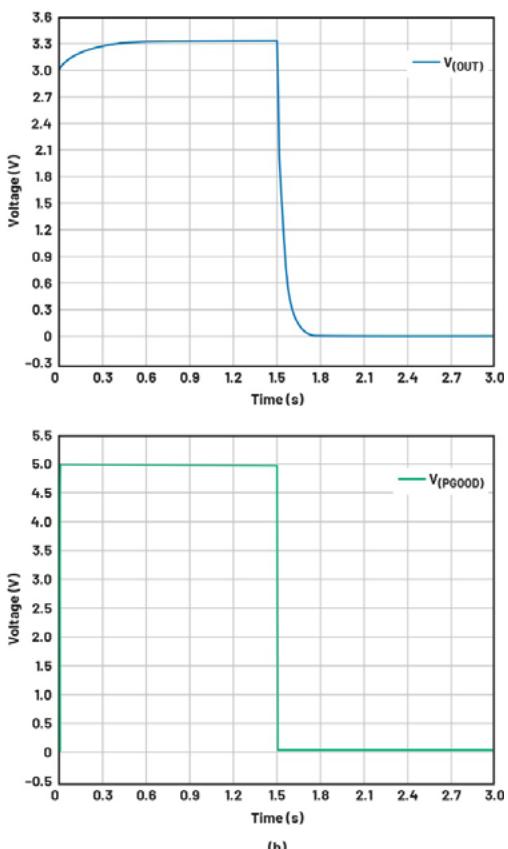


Figure 3 shows an example of an output voltage curve with and without output discharge function.

Adding an External MOSFET as a Discharge Circuit

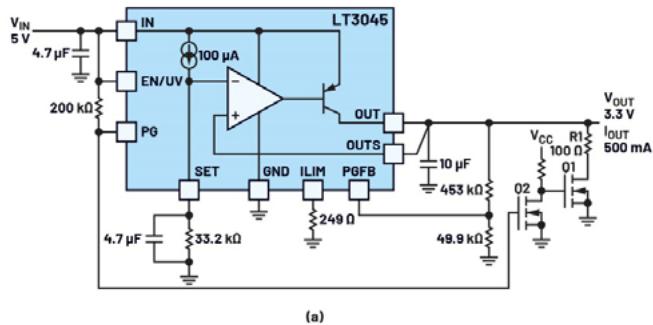
In recent power management designs, more low dropout (LDO) regulators are being released with additional functionality, including the increasingly common power-good signal (PGOOD). Such a PGOOD signal is a status output from the LDO, typically used to inform the system when the output voltage has reached and is maintaining proper regulation. In most implementations, this signal comes from an open-drain MOSFET that changes state based on the regulator's status. When the LDO output is within regulation, the PGOOD MOSFET is turned off—resulting in high impedance at the pin and causing the PGOOD output pin to be pulled up high.

This is shown in Figure 4a. However, when the output is out of regulation, the MOSFET turns on, pulling the PGOOD pin low via its low impedance path. This type of configuration allows the PGOOD signal to interface easily with different logic levels and supply voltages, making it versatile and widely usable. This is shown in Figure 4b.

However, this is also where a design challenge arises. Since the open-drain MOSFET used in most LDO PGOOD outputs is designed primarily for housekeeping, it can only sink a small amount of current. It is not suitable for sinking large currents directly from the output capacitor, especially if the goal is to quickly discharge the output when the LDO is disabled or shut down. Attempting to do so could damage the device or simply prove ineffective.

A more robust solution utilizing the PGOOD signal is by combining it with an external MOSFET circuit, which will act as a controlled discharge path. As shown in Figure 5, this circuit uses a discharge resistor, R_1 , which determines how quickly the output capacitor will discharge. The designer can size this resistor based on the desired discharge time—larger resistors will discharge the capacitor more slowly, while smaller resistors will speed up the discharge time. In this configuration, MOSFET Q1 serves as the discharge switch that turns on when the converter is disabled through the enable pin (EN). Meanwhile, Q2 is responsible for inverting the logic of the PGOOD signal from the LDO, ensuring the correct timing of Q1's activation. This setup allows for a fully customizable active discharge circuit that is responsive to the LDO's status.

By employing this method, any LDO equipped with a PGOOD pin can effectively be upgraded with an external active output discharge feature. This offers great flexibility for designers, allowing them to fine-tune the discharge profile of their power rail. The trade-off, however, is the added cost and board space due to the external components. Nevertheless, in applications where precise discharge control is critical, this approach provides a valuable and customizable solution.



(a)

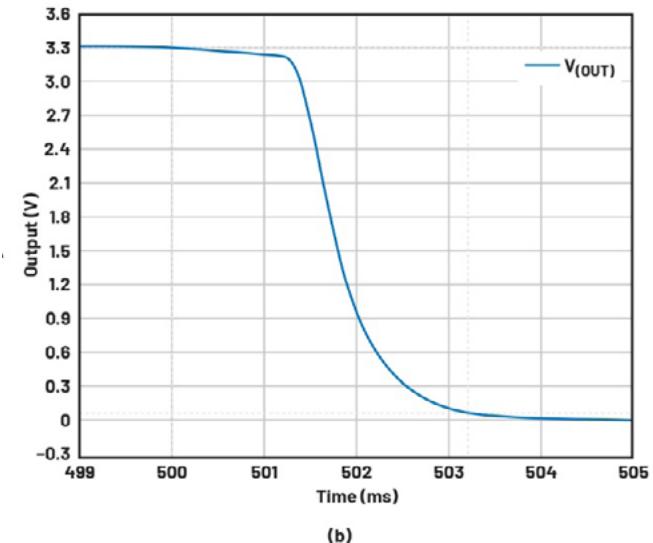
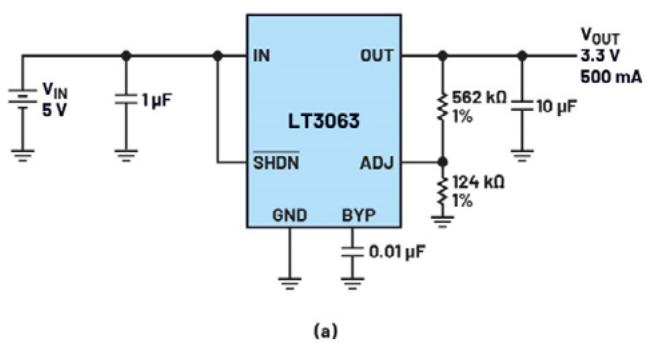


Figure 5: (a) Using the PGOOD signal of the LT3045 to trigger external MOSFETs as a discharge circuit and (b) its discharge time of 3.2 ms at 10 kΩ output load.



(a)

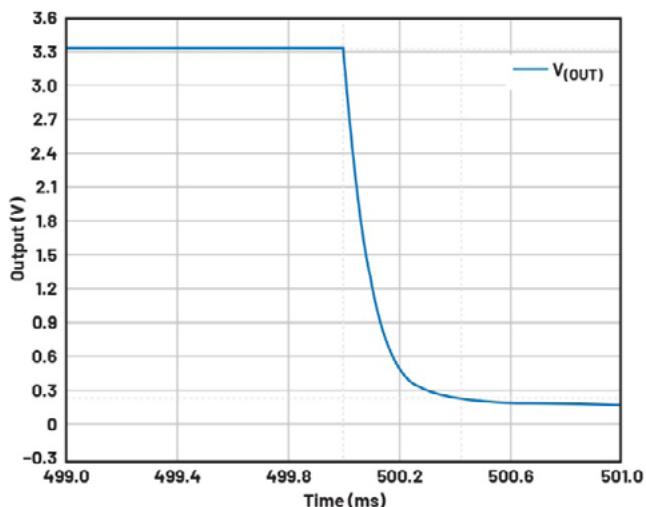
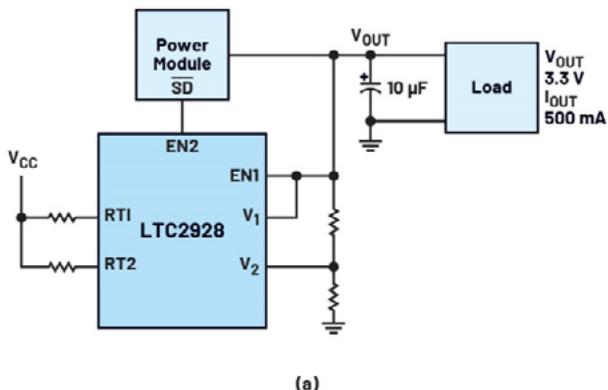


Figure 6: (a) LT3063 example circuit and (b) its discharge time of 0.5 ms at 10 kΩ output load.



(a)

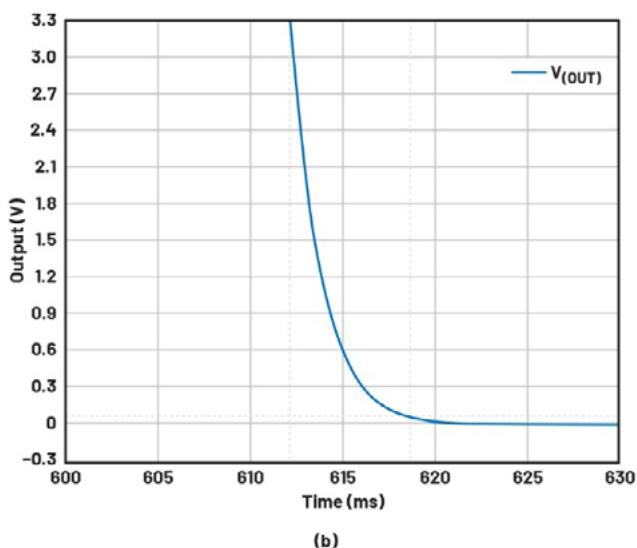


Figure 7: (a) LT2928 example circuit and (b) its discharge time of 6.5 ms at 10 kΩ load.

Implementing an Integrated Solution

To address this need without external circuitry, Analog Devices offers LDO solutions with integrated active discharge functionality. For instance, the LT3063 features a built-in active output discharge mechanism that simplifies the design process, reduces component count, and saves PCB space while still providing quick discharge performance. Figure 6 shows using this device achieves a discharge time of 0.5 ms, a significant improvement over the previous example in Figure 5.

Using a Supervisory Circuit

In safety-critical applications, a separate supervisory circuit may be preferred to provide more reliability and a sufficient degree of independence. A power supply sequencer such as the LTC2928 integrates the overvoltage and undervoltage monitoring features required to comply with functional safety, power sequencing, and output discharge capability. Figure 7 shows an example circuit. Other supervisory circuits with the output discharge feature include the MAX16050 and MAX16051.

Conclusion

Selecting the appropriate approach to address a power supply output's discharge performance requires a thorough evaluation of the design requirements and operating conditions. The methods for implementing active output discharge have their own distinct advantages and trade-offs. A certain solution may be more effective under specific output or application scenarios, while another method could offer better performance in different conditions. Therefore, understanding the unique characteristics and limitations of each technique is essential to ensure optimal implementation.

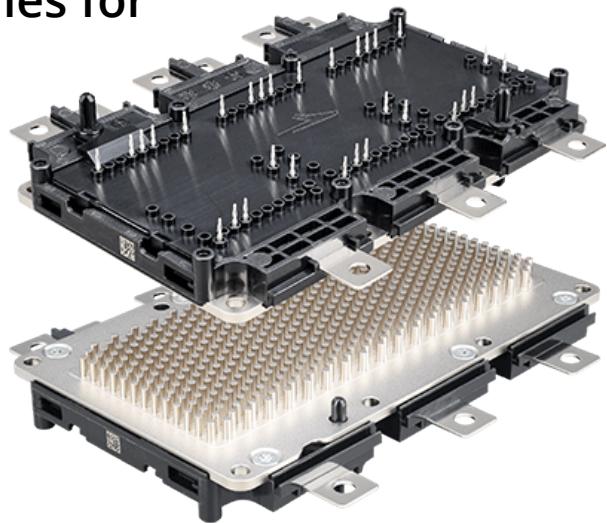
An external MOSFET is typically preferred in applications that demand higher output voltages or where maximum flexibility is needed. However, designers must be willing to accept the trade-offs of higher cost, increased board space, and additional power loss due to the inverter circuit. However, integrated solutions are often the best choice for low power or space-constrained designs, as they require no extra components and avoid further power dissipation. The drawback is limited availability, since only certain LDOs provide this feature. Furthermore, supervisory circuits are well-suited for systems with multiple output rails where power sequencing is also important. Although their MOSFET sink current is limited, making them less effective for large output capacitors, they provide an excellent option when sequencing, system coordination, and a degree of independence for functional safety consideration are critical. In summary, the decision should be based on matching the method's strengths to the specific output voltage, space, required discharge time, and sequencing requirements of the application.

References

- 1 Bryan Borres and Noel Tenorio. "Designing Power Supplies for Industrial Functional Safety—Part 1: What IEC 61508 Tells Us." Analog Devices, Inc., July 2025.
- 2 IEC 61508 All Parts, Functional Safety of Electrical/Electronic/Programmable Electronic Safety-Related Systems. International Electrotechnical Commission, 2010.
- 3 "Linear Regulators with Active Output Discharge Target Systems Needing Fast Power Down." Analog Devices, Inc., July 2014.
- 4 Bryan Borres and Christopher Macatangay. "Improving Industrial Functional Safety Compliance with High Performance Voltage Supervisors—Part 1." Analog Dialogue, Vol. 58, No. 3, August 2024.

1200 V SiC Six-Pack Power Modules for E-Mobility Propulsion Systems

Wolfspeed announced its 1200 V SiC six-pack power modules that "redefine performance benchmarks for high-power inverters". By combining its Gen 4 SiC MOSFET technology and packaging, Wolfspeed's modules are claimed to "deliver three times more power cycling capability at operating temperature than competing solutions, and 15% higher inverter current capability in an industry-standard footprint". In terms of packaging the new modules incorporate e. g. sintered die attach, epoxy encapsulant material, and copper clip interconnects. The company claims that this enables "3X more power cycles than best-in-class competitor devices in the same footprint". The modules achieve a 22 % $R_{DS(ON)}$ improvement at 125 °C compared to the previous generation, while reducing turn-on energy (EON) by approximately 60 % across operating temperatures. Additionally, the soft-body diode is said to enable 30 % lower switching losses and 50 % lower VDS overshoot during reverse recovery compared to previous generation. The modules' industry-standard packaging enables seamless adoption without complex redesign, serving as a direct replacement for IGBT solutions in existing system architectures. This means that there will be no need for power terminal laser welding and complex coldplate



mounting while maintaining compatibility with traditional power ecosystems including capacitors, cooling solutions, gate drivers, and current sensors.

www.wolfspeed.com

MOSFET for 48 V Hot Swap Applications in AI Servers

Alpha and Omega Semiconductor announced its AOLV66935, a 100 V High Safe Operating Area (SOA) MOSFET in an LFPAK 8x8 package. This MOSFET is designed as a solution for 48 V Hot Swap architectures in AI servers. The AOLV66935 utilizes AOS' 100 V AlphaSGT™ proprietary MOSFET technology that combines the advantages of trench technology for low on-resistance with high SOA capability. AOS has tested and characterized the SOA at 25 °C as well at higher operating conditions of 125 °C giving system architects the confidence that the device will operate reliably under harsh conditions. The MOSFET's LFPAK 8x8 gull-wing constructed package is 60 percent smaller compared to the TO-263 (D2PAK) package. The $R_{DS(on)}$ is specified with 1.86 mΩ at $V_{GS} = 10$ V.

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E-Fuse automotive Smart Switch for Protection, Power Saving and Functional Safety

An addition to the STi2Fuse family, the VNF1248F automotive e-fuse MOSFET controller from STMicroelectronics reacts within 100 µs, which is faster than a conventional wire fuse and ensures flexible and robust protection to avoid fault propagation inside the vehicle. The VNF1248F integrates the capacitive charging mode (CCM) functionality to ensure proper driving of large capacitive loads with

high inrush current. In addition, a Standby-ON mode with current capability up to 600 mA and current consumption lower than 75 µA enhances the vehicle's efficiency when in park mode. An optional external supply pin for logic reduces power consumption by 0.4 W in 48 V systems and battery-undervoltage shutdown compatible with the automotive LV124 standard ensures system stability. The chip facilitates reaching high safety-integrity levels (ASIL) in ISO 26262 functional-safety applications thanks comprehensive dedicated features like advanced fault detection and reaction, fail-safe mode and limp-home mode. There are also built-in self tests for automatic diagnosis and a dedicated pin for direct hardware control of the external MOSFET gate in case of a microcontroller fault. The VNF1248F is suitable for 12 V, 24 V, and 48 V boardnets. Other uses include as an ECU main switch and active supply for always-on circuitry in parking mode. The associated EV-VNF1248F evaluation board, simplifies integration of the intelligent fuse protection into prototype circuitry. A software package, STSW-EV-VNF1248F, is also available.

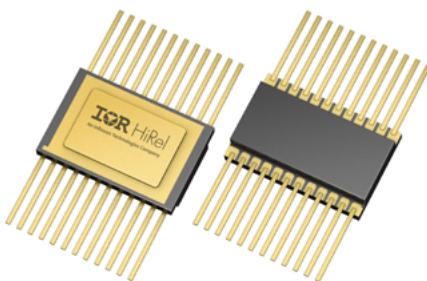


Automotive e-fuse controller ensures flexible and robust protection

www.st.com

Radiation-hardened Buck Controller with integrated Gate Drive

Infineon Technologies announced a radiation-hardened (rad-hard) buck controller with an integrated gate drive. Designed for Point of Load (PoL) power rails in commercial space systems and other extreme environments, the device is particularly well-suited for distributed satellite power

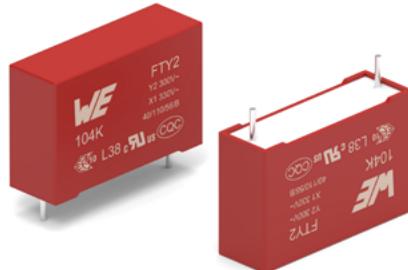


systems and digital processing payloads, including FPGA and ASIC systems. The RIC70847 integrates a radiation hardened 17.1 V buck controller with a 5 V (output) half-bridge gate drive and is targeted for applications with a power input range of 4.75 V to 15 V and power output range of 0.6 V to 5.25 V. It is designed to work seamlessly with logic-level transistors, such as Infineon's rad-hard R8 power FET. The device meets the MIL spec temperature range from -55 °C to 125 °C as well as the stringent requirements of applications that demand a Total Ionizing Dose (TID) rating of up to 100 krad (Si) and Single Event Effects (SEE) characterized up to a Linear Energy Transfer (LET) of 81.9 MeV·cm²/mg.

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Film Capacitors for the Mains Input

Würth Elektronik introduced a series of WCAP-FTY2 film capacitors which is optimized for use in mains noise suppression and complies with X1 or Y2 safety classes in accordance with IEC 60384-14. The high impulse dielectric strength compared to X2 capacitors, along with other product-specific parameters, is confirmed by VDE with ENEC10 certification. The company's WCAP-FTY2 series film capacitors are interference suppression capacitors for use as X1 or Y2 capacitors. When used as an X1 capacitor, it is placed between the phase (L) and neutral conductor (N). In a Y2 application, the capacitor is placed between the phase (L) and ground (PE) or between the neutral conductor and ground. As metallized film capaci-

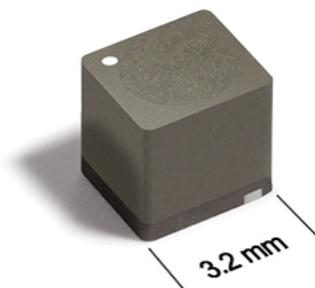


tors, the components are designed to be self-healing, making them particularly fail-safe. Their primary use is as mains filters in household appliances and interference suppression in industrial applications, such as inverters and motor control systems.

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Coilcraft's KTA3030 Series molded power inductors offer specifically low inductance values starting from 40 nH, making them well-suited for today's low-voltage, high-current DC/DC converters. Designed for single-phase and multiphase VRMs and PoL regulators, the KTA3030 delivers fast transient response, high current handling, and low DC as well as AC losses in a compact package. The AEC-200 qualified and RoHS-compliant series may be used with CPUs, GPUs, ASICs, and SoCs in servers, data centers, as well as automotive power applications. The package measures 3.2 x 3.0 x 3.2 mm³.



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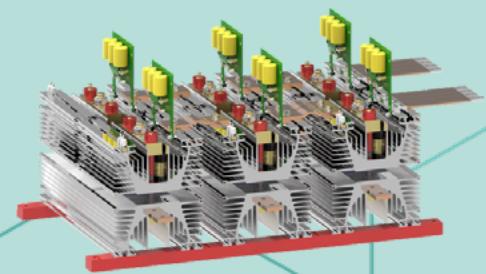
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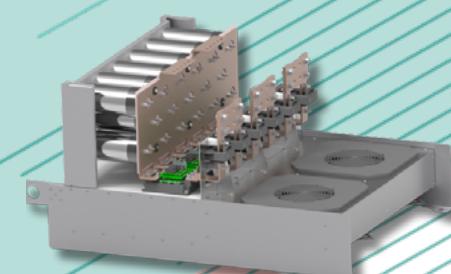
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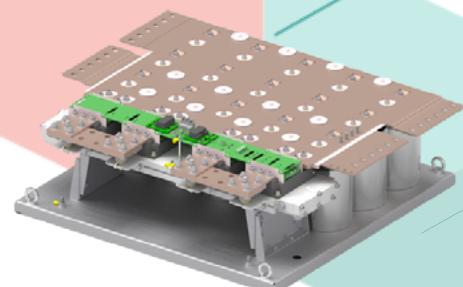
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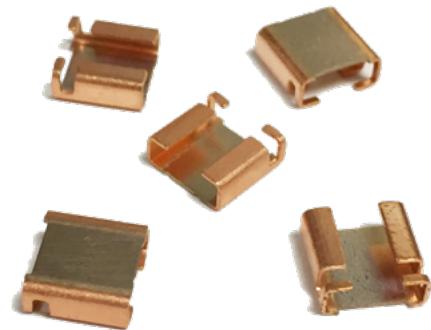
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High Current Four Terminal Shunt Resistors for AI Data Server Power

Stackpole Electronics' HCSK1216 high current four terminal shunt resistor is engineered "to deliver exceptional accuracy and efficiency in current sensing applications". The HCSK1216's four-terminal design separates supply current and voltage sensing paths, minimizing power loss and eliminating lead resistance errors. This all-metal component combines high power handling with ultra-low resistance values, making it suitable for precision current measure-

ment. With a footprint that occupies 75 % less space than traditional 2725-size components, the HCSK1216 is targeted for applications where power density and board space are critical. AI data servers are a prime example of environments that benefit from this advanced solution. Available in 0.3, 0.5, 1, and 2 mΩ resistance values, the HCSK1216 offers tolerances as low as 1 % and a temperature coefficient of resistance (TCR) of 50 ppm.



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1200 V Gen3 SiC MOSFET Modules in SOT-227

SemiQ has expanded its family of 1200 V Gen3 SiC MOSFETs, launching five SOT-227 modules that offer $R_{DS(on)}$ values of 7.4, 14.5, and 34 mΩ. SemiQ's GCMS modules, which feature Schottky Barrier Diodes (SBDs), are claimed to have "lower switching losses at high temperature, especially compared to non-SBDs GCMX modules". The devices target medium-voltage, high-power conversion applications, including battery chargers, photovoltaic inverters, server power supplies, and energy storage systems. All parts are screened using wafer-level gate-oxide burn-in tests exceeding 1400 V and are avalanche tested to 800 mJ (330 mJ for 34 mΩ modules). All modules feature an isolated backplate as well as direct mounts for a heat sink. The 7.4 mΩ GCMX007C120S1-E1 reduces switching losses to 4.66 mJ (3.72 mJ Turn on, 0.94 mJ Turn off) and has a body diode reverse recovery charge of 593 nC. Their junction-to-case thermal resistance ranges from 0.23°C/W for the 7.4 mΩ MOSFET module to 0.70 °C/W for the 34 mΩ MOSFET module.



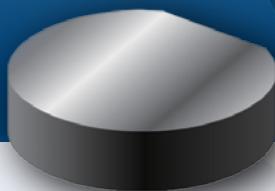
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